RL78/I1D

Battery Voltage Monitoring CC-RL

R01AN3418EJ0100
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Introduction

This application note describes how to implement voltage monitoring during battery charging with a comparator function.

Target Device

RL78/I1D

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Approaches to Monitoring Battery Voltage in Hardware

Battery voltage is monitored by comparing the voltage applied to the IVCMP1 pin (a voltage obtained by resistive division of the battery voltage) and the voltage applied to the IVREF1 pin (a reference voltage).

When the voltage applied to the IVCMP1 pin exceeds the reference voltage (IVREF1), the output of the comparator 1 becomes 1. At this time, by outputting the inverse of the output of the comparator 1 to VCOUT1, an LED is lit.

As indicated in the basic configuration of figure 1.1, a voltage obtained by resistive-dividing the monitored voltage is connected to the non-inverting input of a comparator, and the reference voltage is supplied to the comparator by an external regulator.

In this application note, the comparator 1 is used in window mode. When the voltage applied to the IVCMP1 pin exceeds the high voltage-side reference voltage (IVCMP1 > IVREF1), or when the voltage applied to the IVCMP1 pin falls below the low voltage-side reference voltage (IVCMP1 < IVREF0), the output of the comparator 1 becomes 1.

Table 1.1 Peripheral Functions and Their Usage

Peripheral Function	Usage
Regulator	Generates voltage (1.8 V) through comparison with monitored voltage
Comparator 1	Compares input voltage
Timer array unit	Provides PWM output to control charging

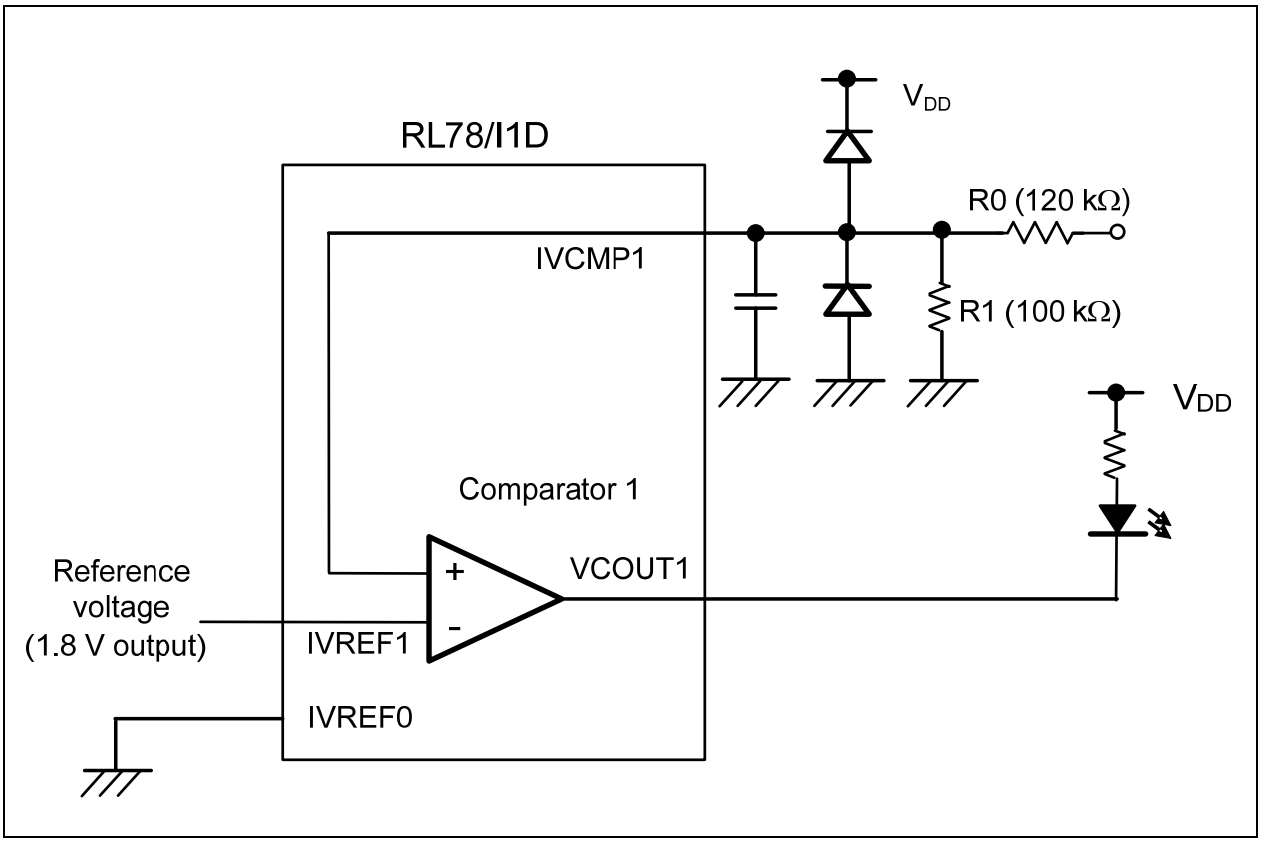

Figure 1.1 Basic Configuration

1.2 Division of Monitored Voltage

The monitored voltage is resistive-divided using 100 kΩ and 120 kΩ resistors. When the monitored voltage rises above 3.96 V, the voltage applied to the IVCMP1 pin exceeds the reference voltage (1.8 V).

1.3 Output of Comparison Result

The comparison result of the comparator 1 can be checked using the output function of the comparator 1. The comparison result is output from the VCOUT1 pin without software intervention. In this application note, by connecting an LED to the VCOUT1 pin, the LED is made to light when the monitored voltage exceeds 3.96 V.

2. Conditions for Confirming Operations

The sample code operations described in this application note are confirmed under the following conditions.

Table 2.1 Conditions for Confirming Operations

Item	Description
Microcontroller used	RL78/I1D (R5F117GC)
Operating frequency	- High-speed on-chip oscillator (HOCO) clock: 16 MHz - CPU/peripheral hardware clock: 16 MHz
Operating voltage	3.3 V (Operation is possible within 2.4 V to 5.5 V) LVD operation (V_{LVD}): Reset mode 2.45 V
Integrated development environment (CS+)	CS+ for CC V3.03.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.02.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.02.00 from Renesas Electronics Corp.

Note: The latest version should be downloaded and evaluated before usage.

3. Related Application Notes

The application notes related to this application note are listed below for reference.

4. Hardware Descriptions

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration described in this application note.

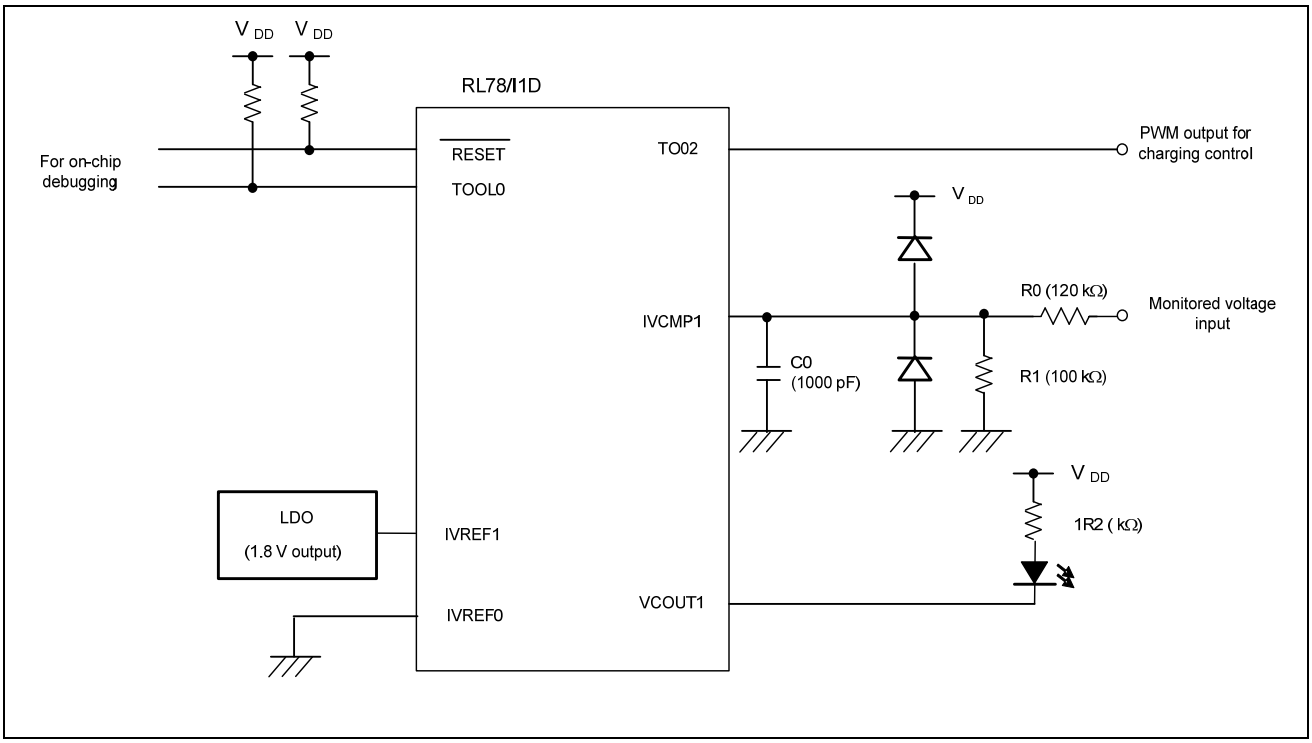

Figure 4.1 Hardware Configuration

Cautions: 1. This circuit diagram is simplified in order to show a summary of connections. When actually creating the circuit, pin processing and the like should be optimized and the circuit designed so as to satisfy the required electrical characteristics (input-only ports should be each connected to V_{DD} or V_{SS} via a resistor).

2. V_{DD} should be made equal to or higher than the reset release voltage (V_{LVD}) set using LVD.

4.2 List of Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P20/ANI13/VCOMP1/AMP30	Input	Monitored voltage input
P30 /TI00/TO01/IVREF0	Input	Low voltage-side reference voltage
P31/TI01/TO00/PCLBUZ0/IVREF1	Input	High voltage-side reference voltage
P57/INTP4/VCOUT1	Output	Output for LED1 control
P51/KR0/SCK01/SCL01/TI02/TO02	Output	PWM output for charging control

5. Software Descriptions

5.1 Operation Summary

This application note describes how to implement voltage monitoring during battery charging with a comparator function.

Battery voltage is monitored by comparing the voltage applied to the IVCMP1 pin (a voltage obtained by resistive division of the battery voltage) and the voltage applied to the IVREF1 pin (a reference voltage).

When the voltage applied to the IVCMP1 pin exceeds the reference voltage (IVREF1), the output of the comparator 1 becomes 1. At this time, by outputting the inverse of the output of the comparator 1 to VCOUT1, an LED is lit.

- The voltage applied to the IVCMP1 pin and the voltage applied to the IVREF1 pin (a reference voltage) is compared using the comparator 1.
- When the voltage applied to the IVCMP1 pin exceeds the reference voltage (IVREF1), the LED is lit.
- The TO02 provides PWM output for charging control.

5.2 List of Option Byte Settings

Table 5.1 shows the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Setting Value	Description
000C0H	11101111B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H	00111111B	LVD reset mode; 2.45 V (2.4 V to 5.5 V)
000C2H	11101010B	HS mode; High-speed on-chip oscillator: 16 MHz
000C3H	10000100B	On-chip debugging is enabled.

5.3 List of Functions

Table 5.2 lists functions.

Table 5.2 Functions

Function Name	Summary
R_COMP1_Start	Comparator 1 start processing
R_TAU0_Channel0_Start	TAU0 channel 0 operation start setting

5.4 Function Specifications

The following gives the specifications of the functions used in the sample code.

[Function name] R_COMP1_Start

Summary	Starts comparator operation.
Header	r_cg_comp.h, r_cg_userdefine.h
Declaration	void R_ COMP1_Start(void)
Description	Starts comparator operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_TAU0_Channel0_Start

Summary	TAU0 channel 0 operation start setting
Header	r_cg_tau.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel1_Start (void)
Description	Cancels TAU0 channel 1 interrupt mask.
Arguments	None
Return values	None
Remarks	None

5.5 Flowcharts

Figure 5.1 shows the overall flow of the process described in this application note.

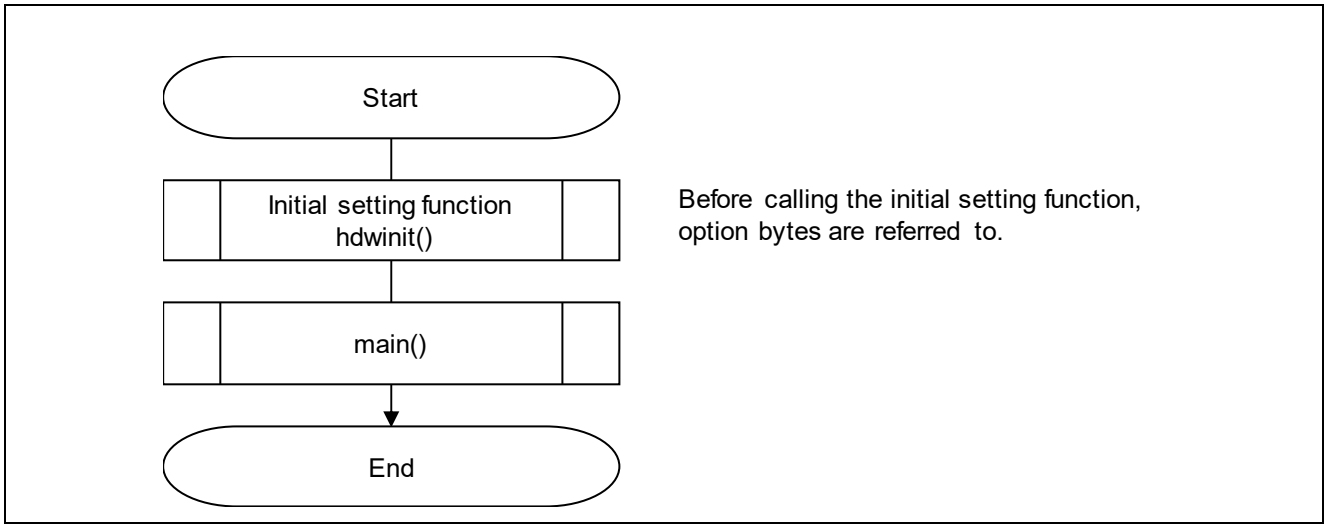

Figure 5.1 Overall Flow

Note: The start-up routine is executed before and after the initial setting function.

5.5.1 Initial Setting Function

Figure 5.2 shows the flowchart of the initial setting function.

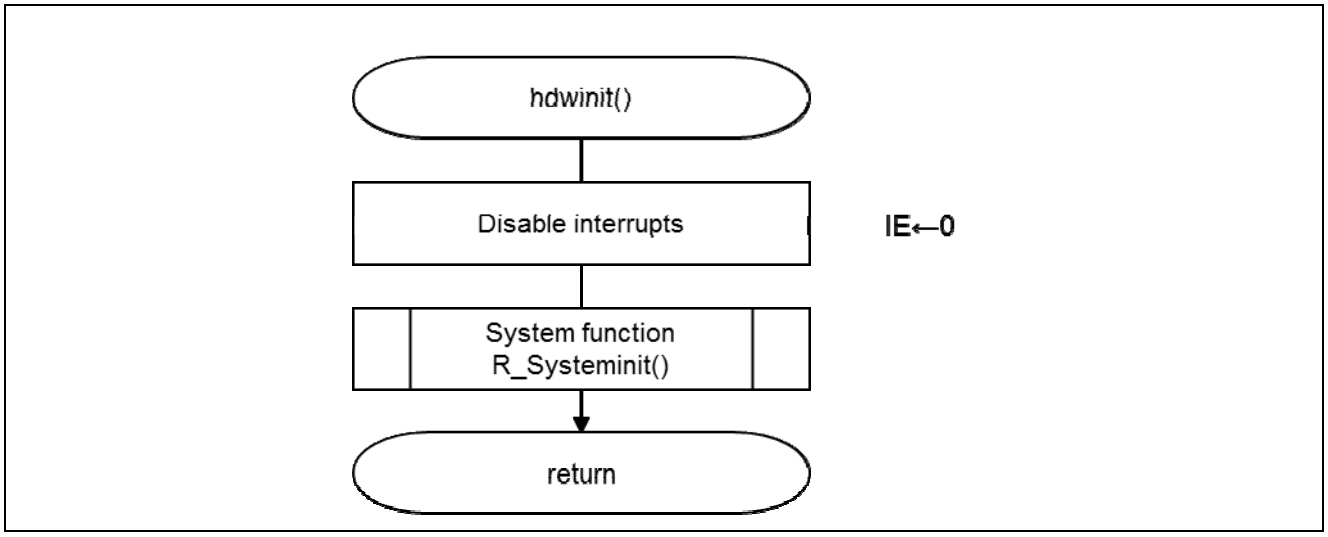

Figure 5.2 Initial Setting Function

5.5.2 System Function

Figure 5.3 shows the flowchart of the system function.

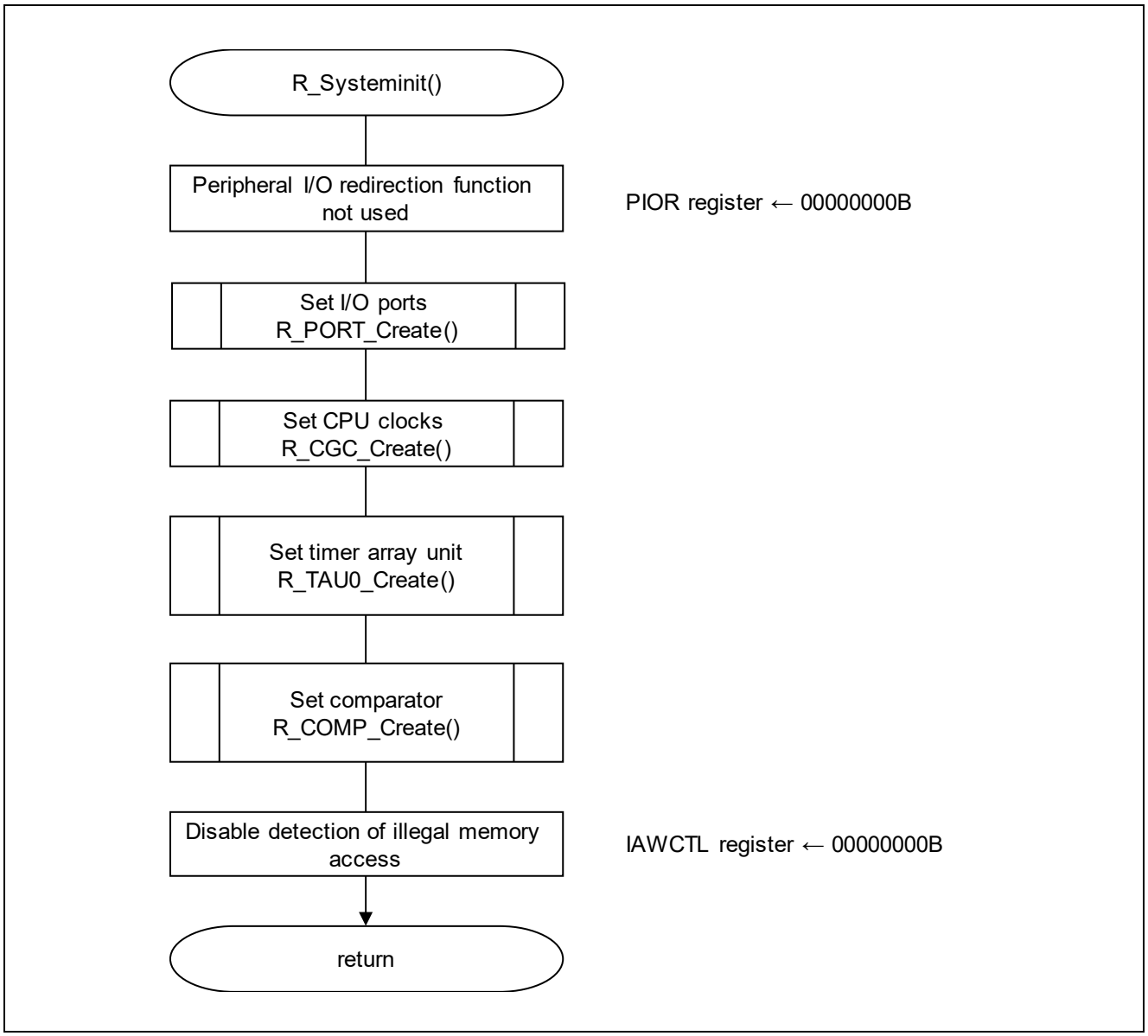

Figure 5.3 System Function

5.5.3 Setting I/O Ports

Figure 5.4 shows the flowchart for setting the I/O ports.

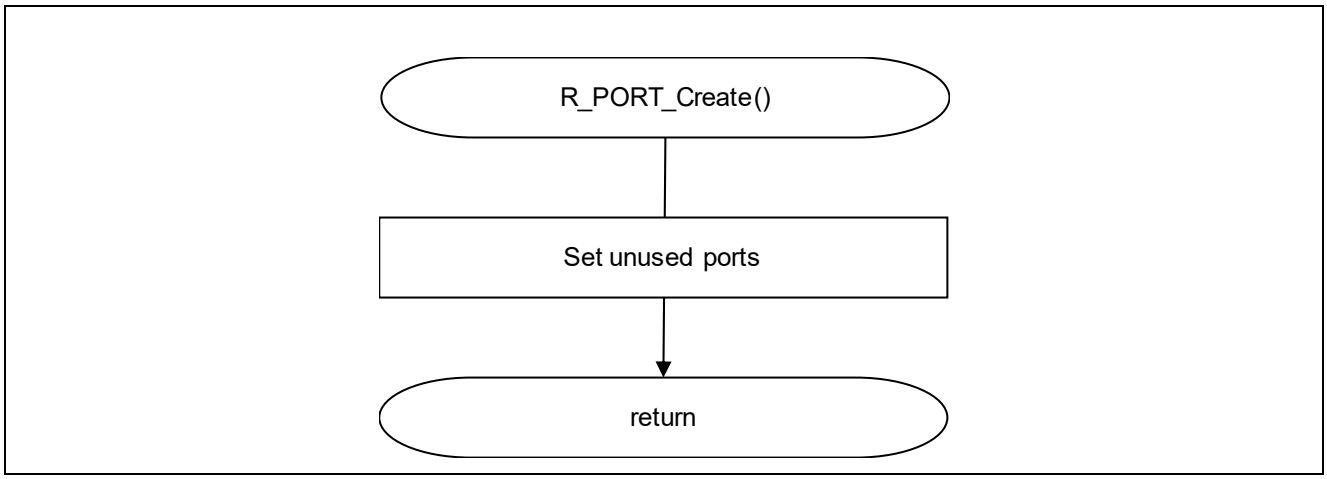

Figure 5.4 Setting I/O Ports

Note: For settings of unused ports, refer to the RL78/I1D User's Manual: Hardware.

Caution: Unused ports should be designed so that the electrical characteristics are satisfied by appropriately treating the pertinent pins. Separately connect unused input-only ports to V_{DD} or V_{SS} via a resistor.

5.5.4 Setting CPU Clocks

Figure 5.5 shows the flowchart for setting the CPU clocks.

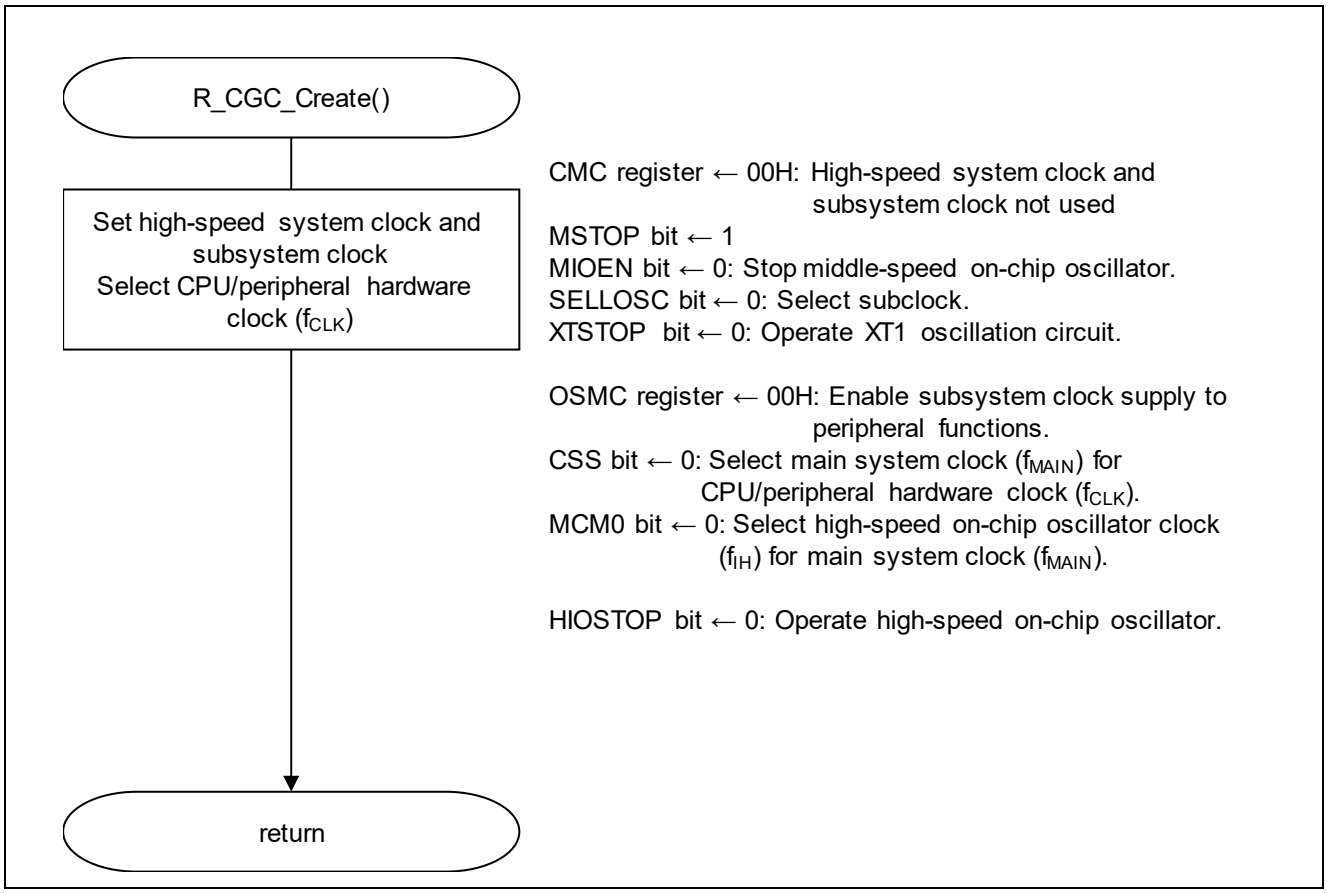

Figure 5.5 Setting CPU Clocks

5.5.5 Setting Comparator

Figure 5.6 shows the flowchart for setting the comparator.

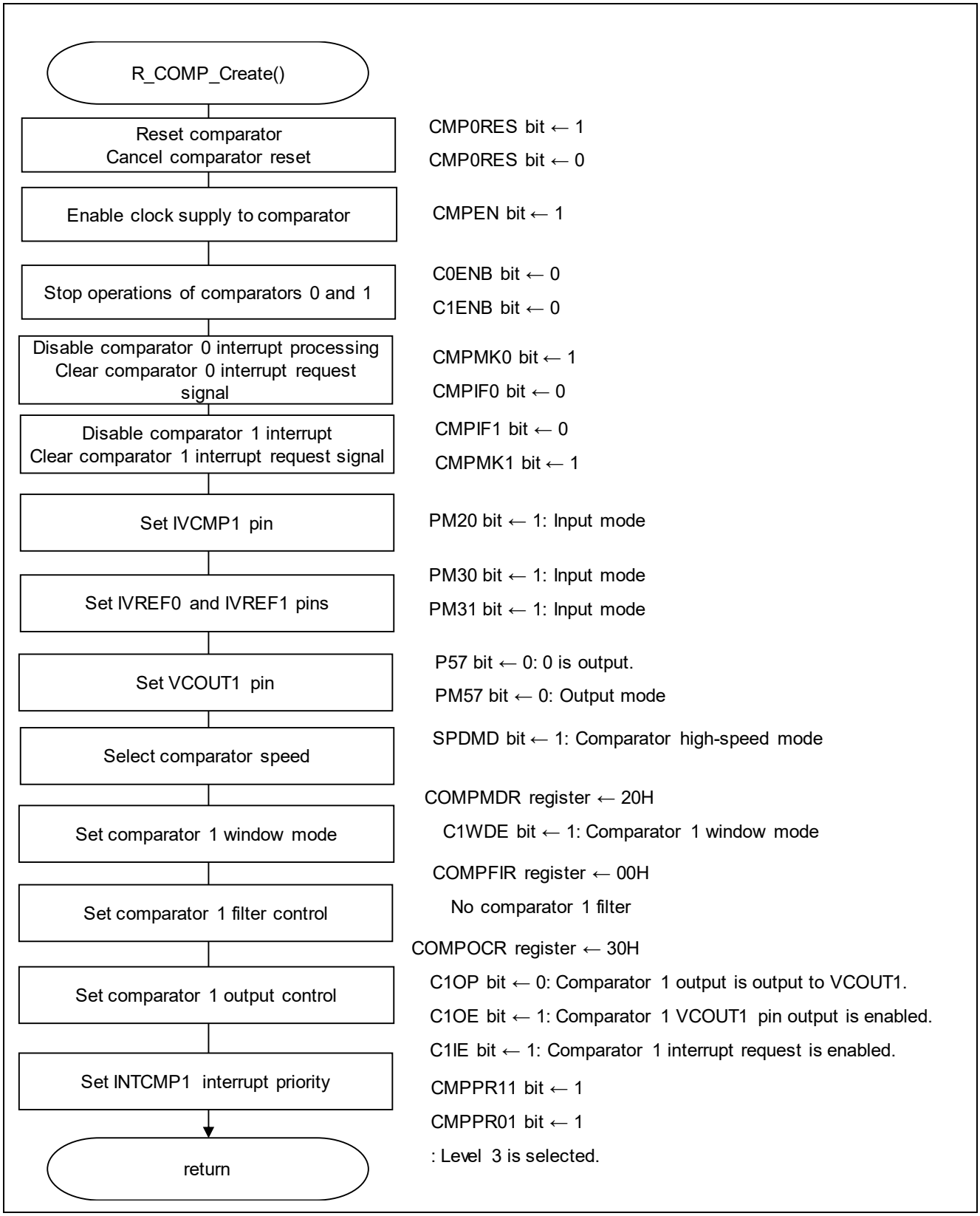

Figure 5.6 Setting Comparator

Starting clock supply to comparator

- Peripheral enable register 1 (PER1)
  Start supplying clock to the A/D converter.

Symbol: PER1

7	6	5	4	3	2	1	0
0	0	CMPEN	0	DTCEN	0	0	0
0	0	**1**	0	x	0	0	0

Bit 5

CMPEN	Control of comparator input clock
0	Stops input clock supply.
1	**Supplies input clock.**

Setting comparator operation

- Comparator mode setting register (COMPMDR)
  Enable comparator operation.

Symbol: COMPMDR

7	6	5	4	3	2	1	0
C1MON	0	C1WDE	C1ENB	C0MON	0	C0WDE	C0ENB
x	0	x	**0**	x	0	x	**0**

Bit 4

C1ENB	Comparator 1 operation enable
0	**Comparator 1 operation disabled**
1	Comparator 1 operation enabled

Bit 0

C0ENB	Comparator 0 operation enable
0	**Comparator 0 operation disabled**
1	Comparator 0 operation enabled

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting comparator interrupt

- Interrupt request flag register (IF1H)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Disable the interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
0	DOCIF	CMPIF1	CMPIF0	KRIF	TMKAIF	RTCIF	ADIF
0	x	**0**	**0**	x	x	x	x

Bits 4 and 5

CMPIF0,1	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
0	DOCMK	CMPMK1	CMPMK0	KRMK	TMKAMK	RTCMK	ADMK
0	x	**1**	**1**	x	x	x	x

Bits 4 and 5

CMPMK0,1	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Setting comparator peripheral reset

- Peripheral reset control register (PRR1)
  Control comparator peripheral resets.

Symbol: PRR1

7	6	5	4	3	2	1	0
0	0	CMPRES	0	0	0	0	0
0	0	**0/1**	0	0	0	0	0

Bit 5

CMPRES	Peripheral reset control on each peripheral hardware
0	**Peripheral reset release**
1	**Peripheral reset state**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

5.5.6 Setting Timer Array Unit

Figure 5.7 shows the flowchart for setting the timer array unit.

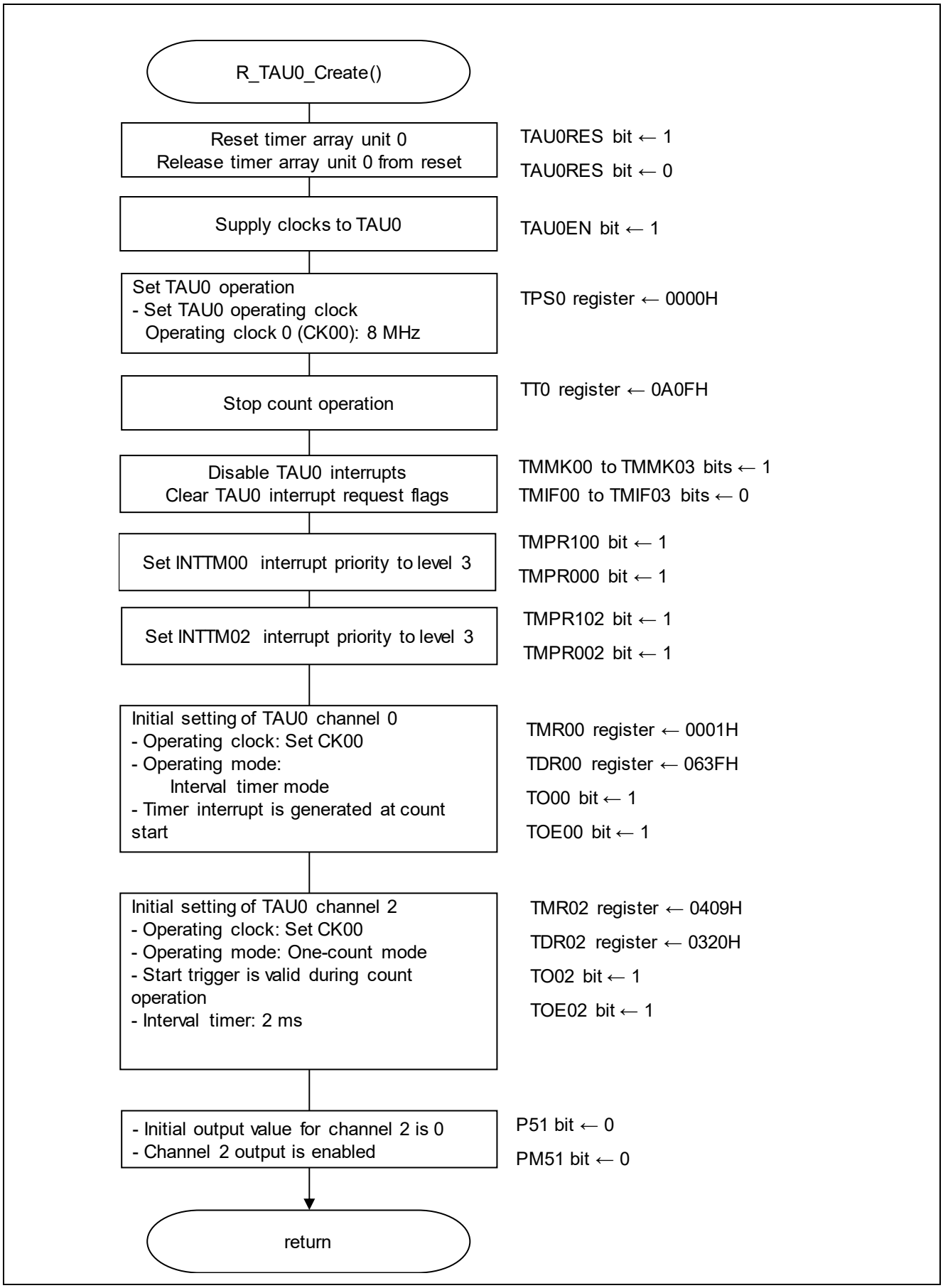

Figure 5.7 Setting Timer Array Unit

Setting timer array unit 0 peripheral reset

- Peripheral reset control register (PRR0)
  Control timer array unit 0 peripheral resets.

Symbol: PRR0

7	6	5	4	3	2	1	0
0	0	ADCRES	0	0	SAU0RES	0	TAU0RES
0	0	**x**	0	0	x	0	**0/1**

Bit 0

TAU0RES	Reset control of timer array unit 0
0	**Peripheral reset release**
1	**Peripheral reset state**

Starting clock supply to timer array unit 0

- Peripheral enable register 0 (PER0)
  Start clock supply to timer array unit 0.

Symbol: PER0

7		6	5	4	3	2	1	0
RTCWEN		0	ADCEN	0	0	SAU0EN	0	TAU0EN
x		0	x	0	0	x	0	**1**

Bit 0

TAU0EN	Control of input clock to timer array unit 0
0	Stops input clock supply.
1	**Enables input clock supply.**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting timer clock frequency

- Timer clock select register 0 (TPS0)

Select the operating clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS031	PRS030	0	0	PRS021	PRS020	PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
x	x	x	x	x	x	x	x	x	x	x	x	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS003	PRS002	PRS001	PRS000		Selection of operation clock (CK00)				
					f_{CLK}= 2MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz	f_{CLK}= 24MHz
0	**0**	**0**	**0**	f_{CLK}	2 MHz	5 MHz	**10 MHz**	20 MHz	24 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	313kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156 kHz	313 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting channel 0 operating mode

- Timer mode register 00 (TMR00)
  Select the operating clock (f_{MCK}).
  Select the counting clock.
  Set the software trigger start.
  Select the operating mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS010 and CKS011 bits**
1	Valid edge of input signal input from the TI00 pin

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
0	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 and 6

CIS001	CIS000	Selection of TI01 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 010	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

Bits 3 to 0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	**0**	**0**	**1**/0	**Interval timer mode**	**Interval timer/square wave output/divider function/PWM output (master)**	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on the MD000 bit (see table below).

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD000	Count operation of TCR
- Interval timer mode (0, 0, 0) **- Capture mode (0, 1, 0)**	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	**Timer interrupt is generated when counting is started (timer output also changes).**
- Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
- One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation. At that time, interrupt is generated.
- Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.
Other than above		Setting prohibited

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting interval timer frequency

- Timer data register 00 (TDR00)
  Set the interval timer comparison value.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer interrupt (INTTM00) generation = (TDR00 setting value + 1) x counting clock frequency

Enabling timer output

- Timer output enable register 0 (TOE0)
  Enable/disable timer output of each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE 07	TOE 06	TOE 05	TOE 04	TOE 03	TOE 02	TOE 01	TOE 00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	1

Bit 1

TOE00	Timer output enable/disable of channel 0
0	Timer output is disabled. Timer operation is not applied to the TM00 bit and the output is fixed. Writing to the TO00 bit is enabled and the level set in the TO00 bit is output from the TO00 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO00 bit and an output waveform is generated.** **Writing to the TO00 bit is ignored.**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting channel 2 operating mode

- Timer mode register 02 (TMR02)
  Select the operating clock (f_{MCK}).
  Select the counting clock.
  Set the software trigger start.
  Select the operating mode.

Symbol: TMR02

15	14		13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS021	CKS020		0	CCS02	MASTER02	STS022	STS021	STS020	CIS021	CIS020	0	0	MD023	MD022	MD021	MD010
0	**0**		0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 15 and 14

CKS021	CKS020	Selection of operation clock (f_{MCK}) of channel 2
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS02	Selection of count clock (f_{TCLK}) of channel 2
0	**Operation clock (f_{MCK}) specified by the CKS020 and CKS021 bits**
1	Valid edge of input signal input from the TI00 pin

Bit 11

MASTER02	Selection between using channel 2 independently or simultaneously with another channel
0	**Operates in independent channel operation function or as slave channel in simultaneous channel operation function.**
1	Operates as master channel in simultaneous channel operation function.

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Symbol: TMR02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS021	CKS020	0	CCS02	MASTER02	STS022	STS021	STS020	CIS021	CIS020	0	0	MD023	MD022	MD021	MD010
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 10 to 8

STS022	STS021	STS020	Setting of start trigger or capture trigger of channel 2
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI02 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI02 pin input are used as a start trigger and a capture trigger.
1	**0**	**0**	**Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).**
Other than above			Setting prohibited

Bits 7 and 6

CIS021	CIS020	Selection of TI02 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Symbol: TMR02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 021	CKS 020	0	CCS 02	MASTER 02	STS 022	STS 021	STS 020	CIS 021	CIS 020	0	0	MD 023	MD 022	MD 021	MD 020
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 3 to 0

MD 023	MD 022	MD 021	MD 020	Operation mode of channel 2	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/square wave output/divider function/PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	**0**	**0**	**1**/0	**One-count mode**	**Delay counter/One-shot pulse output/PWM output (slave)**	**Counting down**
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on the MD020 bit (see table below).

Operating mode (Value set by the MD023 to MD021 bits (see table above))	MD020	Count operation of TCR
- Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
- Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
- Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
- One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	**Start trigger is valid during counting operation. At that time, interrupt is generated.**
- Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.
Other than above		Setting prohibited

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting interval timer frequency

- Timer data register 02 (TDR02)
  Set the interval timer comparison value.

Symbol: TDR02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer interrupt (INTTM02) generation = (TDR02 setting value + 1) x counting clock frequency

Enabling timer output

- Timer output enable register 0 (TOE0)
  Enable/disable timer output of each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	x	x	x	x	x	**1**	x	x

Bit 2

TOE02	Timer output enable/disable of channel 2
0	Timer output is disabled. Timer operation is not applied to the TM02 bit and the output is fixed. Writing to the TO02 bit is enabled and the level set in the TO02 bit is output from the TO02 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO02 bit and an output waveform is generated.** **Writing to the TO02 bit is ignored.**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

5.5.7 Main Function

Figure 5.8 shows the flowchart for the main function.

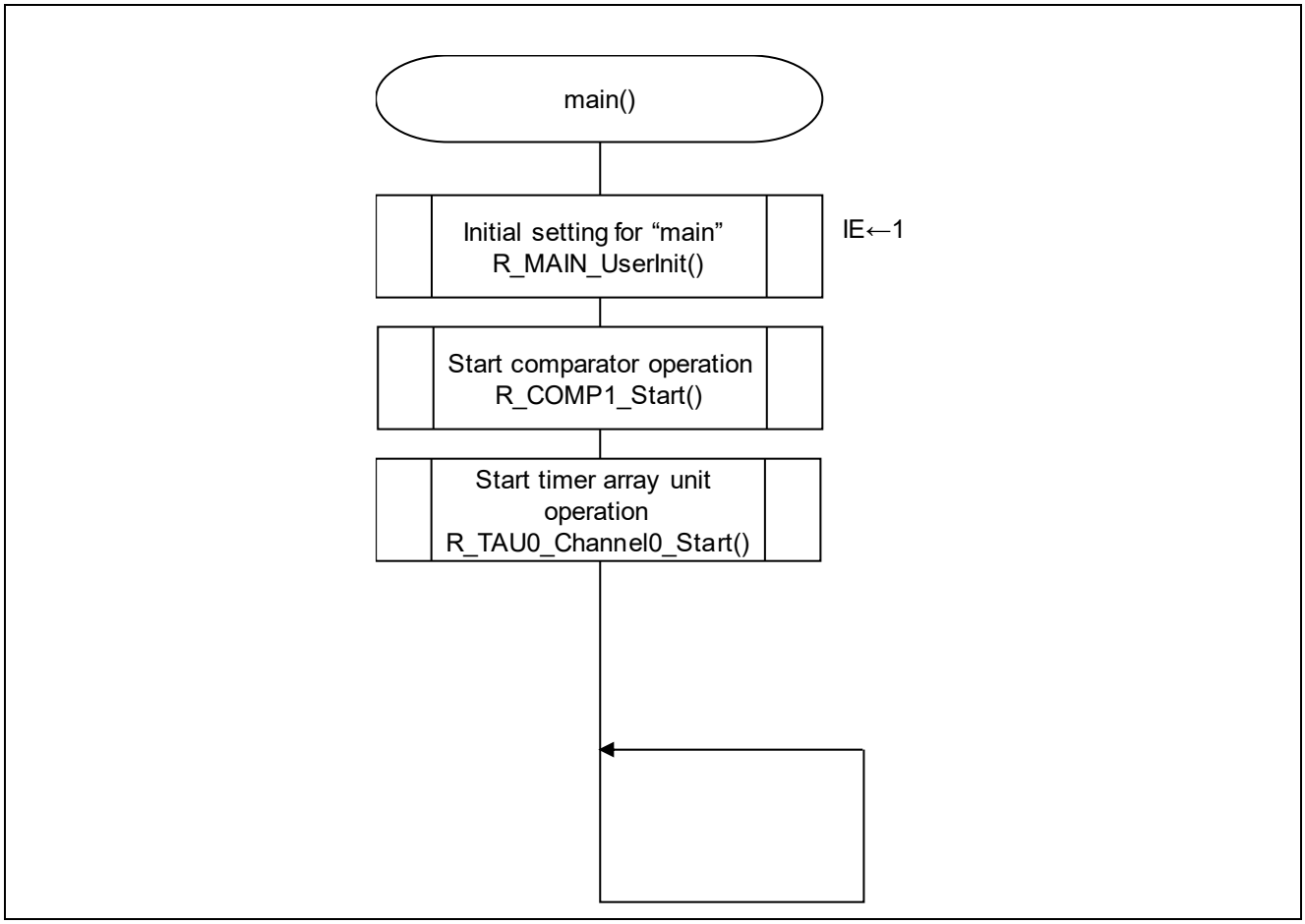

Figure 5.8 Main Function

5.5.8 Initial Setting for “main”

Figure 5.9 shows the flowchart of the initial setting for “main”.

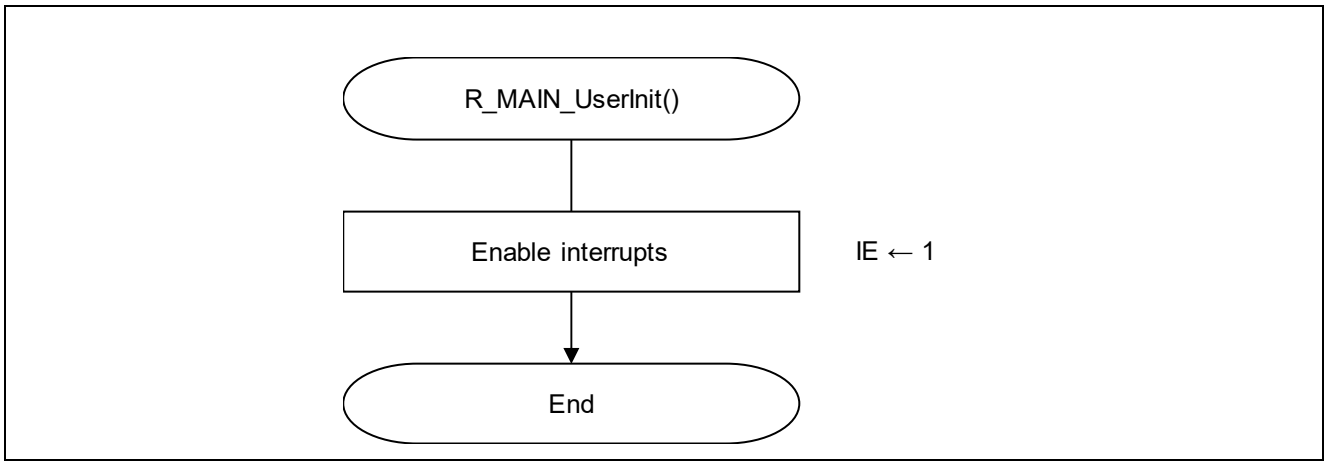

Figure 5.9 Initial Setting for “main”

5.5.9 Comparator 1 Operation Start Function

Figure 5.10 shows the flowchart for the comparator 1 operation start function.

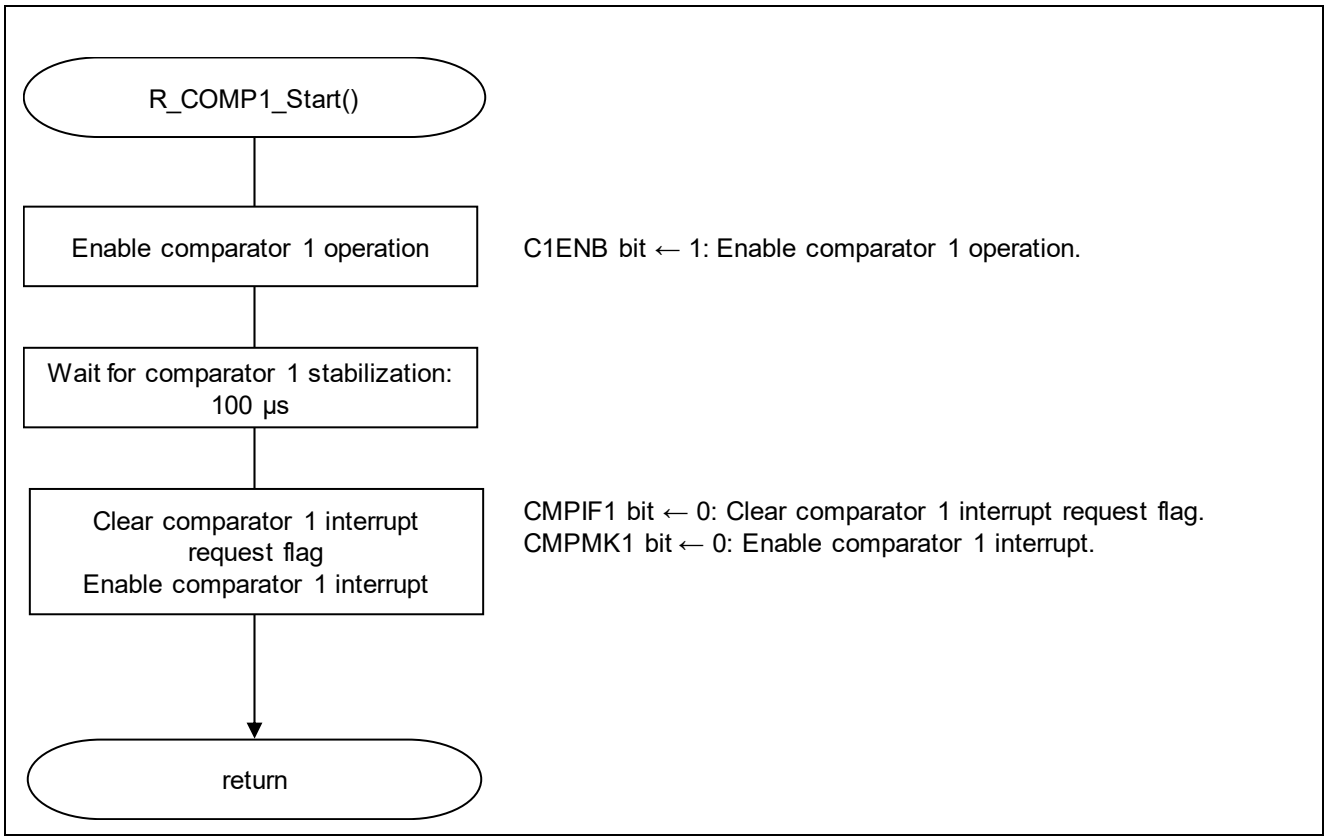

Figure 5.10 Comparator 1 Operation Start Function

5.5.10 TAU0 Channel 0 and Channel 2 Operation Start Function

Figure 5.11 shows the flowchart for TAU0 channel 0 and channel 2 operation start function.

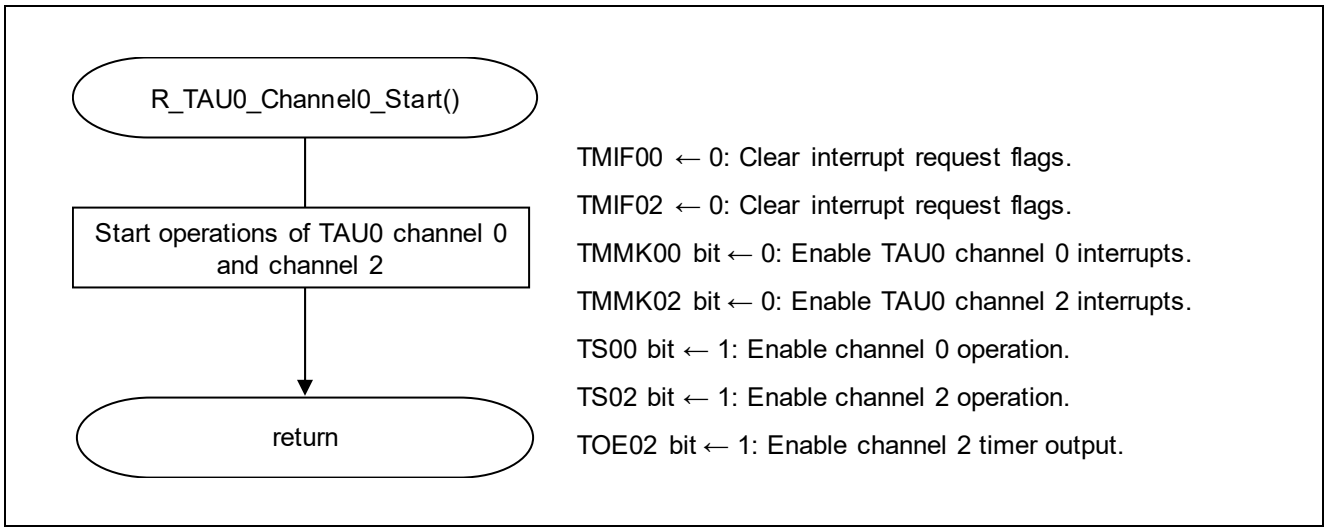

Figure 5.11 TAU0 Channel 0 and Channel 2 Operation Start Function

6. Sample Code

The user can get the sample code from the Renesas Electronics website.

7. Reference Documents

RL78/I1D User's Manual: Hardware (R01UH0474E)

RL78 Family User's Manual: Software (R01US0015E)

(Get the latest version from the Renesas Electronics website.)

Technical Updates/Technical News

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Inquiries

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Revision History	RL78/I1D Battery Voltage Monitoring CC-RL

Rev.	Date	Revision Contents	
		Page	Description
1.00	Jan. 31, 2017	—	Newly created.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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