RL78/G24

Timer RG2 in Phase Counting Mode

Introduction

This application note explains how to utilize the phase counting mode of the RL78/G24's Timer RG2 to detect the phase difference between external input signals coming from the TRGCLKA and TRGCLKB pins. Furthermore, it details the procedure for toggling a port via the effective edge detection on the TRGIDZ pin for TRG counter clearing and the associated counter clear interrupt.

Target Device

RL78/G24

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Specification overview

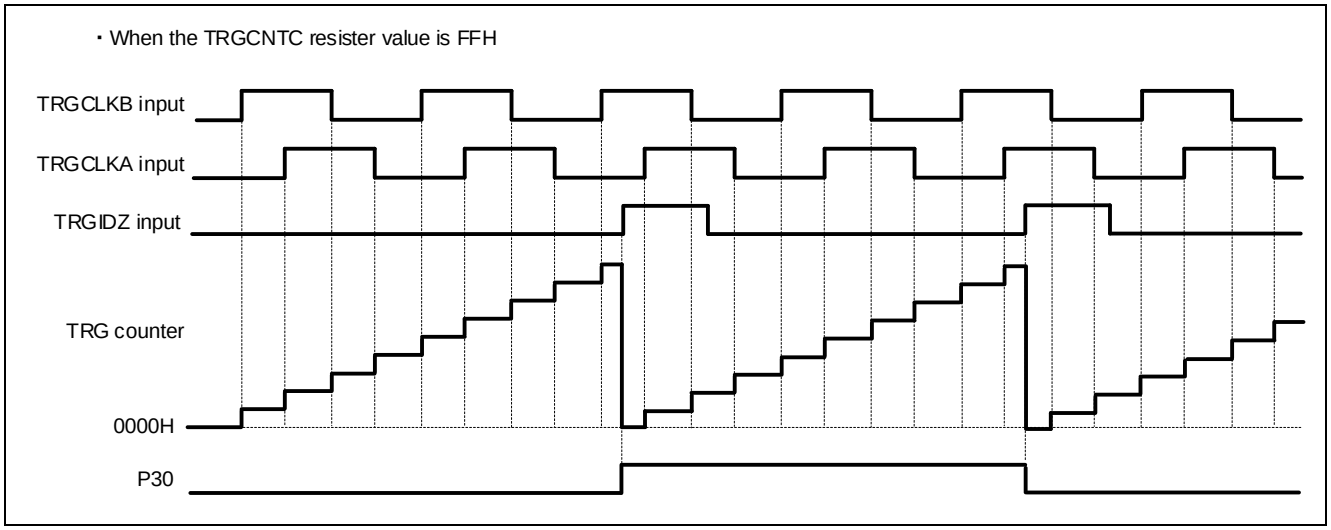
This application note explains how to detect phase differences in external input signals from the TRGCLKA and TRGCLKB pins and perform counting operations. Additionally, the counter is cleared through the effective edge detection of the TRGIDZ pin, triggering an interrupt, which in turn toggles the P30 pin.

Table 1-1 lists the peripheral functions and their purposes, and Figure 1-1 shows the phase counting mode and the output waveform of the port.

Table 1-1 Peripheral Functions and Their Usage

Peripheral	Usage
Timer RG2	Detect the phase difference between the TRGCLKA and TRGCLKB pins.
Port	Detection of the clearing interrupt due to a valid edge input on the TRGIDZ pin.

Figure 1-1 Phase counting mode and the output waveform of the port



1.2 Operation overview

Using Timer RG2 (Phase Counting Mode), the phase difference of external input signals from the TRGCLKA and TRGCLKB pins is detected, and the TRG counter is counted up/down. Also, by detecting a valid edge on the TRGIDZ pin, a clearing interrupt is generated, toggling P30.

The settings for Timer RG2 are shown below:

<Settings>

· Timer RG2 is used in Phase Counting Mode.

· Clearing of the TRG counter is prohibited.

· The method for clearing the TRG counter is set to detect a valid edge on the TRGIDZ pin.

· The input setting for the TRGIDZ pin is configured for a rising edge.

· The initial value of the TRG counter is set to 0000H.

· Conditions for adding/subtracting the TRG count are set.

· Counter interrupt due to TRGZ phase detection is permitted.

Table 1-2 shows the conditions for adding/subtracting the TRG counter.

Table 1-2 The conditions for adding/subtracting the TRG counter

TRGCLKB pin		H		L	H		L	
TRGCLKA pin	L		H			L		H
CNTEN7-CNTEN0 bit of TRGCNTC register	CNTEN7	CNTEN6	CNTEN5	CNTEN4	CNTEN3	CNTEN2	CNTEN1	CNTEN0
adding/subtracting	+1	+1	+1	+1	-1	-1	-1	-1

The port configuration is outlined below:

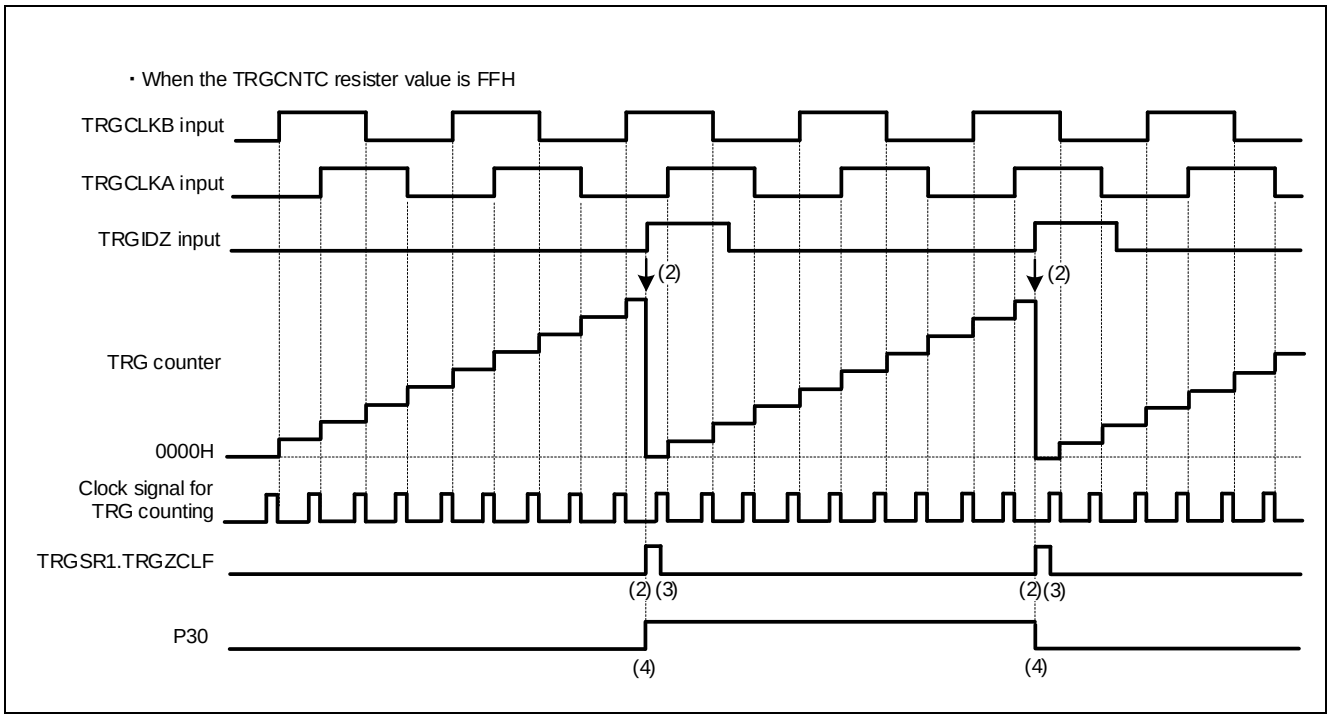
<Settings>

· Set P30 to output mode.

Figure 1-2 illustrates the Phase Counting Mode and the operation of the port.

(1) Start Timer RG2.
(2) When a rising edge is detected at the TRGIDZ terminal, the TRG counter is cleared to 0000H. Simultaneously, TRGSR1.TRGZCLF becomes 1, triggering a counter clearing interrupt.
(3) Within the counter clearing interrupt function, TRGSR1.TRGZCLF is cleared to 0.
(4) Due to the counter clearing interrupt occurrence, P30 toggles.

Figure 1-2 Phase Counting Mode and Port Operation



2. Operation Confirmation Conditions

The sample code described in this application note has been confirmed under the following conditions.

Table 2-1 Operation Confirmation Conditions

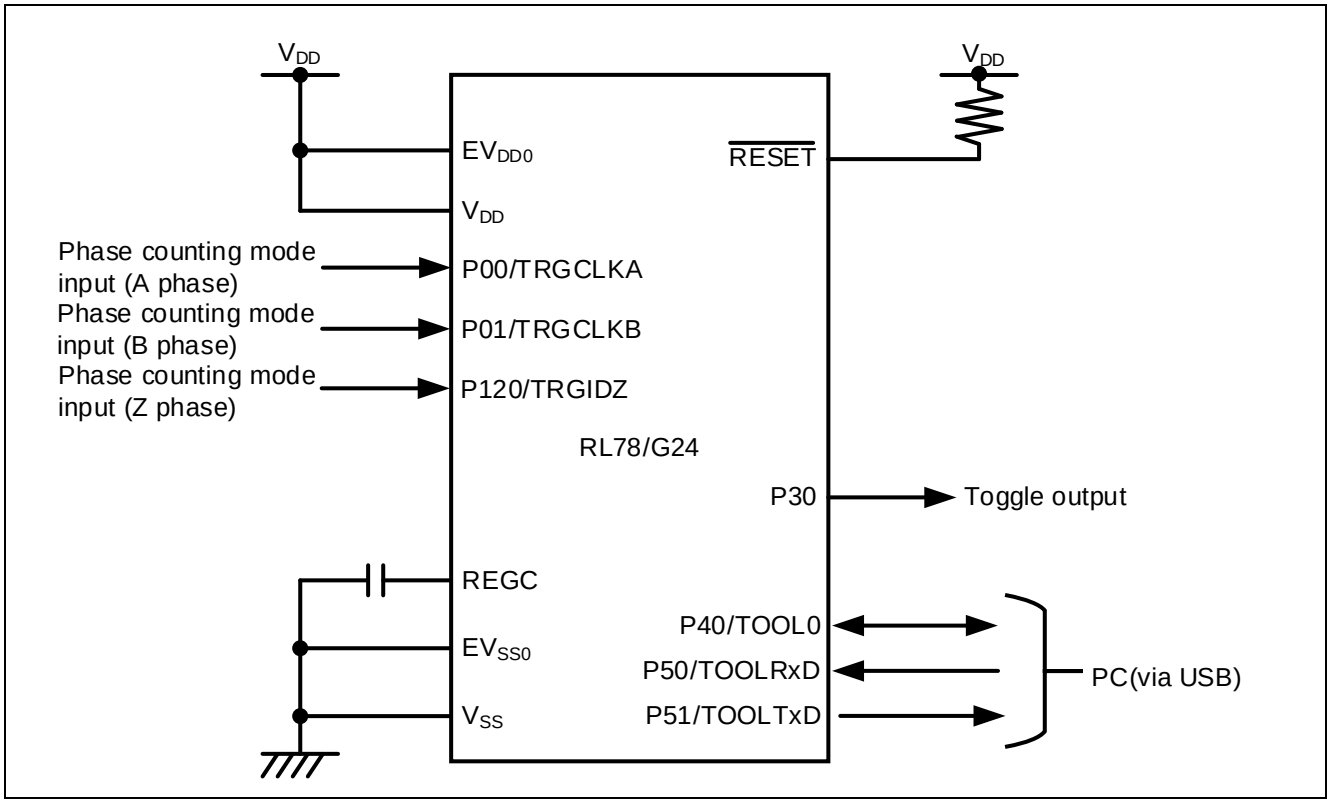
Item	Description
MCU used	RL78/G24 (R7F101GLG)
Operating frequency	· High-Speed On-Chip Oscillator Clock (fHOCO): 8MHz · PLL Oscillator Circuit Output (fPLL): 96MHz · CPU/Peripheral Hardware Clock (fCLK): 48MHz
Operating voltage	· 3.3V (Can operate between 2.7V to 5.5V) · LVD0 Operation (VLVD0): Reset Mode Rising edge = 2.97V Falling edge = 2.91V
Integrated development environment (CS+)	CS+ for CC V8.10.00 Manufactured by Renesas Electronics
C compiler (CS+)	CC-RL V1.12.01 Manufactured by Renesas Electronics
Integrated development environment (e^2 studio)	e^2 studio 2023-07 (23.7.0) Manufactured by Renesas Electronics
C compiler (e^2 studio)	CC-RL V1.12.00 Manufactured by Renesas Electronics
Integrated development Environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.1 Manufactured by IAR Systems
C compiler (IAR)	
Smart Configurator	V.1.7.0
Board Support Package (r_bsp)	V.1.60
Emulator	CS+, e^2 studio: COM port IAR: E2 Emulator Lite
Board used	RL78/G24 Fast Prototyping Board (RTK7RLG240C00000BJ)

3. Hardware Description

3.1 Example of Hardware Configuration

Figure 3-1 shows the hardware configuration example used in the sample code for this application.

Figure 3-1 Example of Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to VDD or VSS through a resistor).

Note 2. Connect any pins whose name begins with EVSS to VSS, and any pins whose name begins with EVDD to VDD, respectively.

Note 3. VDD must not be lower than the reset release voltage (VLVD0) that is specified for the LVD0.

3.2 List of used Pins

Table 3-1 shows the pins used and their functions.

Table 3-1 Pins Used and Their Functions

Pin name	I/O	Function
P00/TRGCLKA	Input	External Signal Input (Phase A)
P01/TRGCLKB	Input	External Signal Input (Phase B)
P120/TRGIDZ	Input	External Signal Input (Phase Z)
P30	Output	Toggled output

Caution: In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Description

4.1 Smart Configurator Settings

This section presents the settings of the Smart Configurator used in this sample program. The items and settings in each table for the Smart Configurator are described as they appear in the configuration screen.

4.1.1 System Configuration

The system configuration used in this sample program are shown below.

Note that the system settings used in this sample program are the same for the integrated development environments e2 studio and CS+, but different for IAR. Please adjust the settings appropriately according to the environment you are using.

Firstly, Figure 4-1 shows the system configuration used in this sample program (for e2 studio and CS+).

If you are conducting a COM port debug on the RL78/G24 Fast Prototyping Board (RTK7RLG240C00000BJ), it is necessary to set the integrated development environments (e2 studio and CS+) appropriately. For details, please refer to the "RL78/G24 Fast Prototyping Board User's Manual (R20UT5091)", specifically "7.1 Using COM Port Debugging with the e^2 studio" and "7.2 Using COM Port Debugging in CS+".

Figure 4-1 System Configuration (e^2 studio, CS+)

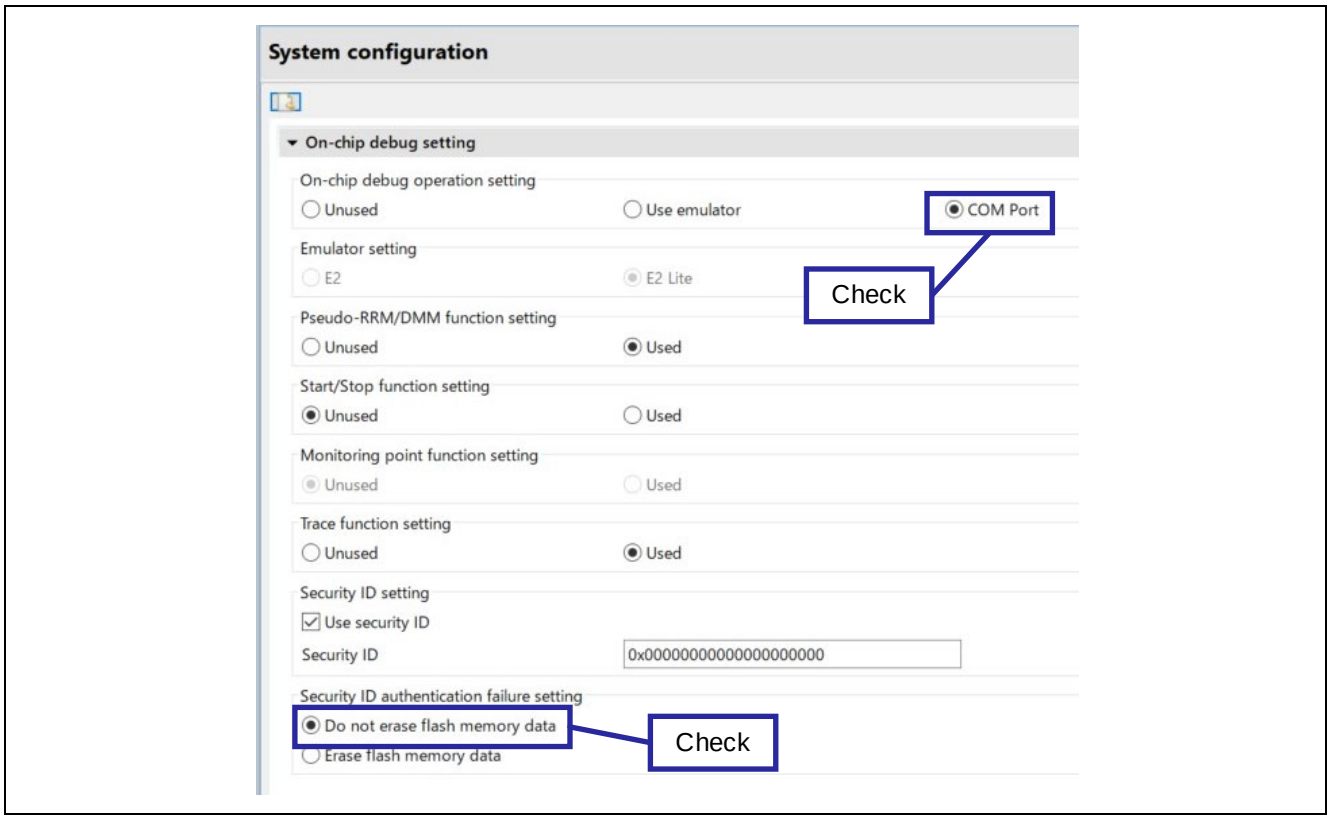
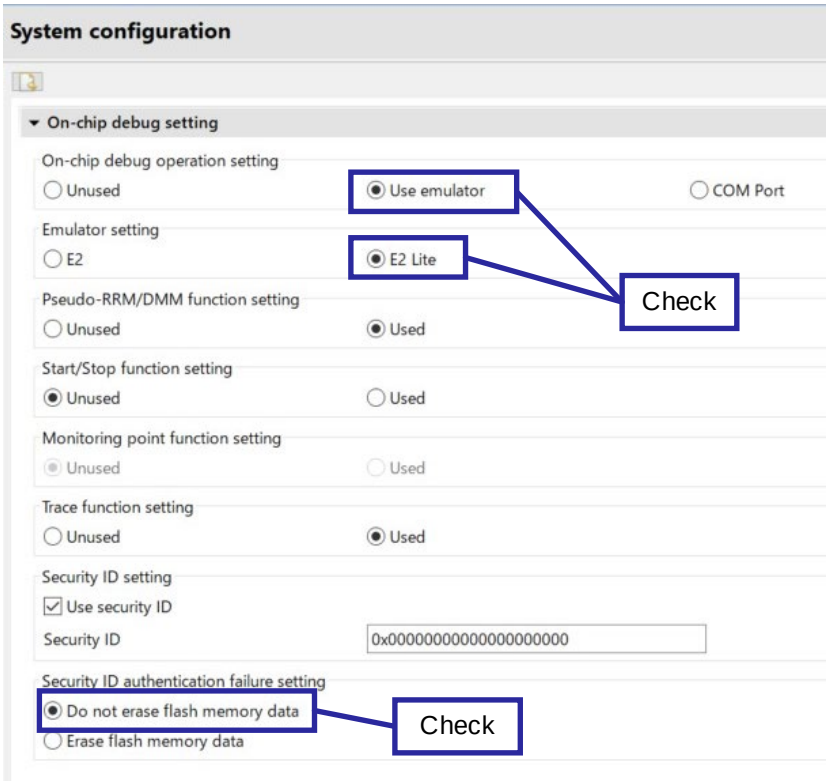


Figure 4-2 shows the system configurations used in this sample program for IAR.

Figure 4-2 System Configurations (IAR)



4.1.2 Component Configurations

This section presents the component configurations used in this sample program.

Table 4-1 Component Configurations (Timer RG2)

Item	Content
Component	Phase Counting Mode
Configuration Name	Config_TRG
Resource	TRG

Figure 4-3 Configuration of Timer RG2

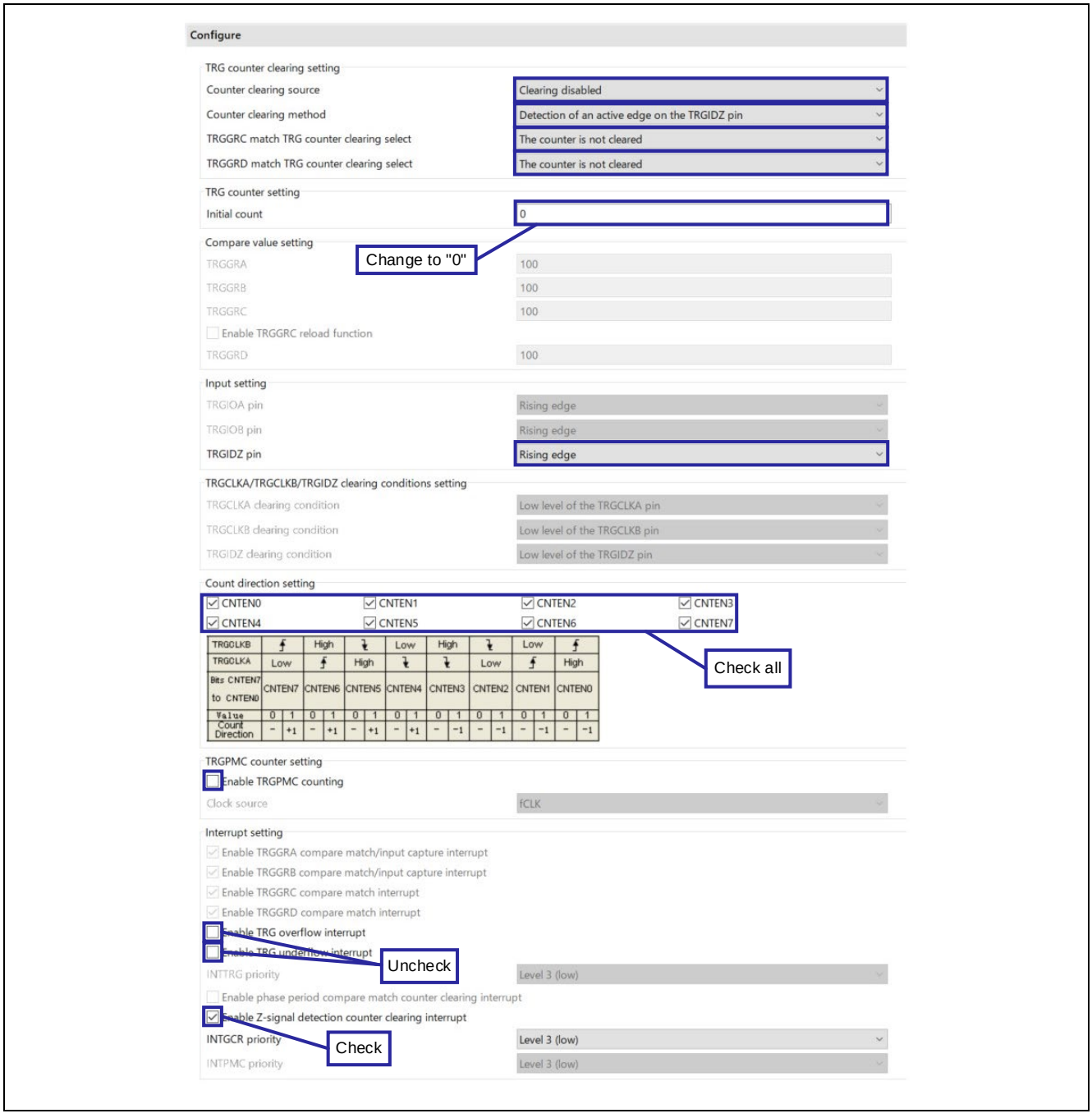
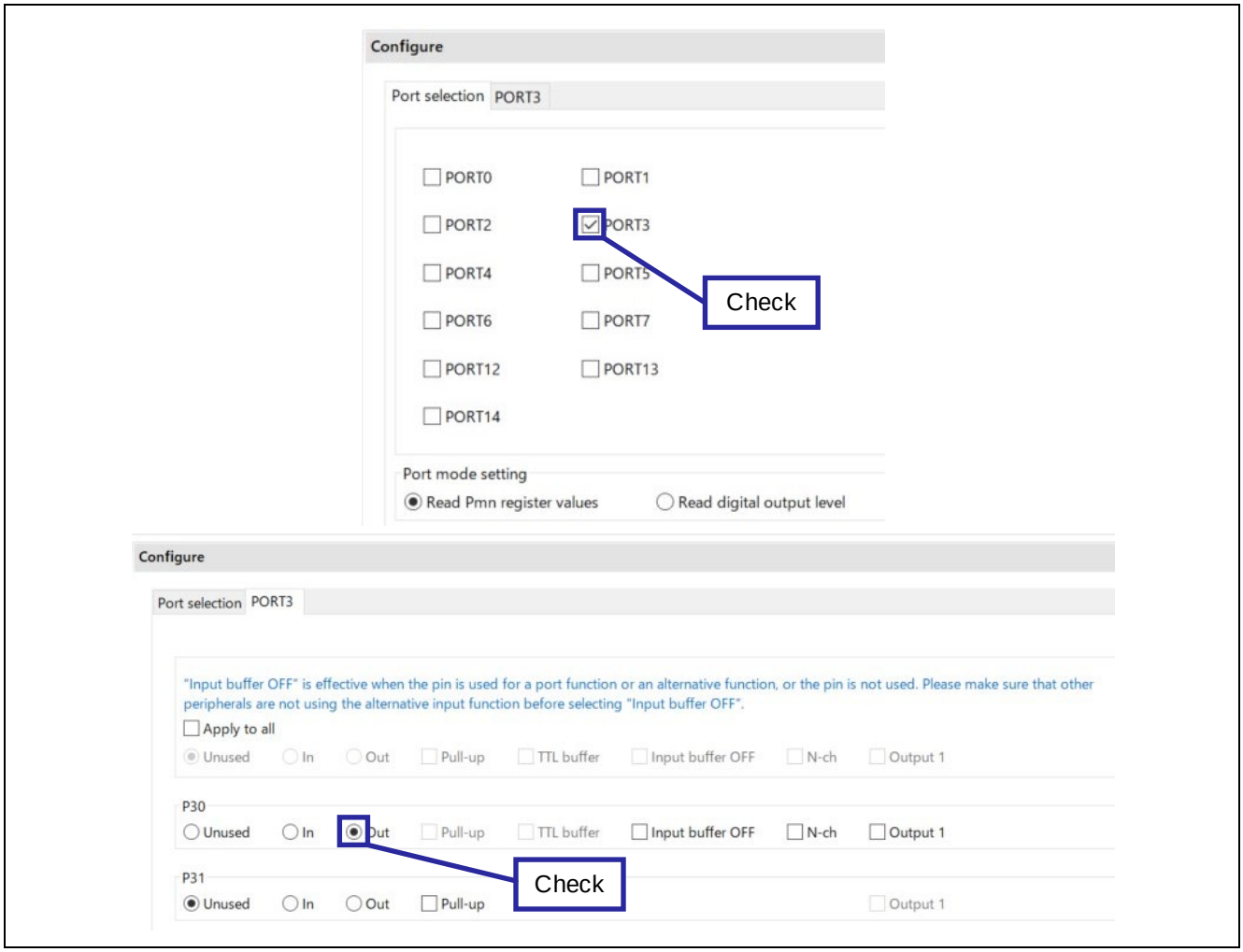


Table 4-2 Component Configurations (PORT)

Item	Content
Component	PORT
Configuration Name	Config_PORT
Resource	PORT

Figure 4-4 Configuration of PORT



4.2 Folder Structure

Table 4-2 shows the structure of the source files/header files used in the sample code. Note that files automatically generated by the integrated development environment and files from the BSP environment are excluded.

Table 4-3 Folder Structure

Folder/File Name	Description	Generated by Smart Configurator
\r01an6786_trg2_phase_counting<DIR>NOTE2	Sample code folder	
\src<DIR>	Program storage folder	
main.c	Sample code source file	
\smc_gen<DIR>	Smart configurator generated folder	√
\Config_PORT<DIR>	PORT program storage folder	√
Config_PORT.c	PORT source file	√
Config_PORT.h	PORT header file	√
Config_PORT_user.c	PORT interrupt source file	√NOTE 1
\Config_TRG<DIR>	TRG program storage folder	√
Config_TRG.c	TRG source file	√
Config_TRG.h	TRG header file	√
Config_TRG_user.c	TRG interrupt source file	√
¥general<DIR>	Initialization and common program storage folder	√
¥r_bsp<DIR>	BSP program storage folder	√
¥r_config<DIR>	Program storage folder	√

Note: "<DIR>" indicates a directory.
Note 1: Not used in the sample code.
Note 2: The sample code for IAR contains the r01an6786_trg2_phase_counting.ipcf file.
For details on the .ipcf file, please refer to "RL78 Smart Configurator User's Guide: IAR" (R20AN0581).

4.3 List of Option Byte Settings

Figure 4-3 shows the option byte settings.

Table 4-4 Option Byte Settings

Address	Setting Value	Description
000C0H/040C0H	1110 1111B (EFH)	Watchdog Timer stopped operation (Count stops after reset release)
000C1H/040C1H	1111 1011B (FBH)	LVD0 reset mode. Detection voltage: Rising 2.97V / Falling 2.91V
000C2H/040C2H	1110 1010B (EAH)	Flash operation mode: High-speed main mode. High-speed on-chip oscillator frequency: 8MHz
000C3H/040C3H	1000 0101B (85H)	On-chip debug operation allowed

4.4 List of Constants

Constant is not used in the sample code.

4.5 List of Global Variables

Table 4-4 shows the variables used in the sample code.

Table 4-5 Variables used in the sample code

Type	Variable Name	Contents	Function that uses the variable
uint8_t	g_trgsr1_dummy	Dummy variable for the TRGSR1 register.	r_Config_TRG_clear_interrupt

4.6 List of Functions

Table 4-5 lists the functions used in the sample code. However, functions generated by the Smart Configurator that have not been modified are excluded.

Table 4-6 List of Functions

Function Name	Description	Source File
main	Main Process	main.c
r_Config_TRG_clear_interrupt	Port toggle processing	Config_TRG_user.c

4.7 Function Specifications

The function specifications of the sample code are presented.

[Function Name] main

Outline	Main process
Header	r_smc_entry.h
Declaration	void main (void);
Explanation	Start the operation of Timer RG2.
Arguments	-
Return value	-
Remarks	-

[Function Name] R_Config_TRG_clear_interrupt

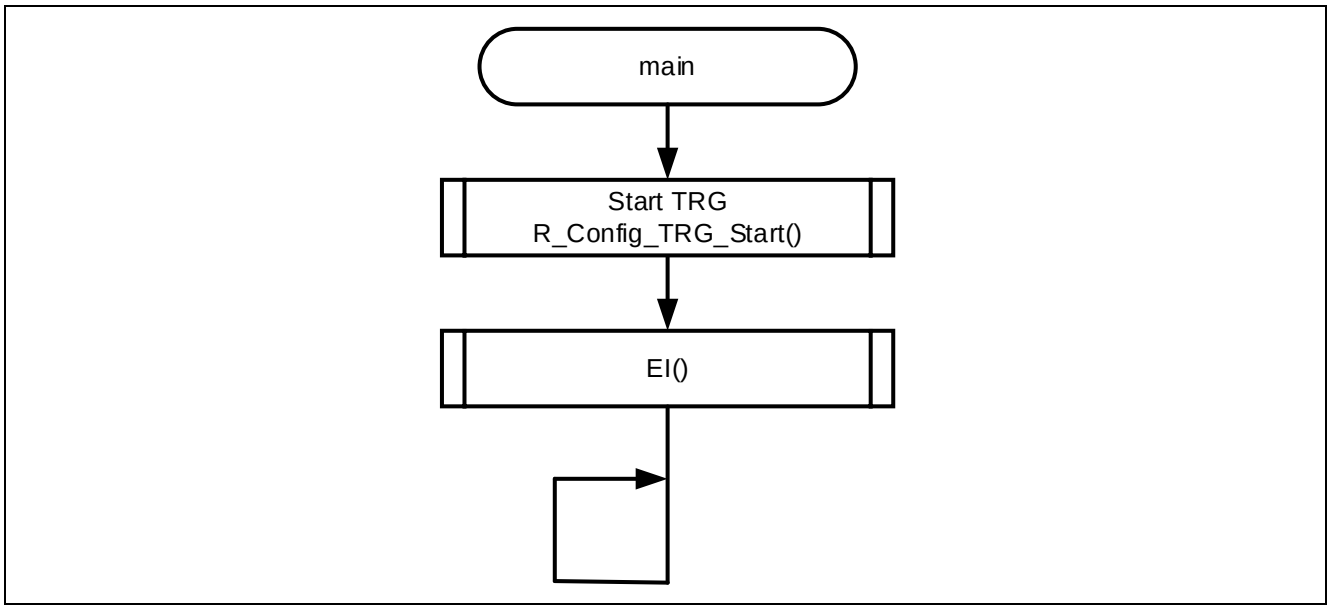
Outline	Port toggle process
Header	Config_TRG.h
Declaration	static void __near r_Config_TRG_clear_interrupt (void);
Explanation	Port toggle process
Arguments	-
Return value	-
Remarks	-

4.8 Flowchart

4.8.1 Main Process

Figure 4-4 shows the flowchart for the main process.

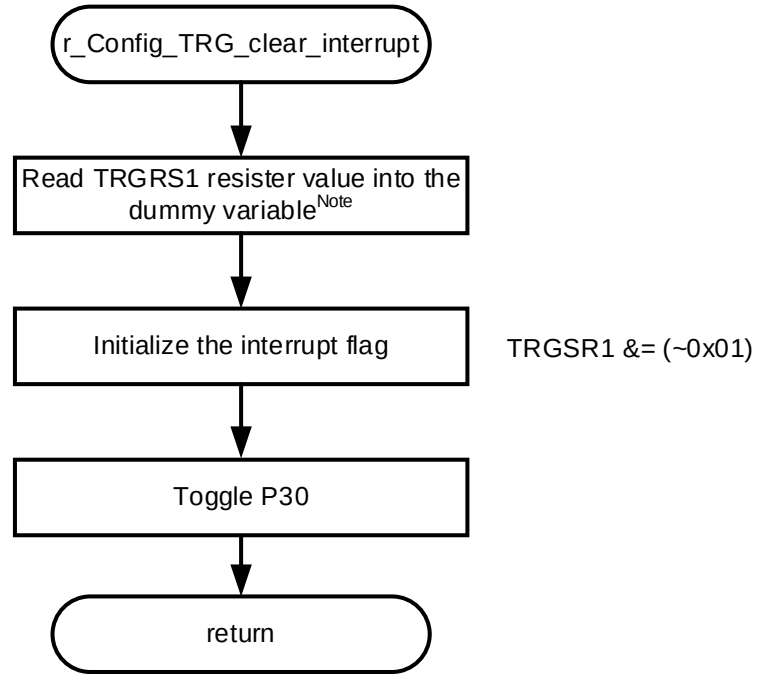
Figure 4-5 Main Process



4.8.2 r_Config_TRG_clear_interrupt Function

Figure 4-5 shows the flowchart for r_Config_TRG_clear_interrupt function.

Figure 4-6 r_Config_TRG_clear_interrupt Function



NOTE: The condition for TRGIMFA to become 0 is "read and then write 0", but since it does not support 1-bit access, we are accessing 1 byte to read and then write 0 to the TRGSR0 register. For details, please refer to the "RL78/G24 User's Manual: Hardware (R01UH0961)".

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G24 User's Manual: Hardware (R01UH0961)

RL78 family User's Manual: Software (R01US0015)

RL78/G24 Fast Prototyping Board User's Manual (R20UT5091)

RL78 Smart Configurator User's Gude: CS+ (R20AN0580)

RL78 Smart Configurator User's Gude: e2 studio (R20AN0579)

RL78 Smart Configurator User's Gude: IAR (R20AN0581)

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.07.23	-	First Edition

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2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
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   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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