RL78/G23

UART Reception in STOP Mode Using the UARTA Function

Introduction

This application node describes how to receive data through UART in STOP mode by using the RL78/G23 serial interface UARTA function and key interrupt function.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specification

1.1 Overview of Specification

The P71/TS03/KR1/SI21/SDA21/RxDA0 pin of 64-pin products are used for UART reception because these pins have the serial interface UARTA function and key interrupt function.

When data is sent from the device on the opposite side, the RL78/G23 detects the falling edge of the start bit by using the key interrupt function, and then releases the STOP mode. When the STOP mode is released, the UARTA function starts reception of data following the start bit through UART.

Note that the time required for releasing the STOP mode causes a delay in starting the UARTA operation. This delay is included in the baud rate tolerance.

Table 1-1 shows the peripheral functions and use. Table 1-2 shows the baud rate error tolerance. Figure 1-1 shows an outline of the operation.

Table 1-1 Peripheral Function and Use

Peripheral Function	Use
Serial Interface UARTA	Perform UART communication using the TxDA0 pin (transmission) and the RxDA0 pin (reception).
KR1	Detects the falling signal of the start bit.
Timer channel 0	Count timeouts.

Table 1-2 Baud rate error tolerance (Starting of the high-speed on-chip oscillator is at high speed, FWKUP = 1)

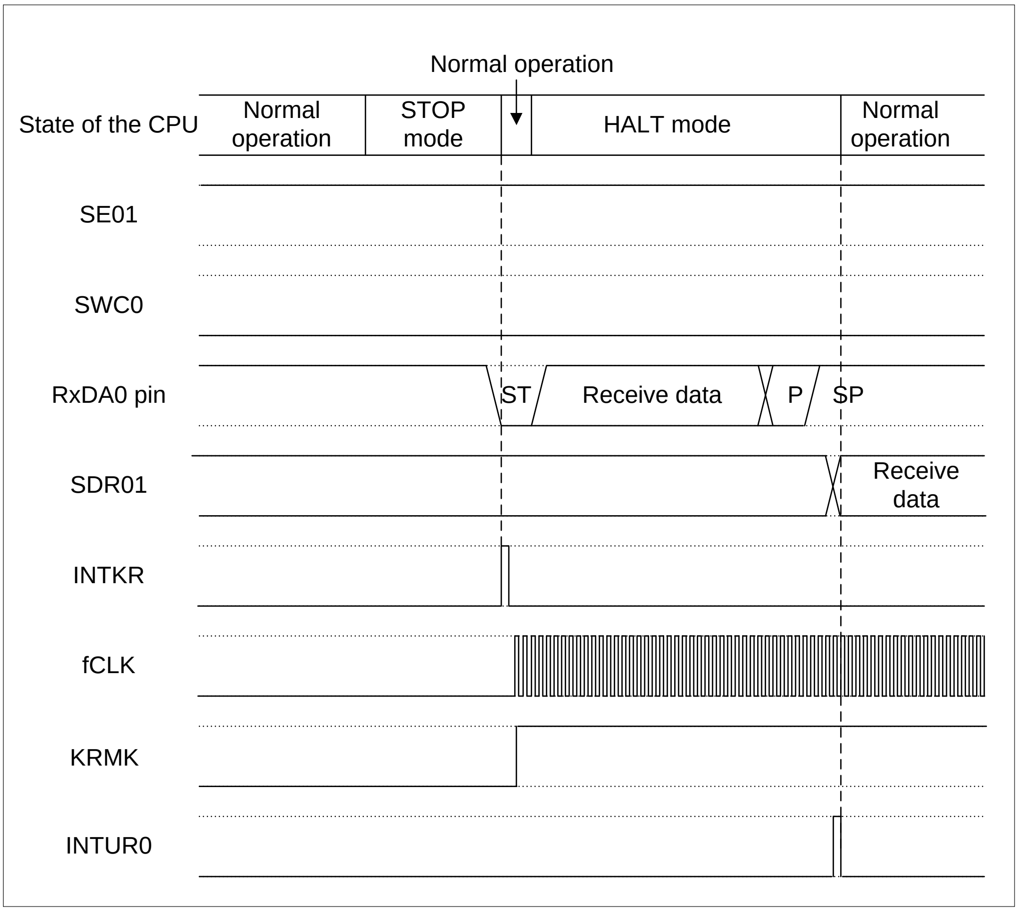
Baud Rate	High-speed On-Chip Oscillator (fCLK)	Operating Clock (fMCK)	BRGCA	Maximum Permissible Value	Minimum Permissible Value
1200bps	32MHz±1%	$fCLK/2^7$	104	4.35%	-3.66%
2400bps		$fCLK/2^6$	104	4.33%	-3.66%
4800bps		$fCLK/2^5$	104	4.28%	-3.66%
9600bps		$fCLK/2^4$	104	4.19%	-3.66%
19200bps		$fCLK/2^3$	104	4.00%	-3.66%
38400bps		$fCLK/2^2$	104	3.63%	-3.66%
76800bps		$fCLK/2^1$	104	2.89%	-3.66%
115200bps		$fCLK/2^1$	69	2.65%	-3.19%

Caution 1 When the accuracy of the clock frequency of the high-speed on-chip oscillator is ±1.5% or ±2.0%, the permissible range becomes smaller as shown below.

- In the case of fIH ±1.5%, perform (Maximum permissible value – 0.5%) and (Minimum permissible value + 0.5%) to the values in the above table.
- In the case of fIH ±2.0%, perform (Maximum permissible value – 1.0%) and (Minimum permissible value + 1.0%) to the values in the above table.

Caution 2 When using the product, perform evaluation to confirm that operation is normal.

Figure 1-1 UARTA Reception Timing Chart



1.2 Outline of Operation

When data is sent from the communication partner, the RL78/G23 detects the falling edge of the start bit by using the key interrupt function, and then releases the STOP mode. When the STOP mode is released, the UARTA function starts receiving data following the start bit through UART. When reception of one byte data is completed, the data corresponding to the receive data is sent to the device on the opposite side. If an error occurs, the data corresponding to the error is sent to the device on the opposite side. Tables 1.2 and 1.3 show the correspondence between the receive data and transmit data.

Table 1-3 Correspondence between Receive Data and Transmit Data

Receive Data	Response (Transmit) Data
T (54H)	O (4FH), K (4BH), ”CR” (0DH), ”LF” (0AH)
t (74H)	o (6FH), k (6BH), ”CR” (0DH), ”LF” (0AH)
Other than above	U (55H), C (43H), ”CR” (0DH), ”LF” (0AH)

Table 1-4 Correspondence between Error and Transmit Data

Error	Response (Transmit) Data
Parity error	P (50H), E (45H), ”CR” (0DH), ”LF” (0AH)
Framing error	F (46H), E (45H), ”CR” (0DH), ”LF” (0AH)
Overrun error	O (4FH), E (45H), ”CR” (0DH), ”LF” (0AH)

The following describes the major settings of the peripheral functions.

(1) Initial settings of the UARTA

- Use the P72/TxDA0 pin and the P71/RxDA0 pin for data output and data input, respectively.
- The data length is 8 bits.
- Set the data transfer direction to LSB first.
- Use even parity as the parity setting.
- Set the receive data level to standard.
- Set the transfer rate to 9600 bps.
- Use reception end interrupt (INTUR0), transmission end interrupt (INTUT0), and error interrupt (INTURE0).
- Set the interrupt priority orders of INTUR0, INTUT0, and INTURE0 to low priority.

(2) Initial settings of the key interrupt

- Enables the key interrupt function of KR1.
- Sets the detection edge to the falling edge.

(3) Initial settings of the timer array unit

- Set channel 0 to interval timer.
- Set the interval time for channel 0 to 2ms.

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

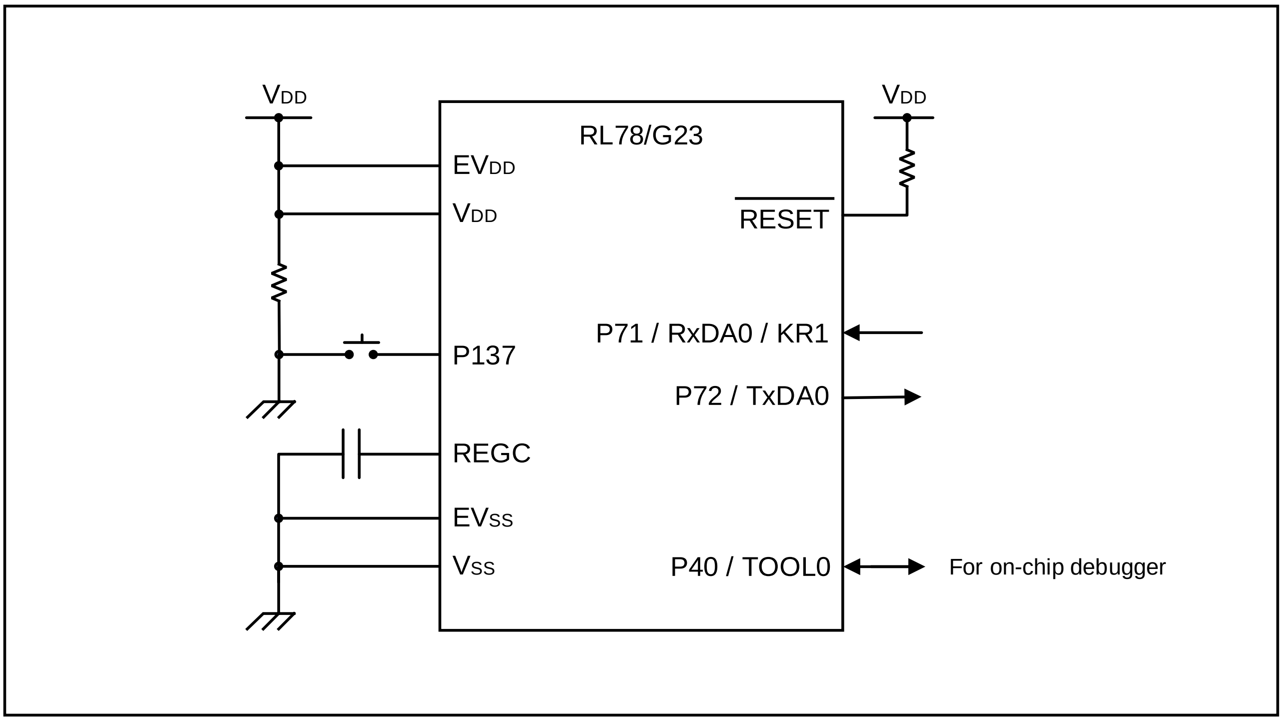
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	● High-speed on-chip oscillator clock (f_{IH}): 32 MHz ● CPU/peripheral hardware clock: 32 MHz
Operating voltage	During V_{DD} operation: 3.3 V LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ V8.09.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2 studio V2023-01 (23.1.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.2 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.2.2420 from IAR Systems Corp.
Smart Configurator	V.1.4.0
Board support package (r_bsp)	V.1.30

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This schematic circuit diagram is simplified to show the outline of connections. When creating circuits, design them so that they meet electrical characteristics by properly performing pin processing. (Connect input-only ports to V_{DD} or V_{SS} individually through a resistor.)

Note 2. Connect pins (with a name beginning with EV_{SS}), if any, to V_{SS}, and connect pins (with a name beginning with EV_{DD}), if any, to V_{DD}.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Function
P72 / TxDA0	Output	Data transmission pin
P71 / RxDA0 / KR1	Input	Data reception pin

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 040C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 040C1H	11111110B	LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V ～ 1.95 V) At falling edge TYP. 1.86 V (1.80 V ～ 1.91 V)
000C2H / 040C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 040C3H	10000100B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 Constants lists the constants that are used in the sample code.

Table 4-2 Constants

Constant Name	Setting Value	Description
s_messageOK[4]	"OK¥r¥n"	Response message to reception of “T”.
s_messageok[4]	"ok¥r¥n"	Response message to reception of “t”.
s_messageUC[4]	"UC¥r¥n"	Response message to reception of characters other than “T” or “t”.
s_messageFE[4]	"FE¥r¥n"	Response message to a framing error.
s_messagePE[4]	"PE¥r¥n"	Response message to a parity error.
s_messageOE[4]	"OE¥r¥n"	Response message to an overrun error.

4.3 List of Variables

Table 4-3 lists global variables.

Table 4-3 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	g_uarta0rxbuf	Receive data buffer	main()
uint8_t	g_uarta0rxerr	Receive error factor	main(), r_Config_UARTA0_callback_receiveend, r_Config_UARTA0_callback_error
MD_STATUS	g_uarta0txend	Transmission completion flag	main(), r_Config_UARTA0_callback_sendend
uint8_t	gp_uarta0_tx_address	Transmit data pointer	R_Config_UARTA0_Send, r_Config_UARTA0_interrupt_send
uint16_t	g_uarta0_tx_count	Transmit data number counter	R_Config_UARTA0_Send, r_Config_UARTA0_interrupt_send
uint8_t	gp_uarta0_rx_address	Receive data pointer	R_Config_UARTA0_Receive, r_Config_UARTA0_interrupt_receive, r_Config_UARTA0_interrupt_error
uint16_t	g_uarta0_rx_count	Receive data number counter	R_Config_UARTA0_Receive, r_Config_UARTA0_interrupt_receive
uint16_t	g_uarta0_rx_length	Receive data number	R_Config_UARTA0_Receive, r_Config_UARTA0_interrupt_receive
uint8_t	g_status_flag	Status flag (0x00: initial state, 0x01: Reception complete, 0x02: Timeout occurred)	main(), r_Config_UARTA0_interrupt_receive, r_Config_UARTA0_interrupt_error, r_Config_TAU0_0_interrupt

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function Name	Outline
main()	Main processing
r_Config_UARTA0_interrupt_send()	UARTA0 transmission end interrupt handling
r_Config_UARTA0_interrupt_receive()	UARTA0 reception end interrupt handling
r_Config_UARTA0_interrupt_error()	UARTA0 error interrupt handling
r_Config_KR_interrupt()	Key interrupt handling
r_Config_TAU0_0_interrupt()	Timer interrupt handling

4.5 Specification of Functions

The function specifications of the sample code are shown below.

main()	
Outline	Main processing
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_UART0.h, Config_KR.h, Config_TAU0_0.h
Declaration	void main(void);
Description	This function sends the data corresponding to the data received from the counterpart device to the counterpart device.
Argument	None
Return Value	None

r_Config_UARTA0_interrupt_send()	
Outline	UARTA0 transmission end interrupt handling
Header	r_cg_macrodriver.h、r_cg_userdefine.h、Config_UARTA0.h
Declaration	#pragma interrupt r_Config_UARTA0_interrupt_send(vect=INTUT0)
Description	This function starts sending data. It then updates the send data pointer and the number of data to be sent counter.
Argument	None
Return Value	None

r_Config_UARTA0_interrupt_receive()	
Outline	UARTA0 reception end interrupt handling
Header	r_cg_macrodriver.h、r_cg_userdefine.h、Config_UARTA0.h
Declaration	#pragma interrupt r_Config_UARTA0_interrupt_receive(vect=INTUR0)
Description	This function stores the received data in RAM. It then updates the receive data pointer and the receive data count counter. Sets the status flag to the value of reception complete (0x01).
Argument	None
Return Value	None

r_Config_UARTA0_interrupt_error()	
Outline	UARTA0 error interrupt handling
Header	r_cg_macrodriver.h、r_cg_userdefine.h、Config_UARTA0.h
Declaration	#pragma interrupt r_Config_UARTA0_interrupt_error(vect=INTURE0)
Description	This function stores the error factor in RAM and clears the receive error flag. Sets the status flag to the value of reception complete (0x01).
Argument	None
Return Value	None

r_Config_KR_interrupt()	
Outline	Key interrupt handling
Header	r_cg_macrodriver.h、r_cg_userdefine.h、Config_KR.h、Config_TAU0_0.h
Declaration	#pragma interrupt r_Config_KR_interrupt(vect=INTKR)
Description	This function starts the operation of the timer for timeout (2 ms).
Argument	None
Return Value	None

r_Config_TAU0_0_interrupt()	
Outline	Timer interrupt handling
Header	r_cg_macrodriver.h、r_cg_userdefine.h、Config_TAU0_0.h
Declaration	#pragma interrupt r_Config_TAU0_0_interrupt(vect=INTTM00)
Description	This function sets the status flag to the timeout value (0x02).
Argument	None
Return Value	None

4.6 Flowcharts

4.6.1 Main Processing

Figure 4-1 to 4-3 show flowcharts of the main processing.

Figure 4-1 Main Processing (1/3)

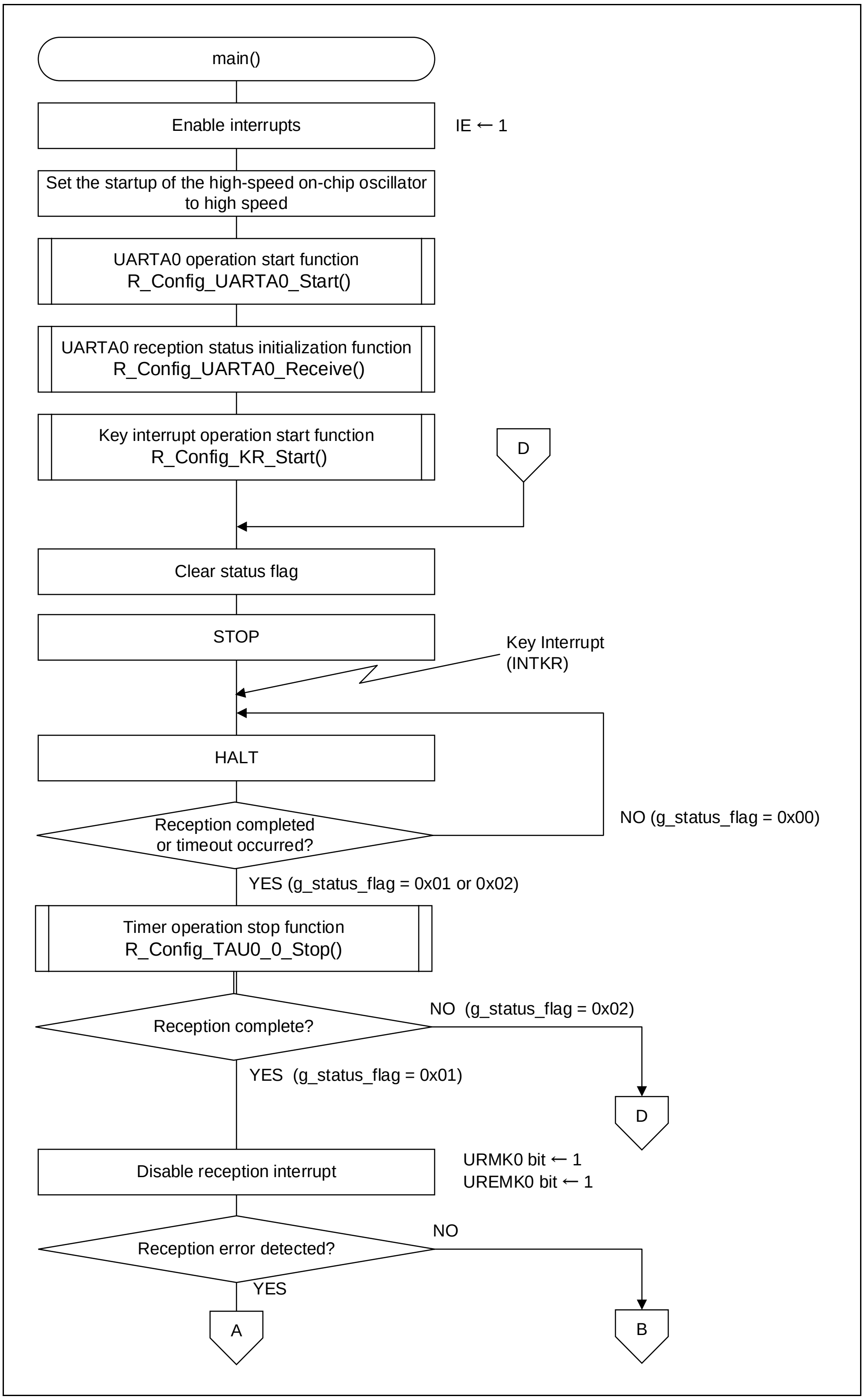


Figure 4-2 Main Processing (2/3)

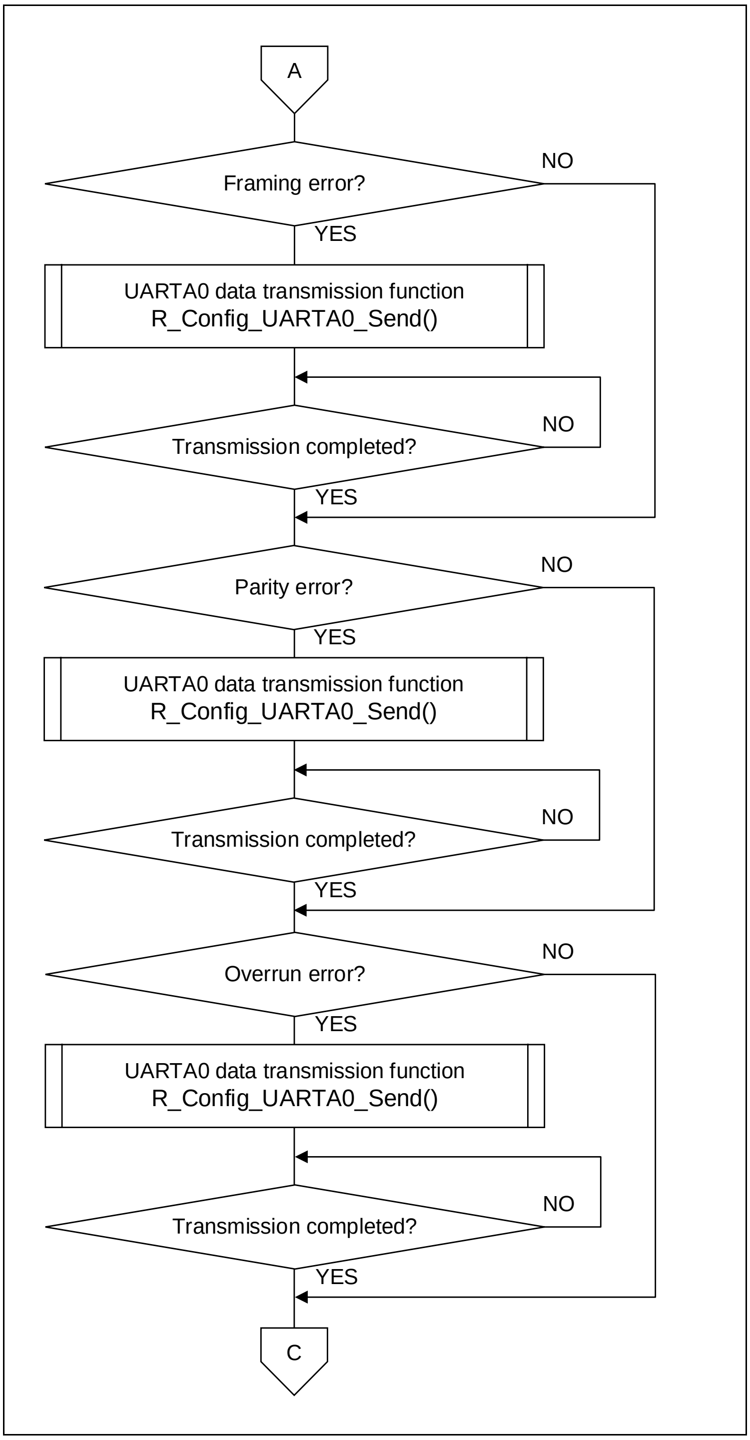
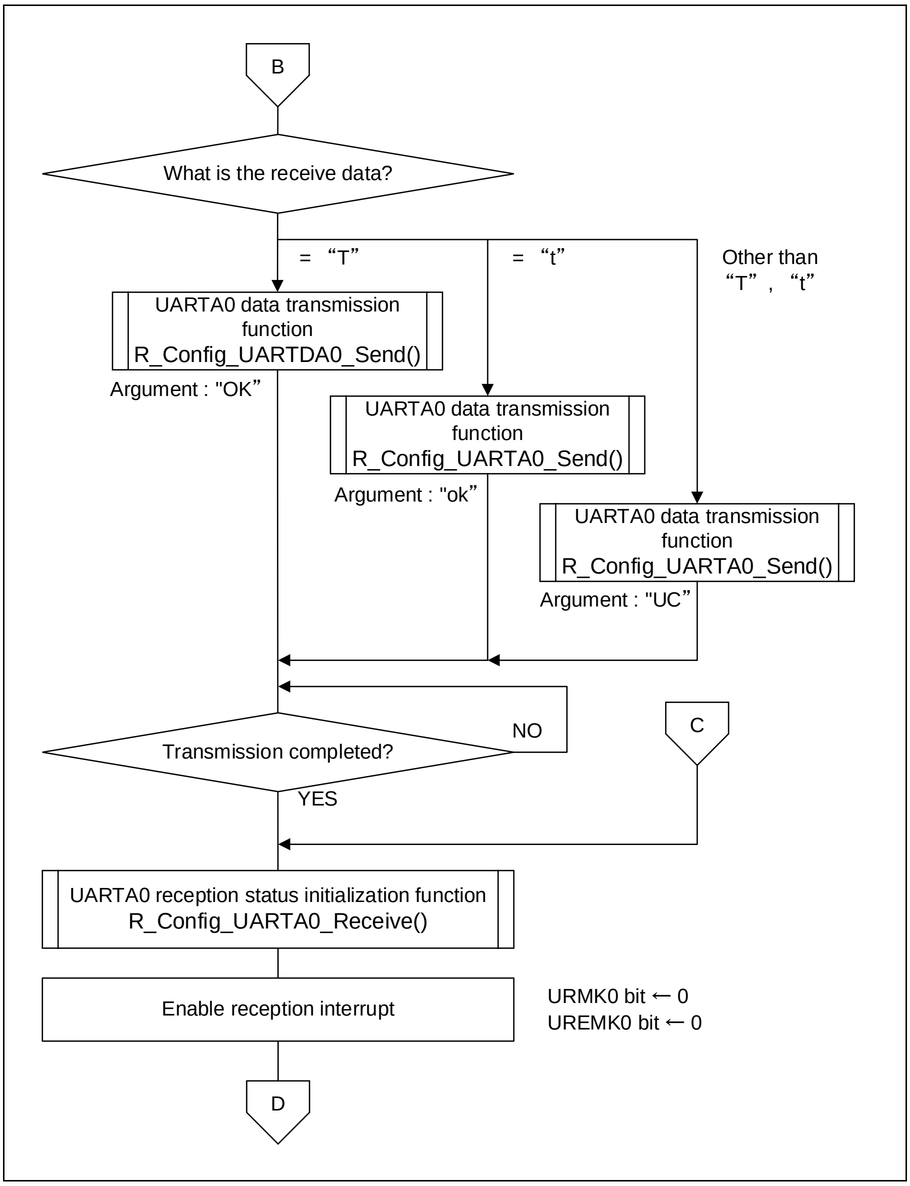


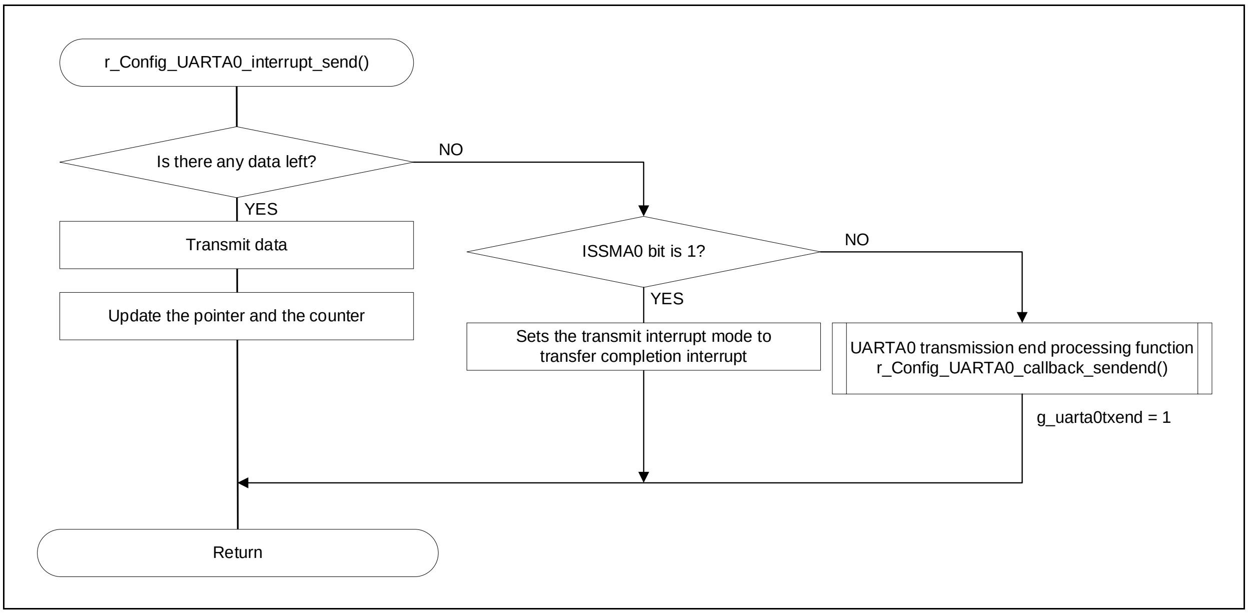
Figure 4-3 Main Processing (3/3)



4.6.2 UARTA0 Transmission End Interrupt Handling

Figure 4-4 shows the flowchart of the UARTA0 transmission end interrupt handling.

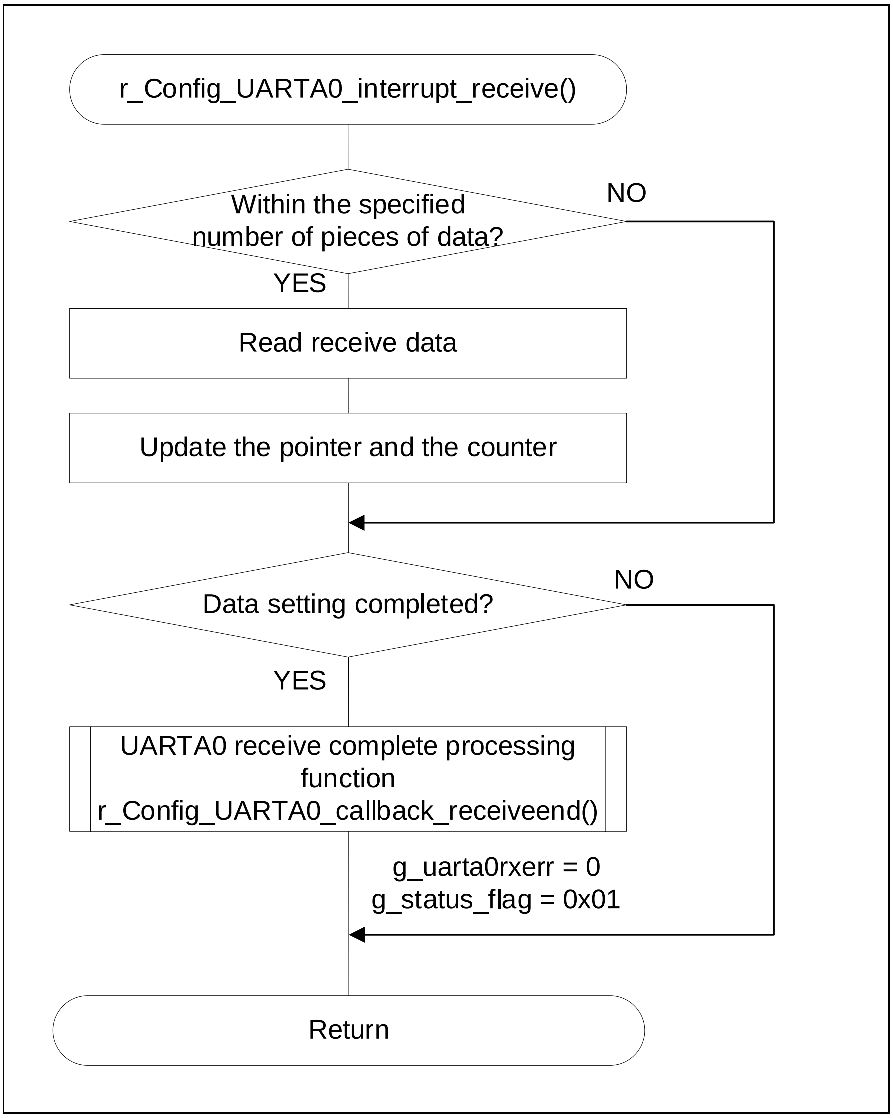
Figure 4-4 UARTA0 Transmission End Interrupt Handling



4.6.3 UARTA0 Reception End Interrupt Handling

Figure 4-5 shows the flowchart of the UARTA0 reception end interrupt handling.

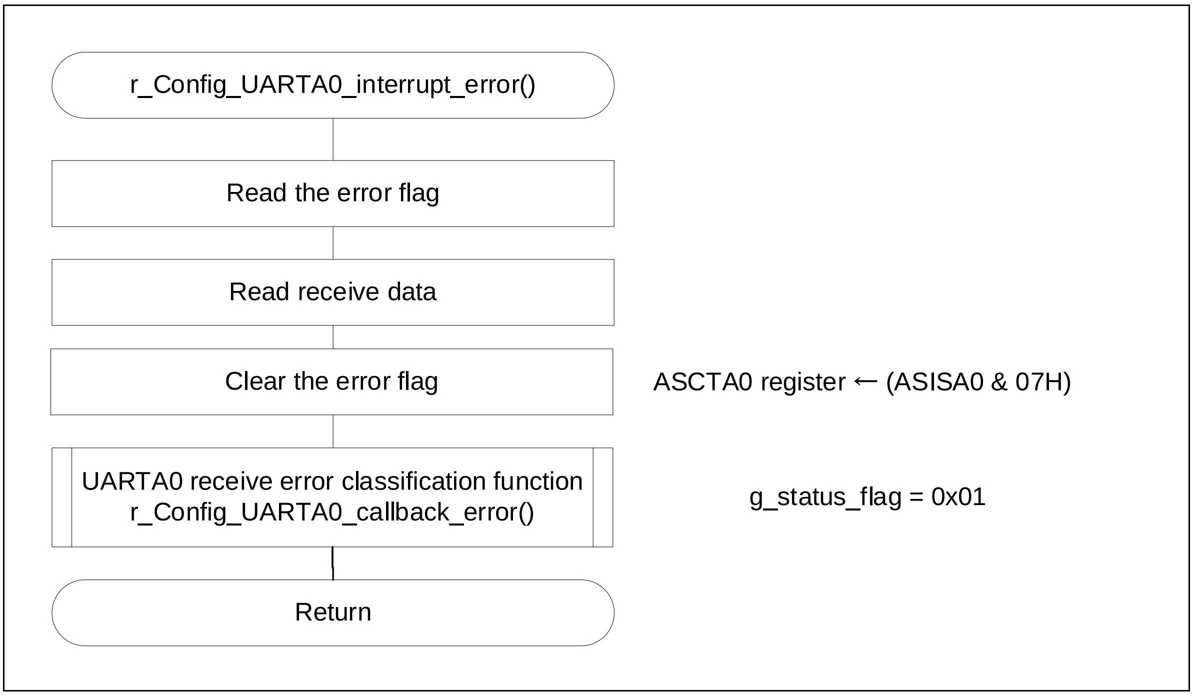
Figure 4-5 UARTA0 Reception End Interrupt Handling



4.6.4 UARTA0 Error Interrupt Handling

Figure 4-6 shows the flowchart of the UARTA0 error interrupt handling.

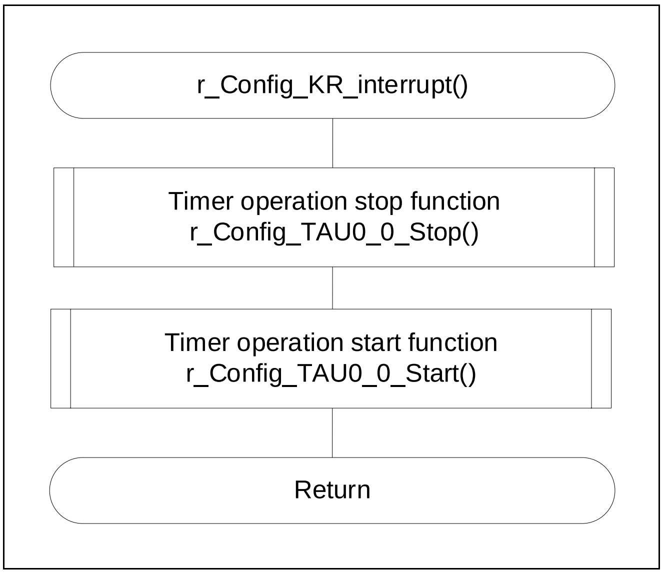
Figure 4-6 UARTA0 Error Interrupt Handling



4.6.5 Key Interrupt Handling

Figure 4-7 shows the flowchart of the Key interrupt handling.

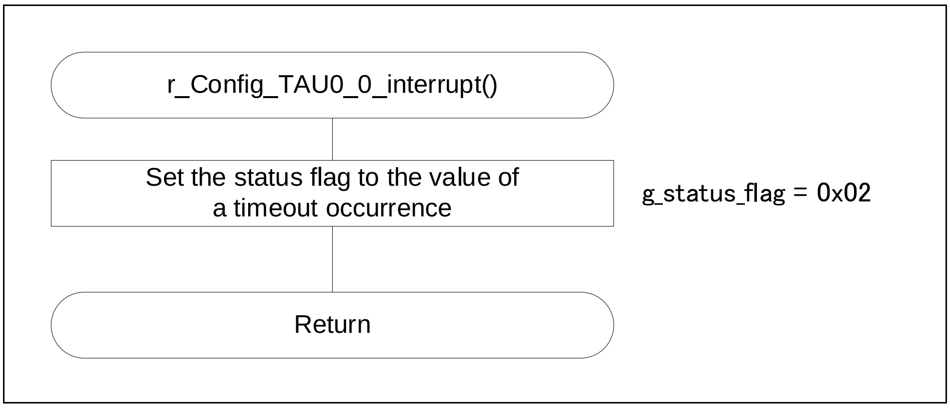
Figure 4-7 Key Interrupt Handling



4.6.6 Timer interrupt handling

Figure 4-8 shows the flowchart of the timer interrupt handling.

Figure 4-8 Timer interrupt handling



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896)
RL78 family user's manual software (R01US0015)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.3.17	-	First Edition
1.10	2023.10.6	p.6	Corrected version of development environment

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   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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(Rev.5.0-1 October 2020)

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