RL78/G23

Transferring A/D Conversion Result Using the DTC

Introduction

This application note describes how to store A/D conversion results of multiple channels in the on-chip RAM using the RL78/G23 DTC and A/D converter (hardware trigger wait mode, select mode, and sequential conversion mode).

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Overview of Specifications

In this application note, the analog input channels of pins P22/ANI2 to P156/ANI7 and P03/ANI16 to P120/ANI19 are converted to digital data, and then A/D conversion results are stored in the on-chip RAM using the DTC.

Table 1-1 lists peripheral functions to be used and their use. Figure 1-1 and Figure 1-2 show the outline of A/D conversion result transfer using the DTC.

Table 1-1 Peripheral Function and Use

Peripheral Function	Use
A/D converter	Converts the analog signal input levels of pins P22/ANI2 to P27/ANI7 and P03/ANI16 to P120/ANI19.
Data transfer controller (DTC)	Transfers A/D conversion results to the on-chip RAM and the ADS register set value from the on-chip RAM.
Realtime clock	Uses the realtime clock interrupt signal (INTRTC) as a hardware trigger.

Figure 1-1 Outline of A/D Conversion Result Transfer Using DTC (Block Diagram)

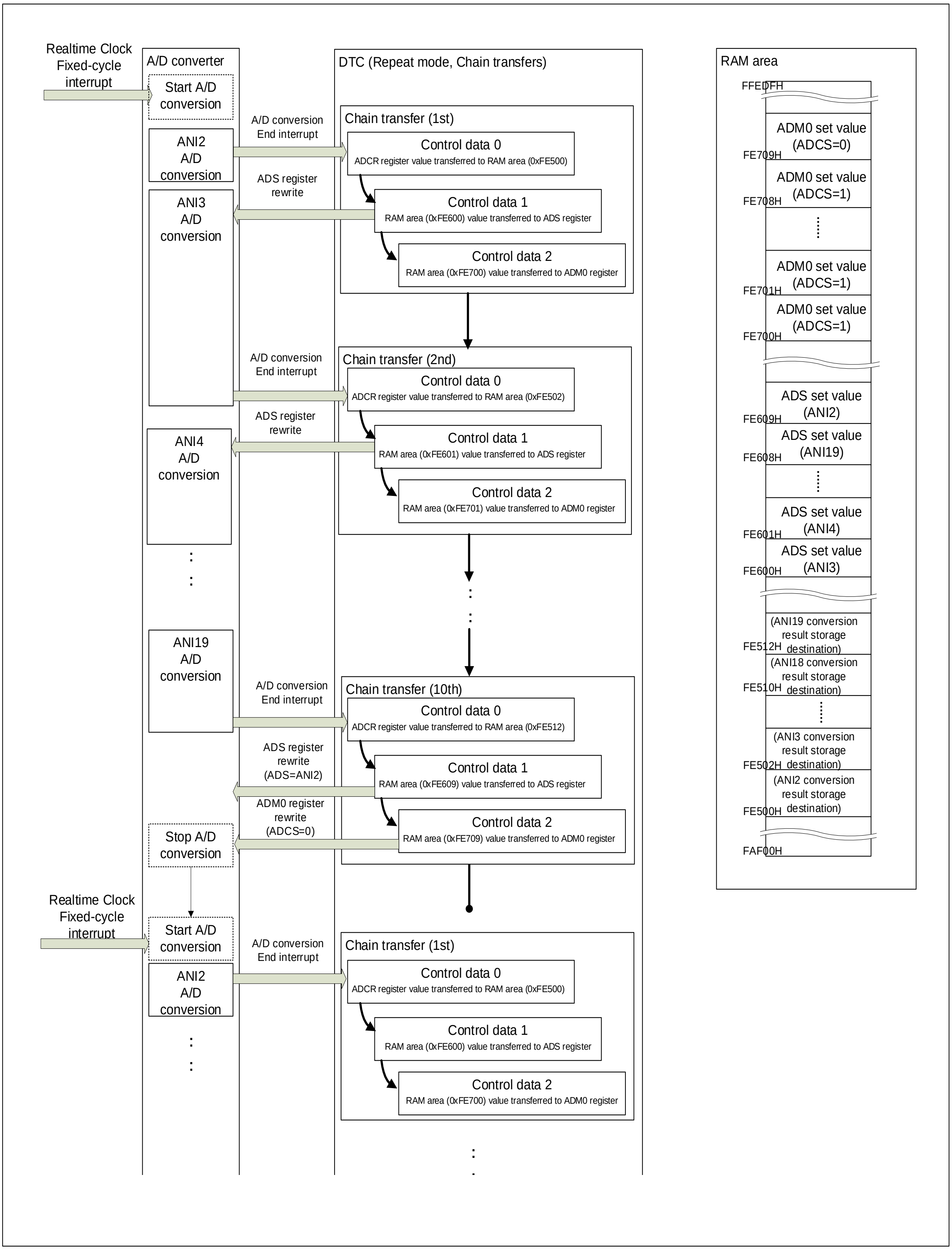
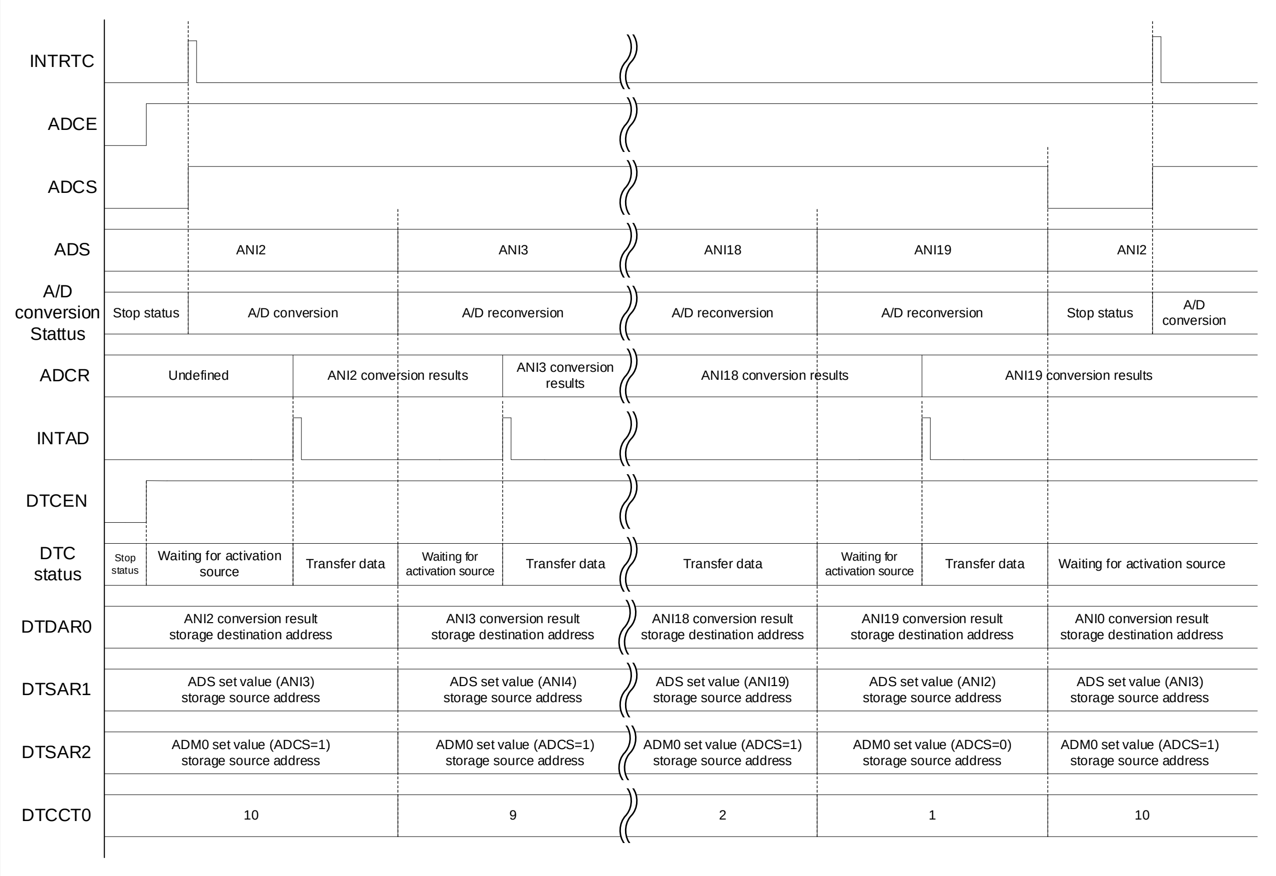


Figure 1-2 Outline of A/D Conversion Result Transfer Using DTC (Timing Chart)



1.2 Outline of Operation

In this sample code, the analog voltages that are input to pins ANI2 to ANI7 and ANI16 to ANI19 are converted to digital data using the A/D converter (hardware trigger wait mode, select mode, and sequential conversion mode). Each A/D conversion result is stored in the on-chip RAM (0xFE500 to 0xFE512) using the DTC.

A/D conversion starts at fixed-cycle interrupts of the realtime clock that occur in HALT mode. The DTC is activated by an A/D conversion end interrupt, and then transfers the A/D conversion result to the on-chip RAM. Furthermore, the DTC transfers the ADS and ADM0 register set values (required for A/D conversion of the next analog input channel) from the on-chip RAM to each register using the DTC's chain transfer. Through repetition of these operations, A/D conversion results of multiple channels are stored in the on-chip RAM. During the last DTC transfer, the ADCS bit in the ADM0 register is cleared to 0 to place the A/D converter in the standby state.

When a fixed-cycle interrupt of the realtime clock occurs again, these operations are repeated.

(1) Initialize the realtime clock (RTC)

<Setting conditions>

- Select the Low-speed on-chip oscillator clock (f_{IL}=32.768kHz) at the RTC operation clock.
- Disable RTC1Hz pin output.
- Enable fixed-cycle interrupt and set their cycle time to 1.0 minute.
- Enable INTRTC interrupts.

(2) Make initial settings for the A/D converter.

<Setting conditions>

- Select 12-bit resolution for A/D conversion.
- Select VDD as the (+) side reference voltage of the A/D converter, and VSS as the (-) side reference voltage.
- Select hardware trigger wait mode, select mode, sequential conversion mode, standard 1, and conversion clock f_{CLK}/32.
- Specify the P22/ANI2 pin as an analog input channel.
- Specify the realtime clock interrupt signal (INTRTC) as a hardware trigger.
- Set the conversion result comparison upper-limit value setting register to FFH, and the conversion result comparison lower-limit value setting register to 00H.
- Select 4 MHz or more as the clock f_{CLK} input frequency.
- Enable A/D conversion end interrupts (INTAD).

(3) Make initial settings for DTCCR0 for data transfer from the ADCR register to the on-chip RAM area.

<Setting conditions>

- Specify A/D conversion completion (source number 10) as a DTC activation source.
- Set the data transfer size to16 bits, and the block size to 2 bytes.
- Set the number of data transfers and the reload value to 10 (number of ANI pins).
- Use chain transfer.
- For repeat mode, set transfer destination to repeat area and specify fixed transfer source address control.
- Specify the 12-bit/10-bit A/D conversion result register (ADCR) for source address.
- Specify the on-chip RAM area for destination address.
- Enable repeat mode interrupts.

(4) Make initial settings for DTCCR1 for data transfer from the on-chip RAM area to the ADS register.

<Setting conditions>

- Set the data transfer size to 8 bits, and the block size to 1 byte.
- Set the number of data transfers and the reload value to 10 (number of A/D conversions).
- Use chain transfer.
- For repeat mode, set transfer source to repeat area and specify fixed transfer destination address control.
- Specify the on-chip RAM area for source address. In this area, arrange ADS register set values consecutively for ANI3 to ANI19 in advance. However, specify ANI2 for the final data (to restart A/D conversion from the ANI2 pin).
- Specify the ADS register for destination address.
- Disable repeat mode interrupts.

(5) Make initial settings for DTCCR2 for data transfer from the on-chip RAM area to the ADM0 register.

<Setting conditions>

- Set the data transfer size to 8 bits, and the block size to 1 byte.
- Set the number of data transfers and the reload value to 10 (number of A/D conversions).
- Disable chain transfer.
- For repeat mode, set transfer source to repeat area and specify fixed transfer destination address control.
- Specify the on-chip RAM area for source address. In this area, arrange ADM0 register set values in advance. First nine set values are ADCS = 1 and the last one is ADCS = 0 (to place the A/D converter in the standby state).
- Specify the ADM0 register for destination address.
- Disable repeat mode interrupts.

(6) Set the ADCE bit in the ADM0 register to 1 (to enable the A/D voltage comparator) to enter the hardware trigger standby state.

(7) Set the DTCEN15 bit in the DTCEN1 register to 1 to activate the DTC at an A/D conversion end interrupt.

(8) Execute the HALT instruction to enter HALT mode.

(9) When a fixed-cycle interrupt of the realtime clock occurs, the ADCS bit in the ADM0 register is set to 1 and A/D conversion starts.

(10) Upon completion of the A/D conversion, the A/D conversion result is stored in the ADCR register and an A/D conversion end interrupt occurs.

(11) The DTC is activated by an A/D conversion end interrupt and the control data in DTCCR0 is read. The A/D conversion result is read from the ADCR register, and is then transferred to the on-chip RAM. After the DTC transfer, the destination address is incremented.

(12) The control data in DTCCR1 is read by chain transfer. Set values stored in the on-chip RAM are transferred to the ADS register. After the transfer, the source address is incremented.

(13) The control data in DTCCR2 is read by chain transfer. Set values stored in the on-chip RAM are transferred to the ADM0 register. After the transfer, the source address is incremented.

(14) Steps (11) to (14) are repeated until the A/D conversion of the analog voltage input to the ANI19 pin finishes. In the last chain transfer, specify ANI2 as an analog input channel and set ADCS to 0 to place the A/D converter in the conversion standby state.

(15) In the interrupt processing after the DTC transfer finishes, reset the HALT mode to return to the processing in step (6).

Table 1-2 shows RAM area information of data used in the DTC.

Table 1-2 RAM Area for Data Used in the DTC

Item	Start Address	Data Size [Byte]	Description
DTC vector table	0xFFD00	40	DTC interrupt source setting table Control data 0 is used at an A/D conversion end interrupt
Control data 0	0xFFD40	8	Control data to transfer the ADCR register value to the RAM area
Control data 1	0xFFD48	8	Control data to transfer the RAM area value to the ADS register
Control data 2	0xFFD50	8	Control data to transfer the RAM area value to the ADM0 register
Control data 0 transfer destination area	0xFE500	20	ADCR register value storage area
Control data 1 transfer source area	0xFE600	10	ADS register set value storage area
Control data 2 transfer source area	0xFE700	10	ADM0 register set value storage area

2. Operation Confirmation Conditions

Operation of the sample code in this application note is confirmed with the conditions shown in Table 2-1.

Table 2-1 Operation Confirmation Conditions

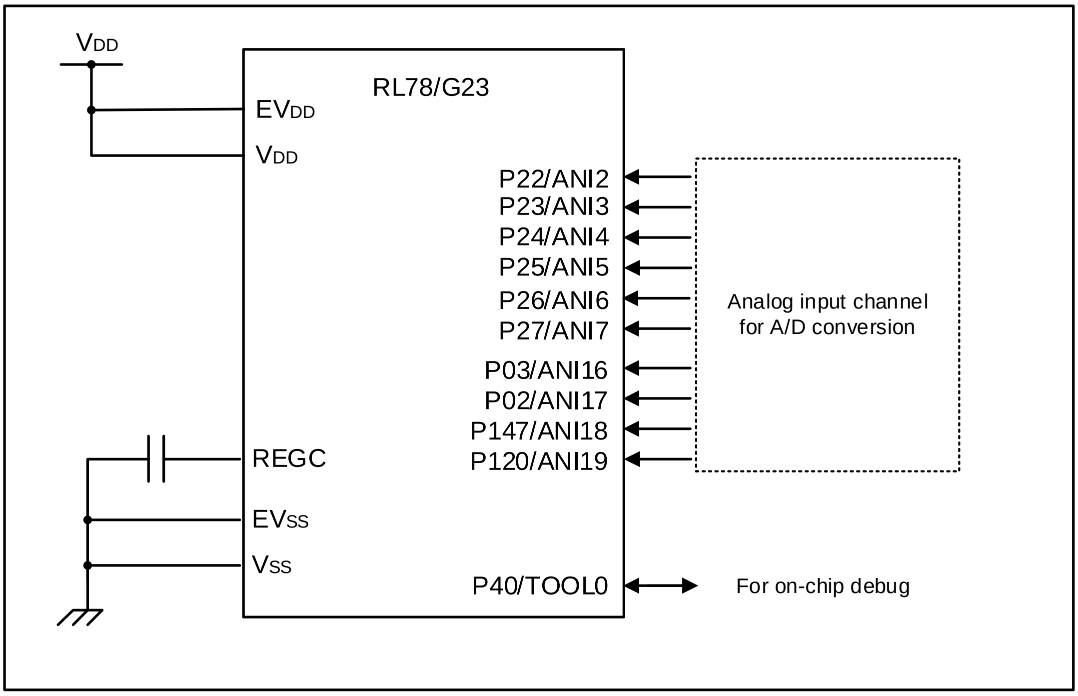
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23-64p Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	• High-speed on-chip oscillator clock (f_{IH}): 32 MHz • Low-speed on-chip oscillator clock (f_{IL}): 32.768 kHz
Operating voltage	5.0 V (can be operated at 2.0 V to 5.5 V) LVD0 operations (V_{LVD0}): Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ for CC E8.09.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2023-04 (23.4.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.2 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.2.2420 from IAR Systems Corp.
Smart configurator (SC)	V1.6.0 from Renesas Electronics Corp.
Board support package (BSP)	V1.60 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This schematic circuit diagram is simplified to show the outline of connections. When creating actual circuits, design them using appropriate pin processing so that the circuits meet electrical characteristics. (Connect input-only ports to V_{DD} or V_{SS} individually through a resistor.)

Note 2. Connect pins (with a name beginning with EV_{SS}), if any, to V_{SS}, and connect pins (with a name beginning with EV_{DD}), if any, to V_{DD}.

Note 3. Set V_{DD} to a voltage not less than the reset release voltage (V_{LVD0}) set by the LVD0.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Function
P22 / ANI2, P23 / ANI3, P24 / ANI4, P25 / ANI5, P26 / ANI6, P27 / ANI7, P03 / ANI16, P02 / ANI17, P147 / ANI18, P120 / ANI19	Input	A/D converter analog input port

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H/ 0 40C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 040C1H	11111110B	LVD0 detection voltage: reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
000C2H / 040C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 040C3H	10000100B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2 Constant

Constant Name	Setting Value	Description
DTC_BASE_ADDR	0x0FFD00	Base address of DTC control data

4.3 List of Variables

Table 4-3 lists global variables.

Table 4-3 Global Variables

Type	Variable Name	Description	Function Used
uint16_t	dtcd0_dst[10]	RAM area to be the DTC control data 0 transfer destination (Address: 0xFE500)	r_Config_DTC_Create_UserInit
uint8_t	dtcd1_src[10]	RAM area to be the DTC control data 1 transfer source (Address: 0xFE600)	r_Config_DTC_Create_UserInit
uint8_t	dtcd2_src[10]	RAM area to be the DTC control data 2 transfer source (Address: 0xFE700)	r_Config_DTC_Create_UserInit

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function Name	Outline
R_Config_DTC_Create_UserInit	User-specified DTC initialization processing

4.5 Specification of Functions

The function specifications of the sample code are shown below.

R_DTC_Create_UserInit

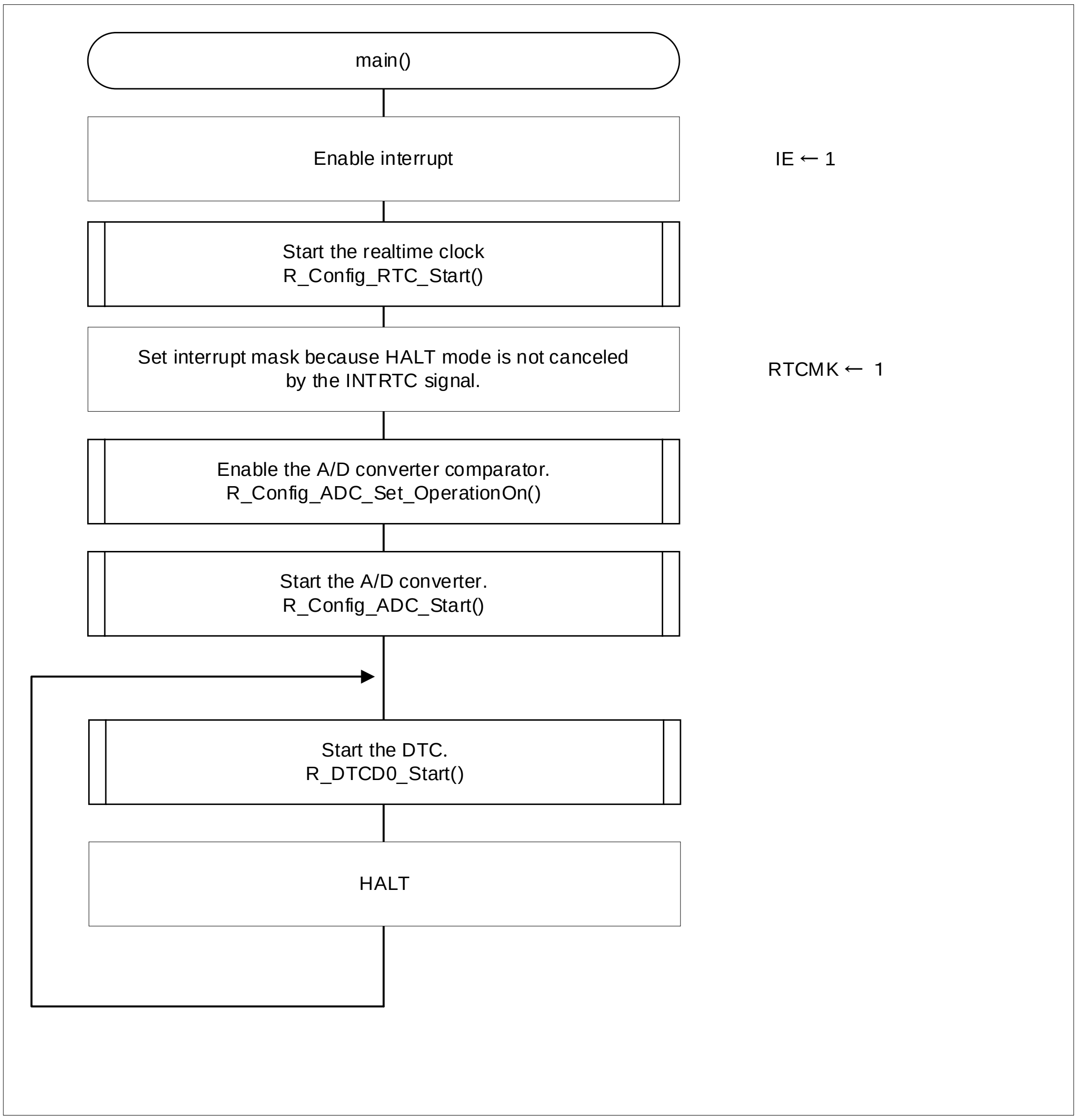
Outline	User-specified DTC initialization processing
Header	Config_DTC.h
Declaration	void R_Config_DTC_Create_UserInit (void) ;
Description	Performs the user-specified processing for initialization required before starting the DTC.
Argument	None
Return Value	None

4.6 Flowcharts

4.6.1 Main Processing

Figure 4-1 shows the flowchart of the main processing.

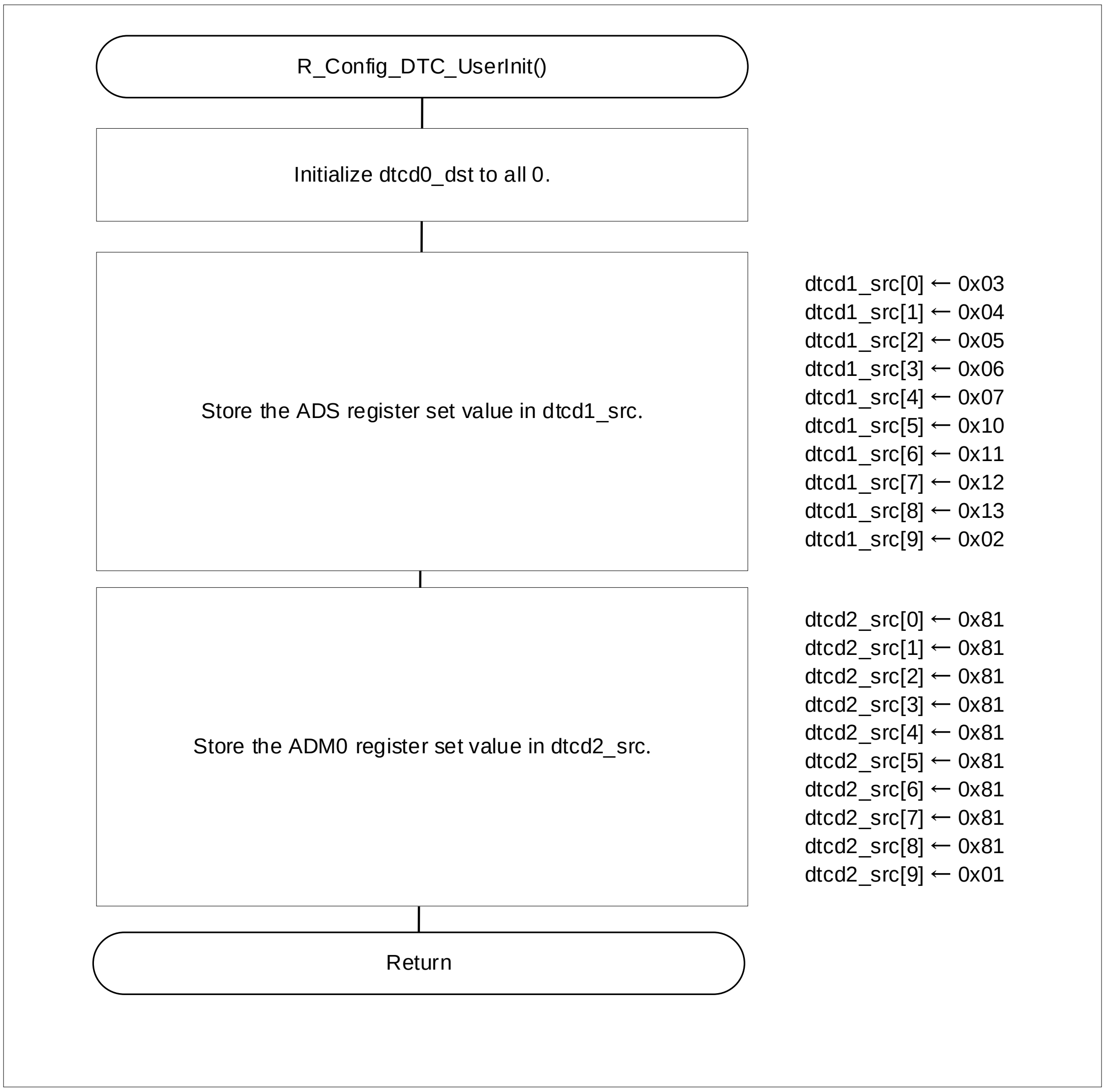
Figure 4-1 Main Processing



4.6.2 User-Specified DTC Initialization Processing

Figure 4-2 shows the flowchart of the user-specified DTC initialization processing.

Figure 4-2 User-Specified DTC Initialization Processing



5. Sample code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896)
RL78 family user's manual software (R01US0015)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2021.04.13	—	First Edition
1.01	2021.07.12	9	Updated the Operation Confirmation Conditions
1.02	2023.10.6	9	Updated the Operation Confirmation Conditions

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2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
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   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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