RL78/G23
Timer Array Unit (PWM output)

Introduction

This application note describes how to use the PWM output function of the timer array unit (TAU). This unit changes the duty cycle of the PWM output pulse cycle and inverts the LED indication at 500 ms intervals.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.
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1. Specifications

1.1 Overview of Specifications

This application note describes the PWM output function which is realized using timer array unit 0 (TAU0) channel 0 as the master and channel 1 as the slave in simultaneous channel operation mode. The brightness of the LEDs is controlled by connecting the PWM output to LED1 (for PWM output). Timing signals with fixed cycle time (500 ms) are created by counting the number of timer interrupts (INTT M00) generated by channel 0. Using these timing signals, the duty cycle of the PWM output pulse cycle is changed and the output of LED2 (for duty cycle updating) is inverted.

Table 1-1 lists the peripheral function to be used and its use. Figure 1-1 shows an overview of PWM output operation. Table 1-2 lists the relation between PWM output duty cycles and LED brightnesses. Figure 1-2 shows a simplified timing chart for PWM output operation.

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer array unit 0 (TAU0) channel 0, channel 1</td>
<td>This unit is used to realize the PWM function by operating channel 0 and channel 1 together and deliver a PWM output from the TO01 pin.</td>
</tr>
</tbody>
</table>

Figure 1-1 Overview of PWM Output Operation

<table>
<thead>
<tr>
<th>Duty cycle</th>
<th>LED1 brightness</th>
</tr>
</thead>
<tbody>
<tr>
<td>10%</td>
<td>90%</td>
</tr>
<tr>
<td>30%</td>
<td>70%</td>
</tr>
<tr>
<td>50%</td>
<td>50%</td>
</tr>
<tr>
<td>70%</td>
<td>30%</td>
</tr>
<tr>
<td>90%</td>
<td>10%</td>
</tr>
</tbody>
</table>

Table 1-2 Relation between PWM Output Duty Cycles and LED Brightnesses
Figure 1-2 Simplified Timing Chart for PWM Output Operation

Master channel

Slave channel

Software

Counts INTTM00 interrupts

Duty cycle: 10%

Duty cycle: 30%

Duty factor updated 250
1.2 Outline of Operation

The sample program covered in this application note implements PWM by operating channel 0 and channel 1 together and delivers a PWM output from P16/TO01.

Also, this program counts 250 timer interrupts (INTTM00) with 2 ms cycle time which are generated by channel 0. Then, it changes the duty cycle of the PWM output pulse cycle and inverts the LED indication at 500 ms intervals.

1. Initialize the TAU.
   - Set TAU0 channel 0 (master channel) to interval timer mode.
   - Set TAU0 channel 1 (slave channel) to one-count mode.
   - Set PWM output pulse cycle to 2 ms.
   - Set the output level of TO01 pin to active-low.
   - Set the low-level output width of TO01 pin to 90% of the PWM output pulse cycle.
   - Set the P16/TO01 pin to a PWM output.
   - Set the initial output value of TO01 pin to 1.
   - Use timer interrupts (INTTM00) from timer channel 0.

2. Initialize the I/O port.
   - P52 pin: Set as an output port.

3. Operation starts when both trigger bits to enable operation for TAU0’s channel 0 and channel 1 are set to 1 simultaneously. The sample program executes a HALT instruction to wait for a timer interrupt (INTTM00) from channel 0.

4. After the start of timer operation, channel 0 generates a timer interrupt (INTTM00) at 2 ms intervals.

5. When the HALT mode is canceled by a timer interrupt (INTTM00) from channel 0, the sample program starts counting the number of INTTM00 interrupts generated. After channel 0 has generated 250 timer interrupts (i.e., after 500 ms), the sample program changes the duty cycle by updating timer data register (TDR01) of channel 1. This duty cycle is increased from 10% to 90% (10% → 30% → 50% → 70% → 90%). It is incremented by 20% each time the number of channel 0 timer interrupts (INTTM00) generated reaches 250. (Thus, it is incremented at 500 ms intervals). It is reset to 10% after it becomes 90%.

6. After processing timer interrupts (INTTM00) from channel 0, the sample program executes another HALT instruction and waits for the next timer interrupt (INTTM00) from channel 0.
2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU used</td>
<td>RL78/G23 (R7F100GLG)</td>
</tr>
<tr>
<td>Board used</td>
<td>RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>High-speed on-chip oscillator clock: 32 MHz</td>
</tr>
<tr>
<td></td>
<td>CPU/peripheral hardware clock: 32 MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>3.3 V (can be operated at 1.8 V to 5.5 V)</td>
</tr>
<tr>
<td></td>
<td>LVD0 detection voltage: Reset mode</td>
</tr>
<tr>
<td></td>
<td>At rising edge TYP. 1.90 V (1.84 V to 1.95 V)</td>
</tr>
<tr>
<td></td>
<td>At falling edge TYP. 1.86 V (1.80 V to 1.91 V)</td>
</tr>
<tr>
<td>Integrated development environment (CS+)</td>
<td>CS+ V8.05.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>C compiler (CS+)</td>
<td>CC-RL V1.10.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development environment (e2studio)</td>
<td>e2 studio V2021-04 (21.4.0) from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>C compiler (e2studio)</td>
<td>CC-RL V1.10.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development environment (IAR)</td>
<td>IAR Embedded Workbench for Renesas RL78 V4.21.1 from IAR Systems Corp.</td>
</tr>
<tr>
<td>C compiler (IAR)</td>
<td>IAR C/C++ Compiler for Renesas RL78 V4.21.1 from IAR Systems Corp.</td>
</tr>
<tr>
<td>Smart configurator (SC)</td>
<td>V1.0.1 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Board support package (BSP)</td>
<td>V1.00 from Renesas Electronics Corp.</td>
</tr>
</tbody>
</table>
3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration

Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to VDD or VSS through a resistor).

Note 2. Connect any pins whose name begins with EVSS to VSS, and any pins whose name begins with EVDD to VDD, respectively.

Note 3. VDD must not be lower than the reset release voltage (VLVD0) that is specified for the LVD0.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

<table>
<thead>
<tr>
<th>Pin name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P16 / TO01</td>
<td>Output</td>
<td>PWM output port (controls LED1)</td>
</tr>
<tr>
<td>P52</td>
<td>Output</td>
<td>Output port for LED indications (controls LED2)</td>
</tr>
</tbody>
</table>
4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings. Set the values that are most suited to your system as necessary.

<table>
<thead>
<tr>
<th>Address</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>000C0H / 040C0H</td>
<td>11101111B</td>
<td>Disables the watchdog timer. (Counting stopped after reset)</td>
</tr>
<tr>
<td>000C1H / 040C1H</td>
<td>11111110B</td>
<td>LVD0 detection voltage: reset mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At rising edge TYP. 1.90 V (1.84 V to 1.95 V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At falling edge TYP. 1.86 V (1.80 V to 1.91 V)</td>
</tr>
<tr>
<td>000C2H / 040C2H</td>
<td>11101000B</td>
<td>HS mode,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-speed on-chip oscillator clock (fIH): 32 MHz</td>
</tr>
<tr>
<td>000C3H / 040C3H</td>
<td>10000101B</td>
<td>Enables on-chip debugging</td>
</tr>
</tbody>
</table>

4.2 List of Constants

Table 4-2 shows the constants that are used in this sample program.

<table>
<thead>
<tr>
<th>Constant</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>_E100_TAU_TDR01_VALUE</td>
<td>E100H</td>
<td>Initial setting value of TDR01</td>
</tr>
</tbody>
</table>

4.3 List of Functions

Table 4-3 shows a list of functions.

<table>
<thead>
<tr>
<th>Function name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>r_Config_TAU0_0_interrupt()</td>
<td>TAU0 channel 0 timer interrupt processing</td>
</tr>
</tbody>
</table>

4.4 Specification of Functions

The function specifications of the sample code are shown below.

```
r_Config_TAU0_0_interrupt()
Outline    TAU0 channel 0 timer interrupt processing
Header     r_cg_macroadriver.h, r_cg_userdefine.h, Config_TAU0_0.h
Declaration static void __near r_Config_TAU0_0_interrupt(void)
Description This function counts the number of INTTM00 interrupts generated. Each time the count reaches 250, it updates the duty cycle of the PWM output pulse cycle. (Thus, it updates the duty cycle at 500 ms intervals.)
Argument   None
Return Value None
```
4.5 Flowcharts
4.5.1 Main Processing

Figure 4-1 shows the flowchart of the main processing.

Figure 4-1  Main Processing

```
main

Start operation of TAU0 channel 0 and channel 1
R_Config_TAU0_0_Start()

Enable interrupts

HALT

IE ← 1

: while(1) loop

TAU0 channel 0 timer interrupt (INTTM00)
```
4.5.2 TAU0 Channel 0 Timer Interrupt Processing

Figure 4-2 shows the flowchart of TAU0 channel 0 timer interrupt processing.

Figure 4-2 TAU0 Channel 0 Timer Interrupt Processing

```
   r_Config_TAU0_0_interrupt
       Counter + 1
           tm00_count + 1
       NO
           500 ms have elapsed?
               YES
                   Counter = 0
                       tm00_count = 0
                   Invert P52 output
                   Read current duty cycle
                       temp_duty ← TDR01 register
                       Current duty cycle ?
                           Less than 90%
                                           Initialize duty cycle to 10%
                                           Update duty cycle
                                           return
                           90% or more
                                           Increase duty cycle by 20%
                                           TDR01 register ← temp_duty
                       Update duty cycle
```
5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896J)
RL78 family user’s manual software (R01US0015J)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

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### Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Jun.09.2021</td>
<td>-</td>
<td>-</td>
<td>First Edition</td>
</tr>
</tbody>
</table>

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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

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   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

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