

RL78/G23

Safety Function (Flash Memory CRC Operation Function)

Introduction

This application note explains how to use the flash memory CRC operation function, which is one of the safety functions incorporated in the RL78/G23.

The high-speed CRC performs operation on and compares the data in the code flash memory (addresses 00000H to 0FFFBH) with the results of the operation performed by the object converter.

The general-purpose CRC performs operation on the data in a part of the on-chip RAM and compares their results with the results of the operation performed again in the same area. The data to be operated on can be changed using by switch input.

Both of the high-speed CRC and general-purpose CRC turn on an LED when the results of the operation match.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specifications

1.1 Specification Outline

This application note explains how to use the flash memory CRC operation function, which is one of the safety functions incorporated in the RL78/G23.

The high-speed CRC performs operation on and compares the data in the code flash memory (addresses 00000H to 0FFFBH) with the results of the operation performed by the object converter.

The general-purpose CRC performs operation on the data in a part of the on-chip RAM and compares their results with the results of the operation performed again in the same area. The data to be operated on can be changed using switch input.

Both of the high-speed CRC and general-purpose CRC turn on an LED when the results of the operation match.

Table 1 - 1 lists the Peripheral Functions to be Used and their Uses. Figure 1 - 1 shows the Outline of High-speed CRC Operation. Figure 1 - 2 shows the Outline of General-purpose CRC Operation.

Table 1 - 1 Peripheral Functions to be Used and their Uses

Peripheral Function	Use
Safety function: Flash memory CRC operation function	Performs high-speed CRC and general-purpose CRC operation in a specified memory area and compares their results with the separately prepared values to verify the validity of the data.

Figure 1 - 1 Outline of High-speed CRC Operation

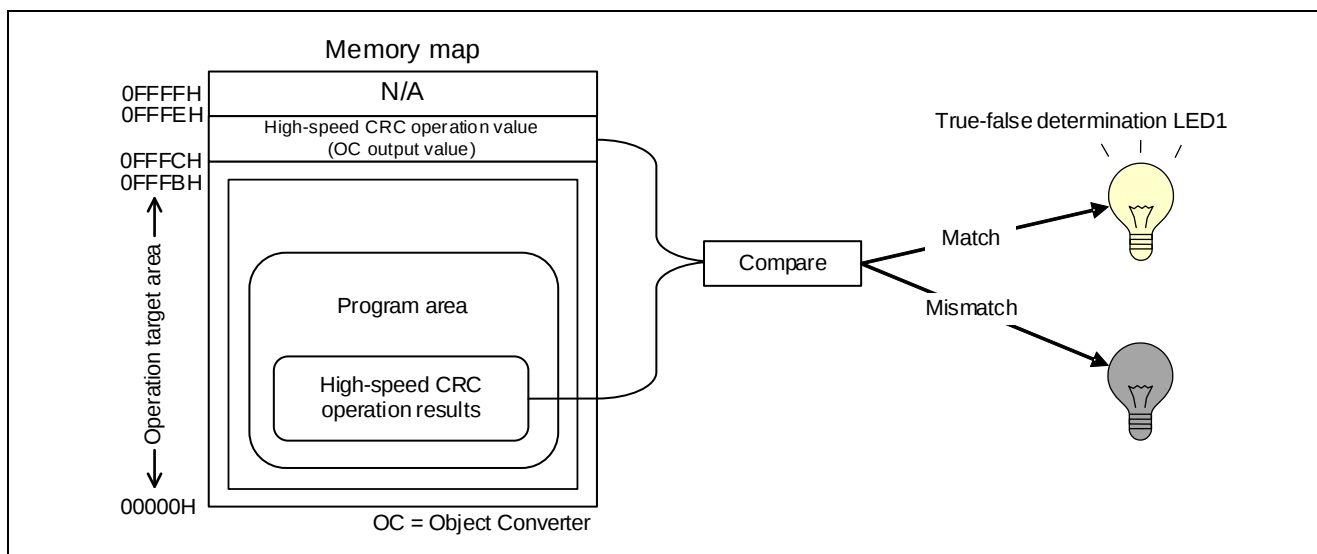
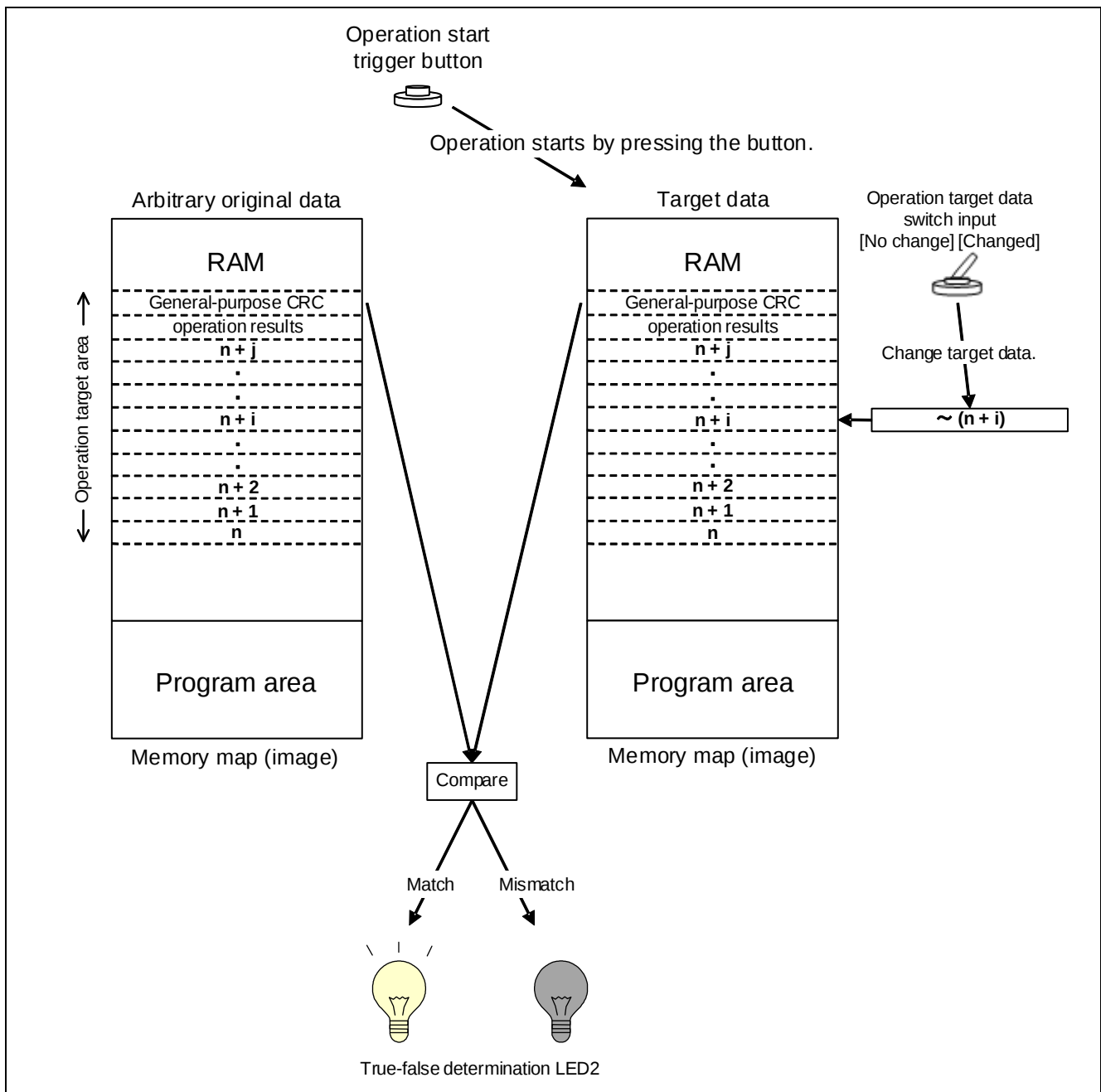


Figure 1 - 2 Outline of General-purpose CRC Operation



1.2 Operation Outline

The sample application covered in this application note uses the flash memory CRC operation function, which is one of the safety functions incorporated in the RL78/G23.

The high-speed CRC performs operation on and compares the data in the code flash memory (addresses 00000H to 0FFFBH) with the results of the operation performed by the object converter.

The general-purpose CRC performs operation on the data in a part of the on-chip RAM and compares their results with the results of the operation performed again in the same area. The data to be operated on can be changed by using switch input.

Both of the high-speed CRC and general-purpose CRC turn on an LED when the results of the operation match.

(1) Initialize the flash memory CRC operation function.

<Conditions for setting>

- Set the range of the area on which high-speed CRC operation is to be performed to the flash memory (addresses 00000H to 0FFFBH).
- Set the operation mode of the high-speed CRC to "Start operation on the execution of a HALT instruction."

(2) Initialize the operation control ports.

<Conditions for setting>

- General-purpose CRC operation target data switching: Set up P50 as an input port (using an on-chip pull-up resistor).
- LED1 /2 output (CRC operation true-false determination result): Set up P53 and P52 as output ports.
- General-purpose CRC operation start trigger button: Set up P137/INTP0 in INTP0 falling edge detection interrupt mode (using an on-chip pull-up resistor).

(3) Perform high-speed CRC operation on the flash memory (addresses 00000H to 0FFFBH).

(4) Compare the results obtained in step (3) with the target values (specified in advance at build time) that are generated in the flash memory (addresses 0FFFCH to 0FFFDH) by the object converter and turns on LED1 if they match.

(5) Store arbitrary data and the results of general-purpose CRC operation in the general-purpose CRC operation target area (part of the on-chip RAM).

(6) Enter the HALT mode and waits for a general-purpose CRC operation start trigger (INTP0).

(7) Exit the HALT mode on the occurrence of a CRC operation start trigger and update the general-purpose CRC operation target data if the state of the general-purpose CRC operation target data switch is "Changed."

(8) Perform general-purpose CRC operation.

(9) Turn on LED2 if the results obtained in step (8) match the ones obtained in step (5). Otherwise, turn off the LED2.

(10) Repeat steps (5) to (9).

Caution 1. When building the application, disable on-chip debugging with the link option. This is because addresses 0FFFCH to 0FFFDH which are to be used to store the results of high-speed CRC operation as the target of comparison are also reserved for the on-chip debugger and a conflict would otherwise occur.

Caution 2. When checking the application for normal operation, write HEX data (File format: mot, srec, and so on) into the RL78/G23 using a flash memory programmer that is compatible with the RL78/G23.

Caution 3. For detailed usage notes on the product, refer to RL78/G23 User's Manual: Hardware.

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2 - 1 Operation Confirmation Conditions

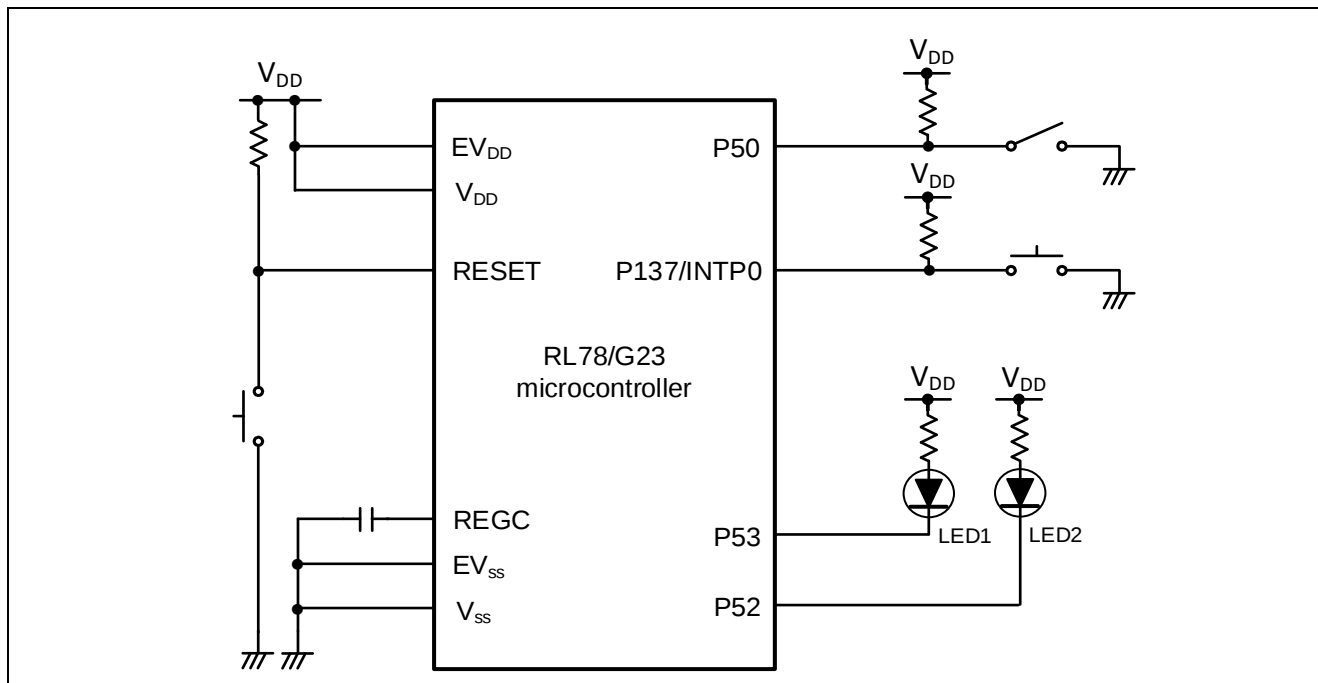
Item	Description
Microcontroller used	RL78/G23 (R7F100GLG)
Operating frequency	- High-speed on-chip oscillator (HOCO) clock: 32 MHz - CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can be operated at 1.8 V to 5.5 V) LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ for CC V8.10.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.01 from Renesas Electronics Corp.
Integrated development environment (e ² studio)	e ² studio V2023-10 (23.10.0) from Renesas Electronics Corp.
C compiler (e ² studio)	CC-RL V1.12.01 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V5.10.1 from IAR Systems
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V5.10.1 from IAR Systems Corp.
Smart configurator (SC)	V1.8.0 from Renesas Electronics Corp.
Board support package (BSP)	V1.00 from Renesas Electronics Corp.
Flash memory programmer	E2 emulator Lite (RTE0T0002LKCE00000R) from Renesas Electronics Corp.
Flash memory programming software	Renesas Flash Programmer V3.11.02 from Renesas Electronics Corp.

3. Description of the Hardware

3.1 Hardware Configuration Example

The example of configuration of the hardware that is used for this application note is shown below.

Figure 3 - 1 Hardware Configuration



Note 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

Note 2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD} , respectively.

Note 3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

3.2 List of Pins to be used

Table 3 - 1 lists the pins to be used and their functions.

Table 3 - 1 Pins to be Used and their Functions

Pin Name	I/O	Description
P50	Input	General-purpose CRC operation target data switching input (changed/no change)
P53	Output	LED1 lighting control port (high-speed CRC operation result output)
P52	Output	LED2 lighting control port (general-purpose CRC operation result output)
P137/INTP0	Input	General-purpose CRC operation start trigger input

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Description of the Software

4.1 List of Option Byte Settings

Table 4 - 1 summarizes the settings of the option bytes.

Table 4 - 1 Option Byte Settings

Address	Value	Description
000C0H / 010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H / 010C1H	11111110B	LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
000C2H / 010C2H	11101000B	HS mode HOCO: 32 MHz
000C3H / 010C3H	00000100B	Prohibits the on-chip debugger.

4.2 List of Constants

Table 4 - 2 lists the constants that are used in this sample program.

Table 4 - 2 Constants for the Sample Program

Constant	Setting	Description
HIGHSPEED_CALC_ADDR	0x0FFFC	Address at which the results of the high-speed CRC operation generated by the object converter are to be stored
GP_CALC_BUFF_SIZE	254	Size of the general-purpose CRC operation target buffer (excluding the 2 bytes in the area storing operation result)

4.3 List of Variables

Table 4 - 3 lists the global variable that is used by this sample program.

Table 4 - 3 Global Variable

Type	Variable Name	Contents	Function Used
uint8_t	calc_data[GP_CALC_BUFF_SIZE+2]	Area for storing the general-purpose CRC operation target data	main() R_CreateDataForComparison() R_GeneralPurposeCRCProc()

4.4 List of Functions

Table 4 - 4 lists the functions that are used in this sample program.

Table 4 - 4 Functions

Function Name	Outline
R_HighSpeedCRCProc()	High-speed CRC operation processing
R_CGC_Set_CRCon()	Enable high-speed CRC ALU operation
R_ExecHighSpeedCRC()	Execution of high-speed CRC operation
R_CreateDataForComparison()	Creation of general-purpose CRC operation target data
R_GeneralPurposeCRCProc()	General-purpose CRC operation processing

4.5 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name]] R_HighSpeedCRCProc()

Synopsis	High-speed CRC operation processing
Header	—
Declaration	uint16_t R_HighSpeedCRCProc(void)
Explanation	This function performs high-speed CRC operation and returns the results.
Arguments	None
Return value	Results of high-speed CRC operation
Remarks	None

[Function Name]] R_CGC_Set_CRCon()

Synopsis	Enable high-speed CRC ALU operation
Header	—
Declaration	void R_CGC_Set_CRCon(void)
Explanation	Enable high-speed CRC ALU operation (starts the operation according to HALT instruction execution).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ExecHighSpeedCRC()

Synopsis	Execution of high-speed CRC operation
Header	—
Declaration	void R_ExecHighSpeedCRC(void)
Explanation	This function expands the HALT and RET instructions in the on-chip RAM (stack area) to start high-speed CRC operation. This function also executes the HALT and RET instructions that are expanded in the on-chip RAM.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_CreateDataForComparison()

Synopsis	Creation of general-purpose CRC operation target data	
Header	—	
Declaration	void R_CreateDataForComparison(uint8_t *data, uint8_t size)	
Explanation	This function creates the target data to be subjected to general-purpose CRC operation. Performs general-purpose CRC operation on that data and places the results in the given area.	
Arguments	*data	Pointer to the area storing the target data
Return value	size	Size of the area storing the target data
Remarks	None	
Synopsis	None	

[Function Name] R_GeneralPurposeCRCProc()

Synopsis	General-purpose CRC operation processing	
Header	—	
Declaration	uint16_t R_GeneralPurposeCRCProc(uint8_t *data, uint8_t size)	
Explanation	This function performs general-purpose CRC operation and returns the results.	
Arguments	*data	Pointer to the target data
	size	Size of the target data
Return value	Result of the general-purpose CRC operation	
Remarks	None	

4.6 Flowcharts

4.6.1 Main Processing

Figure 4 - 1 and Figure 4 - 2 show the flowchart for the main processing.

Figure 4 - 1 Main Processing (1/2)

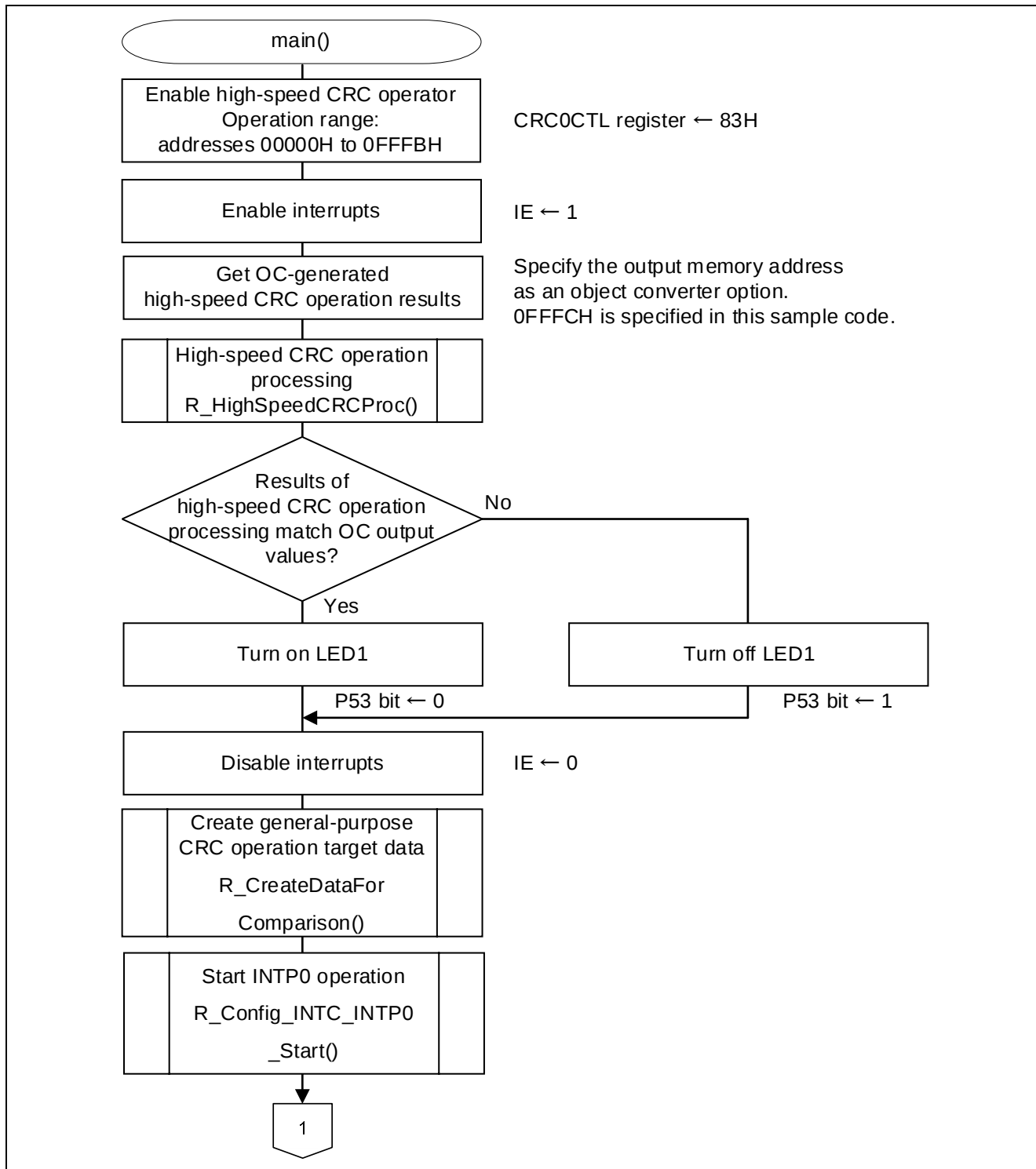
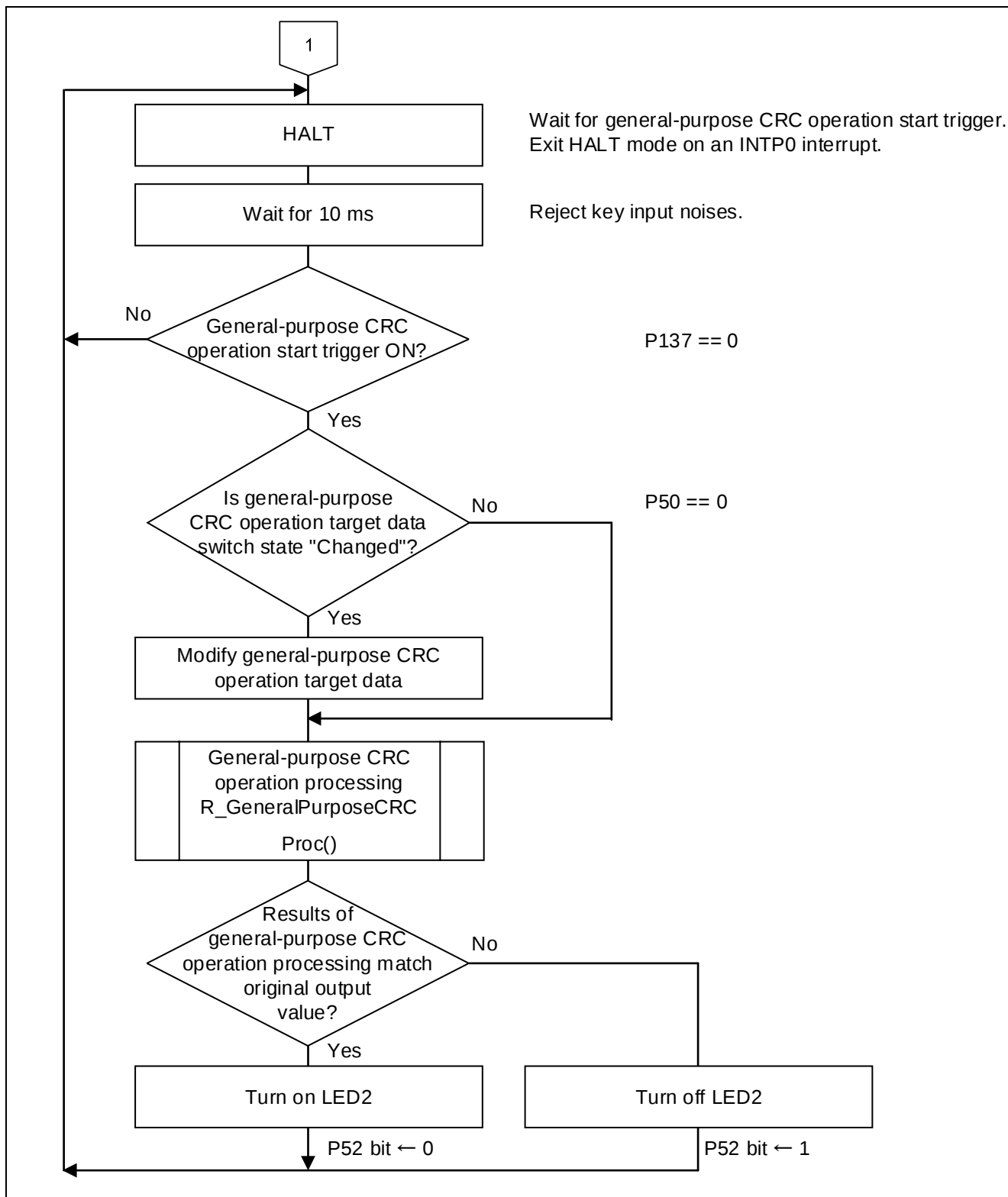


Figure 4 - 2 Main Processing (2/2)



- Object converter option settings
 - CRC operation
 - Do CRC operation: Yes
 - CRC result output address: 0FFFCH
 - CRC operation range: Addresses 00000H to 0FFFBH
 - CRC operation mode: CRC-CCITT(MSB) type

Figure 4 - 3 Object Converter Option Settings (Properties window of CS+ CC-RL build tool)

CC-RL Property

Output File	
Output hex file	Yes
Output folder	%BuildModeName%
Output file name	%ProjectName%.mot
Load address	HEX
Division output file	Division output file[0]
Hex Format	
Hex file format	Motorola S-record file(-F0m=Stype)
Unify record size	No
Output hex file with fixed record length from aligned start address	No
Specify byte count for data record	No
Specify end record	Not specify(No option specified)
Output S9 record at the end	No
CRC Operation	
Outputs the calculation result of CRC	Yes(-CRc)
Output address	HEX FFFC
Target range	Target range[1]
[0]	0-FFFB
Type of CRC	CRC-CCITT(MSB,LITTLE,4 bytes) type(High-speed CRC)
Initial value	HEX 0
Endian	Little endian
Output size	2

Outputs the calculation result of CRC
 Selects whether to generate CRC code.
 This corresponds to the -CRc option of the rlink command.

Common Options / Compile Options / AssembleOptions / SMS Assemble Options / Link Options / **Hex Output Options**

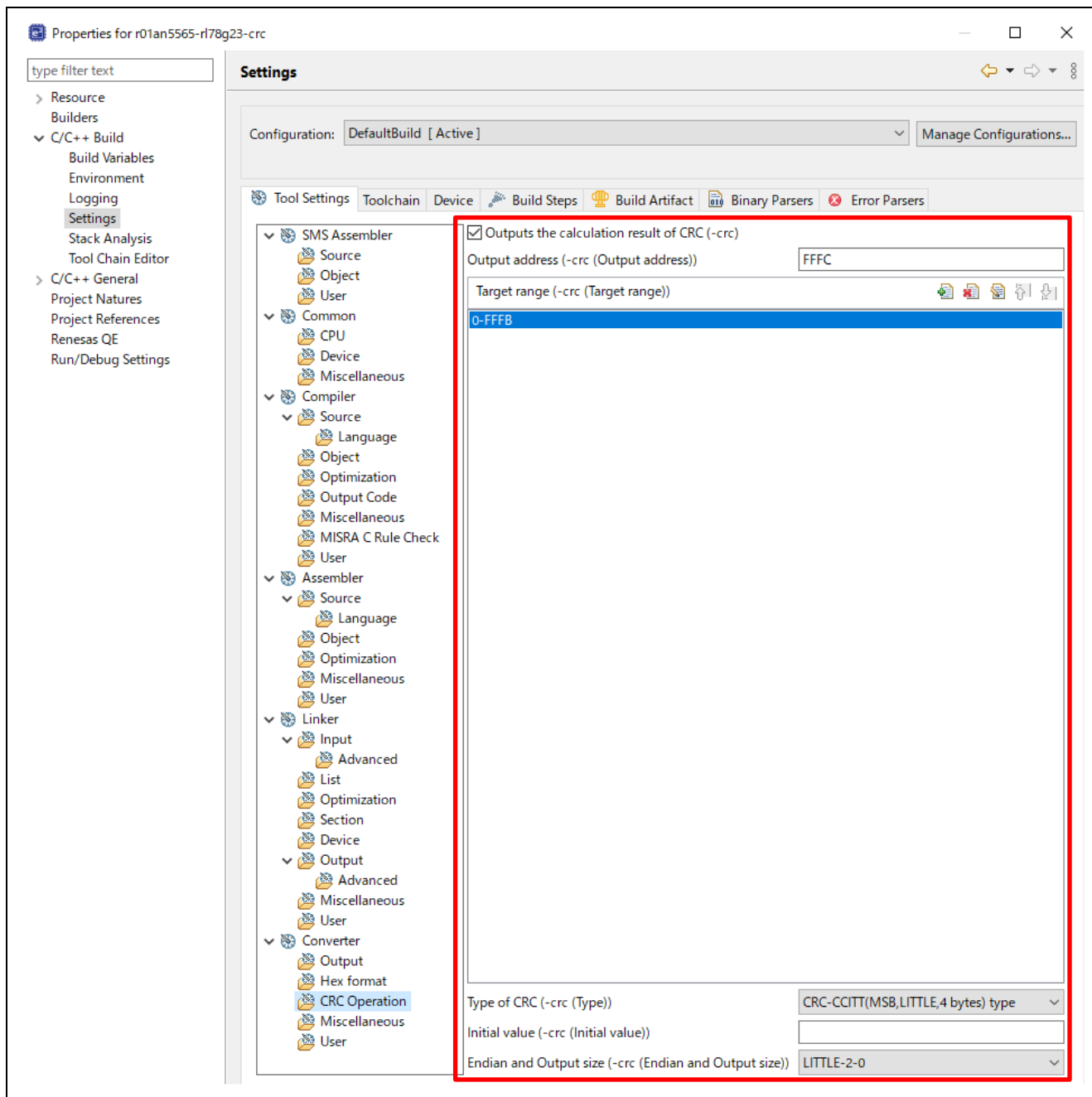
Figure 4 - 4 Object Converter Option Settings (Properties window of e² studio)

Figure 4 - 5 Object Converter Option Settings (Options window of IAR)

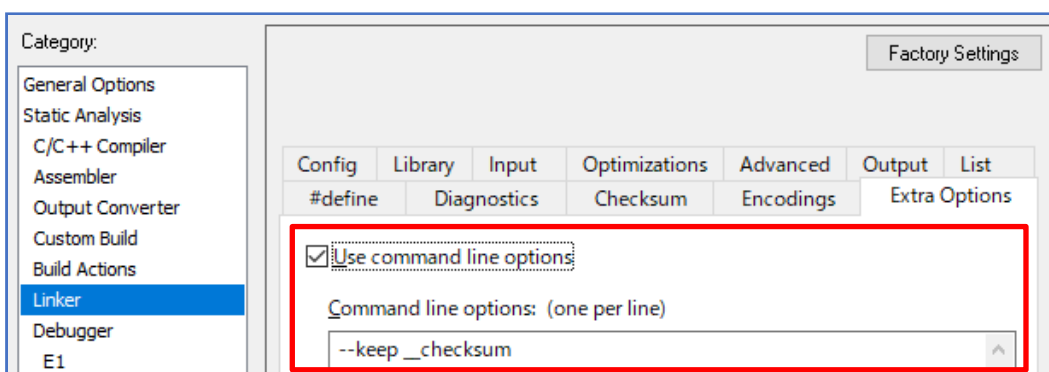
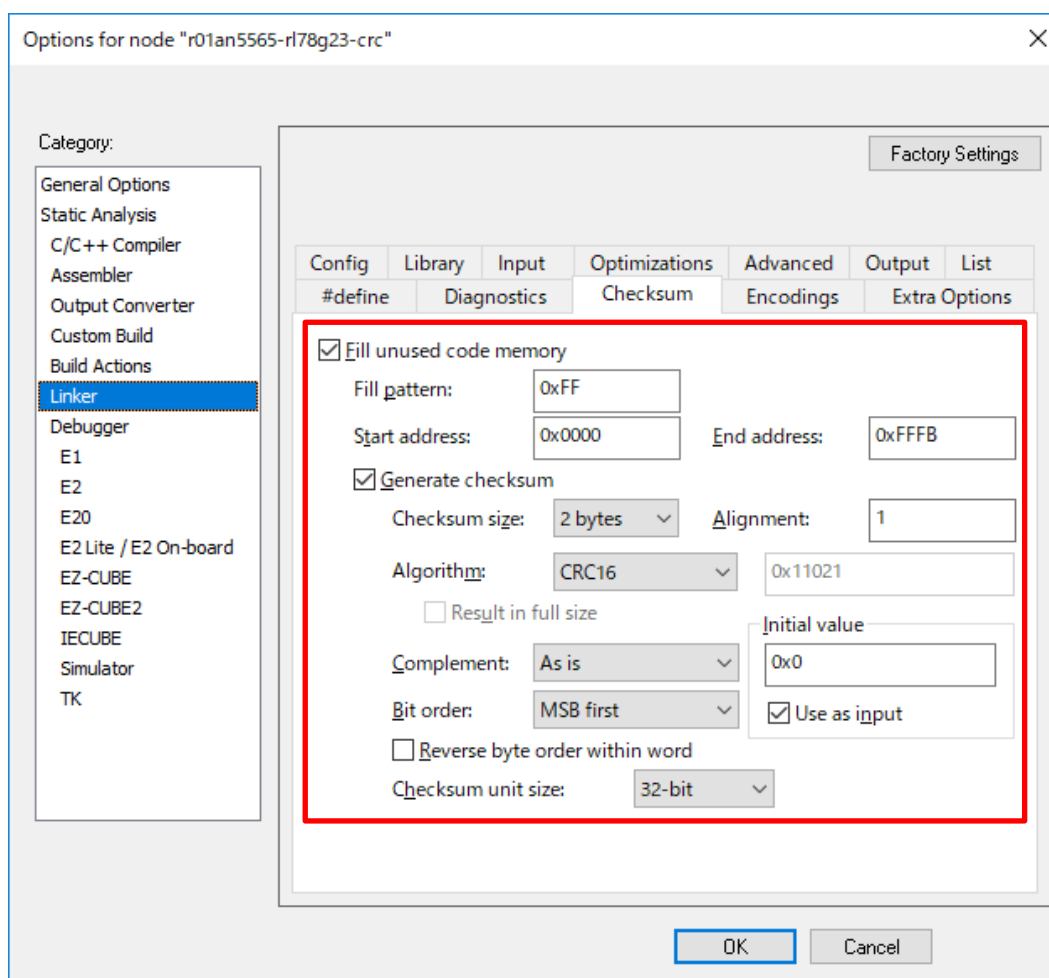
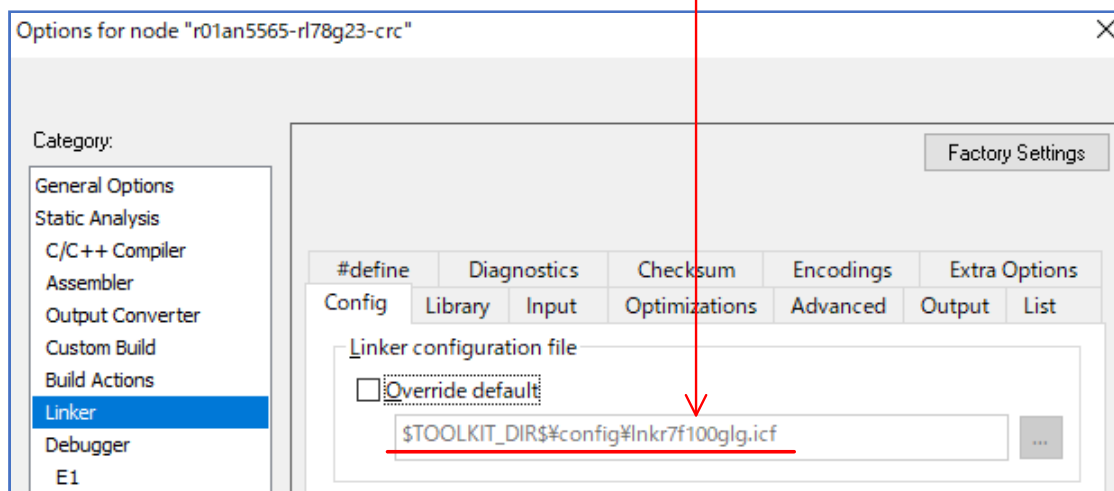


Figure 4 - 6 Checksum Output Address Settings (Options window of IAR) (1/2)

① Check the storage location of the linker configuration file (icf file).

[Example] The storage location of the icf file is as shown below.

“C:\Program Files (x86)\IAR Systems\Embedded Workbench 8.4\rl78\config”



② Copy and rename the default icf file to get the icf file for use in this project.

Then, store the icf file for this project in the project folder.

[Example] Copy and rename “lnkr7f100glg.icf” to create “r01an5565-rl78g23-crc.icf”.

Then, store “r01an5565-rl78g23-crc.icf” in the project folder

“C:\Workspace_IAR_EW\r01an5565-rl78g23-crc”.

Figure 4 - 7 Checksum Output Address Settings (Options window of IAR) (2/2)

③Add the code in the red frame to “r01an5565-rl78g23-crc.icf” as shown in the image below.

```

r01an5565-rl78g23-crc.icf
135 "SADDRMEM":place in SADDR { rw section .sdata,↓
136                               R_SDAT,↓
137                               rw section .sbss*,↓
138                               R_SBSS,↓
139                               rw section .wrkseg };↓
140 ↓
141 ↓
142 ↓
143 define region CHECKSUM_region_plus2 = mem:[from 0x00000 to 0x0FFFD];↓
144 place at end of CHECKSUM_region_plus2 { ro section .checksum };↓
145 ↓
  
```

④Check the "Override default" and select the “r01an5565-rl78g23-crc.icf”.

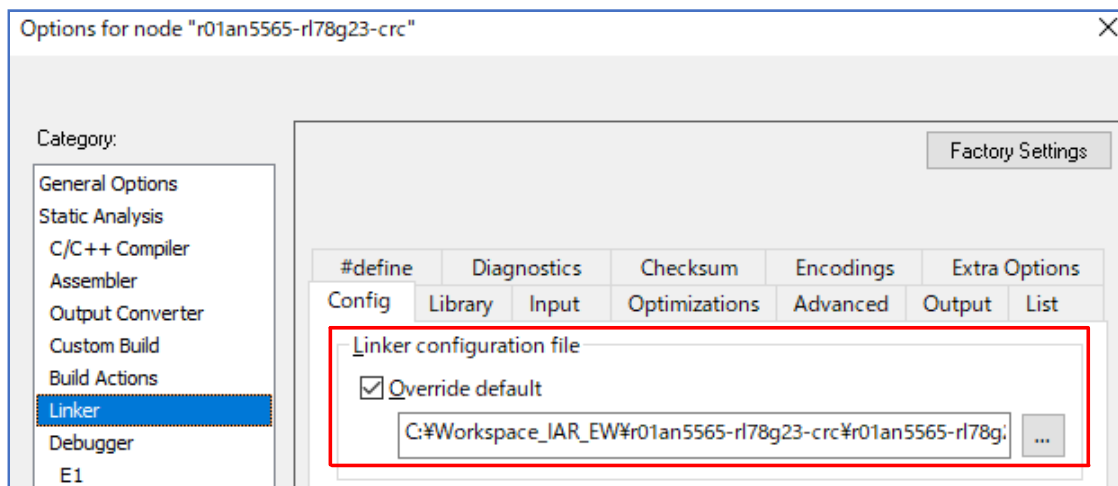
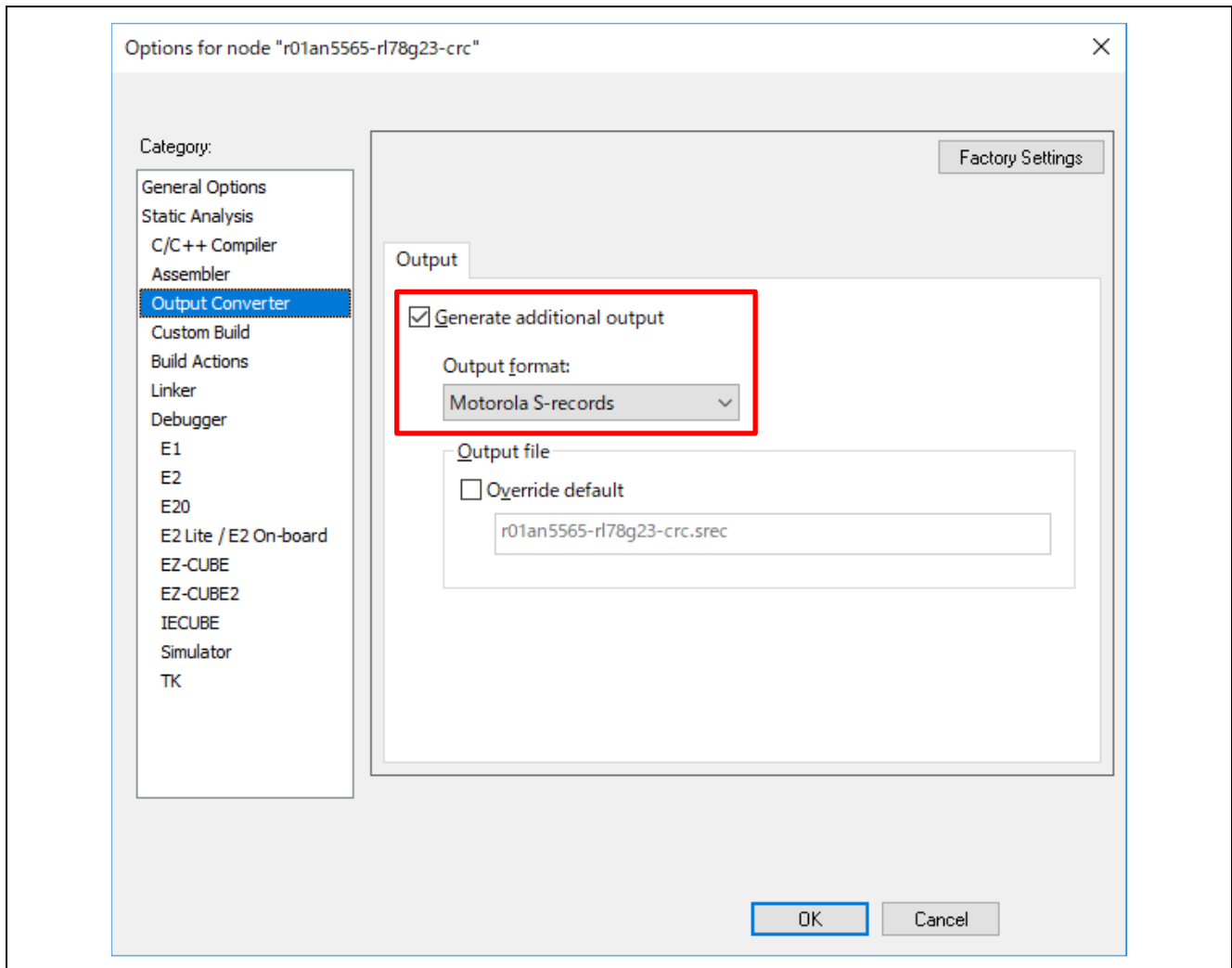


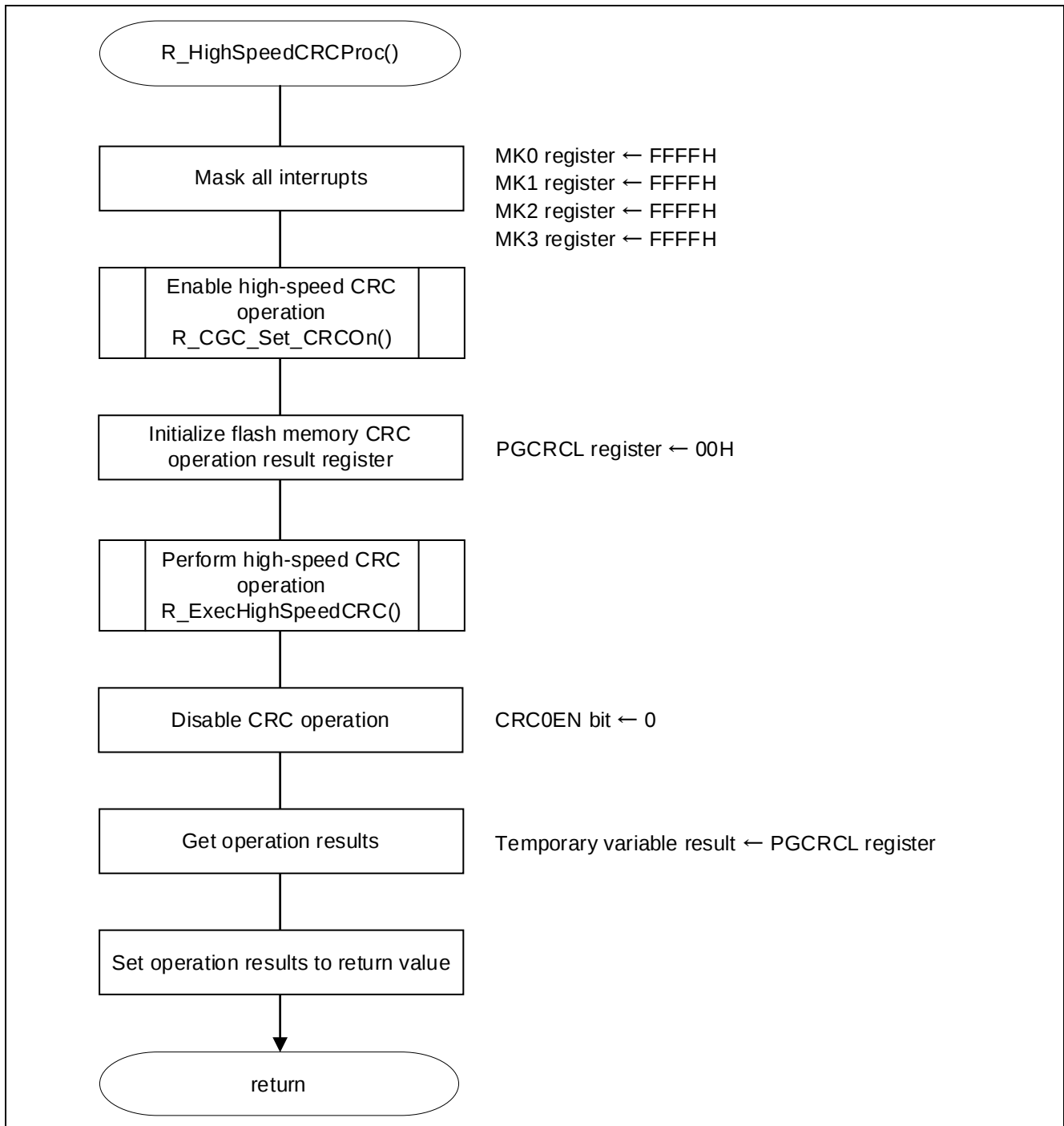
Figure 4 - 8 Output Converter Settings (Options window of IAR)



4.6.2 High-speed CRC Operation Processing

Figure 4 - 9 shows the flowchart for the high-speed CRC operation processing.

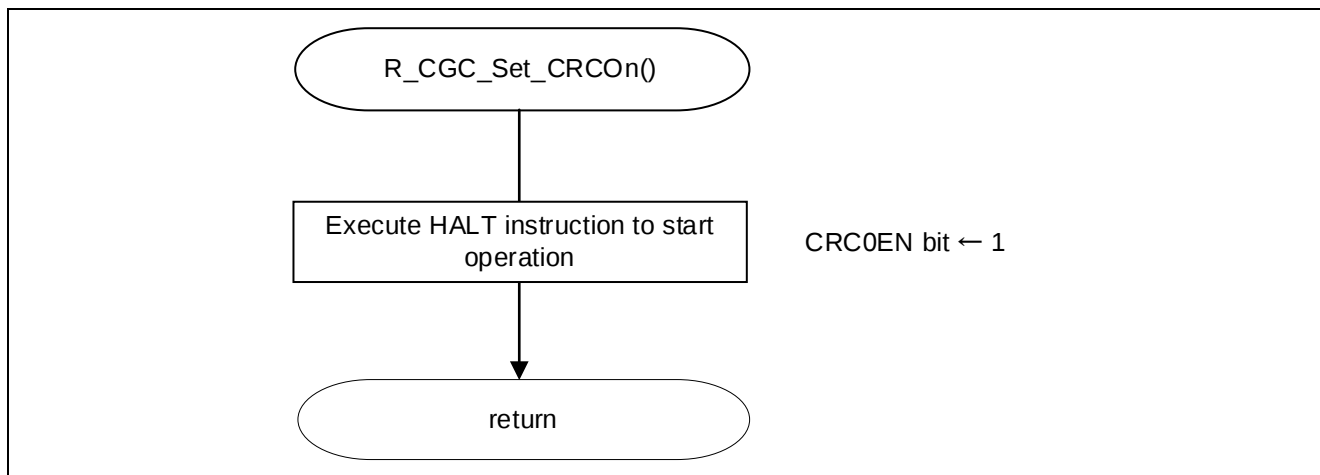
Figure 4 - 9 High-speed CRC Operation Processing



4.6.3 Enabling High-speed CRC Operation

Figure 4 - 10 shows the flowchart for enabling high-speed CRC operation.

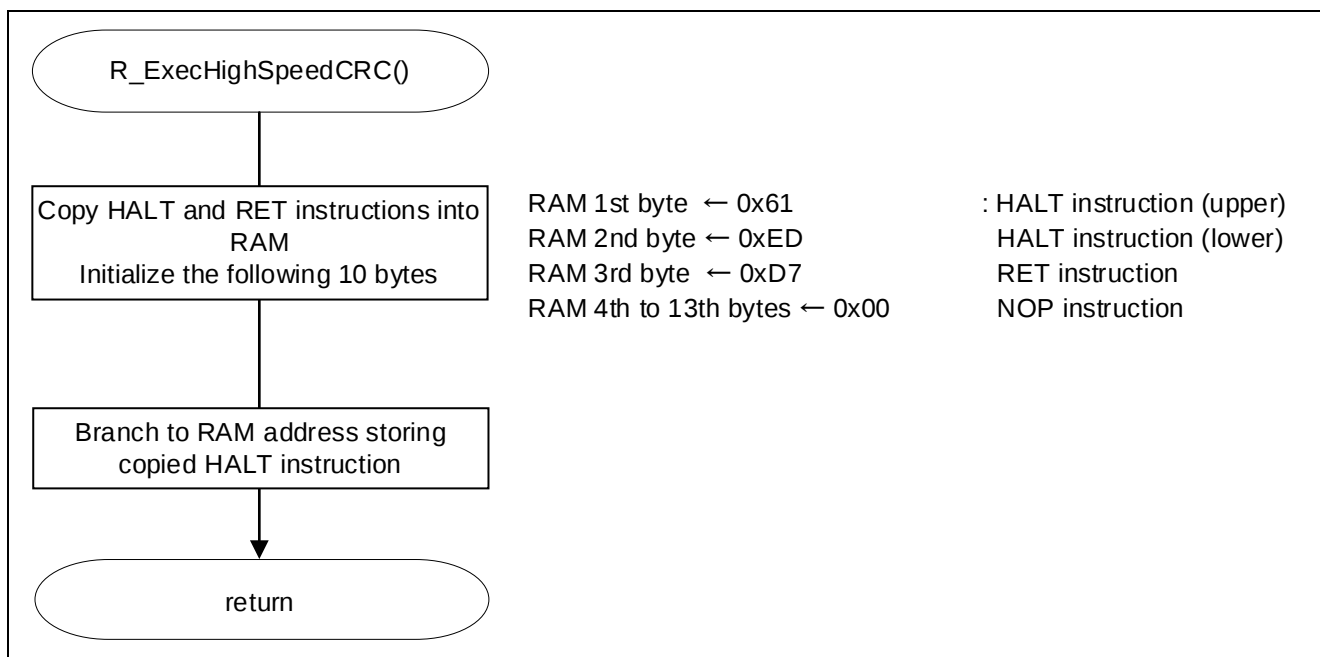
Figure 4 - 10 Enabling High-speed CRC Operation



4.6.4 Performing High-speed CRC Operation

Figure 4 - 11 shows the flowchart for performing high-speed CRC operation.

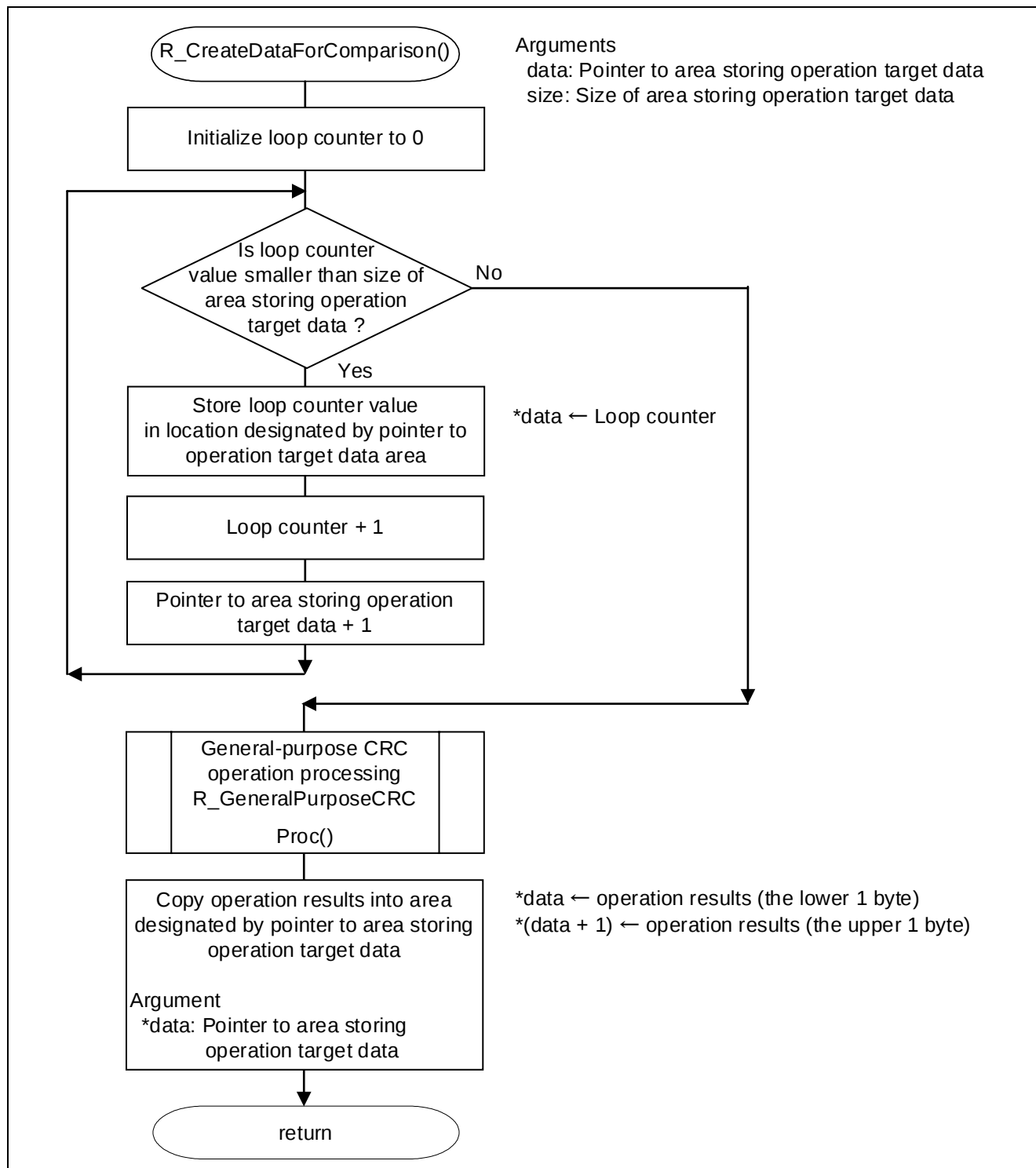
Figure 4 - 11 Performing High-speed CRC Operation



4.6.5 Creating General-purpose CRC Operation Target Data

Figure 4 - 12 shows the flowchart for creating general-purpose CRC operation target data.

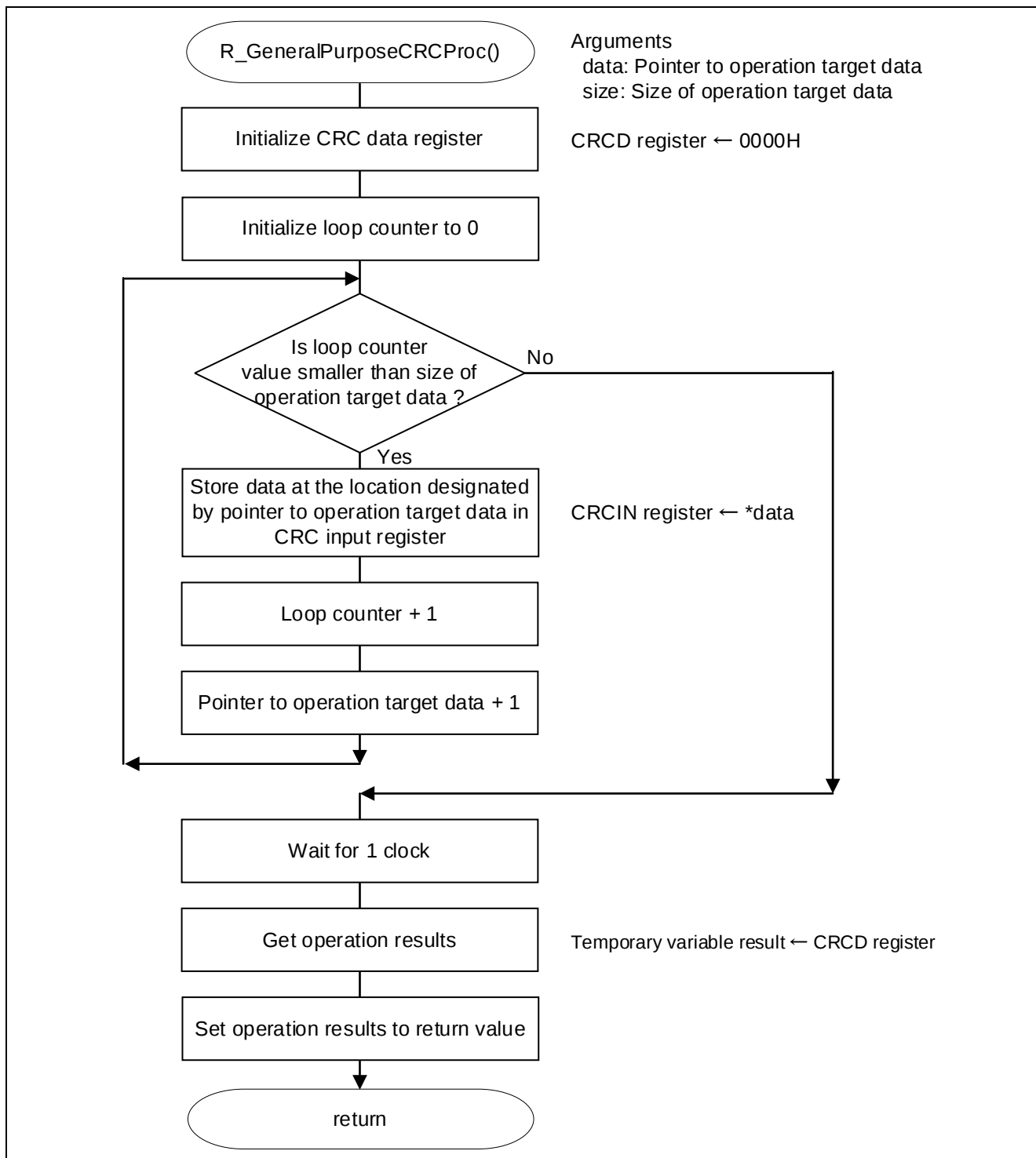
Figure 4 - 12 Creating General-purpose CRC Operation Target Data



4.6.6 General-purpose CRC Operation Processing

Figure 4 - 13 shows the flowchart for the general-purpose CRC operation processing.

Figure 4 - 13 General-purpose CRC Operation Processing



5. Sample Code

The sample code is available on the Renesas Electronics Website.

6. Documents for Reference

RL78/G23 User's Manual: Hardware (R01UH0896)

RL78 Family User's Manual: Software (R01US0015)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.13.21	-	First edition issued
1.01	May.26.21	7	Updated the Operation Confirmation Conditions
1.02	Dec.1.23	7	Updated the Operation Confirmation Conditions
		6	Figure 3-1: Reset Circuit Modification

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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