RL78/G23

Overcurrent protection function for converter using ELCL

Introduction

This application note describes how to implement the overcurrent protection for converters using the logic and event link controller (ELCL). The overcurrent protection function detects abnormalities in the current flowing through the system and stops the controlled PWM output to prevent serious accidents.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note acheives the overcurrent protection function for the converter using ELCL.
Figure 1-1 shows the system configuration of overcurrent protection function for converter using ELCL.

PWM output from TO01 to control LED lighting. At this time, overcurrent flowing to the LED is detected by inputting the voltage of the current measurement resistor terminal connected to the LED to the comparator. This comparator output fixes the pin output level of the PWM output from TO01 to protect the system. INPUT A assumes a reactivation switch.

The forced output stop state is released by generating a pulse from INPUT A. However, while the overcurrent condition continues, the input is disabled and the function works to prohibit operation under abnormal conditions.

Figure 1-1 System Configuration

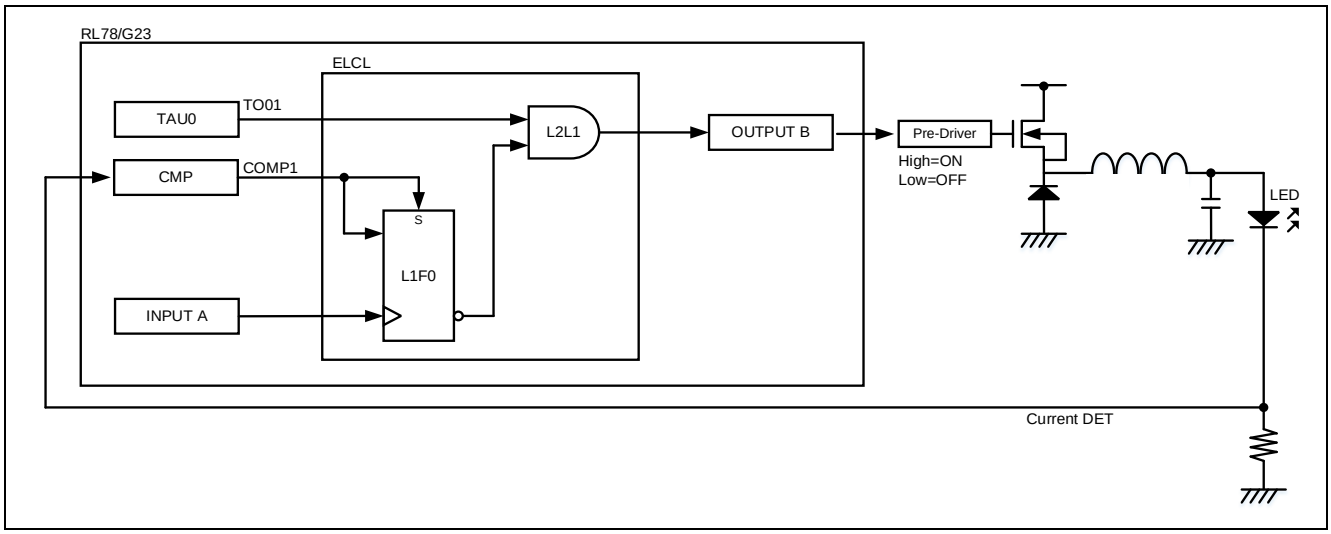
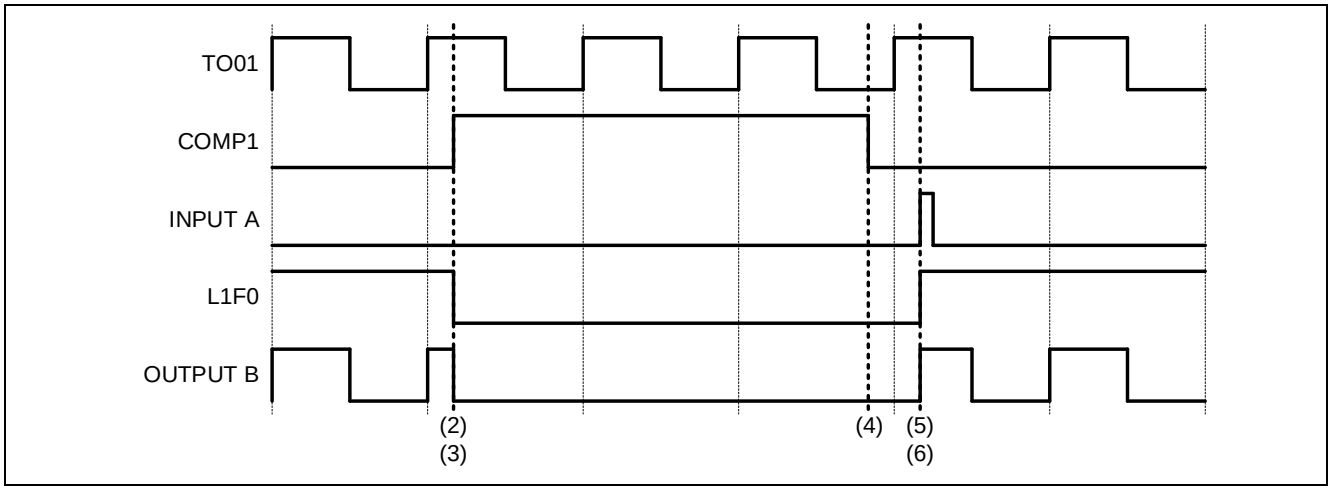


Figure 1-2 shows the timing chart.

(1) Set TAU0 channel 0 and channel 1 to PWM output.
(2) When the comparator detects a voltage higher than the reference voltage, COMP1 signal sets to High.
(3) By (2), the flip-flop (L1F0) output is Low and OUTPUT B is tied Low.
(4) When the voltage falls below the reference voltage, COMP1 signal sets to Low.
(5) Pulse is generated by INPUT A and input to flip-flop (L1F0).
(6) By (5), a High is output from the flip-flop (L1F0) and PWM output of TO01 is output from OUTPUT B.

Figure 1-2 Timing chart



2. Conditions for Operation Confirmation Test

The sample code with this application note runs properly under the condition below.

Table 2-1 Operation Confirmation Condition

Items	Contents
MCU	RL78/G23 (R7F100GLG)
Operating frequencies	• High-speed on-chip oscillator clock: 32MHz • CPU/peripheral hardware clock: 32MHz
Operating voltage	• 3.3V • LVD0 operations (V_{LVD0}): Reset mode Rising edge TYP. 1.90V Falling edge TYP. 1.86V
Integrated development environment (CS+)	CS+ for CC V8.08.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.11 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio 2022-07 (22.07.0) from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.11 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 v4.21.1 from IAR Systems
C compiler (IAR)	
Smart Configurator	V.1.3.0
Board support package (r_bsp)	V.1.20
Emulator	CS+、e^2 studio: COM port IAR: E2 Emulator Lite
Board	RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)

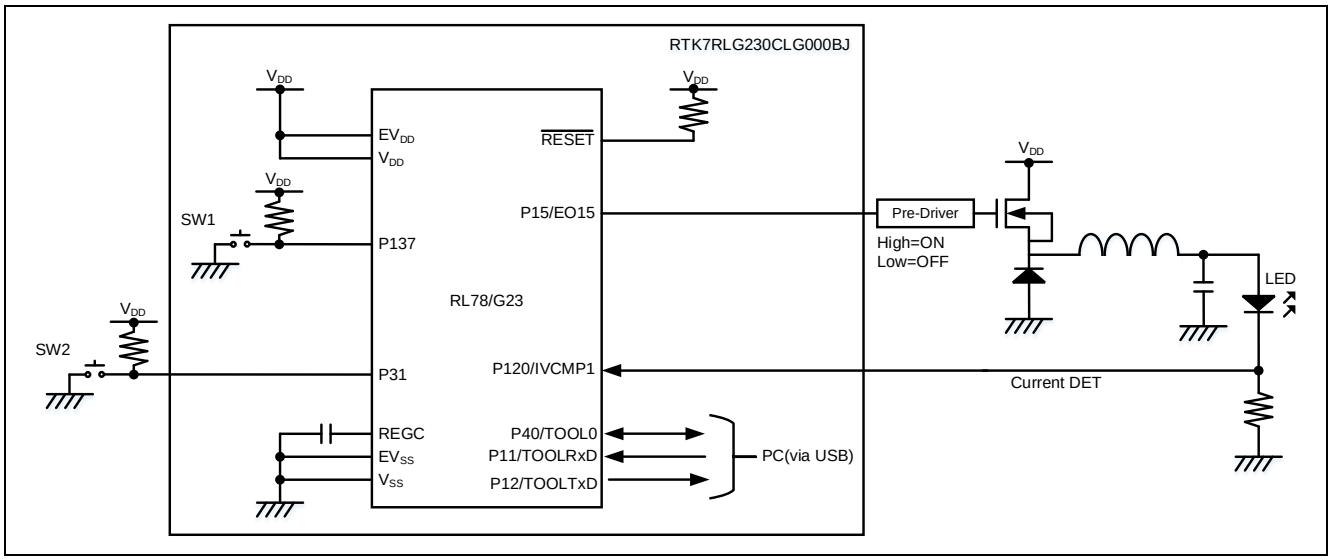
3. Hardware

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration in this application.

SW1 connected to P137 is an on-board switch, but SW2 connected to P31 is configured external to the board.

Figure 3-1 Hardware Configuration



Caution 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

Caution 2. Connect the EV_{SS} pin to V_{SS} and the EV_{DD} pin to V_{DD}.

Caution 3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD0}) that is specified as LVD.

3.2 Used Pins

Table 3-1 shows list of used pins and assigned functions.

Table 3-1 List of Pins and Functions

Pin name	Input/Output	Function
P15/EO15	Output	ELCL output signal (controls LED[Note])
P137/INTP0	Input	SW1 (Low Active)
P31/INTP4	Input	SW2[Note] (Low Active)
P120/IVCMP1	Input	Comparator input signal

Note. Please configure outside the RTK7RLG230CLG000BJ.

Caution. In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

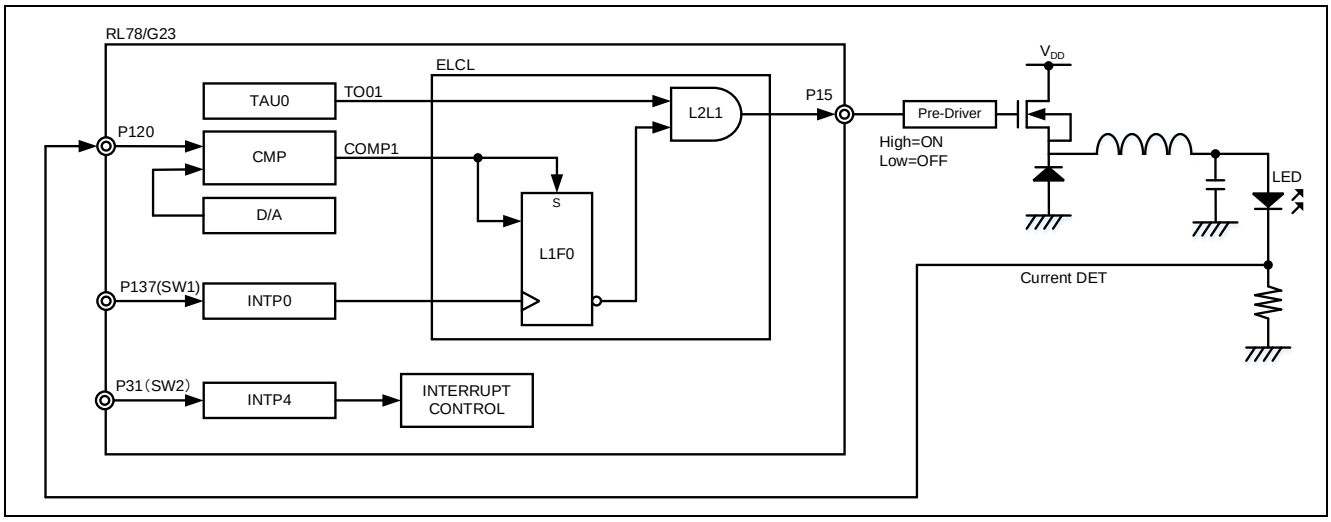
4. Software

4.1 Overview of the sample program

In this sample code, forced output stop of PWM output is performed, and overcurrent protection function for converter can be realized.

Figure 4-1 shows the system configuration of the sample code.

Figure 4-1 System configuration of the sample code

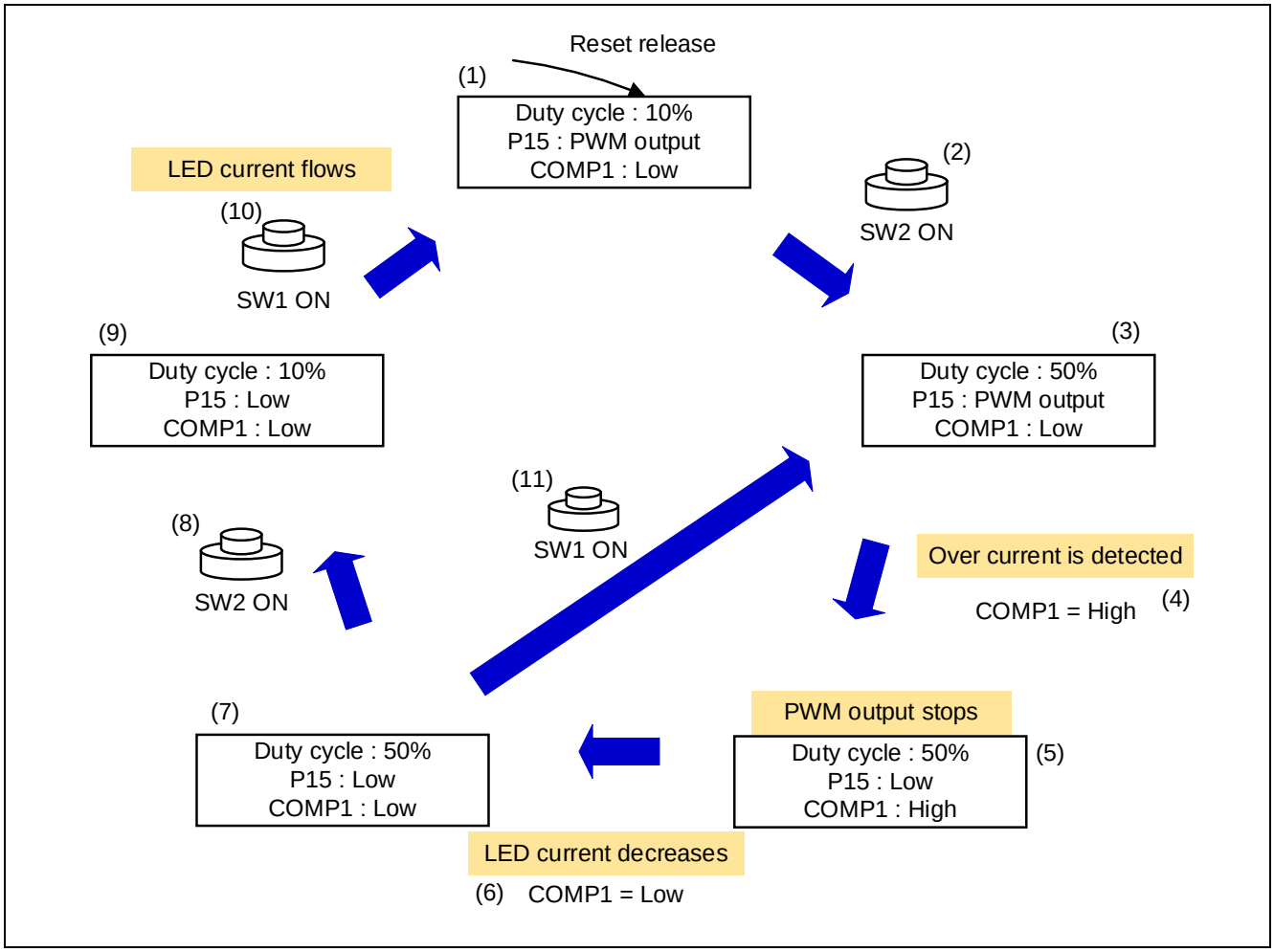


Caution. The LED drive circuit on the right side can be built using the EZ-0012. For details, refer to the EZ-0012 User's Manual in the "Reference".

Figure 4-2 shows operation overview. Return from No. (10) to No. (1) by pressing SW1.

(1) TAU0 starts operation, after that PWM output is outputted from P15.
(2) Press SW2.
(3) By (2), the duty cycle of the PWM output switch to 50%, which increases the current flowing to the LEDs.
(4) The comparator detects the overcurrent according to (3) by the signal converted from the current flowing through the LED to voltage is input to P120. This will drive COMP1 High.
(5) Since the output signal of P15 is forced output stop, the connected LED turns off.
(6) COMP1 changes Low because the LED current flows stopped.
(7) Forced output stop is in progress.
(8) Press SW2.
(9) By (8), the duty cycle of the PWM output switch to 10%, which decreases the current flowing to the LEDs.
(10) By pressing SW1 to generate a pulse, the forced output stop state is released and the LED turns on.
(11) If press SW1 before returning the duty ratio to 10%, it moves to (3).

Figure 4-2 Operation overview



4.2 Folder Configuration

Table 4-1 shows folder configuration of source file and header files using by sample code except the files generated by integrated development environment and the files in the bsp environment.

Table 4-1 Folder configuration

Folder/File configuration	Outline	Created by Smart configurator
¥r01an6565_elcl_protection <DIR>Note 3	Root folder of this sample code	
¥src<DIR>	Folder for program source	
main.c	Sample code source file	
elcl.c	Source file for ELCL	
elcl.h	Header file for ELCL	
¥smc_gen<DIR>	Folder created by Smart Configurator	√
¥Config_TAU0_0<DIR>	Folder for TAU00 program	√
Config_TAU0_0.c	Source file for TAU00	√
Config_TAU0_0.h	Header file for TAU00	√
Config_TAU0_0_user.c	Interrupt source file for TAU00	√Note 1
¥Config_INTC<DIR>	Folder for interrupt program	√
Config_INTC.c	Source file for INTP0 (SW1) and INTP4 (SW2)	√
Config_INTC.h	Header file for INTP0 and INTP4	√
Config_INTC_user.c	Interrupt source file for INTP0 and INTP4	√Note 2
¥Config_DAC0<DIR>	Folder for DAC0 program	√
Config_DAC0.c	Source file for DAC0	√
Config_DAC0.h	Header file for DAC0	√
Config_DAC0_user.c	Interrupt source file for DAC0	√Note1
¥Config_COMP1<DIR>	Folder for COMP1 program	√
Config_COMP1.c	Source file for COMP1	√
Config_COMP1.h	Header file for COMP1	√
Config_COMP1_user.c	Interrupt source file for COMP1	√Note1
¥general<DIR>	Folder for initialize or common program	√
¥r_bsp<DIR>	Folder for BSP program	√
¥r_config<DIR>	Folder for program	√

Note. <DIR> means directory

Note 1. Not used in this sample code.

Note 2. Added the interrupt handling routine to the file generated by the Smart Configurator

Note 3. The IAR version of the sample code contains r01an6565_elcl_protection.ipcf. For the ipcf file, refer to "RL78 Smart Configurator User Guide: IAR (R20AN0581)"

4.3 Option Byte Settings

Table 4-2 shows the option byte settings.

Table 4-2 Option Byte Settings

Address	Setting Value	Contents
000C0H/040C0H	1110 1111B (EFH)	Operation of Watchdog timer is stopped (counting is stopped after reset)
000C1H/040C1H	1111 1110B (FEH)	LVD0 operating mode: reset mode Detection voltage: Rising edge 1.90V Falling edge 1.86V
000C2H/040C2H	1110 1000B (E8H)	Flash operating mode: HS mode High-speed on-chip oscillator clock: 32MHz
000C3H/040C3H	1000 0101B (85H)	On-chip debugging is enabled

4.4 Constants

Constants are not used in this sample code.

4.5 Variables

Table 4-3 shows the global variables used in this sample code.

Table 4-3 Global variables used in the sample code

Type	Variable name	contents	Functions used in
uint8_t	g_intp4_flag	INTP4 interrupt occur flag	main.c r_Config_INTC_intp4_interrupt.c

4.6 Functions

Table 4-4 shows the functions used in the sample code. However, the unchanged functions generated by the Smart Configurator are excluded.

Table 4-4 Functions

Function name	Outline	Source file
main	Main process	main.c
r_elcl_create	ELCL initialize process	elcl.c
r_elcl_start	ELCL operation start process	elcl.c
r_elcl_stop	ELCL operation stop process	elcl.c
r_Config_INTC_intp4_interrupt	INTP4 interrupt process	Config_INTC_user.c

4.7 Function Specifications

This part describes function specifications of the sample code.

[Function name] main

Outline	Main process
Header	r_smc_entry.h, elcl.h
Declaration	int main (void);
Description	This function initializes ELCL, sets ELCL output and sets interrupts. This function starts the operation of CMP, DAC, TAU0 channel 0 and channel 1. Changes duty cycle of LED. Set the flag of INTP4 interrupt generation g_intp4_flag to 0.
Arguments	None
Return value	None
Remarks	None

[Function name] r_elcl_create

Outline	ELCL initialize process
Header	elcl.h, Config_Through.h, platform.h
Declaration	void r_elcl_create (void);
Description	This function initializes ELCL.
Arguments	None
Return value	None
Remarks	None

[Function name] r_elcl_start

Outline	ELCL operation start process
Header	elcl.h, Config_Through.h, platform.h
Declaration	void r_elcl_start (void);
Description	This function enables the ELCL output.
Arguments	None
Return value	None
Remarks	None

[Function name] r_elcl_stop

Outline	ELCL operation stop process
Header	elcl.h, Config_Through.h, platform.h
Declaration	void r_elcl_stop (void);
Description	This function stops the ELCL output.
Arguments	None
Return value	None
Remarks	None

[Function name] r_Config_INTC_into4_interrupt

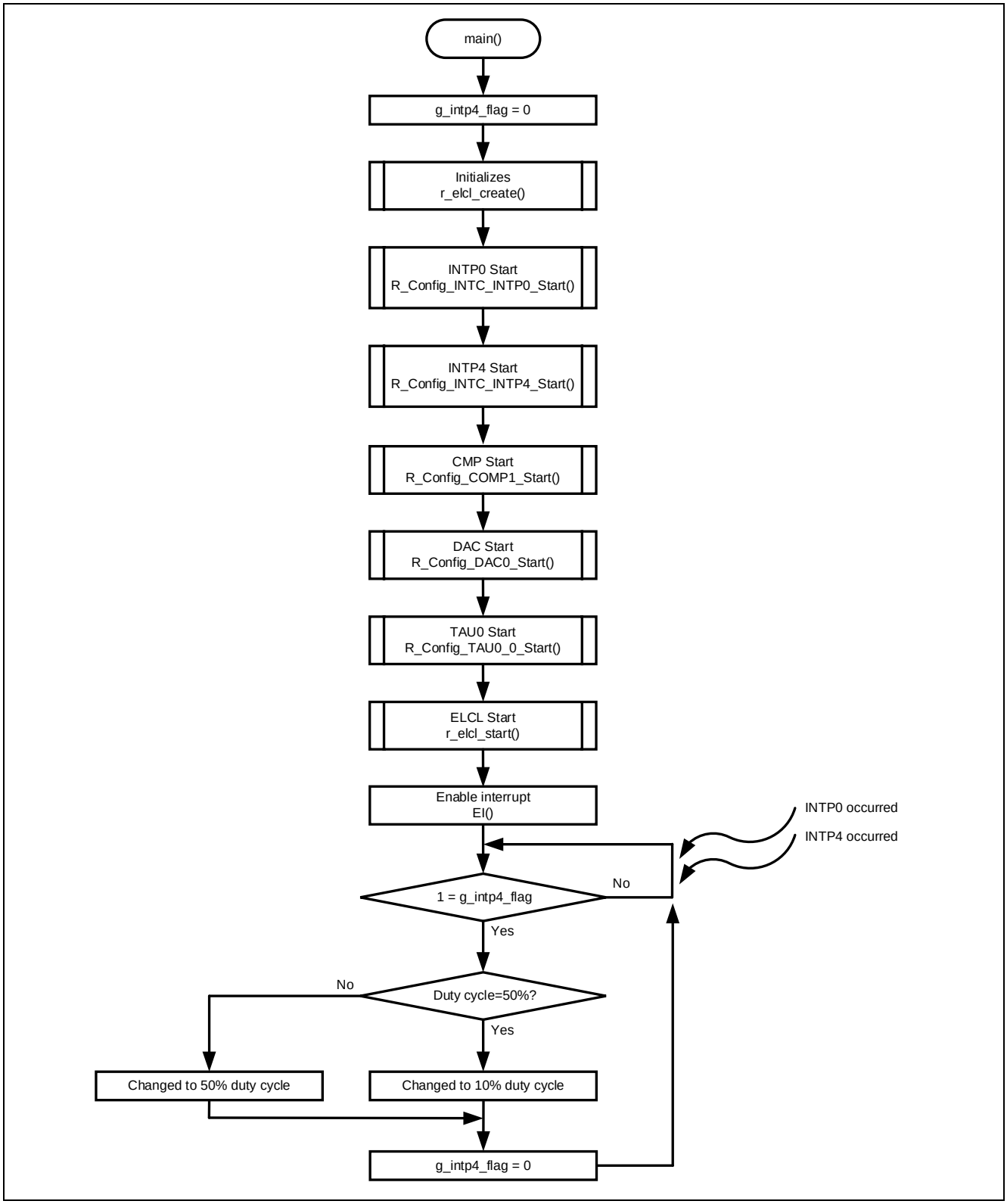
Outline	INTP4 interrupt process
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_INTC.h
Declaration	#pragma interrupt r_Config_INTC_intp4_interrupt (vect=INTP4)
Description	Set the flag of INTP4 interrupt generation g_intp4_flag to 1.
Arguments	None
Return value	None
Remarks	None

4.8 Flow Charts

4.8.1 Main Process

Figure 4-3 shows flowchart of main process.

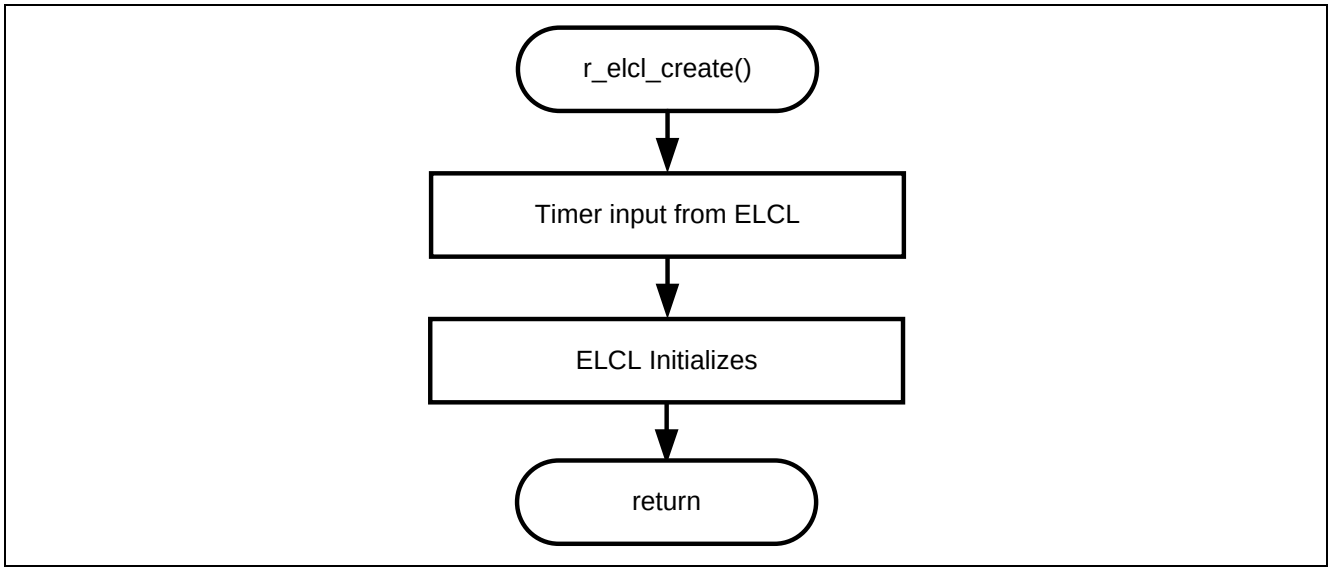
Figure 4-3 Main process



4.8.2 ELCL initialize process

Figure 4-4 shows flowchart of ELCL initialize process.

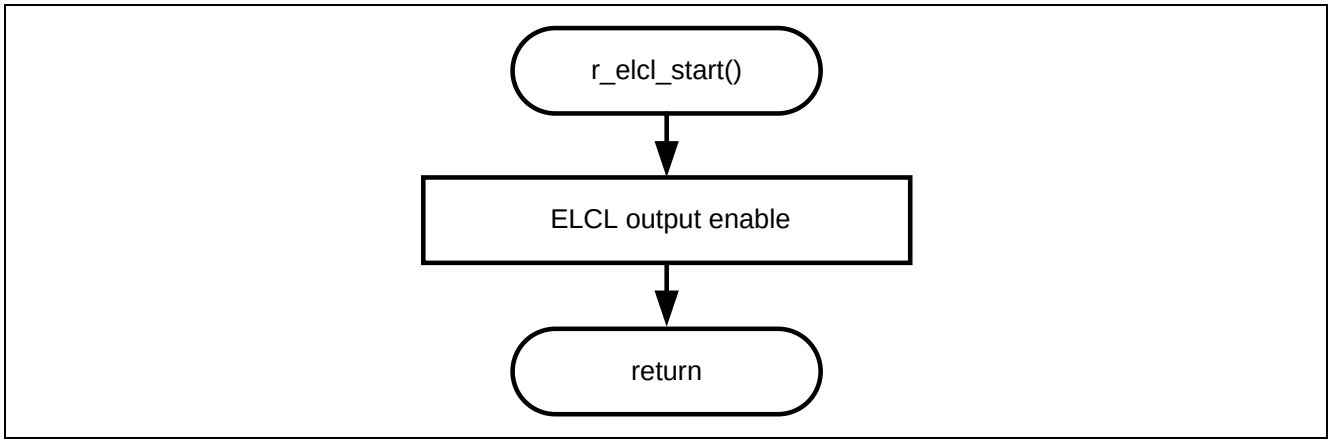
Figure 4-4 ELCL initialize process



4.8.3 ELCL operation start process

Figure 4-5 shows flowchart of ELCL operation start process.

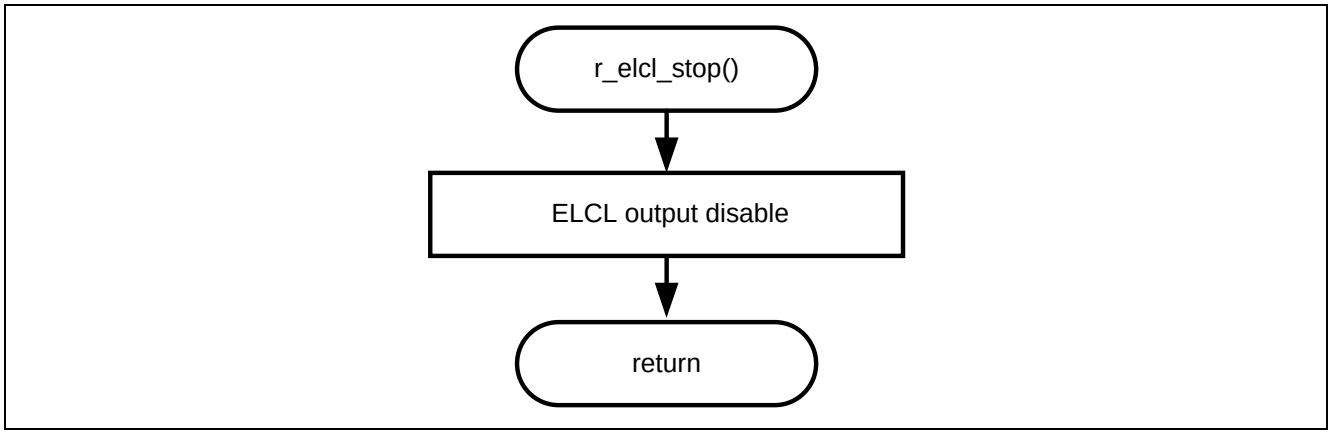
Figure 4-5 ELCL operation start process



4.8.4 ELCL operation stop process

Figure 4-6 shows flowchart of ELCL operation stop process.

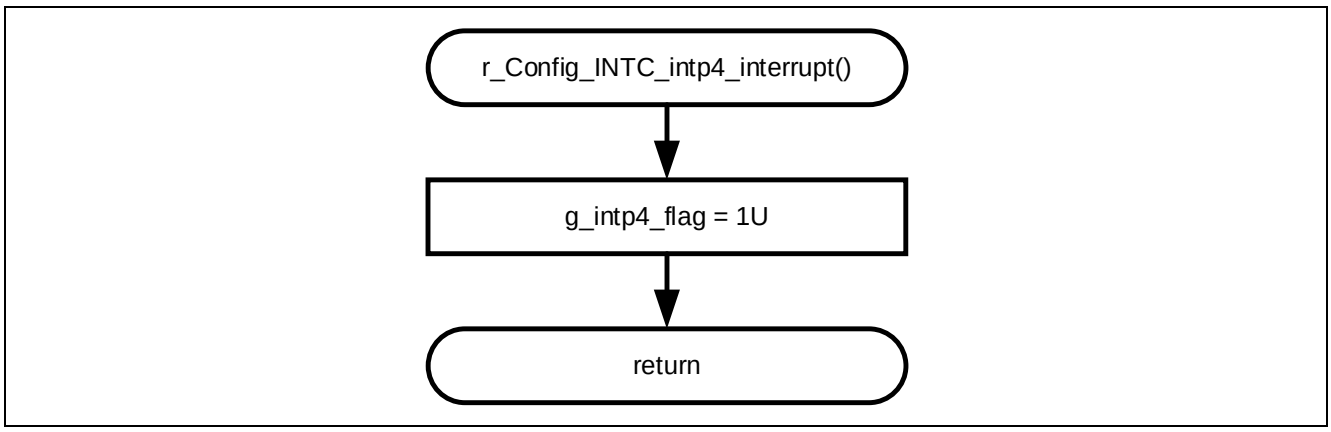
Figure 4-6 ELCL operation stop process



4.8.5 INTP4 interrupt process

Figure 4-7 shows flowchart of INTP4 interrupt process.

Figure 4-7 INTP4 interrupt process



5. Application example

In addition to the sample code, this application note contains the following Smart Configurator configuration files

r01an6565_elcl_protection.scfg

The following is a description of the file and examples of settings and notes for use.

5.1 r01an6565_elcl_protection.scfg

This is the Smart Configurator configuration file used in the sample code. It contains all the features configured in the Smart Configurator. The sample code settings are as follows.

Table 5-1 Parameters of Smart Configurator

Tag name	Component	Contents
Clocks	-	Operation mod: High-speed main mode 2.4 (V) ~ 5.5 (V) EV_{DD} setting: $1.8V \leqq EV_{DD0} < 5.5V$ High-speed on-chip oscillator: 32MHz f_{IHP}: 32MHz f_{CLK}: 32000kHz (High-speed on-chip oscillator) f_{SXP}: 32.768kHz (Subsystem Clock)
System	-	On-chip debug operation setting: COM port Note Pseudo-RRM/DMM function setting: Used Start/Stop function setting: Unused Trace function setting: Used Security ID setting: Use security ID Security ID: 0x00000000000000000000 Security ID authentication failure setting: Do not erase flash memory data
Components	r_bsp	Start up select : Enable (use BSP startup) Control of invalid memory access detection : Disable RAM guard space (GRAM0-1) : Disabled Guard of control registers of port function (GPORT) : Disabled Guard of registers of interrupt function (GINT) : Disabled Guard of control registers of clock control function, voltage detector, and RAM parity error detection function (GCSC) : Disabled Data flash access control (DFLEN) : Disables Initialization of peripheral functions by Code Generator/Smart Configurator : Enable API functions disable : Enable Parameter check enable : Enable Setting for starting the high-speed on-chip oscillator at the times of release from STOP mode and of transitions to SNOOZE mode : High-speed Enable user warm start callback (PRE) : Unused Enable user warm start callback (POST) : Unused Watchdog Timer refresh enable : Unused
	Config_LVD0	Operation mode setting: Reset mode Voltage detection setting: Reset generation level (V_{LVD0}): 1.86 (V)

Table 5-2 Parameters of Smart Configurator

Tag name	Component	Contents
Components	Config_TAU0_0	Components: PWM Output Resource: TAU0_0 Operation clock: CK00 Clock source: f_{CLK} Cycle value: 2μs Interrupt setting: unused (slave1) Duty value: 10% Initial output value: 0 Output level: Active-high Interrupt setting: unused
	Config_INTC	(INTP0) Valid edge: Falling edge Priority: Level 3 (INTP4) Valid edge: Falling edge Priority: Level 3
	Config_DAC0	Components: D/A Converter Resource: DAC0 D/A converter operation mode setting: Normal mode Conversion value setting: 23
	Config_COMP1	Components: Comparator Resource: COMP1 Speed setting: Low speed Reference voltage: D/A converted output 0 Voltage range: 0~V_{DD}-1.4V Edge setting: Rising edge Digital filter setting: Enable Sampling clock: f_{CLK}/8 Interrupt setting: use Priority: Level 3

Note. When using IAR, use the following settings.
On-chip debug operation setting: Use emulator
Emulator setting: E2 Emulator Lite

5.1.1 Clocks

Set the clock used in the sample code.

5.1.2 System

Set the on-chip debug of the sample code.

"Control of on-chip debug operation" and "Security ID authentication failure setting" affect "On-chip debugging is enabled" in "Table 4-2 Option Byte Settings". Note that changing the settings.

5.1.3 r_bsp

Set the startup of the sample code.

5.1.4 Config_LVD0

Set the power management of the sample code.

Affects "Setting of LVD0" in "Table 4-2 Option Byte Settings". Note that changing the settings.

5.1.5 Config_TAU0_0

Set up TAU00 in the sample code.

In the sample code, PWM output with 2µs cycle is used as the LED drive signal.

5.1.6 Config_INTC

Set the interrupt settings of the sample code.

The sample code sets the external maskable interrupt (INTP0, INTP4); delete it if you do not use INTP0 and INTC4.

5.1.7 Config_DAC0

Set up DAC0 in the sample code.

In the sample code, normal mode is selected. Set the “Conversion value setting” to 23 and use it as the reference voltage for the comparator.

5.1.8 Config_COMP1

Set up COMP1 in the sample code.

In the sample code, the “Reference voltage” is set to D/A converter output 0 and used for overcurrent detection.

5.2 Releasing forced output stop of PWM output using INTTM00

The overcurrent protection function for converter can be also realized with the following configuration.

Figure 5-1 shows the system configuration

The PWM output is fixed at a low level asynchronously with the TAU0 operation clock by the detection signal generation of COMP1, and the PWM output is forced output stop. After COMP1 changes to Low, the forced output stop state is released synchronously with the INTTM00 pulse.

Figure 5-1 system configuration

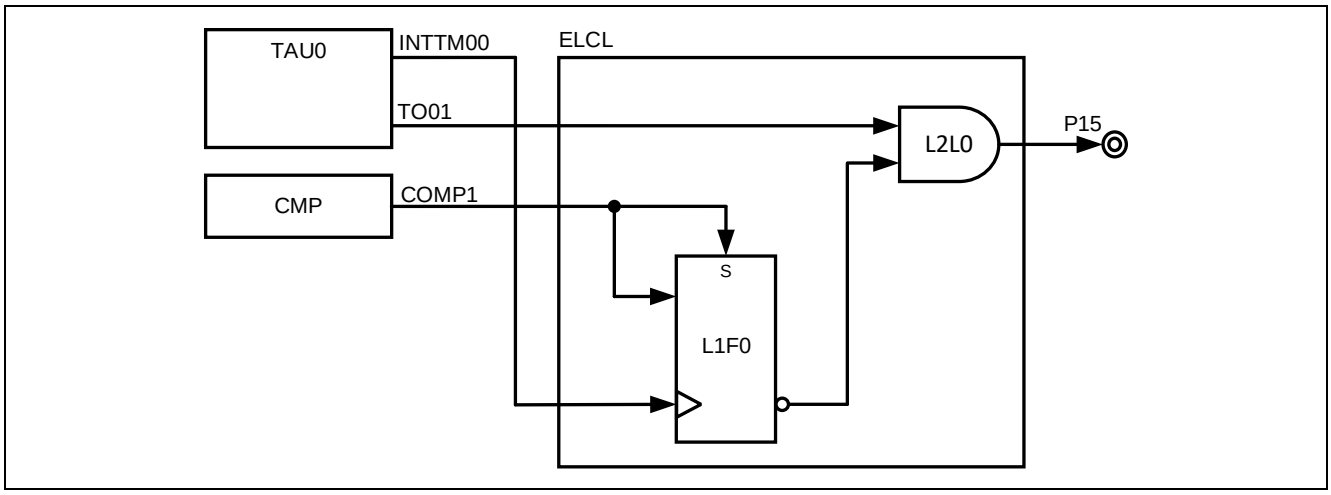
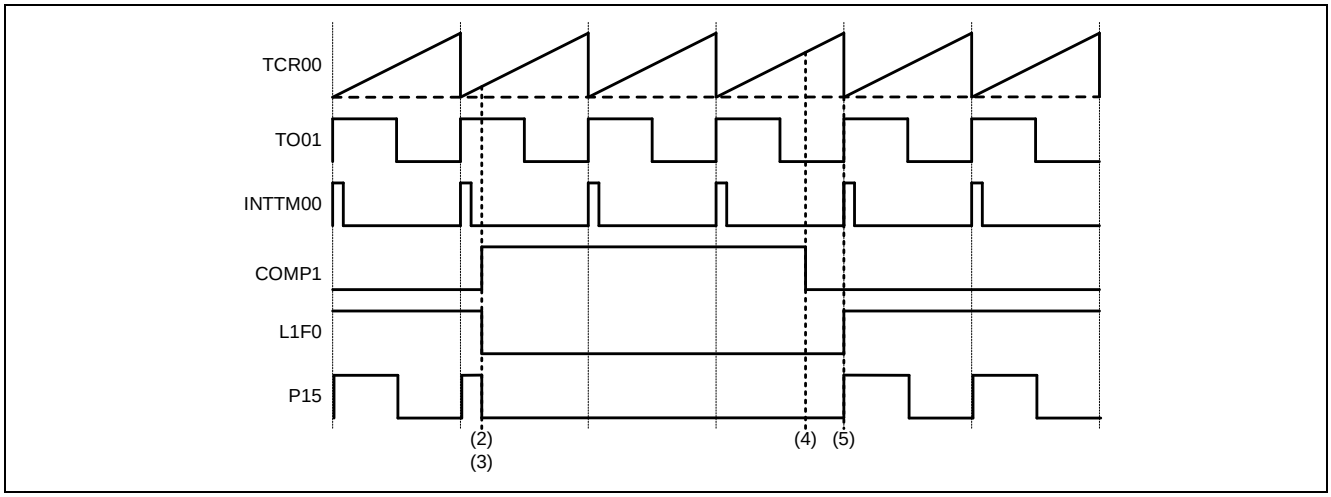


Figure 5-2 shows the timing chart.

(1) Set TAU0 channel 0 and channel 1 to PWM output.
(2) When the comparator detects a voltage higher than the reference voltage, COMP1 signal sets to High.
(3) By (2), the flip-flop (L1F0) output is LOW and P15 is tied LOW.
(4) when the voltage falls below the reference voltage, COMP1 signal sets to Low.
(5) After COMP1 signal changes Low, when INTTM00 occurs, High level is outputted from the flip-flop (L1F0). Then PWM output of TO01 is output from P15.

Figure 5-2 Timing chart



The system configuration in Figure 5-1 can be realized with the following elcl.c.

```
void r_elcl_create(void)
{
    /* L2L1 Start */
    PFOE0    &= 0xFDU; /* TO01 */
    ELISEL4   = 0x08U; /* TAU0_1 */
    ELL2SEL2  = 0x05U; /* Link target is ELISEL4 */
    ELL2SEL3  = 0x90U; /* Link to L1 output signal 3 */
    ELL2LNK2  = 0x03U; /* Link to L2L1 inout 0 */
    ELL2LNK3  = 0x04U; /* Link to L2L1 inout 1 */
    ELL2CTL  |= 0x04U; /* Select L2L1 AND circuit */
    PM1      &= 0xDFU; /* P15  Set to Output mode */
    PMCE1    |= 0x20U; /* P15  Output ELCL */
    ELOSEL5   = 0x07U; /* Select L2 output signal 1 (L2L1 AND) */
    /* L2L1 End */

    /* L1F0 Start */
    ELISEL8   = 0x1AU; /* INTCMP1 */
    ELISEL6   = 0x16U; /* Input INTTM00 */
    ELL1SEL2  = 0x09U; /* Link target is ELISEL8 */
    ELL1SEL4  = 0x03U; /* Link target is ELISEL8 */
    ELL1SEL5  = 0x00U; /* No link target */
    ELL1SEL6  = 0x01U; /* Link target is ELISEL6 */
    ELL1LNK2  = 0x08U; /* Link to L1F0 Input */
    ELL1LNK4 |= 0x01U; /* Link to L1F0 SET */
    ELL1LNK5 |= 0x02U; /* Link to L1F0 RESET */
    ELL1LNK6 |= 0x01U; /* Link to L1F0 CLK */
    ELL1CTL  |= 0x40U; /* Select L1F0 FF0 */
    ELOSEL6   = 0x04U; /* Select L1 output signal 3 (L1F0) */
    /* L1F0 End */
}
```

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference

RL78/G23 User's Manual: Hardware (R01UH0896E)

RL78 Family User's Manual: Software (R01US0015E)

RL78 Smart Configurator User's Guide: CS+ (R20AN0580E)

RL78 Smart Configurator User's Guide: e^2 studio (R20AN0579E)

RL78 Smart Configurator User's Guide: IAREW (R20AN0581E)

RL78/I1A DC/DC LED Control Evaluation Board (EZ-0012) User's Manual: Hardware (R01UH0363EJ0200)

(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update / Technical News

(The latest version can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.26.22	–	First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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