RL78/G23

Operation State Switching

Introduction

The application note shows the register setting sequence for the switch of RL78/G23 operation state, using the Operation State Control. After reset, it operates in the HS mode. The flash operation mode is switched one by one by the button pressing (HS mode → LS mode → LP mode → HS mode, repetition at the following).

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Overview of Specifications

Pressing the button generates an INTP0 interrupt and changes flash operation mode. After cycling through all operation transition states supported by RL78/G23, the state immediately after a reset is restored. LED1 and LED2 indicate flash operation modes.

Table 1-1 shows the peripheral function to be used and its use. Figure 1-1 shows the transitions of flash operation modes. Table 1-2 provides details and transitions of operation states.

Table 1-1 Peripheral functions used and their uses

Peripheral Function	Use
External interrupt	Switch input
Port output	Controls the LEDs (LED1, LED2) connected to the P52 and P53 pins.

Figure 1-1 Operation state transition sequence order

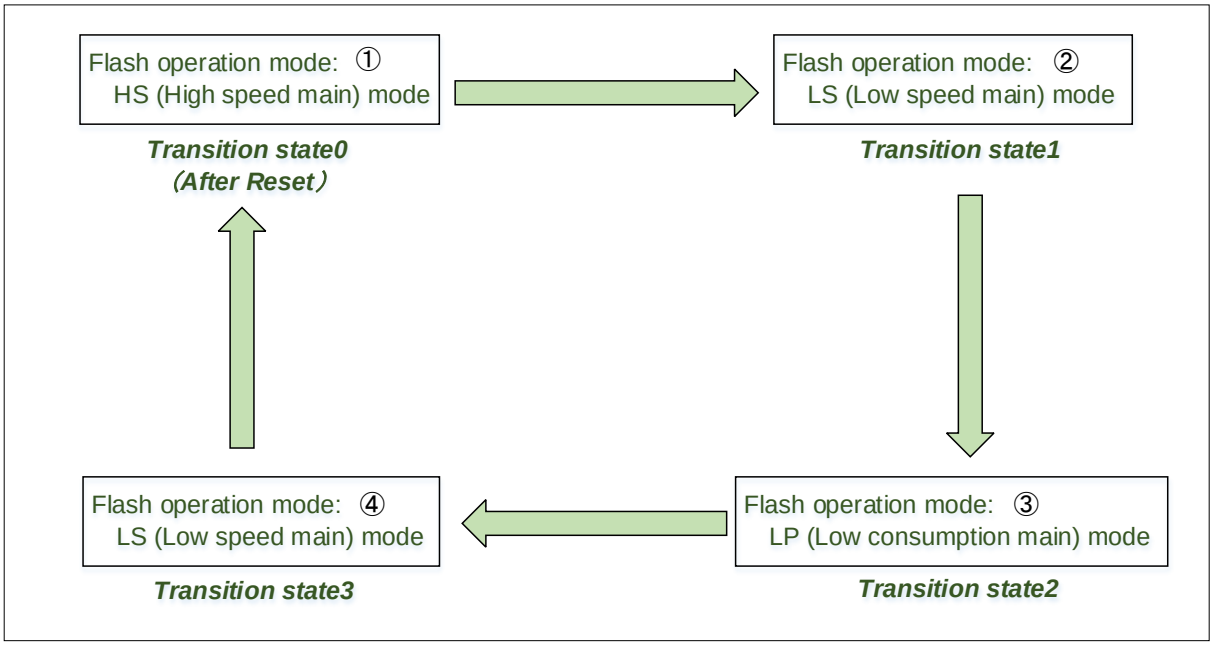


Table 1-2 Operation state detail and operation state transition

Flash operation mode		LED1	LED2	Operation clock	Range of operation voltage (Electrical characteristics)
①	HS mode (after reset)	Turning on	Turning on	32 MHz	1.8 V to 5.5 V (1 to 32MHz: 1. 8 V to 5.5 V)
②	LS mode	Turning on	Turning off	16 MHz	1.8 V to 5.5 V (1 to 24 MHz: 1.8 V to 5.5 V)
③	LP mode	Turning off	Turning on	2 MHz	1.8 V to 5.5 V (1 to 2 MHz: 1.6 V to 5.5 V)
④	LS mode	Turning on	Turning off	16 MHz	1.8 V to 5.5 V (1 to 24 MHz: 1.8 V to 5.5 V)

Modes ① to ④ are cycled through when the button is pressed.

1.2 Outline of Operation

Each time a falling edge of the P137 / INTP0 pin is detected when the switch is pressed, the CPU clock and operating mode are switched.

The following describes the main settings.

(1) Initial settings for input/output ports

P52 and P53 pins: Set as output ports (used for LED ON control)

Table 1-3 Initial Settings for Input/Output Ports (P52 and P53 Pins)

Register/Bit Name	Setting Value	Content
P5 register	00H	Output data of P52 and P53 is set to 0.
POM5 register	00H	Output mode of P52 and P53 is set to normal output mode.
PM5 register	00H	P52 and P53 are set to output mode.

(2) Initial settings for the clock generation circuit.

- Set flash operation mode to HS (high-speed main) mode.
  (Use the user option byte (000C2H/ 040C2H) for this setting.)
- Set the frequency of the high-speed on-chip oscillator clock to 32 MHz.
- Select the main system clock (f_{MAIN}) for the CPU/peripheral hardware clock (f_{CLK}).

(3) Initial settings for interrupt processing

- Set the effective edge of the INTP0 pin to falling edge to enable switch input.
- Check the pin voltage level at intervals of approximately 5 ms for determining switch input. When the voltage level is identical twice in a row, switch input is determined to be effective (chattering removed).

Table 1-4 Initial Settings for Input/Output Ports (P137/INTP0 Pin)

Register/Bit Name	Setting Value	Content
MK0L register	FFH	INTP0 interrupt prohibited
IF0L register	00H	INTP0 interrupt request flag clear
PR10L register	FFH	Level 3 is specified as INTP0 interrupt priority.
PR00L register	FFH	
EGP0 register	00H	Falling edge is specified as INTP0 effective edge.
EGN0 register	01H	

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

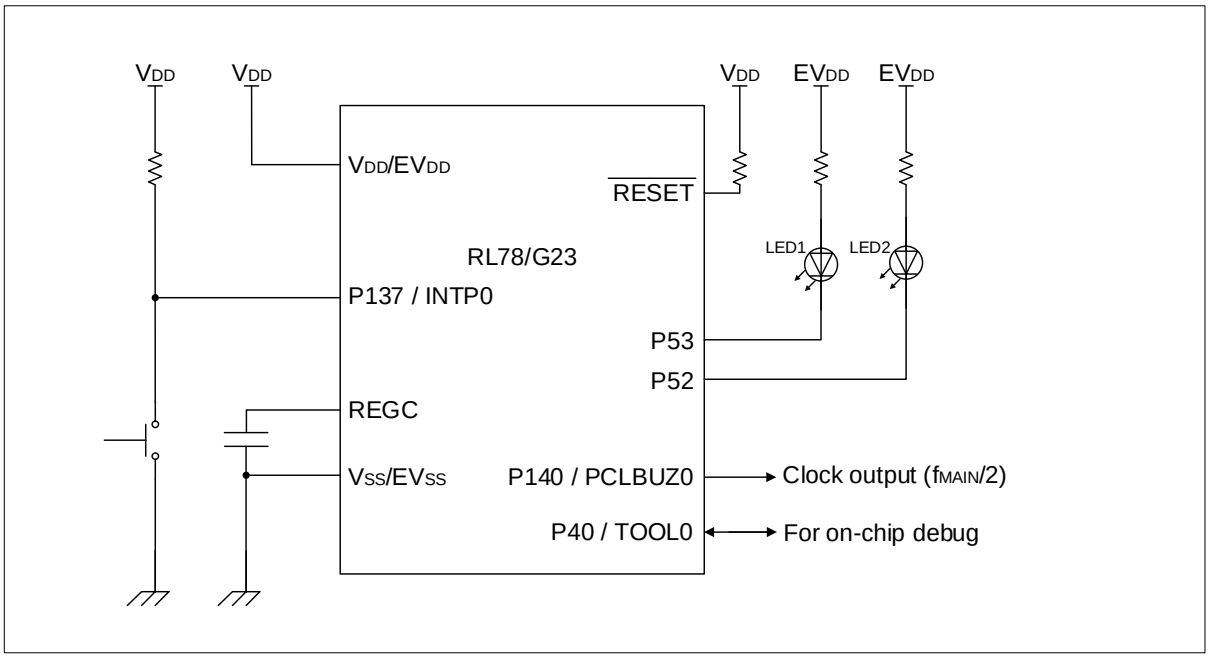
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23-64p Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	• High-speed on-chip oscillator clock (f_{IH}): 32 MHz, 16 MHz, 2 MHz
Operating voltage	5.0 V (can be operated at 2.0 V to 5.5 V) LVD0 detection voltage: Reset mode At rising edge TYP. 1.90V (1.84 V to 1.95 V) At falling edge TYP. 1.86V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ for CC E8.09.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2023-04 (23.4.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.2 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.2.2420 from IAR Systems Corp.
Smart configurator (SC)	V1.6.0 from Renesas Electronics Corp.
Board support package (BSP)	V1.60 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to V_{DD} or V_{SS} through a resistor).

Note 2. Connect any pins whose name begins with EV_{SS} to V_{SS}, and any pins whose name begins with EV_{DD} to V_{DD}, respectively.

Note 3. V_{DD} must not be lower than the reset release voltage (V_{LVD0}) that is specified for the LVD0.

3.2 List of Pins Used

Table 3-1 shows the pins used and their functions.

Table 3-1 Pins used and their functions

Pin name	I/O	Function
P53	Output	LED1 turning on control
P52	Output	LED2 turning on control
P137 / INTP0	Input	Operation state switching
P140 / PCLBUZ0	Output	Clock output

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option byte

Table 4-1 shows the option byte settings. Please set the appropriate value to fit the different system.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 040C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 040C1H	11111110B	LVD0 detection voltage: reset mode At rising edge TYP. 1.90V (1.84 V to 1.95 V) At falling edge TYP. 1.86V (1.80 V to 1.91 V)
000C2H / 040C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 040C3H	10000101B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2 Constants used in sample code

Constant Name	Setting Value	Description
_00_TRANSITION_STATUS_0	00H	Transition status 0
_01_TRANSITION_STATUS_1	01H	Transition status 1
_02_TRANSITION_STATUS_2	02H	Transition status 2
_03_TRANSITION_STATUS_3	03H	Transition status 3
LED_ON	00H	LED control: ON
LED_OFF	01H	LED control: OFF
WAITCOUNT_32M	8000	5 ms count value during HS 32 MHz operation
WAITCOUNT_16M	4000	5 ms count value during LS 16 MHz operation
WAITCOUNT_2M	500	5 ms count value during LP 2 MHz operation

4.3 List of Variables

Table 4-3 lists global variables.

Table 4-3 Global variables

Type	Variable identifier	Content	Use function
uint16_t	g_transition_status	Transition state variable	main (), r_Config_INTC_intp0_interrupt ()

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function name	Outline
r_switch_flashmode_to_HS	The flash operation state is switched to the HS mode.
r_switch_flashmode_to_LS	The flash operation state is switched to the LS mode.
r_switch_flashmode_to_LP	The flash operation state is switched to the LP mode.
r_Config_INTC_intp0_interrupt	External interrupt processing.

4.5 Specification of Functions

The function specifications of the sample code are shown below.

r_switch_flashmode_to_HS	
Overview	The flash operation state is switched to the HS mode.
Header	r_cg_macrodriver.h, r_cg_userdefine.h
Declaration	void r_switch_flashmode_to_HS (void)
Description	The flash operation state is switched to the HS mode.
Argument	None
Return value	None

r_switch_flashmode_to_LS	
Overview	The flash operation state is switched to the LS mode.
Header	r_cg_macrodriver.h, r_cg_userdefine.h
Declaration	void r_switch_flashmode_to_LS (void)
Description	The flash operation state is switched to the LS mode.
Argument	None
Return value	None

r_switch_flashmode_to_LP	
Overview	The flash operation state is switched to the LP mode.
Header	r_cg_macrodriver.h, r_cg_userdefine.h
Declaration	void r_switch_flashmode_to_LP (void)
Description	The flash operation state is switched to the LP mode.
Argument	None
Return value	None

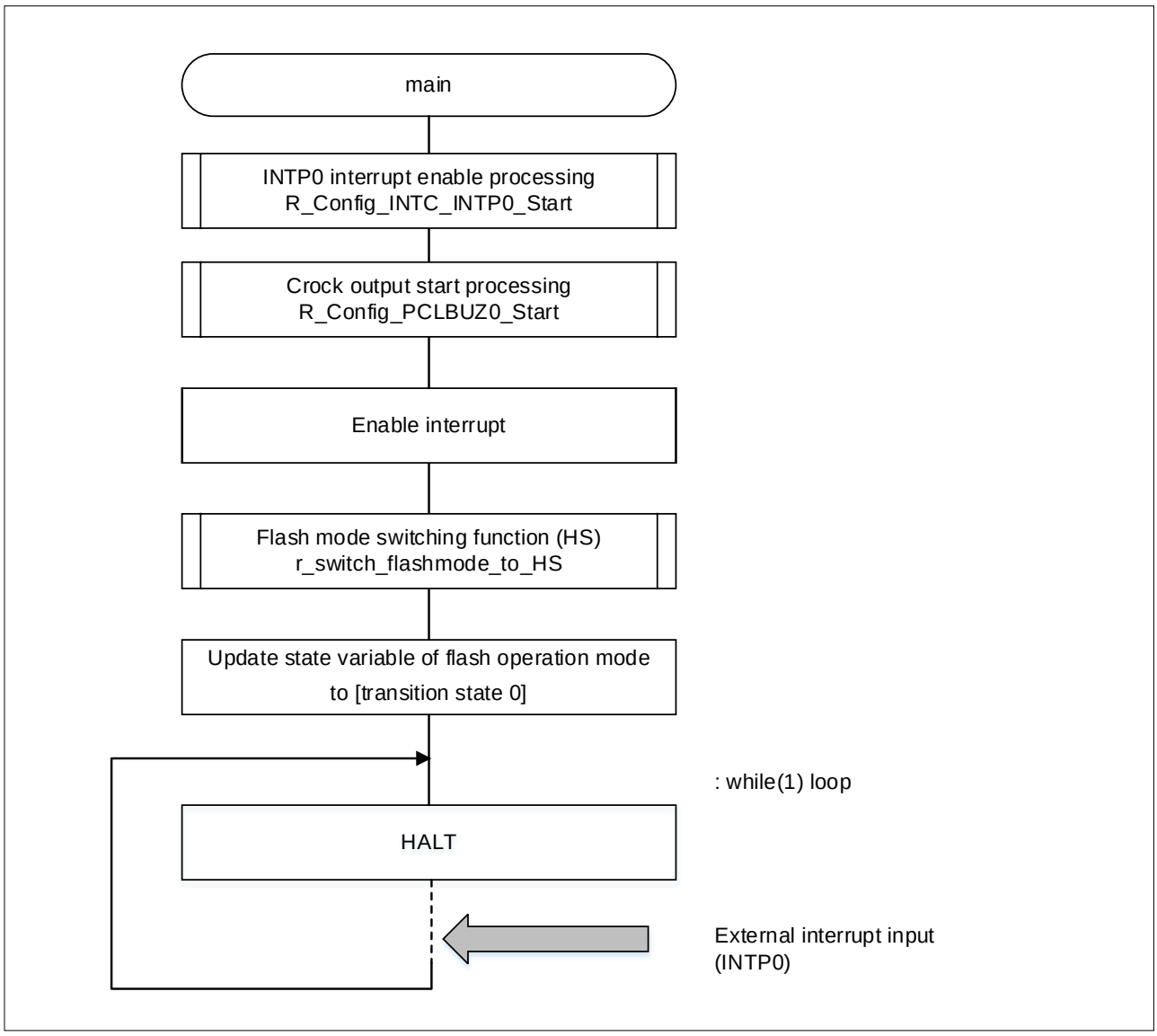
r_Config_INTC_intp0_interrupt	
Overview	External interrupt processing
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_INTC.h
Declaration	static void __near r_Config_INTC_intp0_interrupt (void)
Description	Pushing button calls this function where operation state switching is executed.
Argument	None
Return value	None

4.6 Flowcharts

4.6.1 Main Processing

Figure 4-1 shows the flowchart of the main processing.

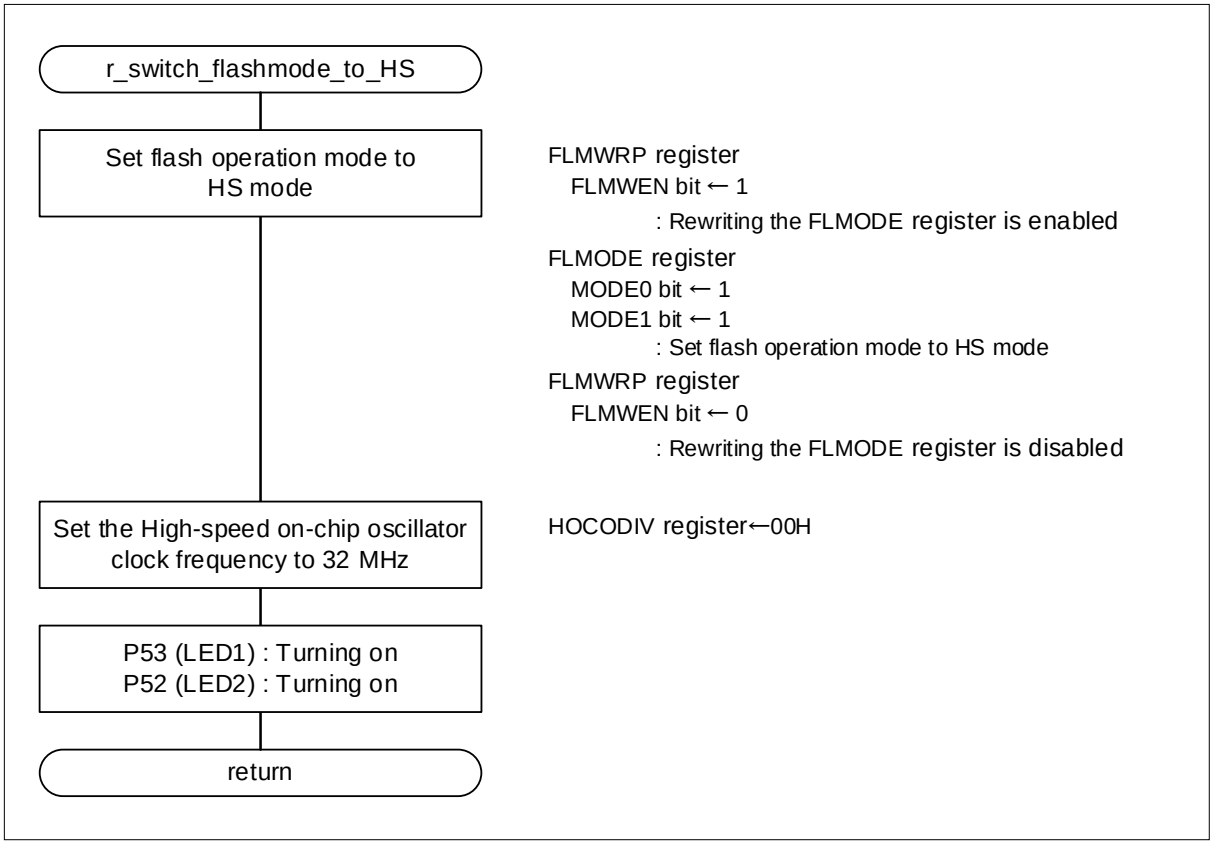
Figure 4-1 Main Processing



4.6.2 Flash Operation Mode Switching (HS) Processing

Figure 4-2 shows the flowchart of the flash operation mode switching (HS) processing.

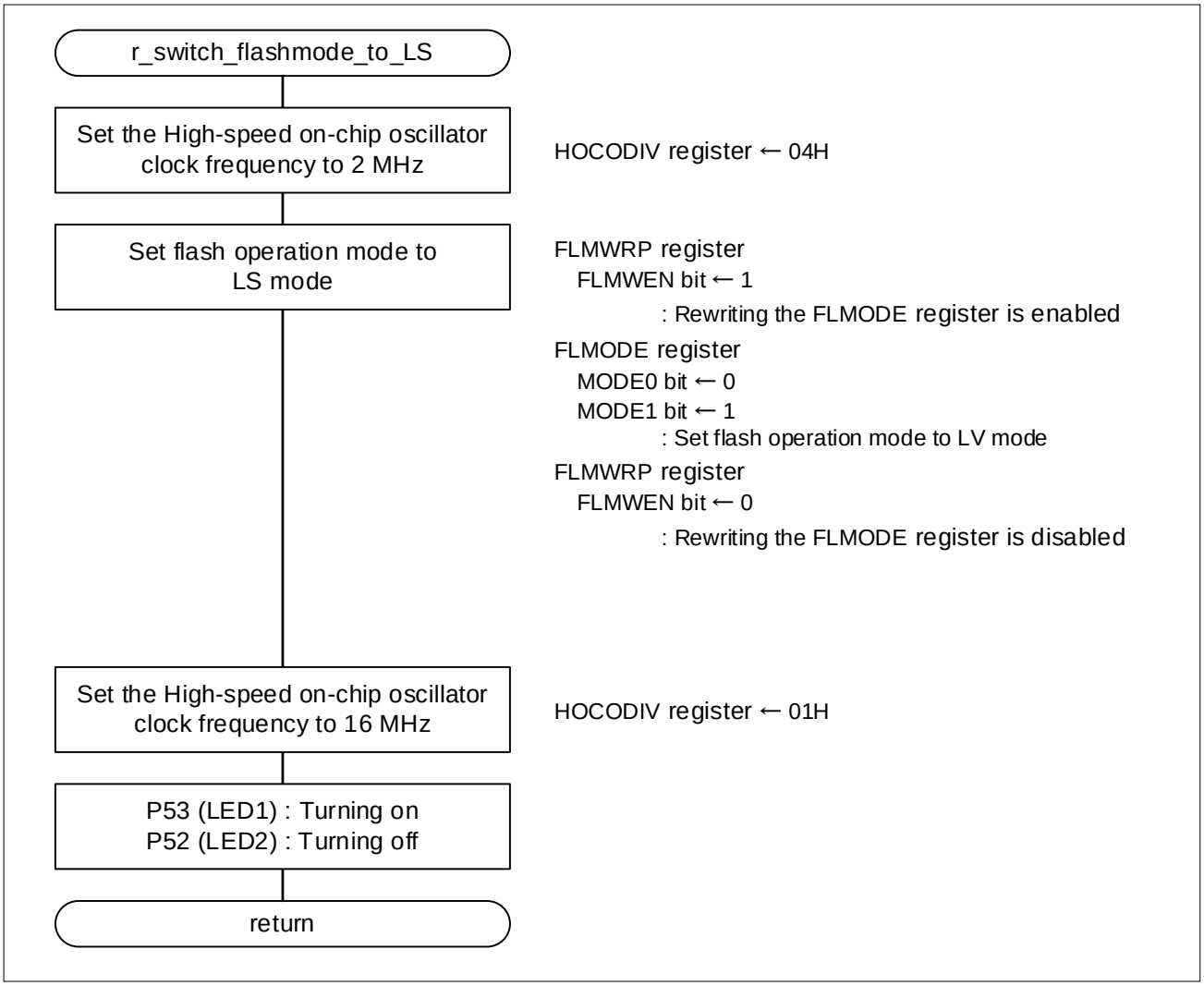
Figure 4-2 Flash Operation Mode Switching (HS) Processing



4.6.3 Flash Operation Mode Switching (LS) Processing

Figure 4-3 shows the flowchart of the flash operation mode switching (LS) processing.

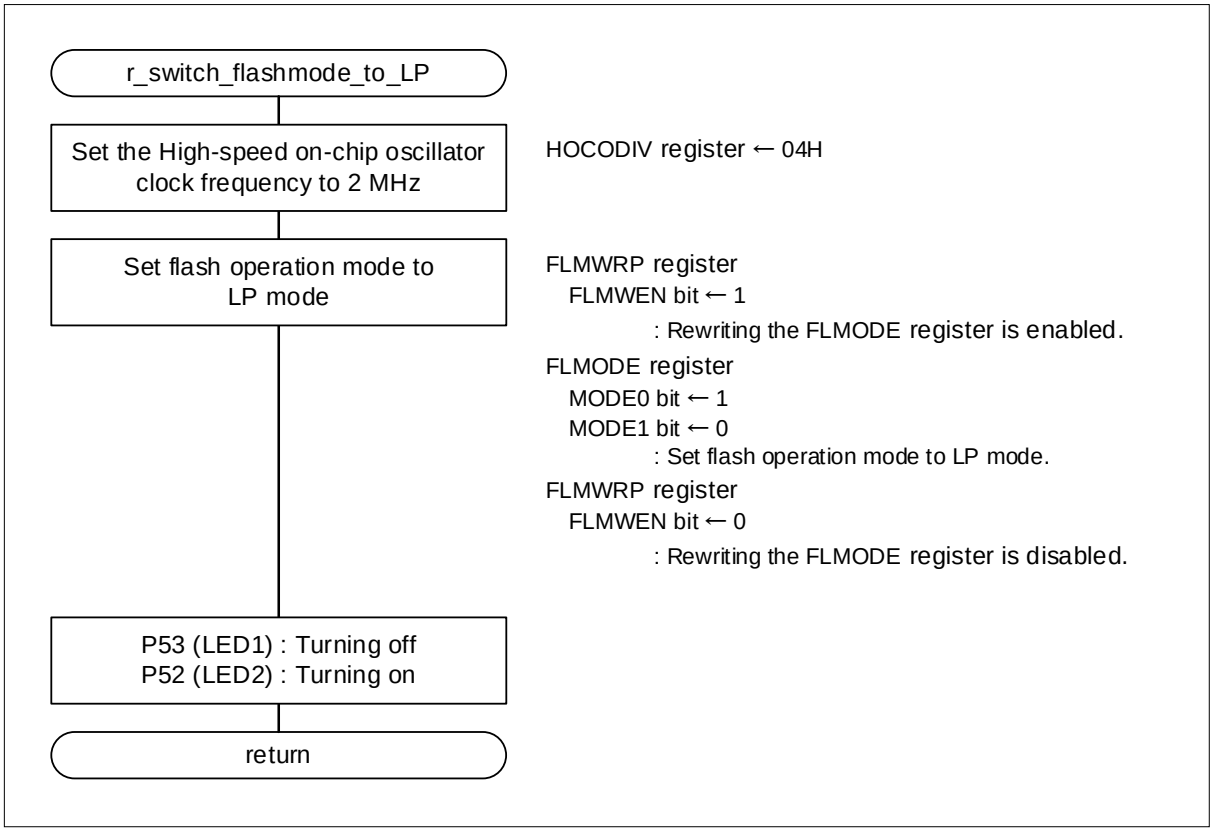
Figure 4-3 Flash Operation Mode Switching (LS) Processing



4.6.4 Flash Operation Mode Switching (LP) Processing

Figure 4-4 shows the flowchart of the flash operation mode switching (LP) processing.

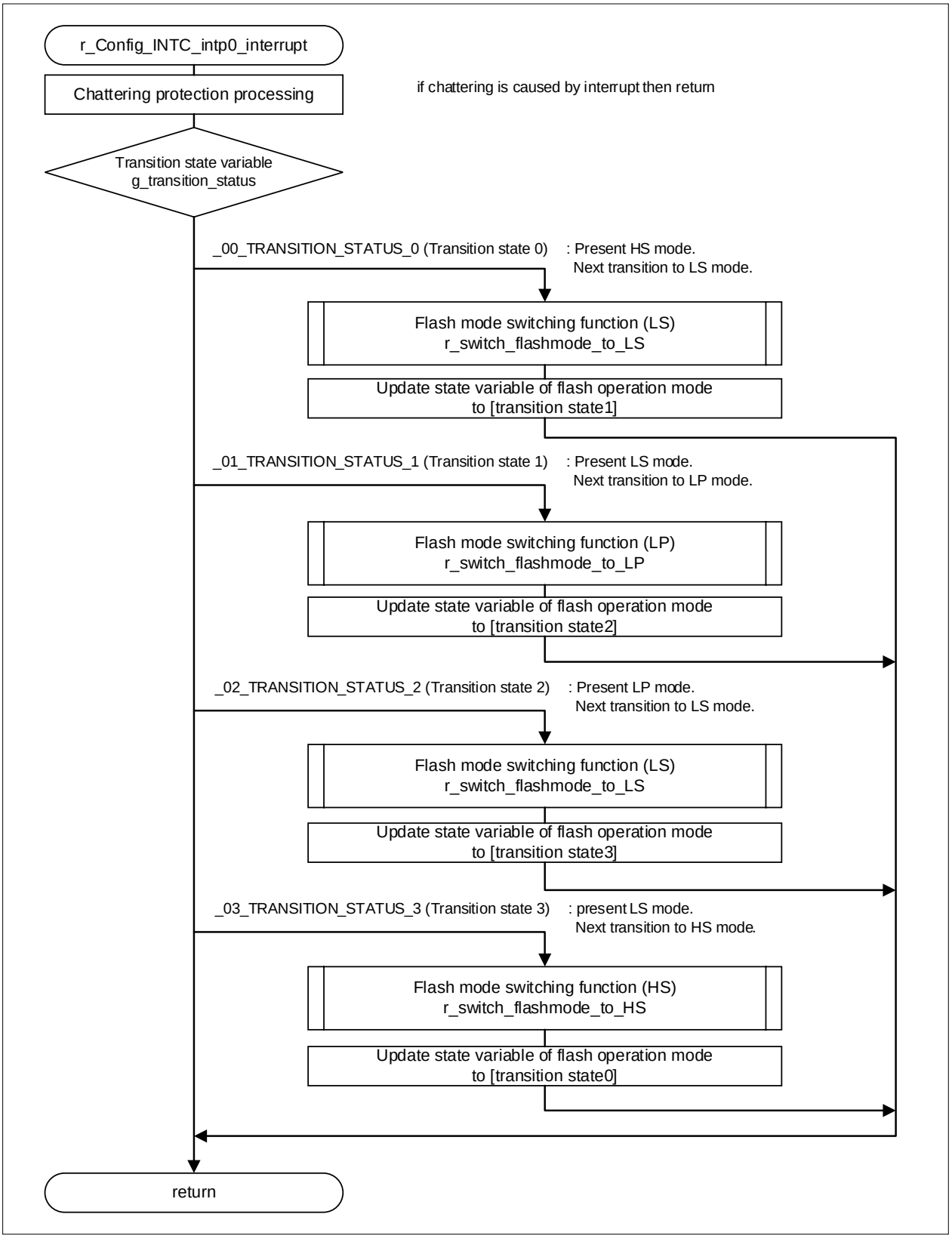
Figure 4-4 Flash Operation Mode Switching (LP) Processing



4.6.5 External Interrupt (INTP0) Processing

Figure 4-5 shows the flowchart of the external interruption (INTP0) processing.

Figure 4-5 External Interrupt (INTP0) Processing



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896J)
RL78 family user's manual software (R01US0015J)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2021.04.13	—	First Edition
1.01	2021.07.12	5	Updated the Operation Confirmation Conditions
1.02	2023.10.6	5	Updated the Operation Confirmation Conditions

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1. Precaution against Electrostatic Discharge (ESD)

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2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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