RL78/G23
Operation State Switching

Introduction

The application note shows the register setting sequence for the switch of RL78/G23 operation state, using the Operation State Control. After reset, it operates in the HS mode. The flash operation mode is switched one by one by the button pressing (HS mode → LS mode → LP mode → HS mode, repetition at the following).

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.
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1. Specifications

1.1 Overview of Specifications

Pressing the button generates an INTP0 interrupt and changes flash operation mode. After cycling through all operation transition states supported by RL78/G23, the state immediately after a reset is restored. LED1 and LED2 indicate flash operation modes.

Table 1-1 shows the peripheral function to be used and its use. Figure 1-1 shows the transitions of flash operation modes. Table 1-2 provides details and transitions of operation states.

Table 1-1  Peripheral functions used and their uses

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>External interrupt</td>
<td>Switch input</td>
</tr>
<tr>
<td>Port output</td>
<td>Controls the LEDs (LED1, LED2) connected to the P52 and P53 pins.</td>
</tr>
</tbody>
</table>

Figure 1-1  Operation state transition sequence order

Table 1-2  Operation state detail and operation state transition

<table>
<thead>
<tr>
<th>Flash operation mode</th>
<th>LED1</th>
<th>LED2</th>
<th>Operation clock</th>
<th>Range of operation voltage (Electrical characteristics)</th>
</tr>
</thead>
<tbody>
<tr>
<td>① HS mode</td>
<td>Turning on</td>
<td>Turning on</td>
<td>32 MHz</td>
<td>1.8 V to 5.5 V (1 to 32MHz: 1.8 V to 5.5 V)</td>
</tr>
<tr>
<td>② LS mode</td>
<td>Turning on</td>
<td>Turning off</td>
<td>16 MHz</td>
<td>1.8 V to 5.5 V (1 to 24 MHz: 1.8 V to 5.5 V)</td>
</tr>
<tr>
<td>③ LP mode</td>
<td>Turning off</td>
<td>Turning on</td>
<td>2 MHz</td>
<td>1.8 V to 5.5 V (1 to 2 MHz: 1.6 V to 5.5 V)</td>
</tr>
<tr>
<td>④ LS mode</td>
<td>Turning on</td>
<td>Turning off</td>
<td>16 MHz</td>
<td>1.8 V to 5.5 V (1 to 24 MHz: 1.8 V to 5.5 V)</td>
</tr>
</tbody>
</table>

Modes ① to ④ are cycled through when the button is pressed.
1.2 Outline of Operation

Each time a falling edge of the P137/INTP0 pin is detected when the switch is pressed, the CPU clock and operating mode are switched.

The following describes the main settings.

(1) Initial settings for input/output ports

P52 and P53 pins: Set as output ports (used for LED ON control)

Table 1-3 Initial Settings for Input/Output Ports (P52 and P53 Pins)

<table>
<thead>
<tr>
<th>Register/Bit Name</th>
<th>Setting Value</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>P5 register</td>
<td>00H</td>
<td>Output data of P52 and P53 is set to 0.</td>
</tr>
<tr>
<td>POM5 register</td>
<td>00H</td>
<td>Output mode of P52 and P53 is set to normal output mode.</td>
</tr>
<tr>
<td>PM5 register</td>
<td>00H</td>
<td>P52 and P53 are set to output mode.</td>
</tr>
</tbody>
</table>

(2) Initial settings for the clock generation circuit.

- Set flash operation mode to HS (high-speed main) mode.
  (Use the user option byte (000C2H/040C2H) for this setting.)
- Set the frequency of the high-speed on-chip oscillator clock to 32 MHz.
- Select the main system clock (f\textsubscript{MAIN}) for the CPU/peripheral hardware clock (f\textsubscript{CLK}).

(3) Initial settings for interrupt processing

- Set the effective edge of the INTP0 pin to falling edge to enable switch input.
- Check the pin voltage level at intervals of approximately 5 ms for determining switch input. When the voltage level is identical twice in a row, switch input is determined to be effective (chattering removed).

Table 1-4 Initial Settings for Input/Output Ports (P137/INTP0 Pin)

<table>
<thead>
<tr>
<th>Register/Bit Name</th>
<th>Setting Value</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>MK0L register</td>
<td>FFH</td>
<td>INTP0 interrupt prohibited</td>
</tr>
<tr>
<td>IF0L register</td>
<td>00H</td>
<td>INTP0 interrupt request flag clear</td>
</tr>
<tr>
<td>PR10L register</td>
<td>FFH</td>
<td>Level 3 is specified as INTP0 interrupt priority.</td>
</tr>
<tr>
<td>PR00L register</td>
<td>FFH</td>
<td></td>
</tr>
<tr>
<td>EGP0 register</td>
<td>00H</td>
<td>Falling edge is specified as INTP0 effective edge.</td>
</tr>
<tr>
<td>EGN0 register</td>
<td>01H</td>
<td></td>
</tr>
</tbody>
</table>
2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1  Operation Confirmation Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU used</td>
<td>RL78/G23 (R7F100GLG)</td>
</tr>
<tr>
<td>Board used</td>
<td>RL78/G23-64p Fast Prototyping Board (RTK7RLG230CLG000BJ)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>• High-speed on-chip oscillator clock (fIH): 32 MHz, 16 MHz, 2 MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5.0 V (can be operated at 2.0 V to 5.5 V)</td>
</tr>
<tr>
<td></td>
<td>LVD0 detection voltage: Reset mode</td>
</tr>
<tr>
<td></td>
<td>- At rising edge TYP. 1.90V (1.84 V to 1.95 V)</td>
</tr>
<tr>
<td></td>
<td>- At falling edge TYP. 1.86V (1.80 V to 1.91 V)</td>
</tr>
<tr>
<td>Integrated development environment (CS+)</td>
<td>CS+ for CC E8.05.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>C compiler (CS+)</td>
<td>CC-RL V1.10.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development environment (e2studio)</td>
<td>e2studio V2021-04 (21.4.0) from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>C compiler (e2studio)</td>
<td>CC-RL V1.10.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development environment (IAR)</td>
<td>IAR Embedded Workbench for Renesas RL78 V4.21.1 from IAR Systems Corp.</td>
</tr>
<tr>
<td>C compiler (IAR)</td>
<td>IAR C/C++ Compiler for Renesas RL78 V4.21.1.2260 from IAR Systems Corp.</td>
</tr>
<tr>
<td>Smart configurator (SC)</td>
<td>V1.0.1 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Board support package (BSP)</td>
<td>V1.00 from Renesas Electronics Corp.</td>
</tr>
</tbody>
</table>
3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

![Hardware Configuration Diagram]

Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to VDD or VSS through a resistor).

Note 2. Connect any pins whose name begins with EVSS to VSS, and any pins whose name begins with EVDD to VDD, respectively.

Note 3. VDD must not be lower than the reset release voltage (VLVD0) that is specified for the LVD0.

3.2 List of Pins Used

Table 3-1 shows the pins used and their functions.

<table>
<thead>
<tr>
<th>Pin name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P53</td>
<td>Output</td>
<td>LED1 turning on control</td>
</tr>
<tr>
<td>P52</td>
<td>Output</td>
<td>LED2 turning on control</td>
</tr>
<tr>
<td>P137 / INTP0</td>
<td>Input</td>
<td>Operation state switching</td>
</tr>
<tr>
<td>P140 / PCLBUZ0</td>
<td>Output</td>
<td>Clock output</td>
</tr>
</tbody>
</table>

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.
4. Software Explanation

4.1 Setting of Option byte

Table 4-1 shows the option byte settings. Please set the appropriate value to fit the different system.

Table 4-1  Option Byte Settings

<table>
<thead>
<tr>
<th>Address</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>000C0H / 040C0H</td>
<td>11101111B</td>
<td>Disables the watchdog timer. (Counting stopped after reset)</td>
</tr>
<tr>
<td>000C1H / 040C1H</td>
<td>11111110B</td>
<td>LVD0 detection voltage: reset mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At rising edge TYP. 1.90V (1.84 V to 1.95 V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At falling edge TYP. 1.86V (1.80 V to 1.91 V)</td>
</tr>
<tr>
<td>000C2H / 040C2H</td>
<td>11101000B</td>
<td>HS mode, High-speed on-chip oscillator clock (f_H): 32 MHz</td>
</tr>
<tr>
<td>000C3H / 040C3H</td>
<td>10000010B</td>
<td>Enables on-chip debugging</td>
</tr>
</tbody>
</table>

4.2 List of Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2  Constants used in sample code

<table>
<thead>
<tr>
<th>Constant Name</th>
<th>Setting Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>_00_TRANSITION_STATUS_0</td>
<td>00H</td>
<td>Transition status 0</td>
</tr>
<tr>
<td>_01_TRANSITION_STATUS_1</td>
<td>01H</td>
<td>Transition status 1</td>
</tr>
<tr>
<td>_02_TRANSITION_STATUS_2</td>
<td>02H</td>
<td>Transition status 2</td>
</tr>
<tr>
<td>_03_TRANSITION_STATUS_3</td>
<td>03H</td>
<td>Transition status 3</td>
</tr>
<tr>
<td>LED_ON</td>
<td>00H</td>
<td>LED control: ON</td>
</tr>
<tr>
<td>LED_OFF</td>
<td>01H</td>
<td>LED control: OFF</td>
</tr>
<tr>
<td>WAITCOUNT_32M</td>
<td>8000</td>
<td>5 ms count value during HS 32 MHz operation</td>
</tr>
<tr>
<td>WAITCOUNT_16M</td>
<td>4000</td>
<td>5 ms count value during LS 16 MHz operation</td>
</tr>
<tr>
<td>WAITCOUNT_2M</td>
<td>500</td>
<td>5 ms count value during LP 2 MHz operation</td>
</tr>
</tbody>
</table>
4.3 List of Variables

Table 4-3 lists global variables.

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable identifier</th>
<th>Content</th>
<th>Use function</th>
</tr>
</thead>
<tbody>
<tr>
<td>uint16_t</td>
<td>g_transition_status</td>
<td>Transition state variable</td>
<td>main (), r_Config_INTC_intp0_interrupt ()</td>
</tr>
</tbody>
</table>

4.4 List of Functions

Table 4-4 shows a list of functions.

<table>
<thead>
<tr>
<th>Function name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>r_switch_flashmode_to_HS</td>
<td>The flash operation state is switched to the HS mode.</td>
</tr>
<tr>
<td>r_switch_flashmode_to_LS</td>
<td>The flash operation state is switched to the LS mode.</td>
</tr>
<tr>
<td>r_switch_flashmode_to_LP</td>
<td>The flash operation state is switched to the LP mode.</td>
</tr>
<tr>
<td>r_Config_INTC_intp0_interrupt</td>
<td>External interrupt processing.</td>
</tr>
</tbody>
</table>
4.5 Specification of Functions
The function specifications of the sample code are shown below.

<table>
<thead>
<tr>
<th>Function</th>
<th>Overview</th>
<th>Header</th>
<th>Declaration</th>
<th>Description</th>
<th>Argument</th>
<th>Return value</th>
</tr>
</thead>
<tbody>
<tr>
<td>r_switch_flashmode_to_HS</td>
<td>The flash operation state is switched to the HS mode.</td>
<td>r_cg_macrodriver.h, r_cg_userdefine.h</td>
<td>void r_switch_flashmode_to_HS (void)</td>
<td>The flash operation state is switched to the HS mode.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r_switch_flashmode_to_LS</td>
<td>The flash operation state is switched to the LS mode.</td>
<td>r_cg_macrodriver.h, r_cg_userdefine.h</td>
<td>void r_switch_flashmode_to_LS (void)</td>
<td>The flash operation state is switched to the LS mode.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r_switch_flashmode_to_LP</td>
<td>The flash operation state is switched to the LP mode.</td>
<td>r_cg_macrodriver.h, r_cg_userdefine.h</td>
<td>void r_switch_flashmode_to_LP (void)</td>
<td>The flash operation state is switched to the LP mode.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r_Config_INTC_intp0_interrupt</td>
<td>External interrupt processing</td>
<td>r_cg_macrodriver.h, r_cg_userdefine.h, Config_INTC.h</td>
<td>static void __near r_Config_INTC_intp0_interrupt (void)</td>
<td>Pushing button calls this function where operation state switching is executed.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4.6 Flowcharts

4.6.1 Main Processing

Figure 4-1 shows the flowchart of the main processing.

Figure 4-1 Main Processing

```plaintext
main

INTP0 interrupt enable processing
R_Config_INTC_INTP0_Start

Crock output start processing
R_Config_PCLBUZ0_Start

Enable interrupt

Flash mode switching function (HS)
r_switch_flashmode_to_HS

Update state variable of flash operation mode
to [transition state 0]

: while(1) loop

HALT

External interrupt input
(INTP0)
```
4.6.2 Flash Operation Mode Switching (HS) Processing

Figure 4-2 shows the flowchart of the flash operation mode switching (HS) processing.

Figure 4-2 Flash Operation Mode Switching (HS) Processing

r_switch_flashmode_to_HS

Set flash operation mode to HS mode

Set the High-speed on-chip oscillator clock frequency to 32 MHz

P53 (LED1) : Turning on
P52 (LED2) : Turning on

return

FLMWRP register
FLMKEN bit ← 1
: Rewriting the FLMODE register is enabled

FLMODE register
MODE0 bit ← 1
MODE1 bit ← 1
: Set flash operation mode to HS mode

FLMWRP register
FLMKEN bit ← 0
: Rewriting the FLMODE register is disabled

HOCODIV register—00H
4.6.3 Flash Operation Mode Switching (LS) Processing

Figure 4-3 shows the flowchart of the flash operation mode switching (LS) processing.

Figure 4-3 Flash Operation Mode Switching (LS) Processing

```
    r_switch_flashmode_to_LS
    Set the High-speed on-chip oscillator clock frequency to 2 MHz
    Set flash operation mode to LS mode
    HOCODIV register ← 04H

    FLMWRP register
    FLMWEN bit ← 1
    : Rewriting the FLMODE register is enabled
    FLMODE register
    MODE0 bit ← 0
    MODE1 bit ← 1
    : Set flash operation mode to LV mode
    FLMWRP register
    FLMWEN bit ← 0
    : Rewriting the FLMODE register is disabled

    Set the High-speed on-chip oscillator clock frequency to 16 MHz
    HOCODIV register ← 01H

    P53 (LED1): Turning on
    P52 (LED2): Turning off
    return
```
4.6.4 Flash Operation Mode Switching (LP) Processing

Figure 4-4 shows the flowchart of the flash operation mode switching (LP) processing.

Figure 4-4  Flash Operation Mode Switching (LP) Processing

- Set the High-speed on-chip oscillator clock frequency to 2 MHz
- Set flash operation mode to LP mode
- HOCODIV register ← 04H
- FLMWRP register
  - FLMWEN bit ← 1
  - : Rewriting the FLMODE register is enabled.
- FLMODE register
  - MODE0 bit ← 1
  - MODE1 bit ← 0
  - : Set flash operation mode to LP mode.
- FLMWRP register
  - FLMWEN bit ← 0
  - : Rewriting the FLMODE register is disabled.
- P53 (LED1) : Turning off
  - P52 (LED2) : Turning on
- return
4.6.5 External Interrupt (INTP0) Processing

Figure 4-5 shows the flowchart of the external interruption (INTP0) processing.

**Figure 4-5  External Interrupt (INTP0) Processing**

- **r_Config_INTC_intp0_interrupt**
  - Chattering protection processing
  - Transition state variable: `g_transition_status`
  - If chattering is caused by interrupt, return

- **_00_TRANSITION_STATUS_0 (Transition state 0)**: Present HS mode. Next transition to LS mode.
  - Flash mode switching function (LS): `r_switch_flashmode_to_LS`
  - Update state variable of flash operation mode to [transition state 1]

- **_01_TRANSITION_STATUS_1 (Transition state 1)**: Present LS mode. Next transition to LP mode.
  - Flash mode switching function (LP): `r_switch_flashmode_to_LP`
  - Update state variable of flash operation mode to [transition state 2]

- **_02_TRANSITION_STATUS_2 (Transition state 2)**: Present LP mode. Next transition to LS mode.
  - Flash mode switching function (LS): `r_switch_flashmode_to_LS`
  - Update state variable of flash operation mode to [transition state 3]

- **_03_TRANSITION_STATUS_3 (Transition state 3)**: Present LS mode. Next transition to HS mode.
  - Flash mode switching function (HS): `r_switch_flashmode_to_HS`
  - Update state variable of flash operation mode to [transition state 0]

**return**
5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User's Manual: Hardware (R01UH0896J)
RL78 family user's manual software (R01US0015J)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

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## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Description</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>2021.04.13</td>
<td>—</td>
<td>First Edition</td>
<td></td>
</tr>
<tr>
<td>1.01</td>
<td>2021.07.12</td>
<td>5</td>
<td>Updated the Operation Confirmation Conditions</td>
<td></td>
</tr>
</tbody>
</table>
General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.
   Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
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