RL78/G23

I2C Supporting Multiple Slave Addresses (Slave)

Introduction

This application note describes how to use the slave function of the I2C bus that supports multiple slave addresses by using the all addresses matching function of the RL78/G23.

This application note enables a function of four serial memory areas (256 bytes × 4) designated by respective slave addresses.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Basic Specifications of the I2C Bus (Slave)

The following lists the basic specifications of the I2C bus.

・I2C bus to be connected: Fast mode (up to 400 kbps)

・Slave address 1: 0010000B (First serial memory)

・Slave address 2: 0100100B (Second serial memory)

・Slave address 3: 1011010B (Third serial memory)

・Slave address 4: 1101011B (Fourth serial memory)

・Extension code: Not supported (Ignored and escapes from communication)

Note: In the RL78 family, the own address (7 bits) is expressed by the upper 7 bits of the SVA0 register.

　　　The least significant bit (LSB) of the SVA0 register is always 0.

Table 1-1 lists peripheral functions to be used.

Table 1-1　Peripheral Function and Use

Peripheral Function	Use
IICA0	Slave function of the I2C bus
TM07	5 ms interval timer interrupt

The following describes the main settings.

　(1) Initial settings for IICA0

　　Table 1-2 lists Initial Settings for IICA0.

Table 1-2　Initial Settings for IICA0

Register Name	Setting Value	Description
IICCTL01	4DH	All addresses match function enabled, fast mode, digital filter on, IICA0 operating clock f_{CLK}/2
IICWL0	15H	SCLA0 low width
IICWH0	14H	SCLA0 high width
SVA0	50H	Slave address 50H
IICF0	03H	Bus released, communication reservation disabled
IICCTL00	1CH	SPD interrupt enabled, wait at the 9th clock, ACK response enabled
P6	00H	SCL/SDA signal multiplexed pins: Set to 0
PM6	00H	SCL/SDA signal pins: Set to output

(2) Initial settings for TM07

Table 1-3 lists the Initial Settings for TM07.

Table 1-3 Initial Settings for TM07

Register Name	Setting Value	Description
TPS0	0020H	CK00/CK02/CK03: 32 MHz, CK01: 8 MHz
TT0	0AFFH	Count operation of all channels are stopped
TMPR007	0	Interrupt priority: Level 2
TMR07	8000H	TM07 count clock: CK01 (8 MHz)
TDR07	40000	Interval time: 5 ms
TOM0	00H	TM07: Master mode
TOL0	00H	TM07 output: Positive logic
TO0	00H	TM07 output: 0
TOE0	00H	TM07 output: Disabled

1.2 Outline of Operation

Four 256-byte serial memory (serial RAM) areas are enabled. The internal address of each serial RAM is designated by the 1-byte data (register address) next to the slave address. The received slave address is indicated by LEDs.

1.3 Identifying Slave Address

When the all addresses match function is enabled (SVADIS0 = 1), the RL78/G23 operates in the same way as extension code reception. An INTIICA0 interrupt of the slave is generated at the falling edge of the 8th clock during reception of the slave address. When the received slave address is valid, an ACK response (ACKE0 =1) is returned. If it is invalid, the RL78/G23 escapes from communication (LREL0 = 1).

In this application note, WTIM0 is set to 1 to generate an interrupt request at the falling edge of the 9th clock. Therefore, an INTIICA0 interrupt is generated twice during reception of the slave address.

1.4   RAM Function

Data can be written to or read from the slave address and the serial RAM address designated by the next 1-byte data (register address).

When the transfer direction ($\overline{W}$) following the valid slave address is specified, the slave stores the next receive data (register address), and then writes received data to the designated register addresses sequentially.

Figure 1-1 Continuous Data Write to Designated Register Addresses
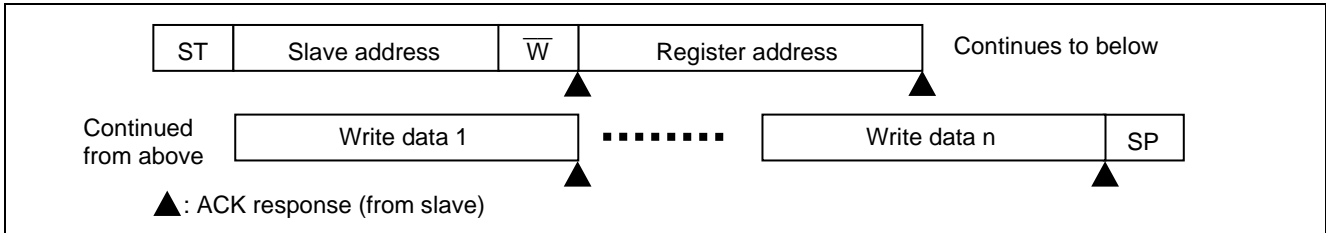
When the transfer direction ($\overline{W}$) following the valid slave address is specified, the slave stores the next receive data (register address). After that, when the slave receives start conditions, valid slave address, and transfer direction (R), the slave sequentially reads data from the previously designated register address, and then sends the data to the master.

Figure 1-2 Continuous Data Read from Designated Register Addresses
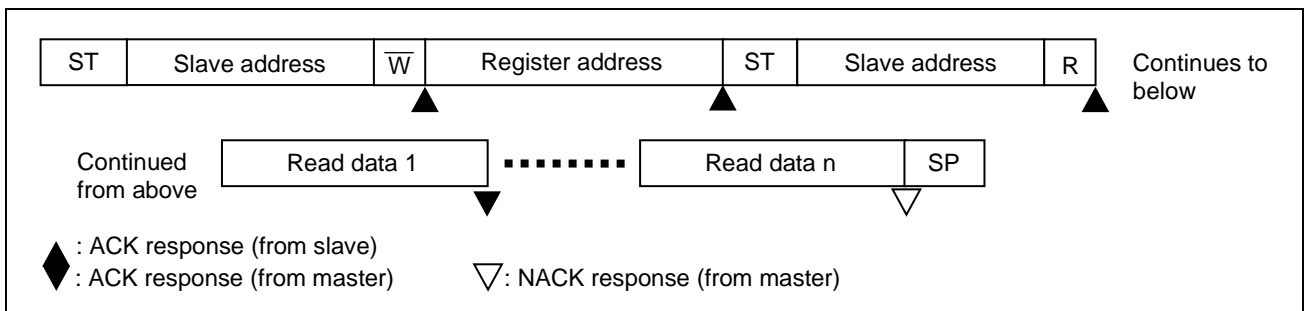
Upon completion of data read or write, the slave increments the designated address to prepare for the next data read or write. After the last address (FFH) is accessed, the next address becomes the first address (00H). The selected serial RAM is not switched by incrementing the address.

2.　Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

**Table 2-1** Operation Confirmation Conditions

Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	High-speed on-chip oscillator clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	3.3 V (can be operated at 1.8 V to 5.5 V) LVD0 detection voltage: Reset mode 　At rising edge TYP. 3.96 V (3.84 V to 4.08 V) 　At falling edge TYP. 3.88 V (3.76 V to 4.00 V)
Integrated development environment (CS+)	CS+ V8.05.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.10.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2 studio V2021-04 (21.4.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.10.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.1 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.1 from IAR Systems Corp.
Smart configurator (SC)	V1.0.1 from Renesas Electronics Corp.
Board support package (BSP)	V1.00 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 Hardware Configuration shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration

Dotted lines indicate RTK7RLG230
Individual LEDs can be used as OSX10201-R
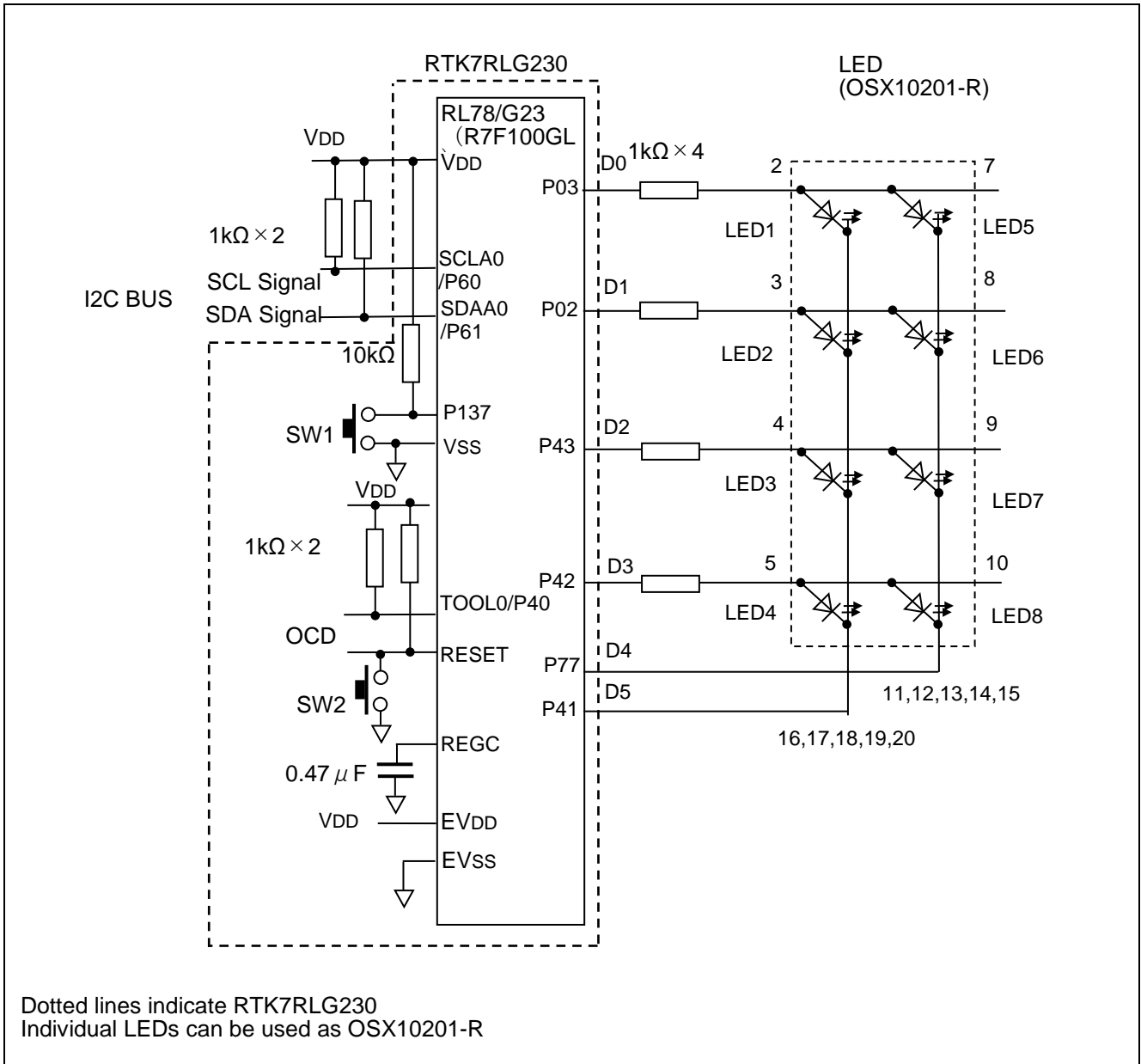
Note 1.   This schematic circuit diagram is simplified to show the outline of connections. When creating actual circuits, design them using appropriate pin processing so that the circuits meet electrical characteristics. (Connect input-only ports to V_{DD} or V_{SS} individually through a resistor.)

Note 2.   Connect pins (with a name beginning with EV_{SS}), if any, to V_{SS}, and connect pins (with a name beginning with EV_{DD}), if any, to V_{DD}.

Note 3.   Set V_{DD} to a voltage not less than the reset release voltage (V_{LVD0}) set by the LVD.

3.2   List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1   Pins to be Used and Their Functions

Pin Name	I/O	Function
P03 (D0)	Output	Drives LED1 and LED5.
P02 (D1)	Output	Drives LED2 and LED6.
P43 (D2)	Output	Drives LED3 and LED7.
P42 (D3)	Output	Drives LED4 and LED8.
P77 (D4)	Output	Lights the lower 4 bits of LEDs.
P41 (D5)	Output	Lights the upper 4 bits of LEDs.
P61 (D14)	Input / Output	SDA signal
P60 (D15)	Input / Output	SCL signal
P137 (D18)	Input	Switch (SW1) input

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Description
000C0H / 010C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 010C1H	11111010B	LVD0 detection voltage: reset mode At rising edge TYP. 3.96 V At falling edge TYP. 3.88 V
000C2H / 010C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 010C3H	10000100B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2 Constants

Constant Name	Setting Value	Description
D0_pin	P0_bit.no3	Port corresponding to the D0 pin
D1_pin	P0_bit.no2	Port corresponding to the D1 pin
D2_pin	P4_bit.no3	Port corresponding to the D2 pin
D3_pin	P4_bit.no2	Port corresponding to the D3 pin
SEL_L	P7_bit.no7	Lower LED select pin
SEL_U	P4_bit.no1	Upper LED select pin
SW_IN	P13_bit.no7	Onboard switch input pin
LED_ON	0	Common data value for turning on LEDs
LED_OFF	1	Common data value for turning off LEDs
RAM1	0b0010000	7-bit slave address of RAM1
RAM2	0b0100100	7-bit slave address of RAM2
RAM3	0b1011010	7-bit slave address of RAM3
RAM4	0b1101011	7-bit slave address of RAM4
PAGE_SIZE	256	RAM size
HIGH	0x01	High level
LOW	0x00	Low level

4.3 List of Variables

Table 4-3 lists global variables.

Table 4-3 Global Variables

Type	Variable Name	Description	Function Used
uint8_t	g_ram_[4][256]	RAM data area (256 bytes × 4)	R_IICA0_Init(), iica0_slave_handler()
uint16_t	gp_ram[4]	Register address	R_IICA0_Init(), iica0_slave_handler()
uint8_t	g_prev_status	Immediately previous communication status	R_IICA0_Init(), iica0_slave_handler()
uint8_t	g_status	Current communication status 0x00: Successful completion (waiting for the next communication) 0x01: Register address is being received 0x02: Data is being transmitted 0x03: Data is being received	R_IICA0_Init(), iica0_slave_handler()
uint8_t	g_sl_addr	Received slave address	R_IICA0_Init(), iica0_slave_handler()
uint8_t	g_selRAM	Selected RAM	iica0_slave_handler()
uint8_t	g_disp_data	LED display data	R_LED_Init(), r_tau0_channel7_interrupt()
uint8_t	g_5ms	5 ms counter	R_LED_Init(), r_tau0_channel7_interrupt()

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function Name	Outline
R_Config_IICA0_Create()	IICA0 initial setting processing
R_Config_IICA0_Create_UserInit()	Enabling the all addresses matching function
R_IICA0_Init()	IICA0 variables initialization processing
r_Config_IICA0_interrupt()	IICA0 interrupt processing
r_IICA0_slave_handler()	IICA0 slave interrupt processing
r_sl_addr_get()	IICA0 reception slave address read processing
r_status_chk()	IICA0 communication status read processing
R_Config_PORT_Create()	Port initial setting processing
R_LED_Init()	LED display initialization processing
R_Config_TAU0_7_Create()	TM07 initial setting processing
r_Config_TAU0_7_interrupt()	Interval timer (5 ms) interrupt processing

4.5   Specification of Functions

The function specifications of the sample code are shown below.

R_Config_IICA0_Create()

Outline	IICA0 initial setting processing
Header	r_cg_macrodriver.h, Config_IICA0.h, r_cg_userdefine.h
Declaration	void R_Config_IICA0_Create(void)
Description	Makes initial settings for the IICA0 function.
Argument	None
Return Value	None

R_Config_IICA0_Create_UserInit ()

Outline	Enabling all addresses matching function
Header	r_cg_macrodriver.h, Config_IICA0.h, r_cg_userdefine.h
Declaration	void R_Config_IICA0_Create_UserInit(void)
Description	Enables the all addresses matching function of IICA0.
Argument	None
Return Value	None

R_IICA0_Init()

Outline	IICA0 variables initialization processing
Header	r_cg_macrodriver.h, Config_IICA0.h, r_cg_userdefine.h
Declaration	void R_IICA0_Init(void)
Description	Initializes variables and registers used for IICA0.
Argument	None
Return Value	None

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r_Config_IICA0_interrupt ()

Outline	IICA0 interrupt processing
Header	r_cg_macrodriver.h, Config_IICA0.h, r_cg_userdefine.h
Declaration	static void __near r_Config_IICA0_interrupt(void)
Description	Receives an IICA0 interrupt request and performs required processing.
Argument	None
Return Value	None

---

r_ IICA0_slave_handler ()

Outline	IICA0 slave interrupt processing
Header	r_cg_macrodriver.h, Config_IICA0.h, LED_LIB.h, r_cg_userdefine.h
Declaration	static void r_IICA0_slave_handler(void)
Description	Checks whether the slave address is valid upon receiving a slave interrupt from IICA0. When the address is valid, a response is returned according to the request from the master. If the address is invalid, the interrupt processing is exited.
Argument	None
Return Value	None

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r_sl_addr_get()

Outline	Slave address read processing	
Header	r_cg_macrodriver.h, Config_IICA0.h, r_cg_userdefine.h	
Declaration	uint8_t r_sl_addr_get(void)	
Description	Returns the received slave address.	
Argument	None	
Return Value	uint8_t	The latest received slave address

r_status_chk()

Outline	IICA0 communication status read processing	
Header	r_cg_macrodriver.h, Config_IICA0.h, r_cg_userdefine.h	
Declaration	uint8_t r_status_chk(void)	
Description	Reads the IICA0 communication status (g_prev_status), and then clears it.	
Argument	None	
Return Value	uint8_t	g_prev_status value

R_Config_PORT_Create()

Outline	Port initial setting processing
Header	r_cg_macrodriver.h, Config_PORT.h, r_cg_userdefine.h
Declaration	void R_Config_PORT_Create(void)
Description	Makes initial settings for ports used for the LED display.
Argument	None
Return Value	uint8_t

R_LED_Init()

Outline	LED display initialization processing
Header	r_cg_macrodriver.h, Config_TAU0_7.h,r_cg_userdefine.h
Declaration	void R_LED_Init(void)
Description	Initializes variables used for the LED display.
Argument	None
Return Value	uint8_t

R_Config_TAU0_7_Create()

Outline	Timer array unit initialization processing
Header	r_cg_macrodriver.h, Config_TAU0_7.h,r_cg_userdefine.h
Declaration	void R_Config_TAU0_7_Create(void)
Description	Makes initial settings for the TAU0 function.
Argument	None
Return Value	None

## r_Config_TAU0_7_interrupt ()

Outline	Slave address read processing
Header	r_cg_macrodriver.h, Config_TAU0_7.h,r_cg_userdefine.h
Declaration	static void __near r_Config_TAU0_7_interrupt (void)
Description	Switches the LED display (between upper 4 bits and lower 4 bits) at intervals of 5 ms.
Argument	None
Return Value	None

4.6 Flowcharts

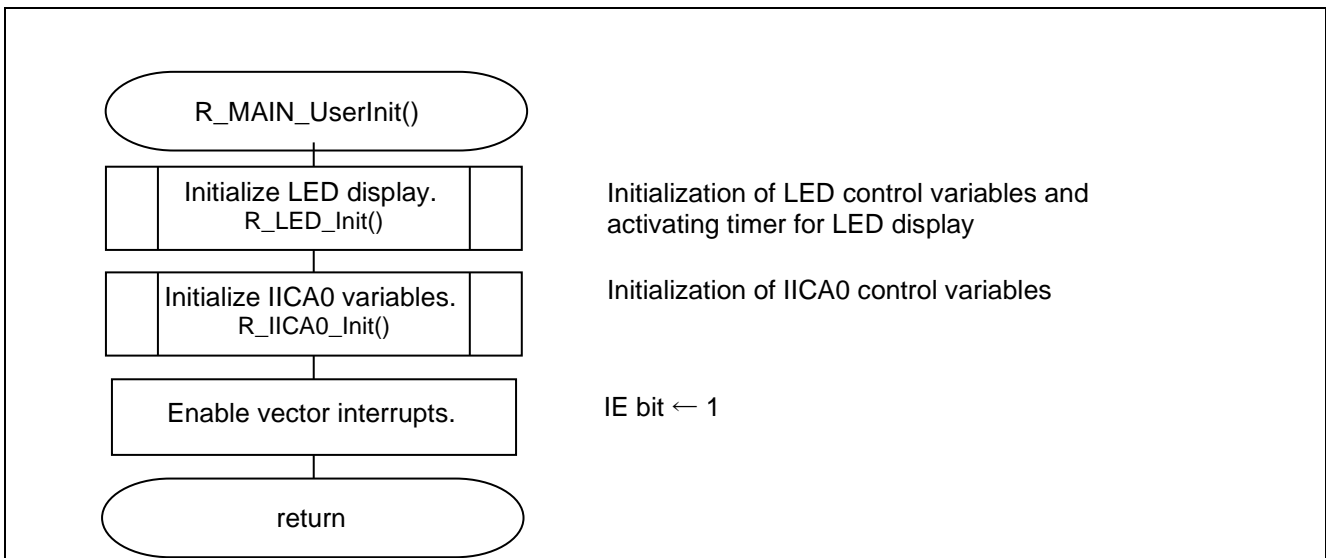### 4.6.1 Main Processing

Figure 4-1 shows the flowchart of the main processing.

Figure 4-1 Main Processing
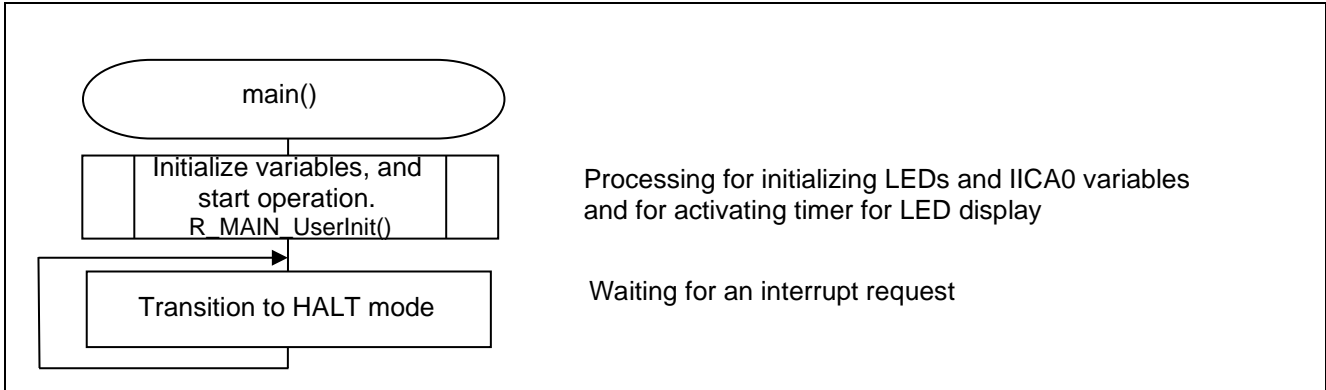
4.6.2 Variables Initialization Processing

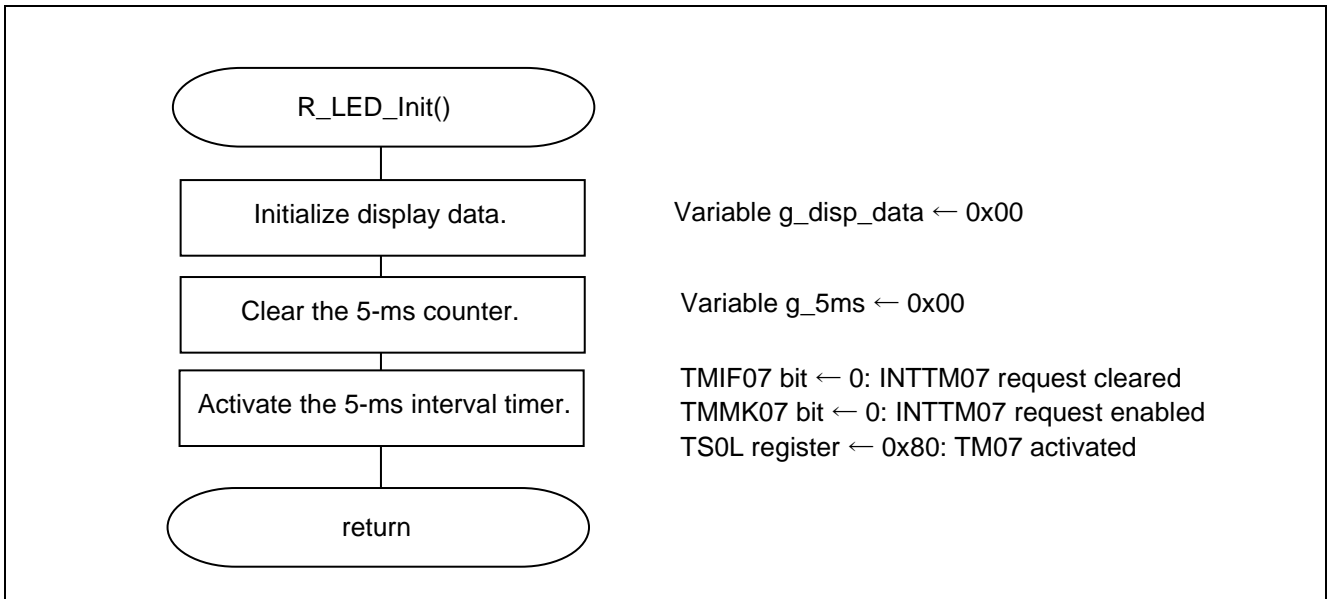Figure 4-2 shows the flowchart of the variables initialization function.

Figure 4-2 Variables Initialization Function

4.6.3 LED Display Initialization Function

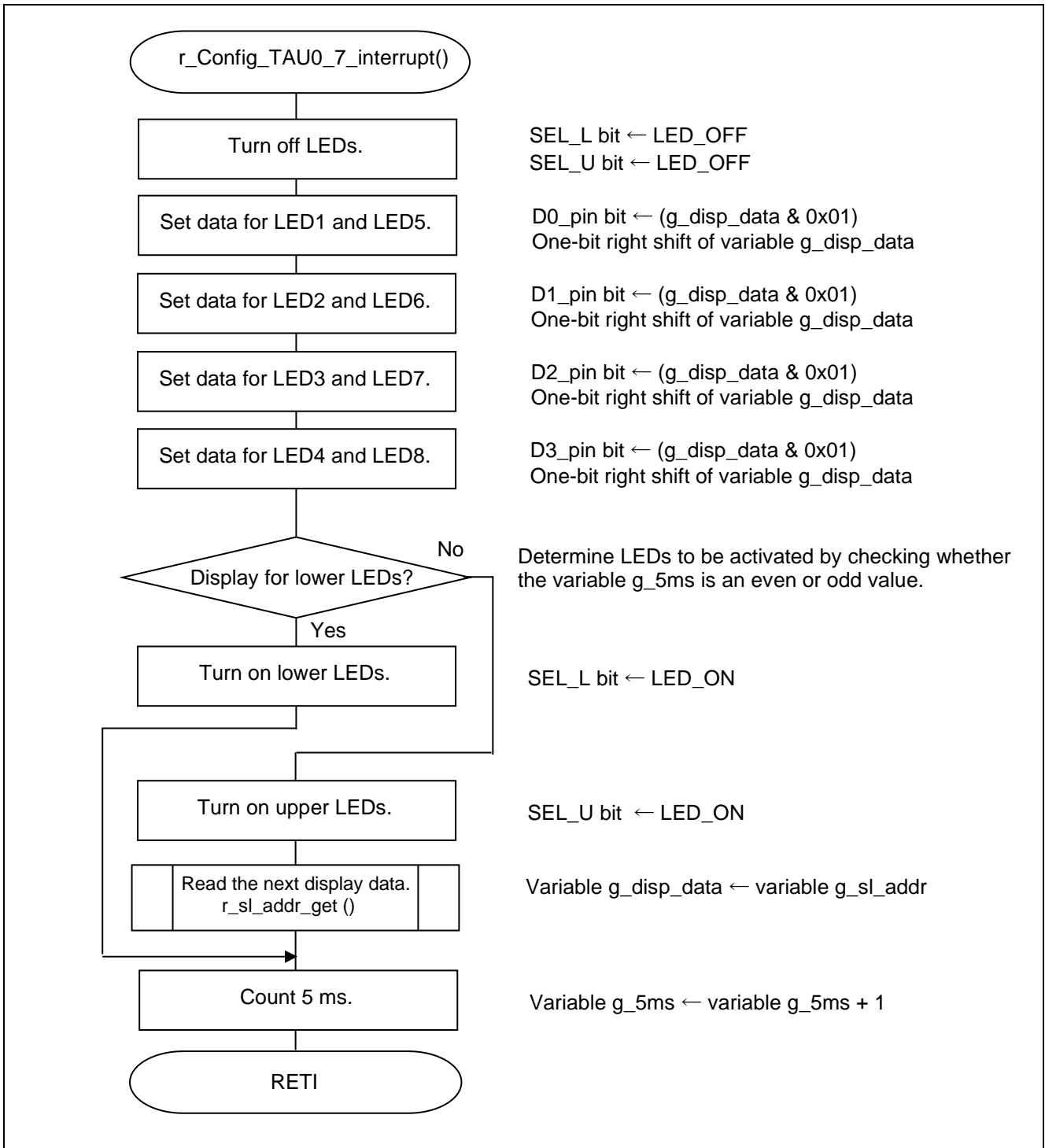Figure 4-3 shows the flowchart of the LED display initialization function.

Figure 4-3 LED Display Initialization Function

R_LED_Init()

Initialize display data.   Variable g_disp_data ← 0x00

Clear the 5-ms counter.   Variable g_5ms ← 0x00

Activate the 5-ms interval timer.   TMIF07 bit ← 0: INTTM07 request cleared
TMMK07 bit ← 0: INTTM07 request enabled
TS0L register ← 0x80: TM07 activated

return

4.6.4 Interval Timer (5 ms) Interrupt Processing Function

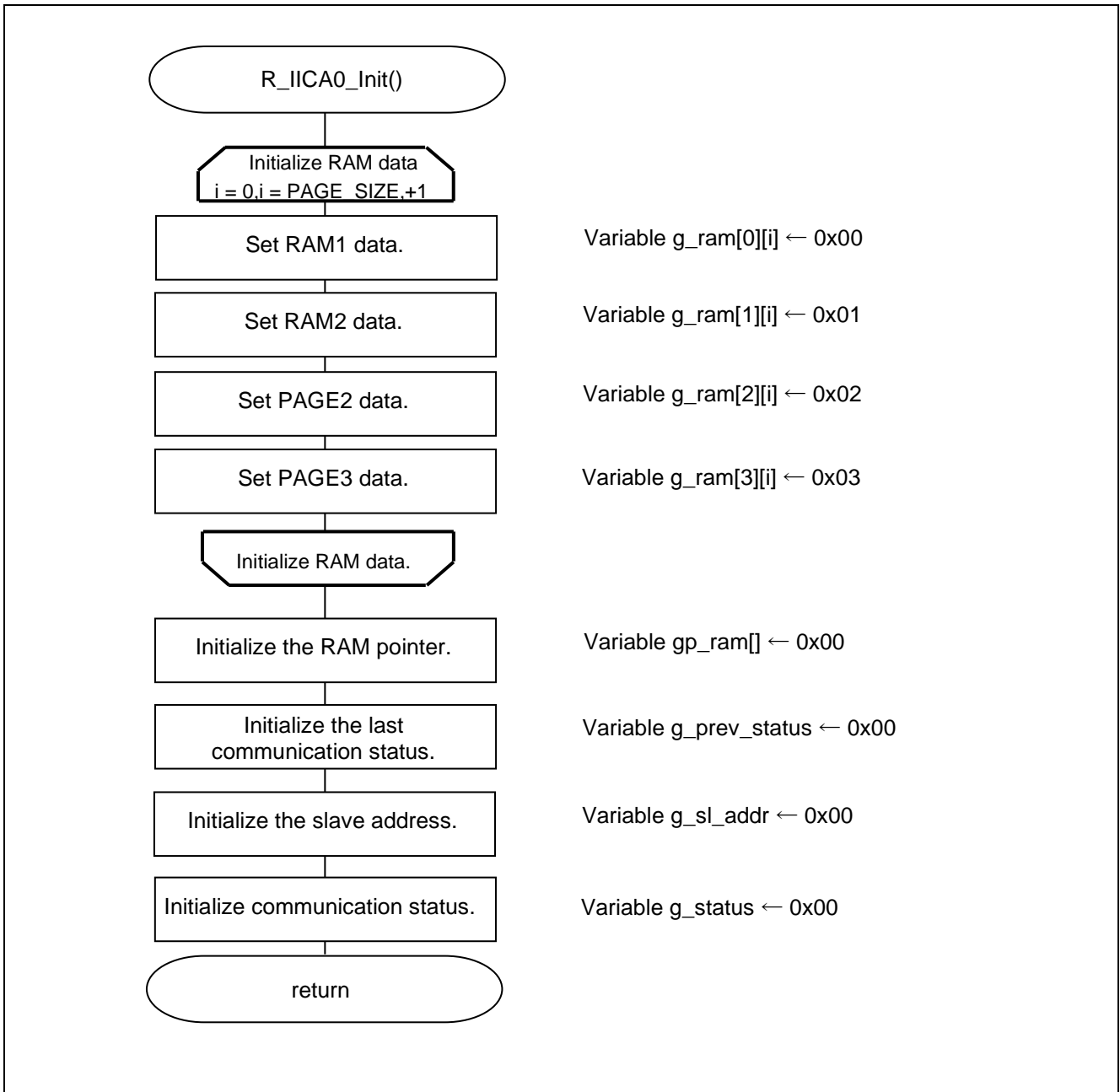Figure 4-4 shows the flowchart of the interval timer (5 ms) interrupt processing function.

Figure 4-4 Interval Timer (5 ms) Interrupt Processing Function

4.6.5 IICA0 Variables Initialization Processing Function

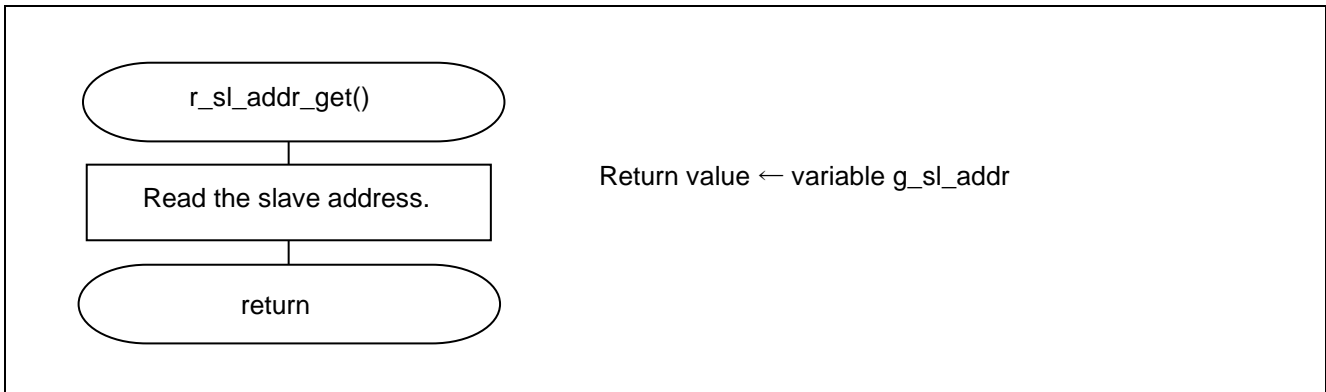Figure 4-5 shows the flowchart of the IICA0 variables initialization processing function.

Figure 4-5   IICA0 Variables Initialization Processing Function

4.6.6 Slave Address Read Processing Function

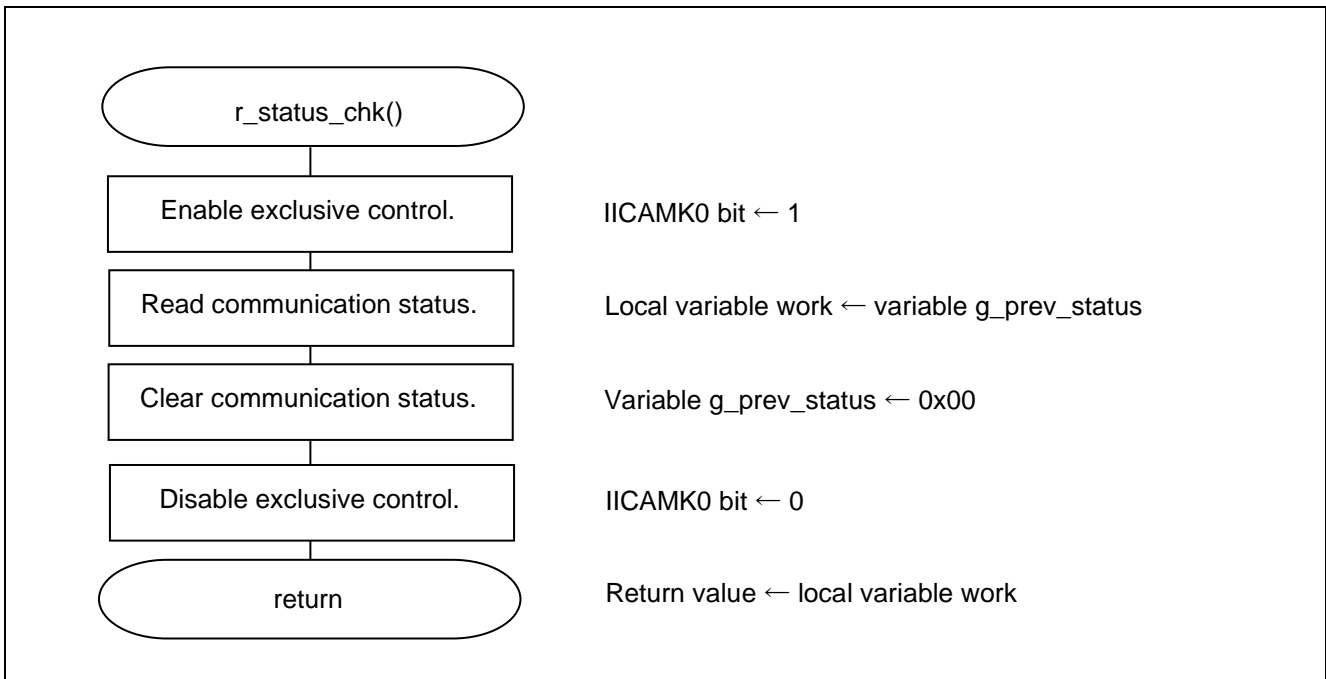Figure 4-6 shows the flowchart of the slave address read processing function.

Figure 4-6 Slave Address Read Processing Function

4.6.7 IICA0 Communication Status Read Processing Function

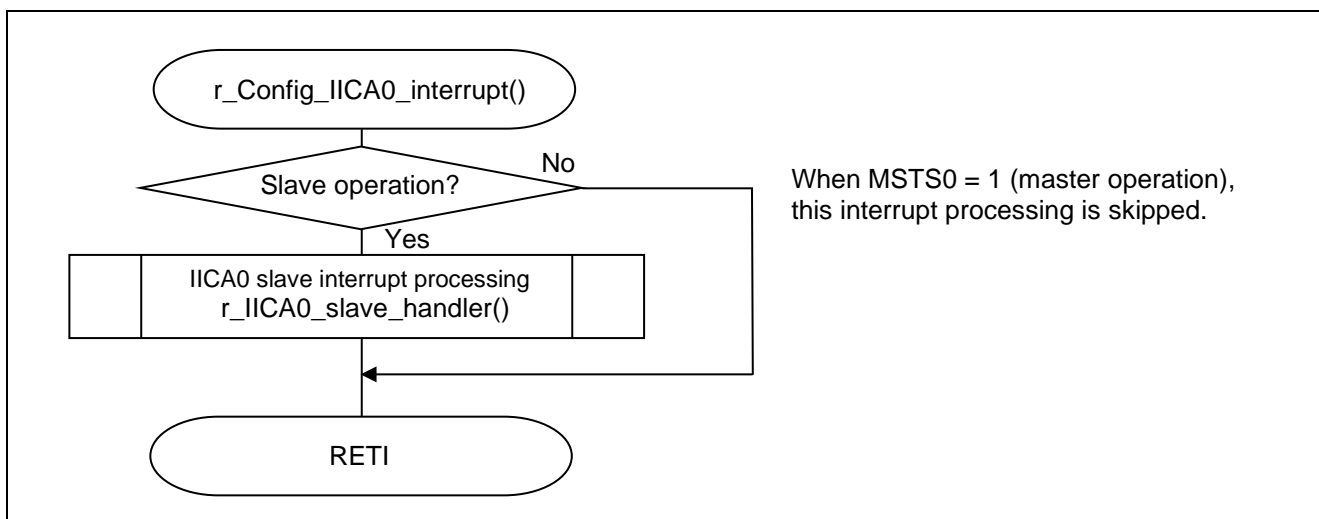Figure 4-7 shows the flowchart of the IICA0 communication status read processing function.

Figure 4-7 IICA0 Communication Status Read Processing Function

4.6.8 IICA0 Interrupt Processing Function

Figure 4-8 shows the flowchart of the IICA0 interrupt processing function.

Figure 4-8 IICA0 Interrupt Processing Function

4.6.9 IICA0 Slave Interrupt Processing Function

Figure 4-9 to Figure 4-12 show the flowchart of the IICA0 slave interrupt processing function.

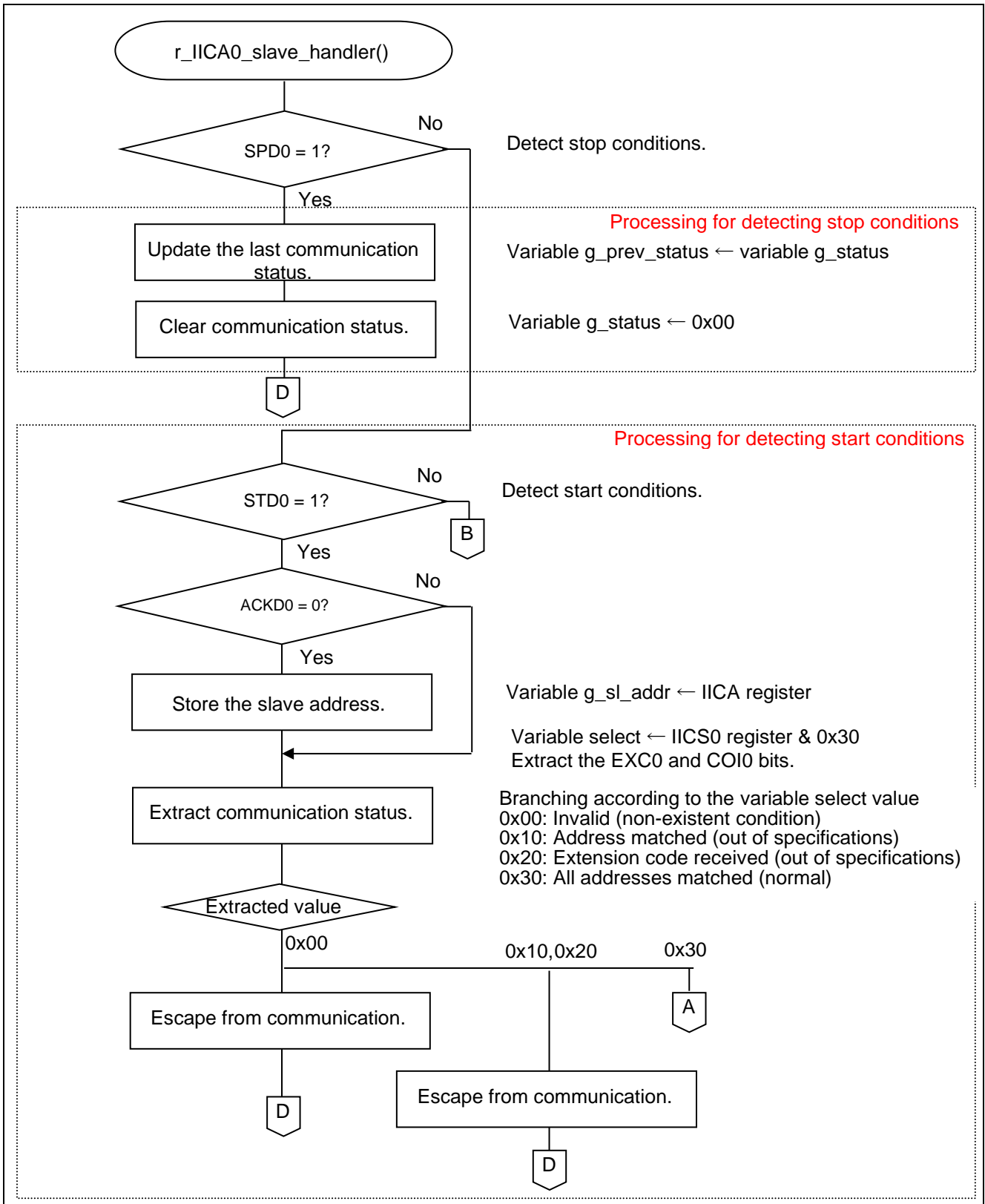**Figure 4-9** IICA0 Slave Interrupt Processing Function (1/4)

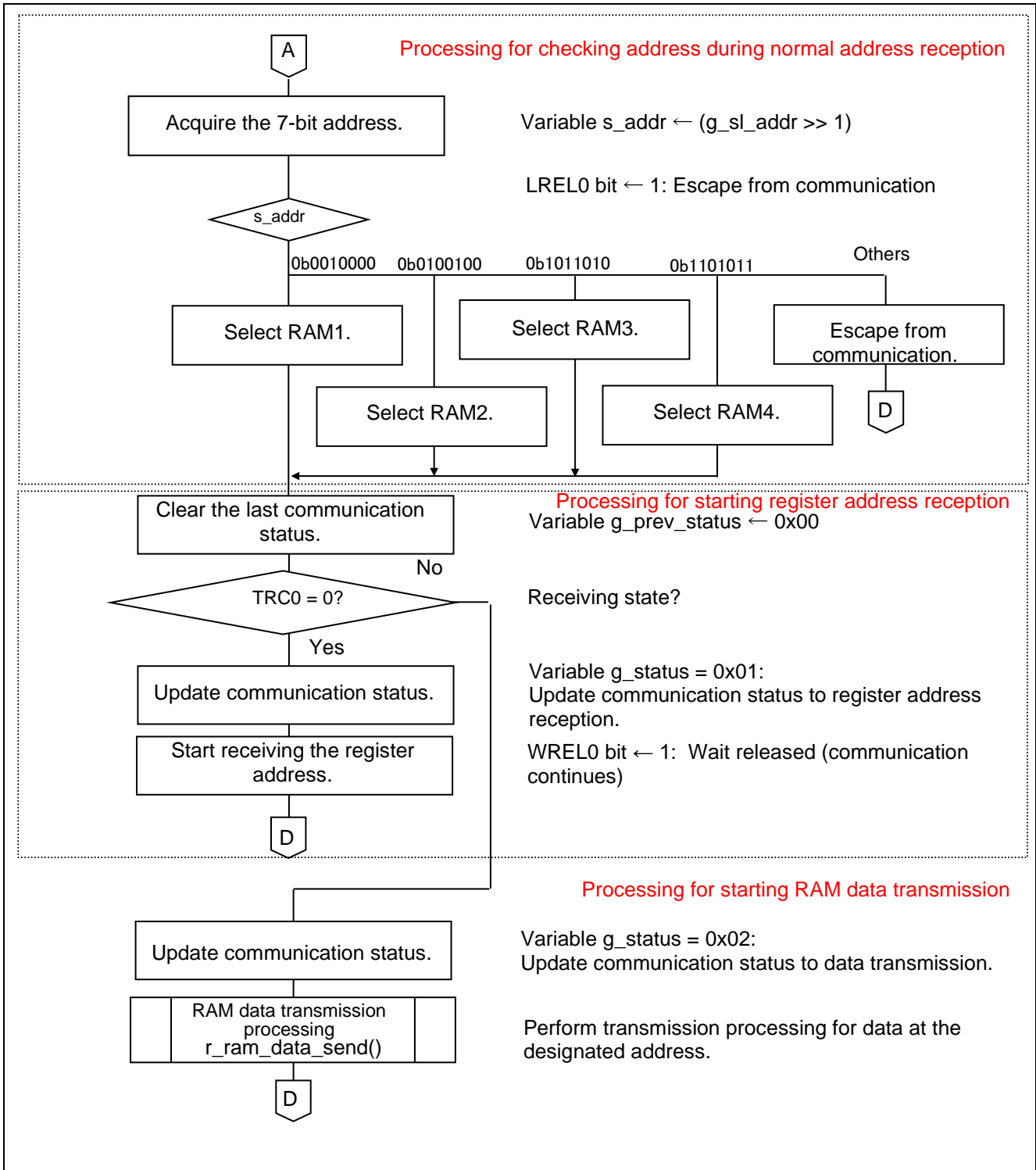**Figure 4-10** IICA0 Slave Interrupt Processing Function (2/4)

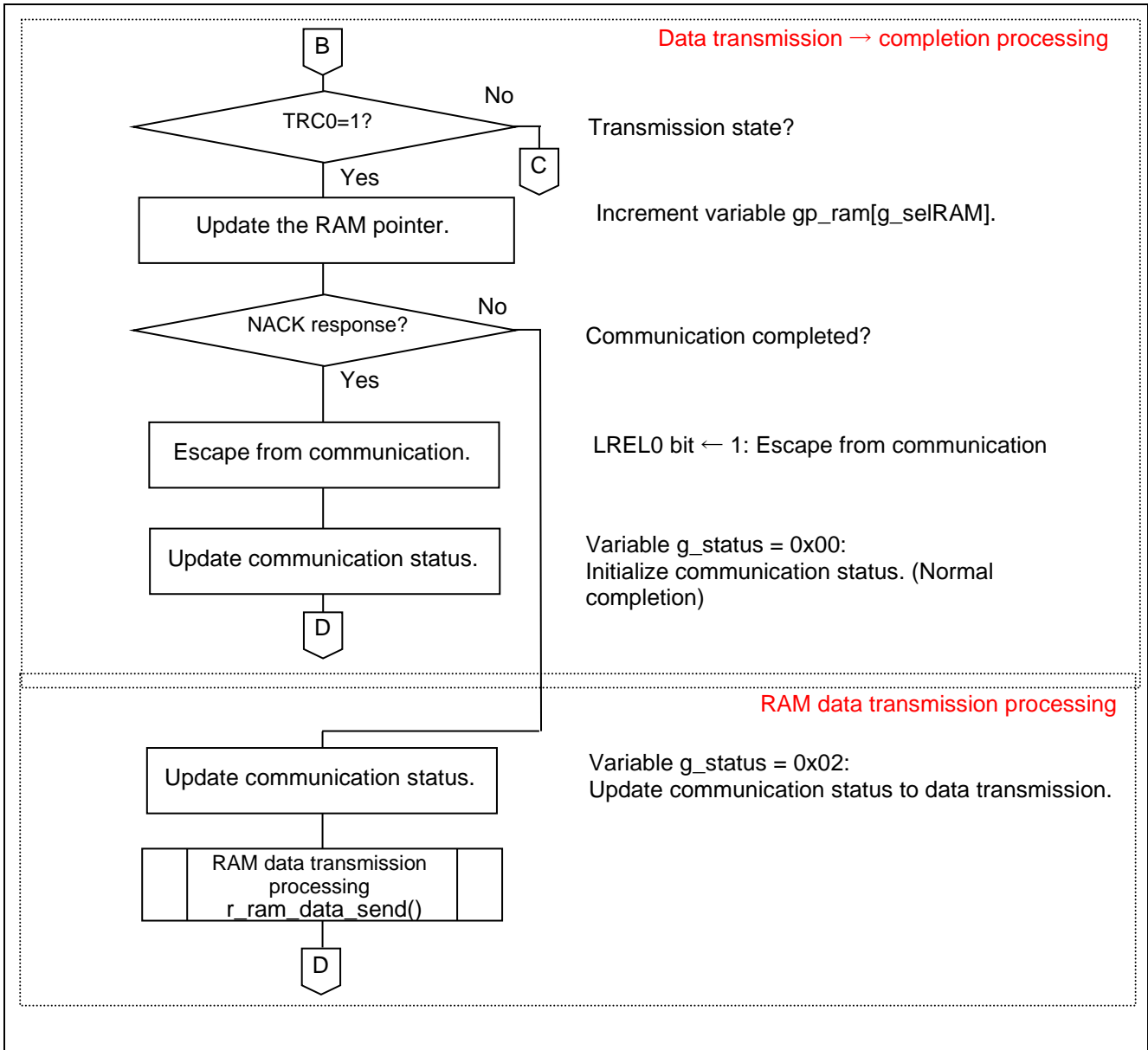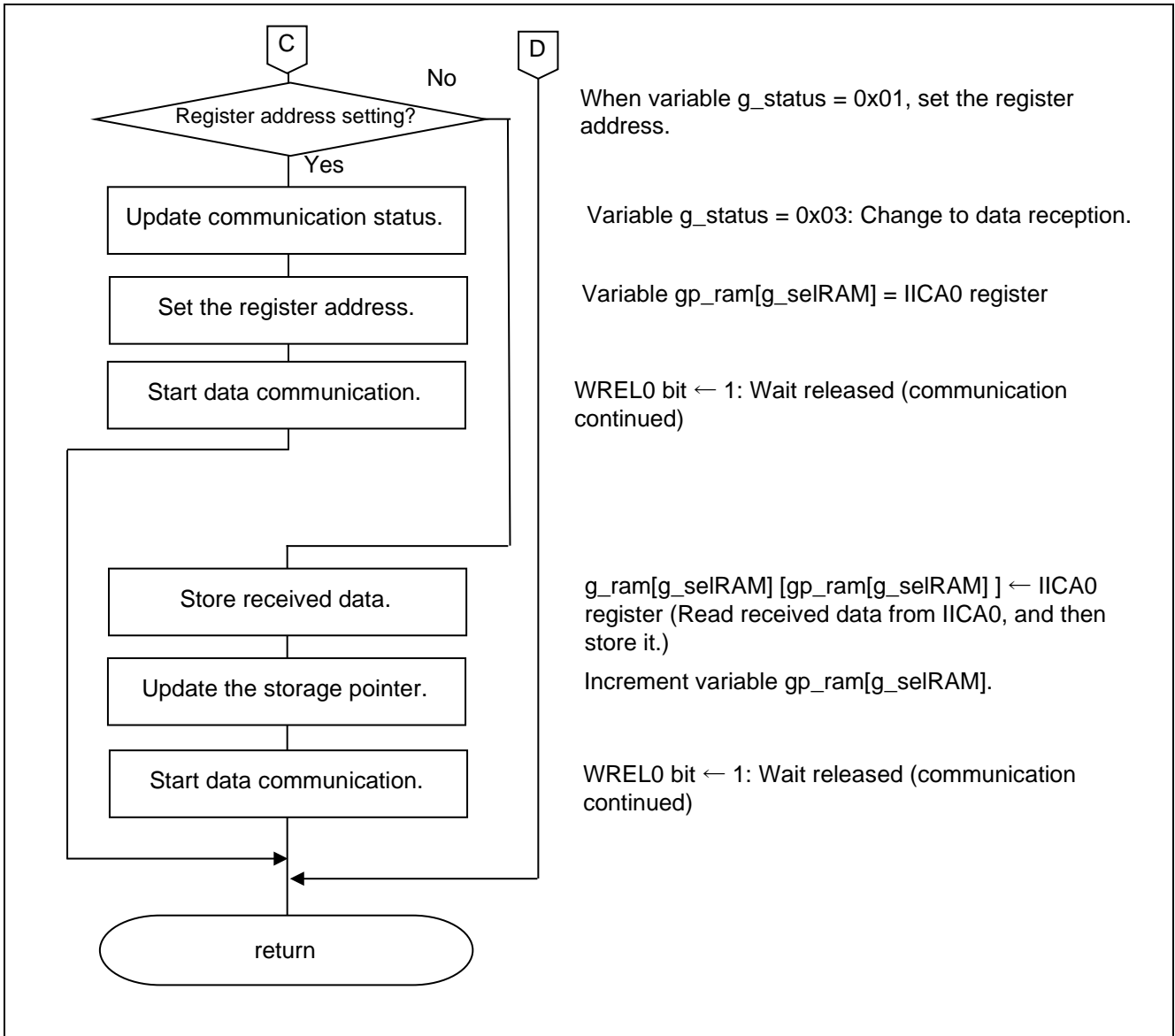**Figure 4-11 IICA0 Slave Interrupt Processing Function (3/4)**

Figure 4-12 IICA0 Slave Interrupt Processing Function (4/4)

4.6.10 RAM Data Transmission Processing Function

Figure 4-13 shows the flowchart of the RAM data transmission processing function.

Figure 4-13 RAM Data Transmission Processing Function
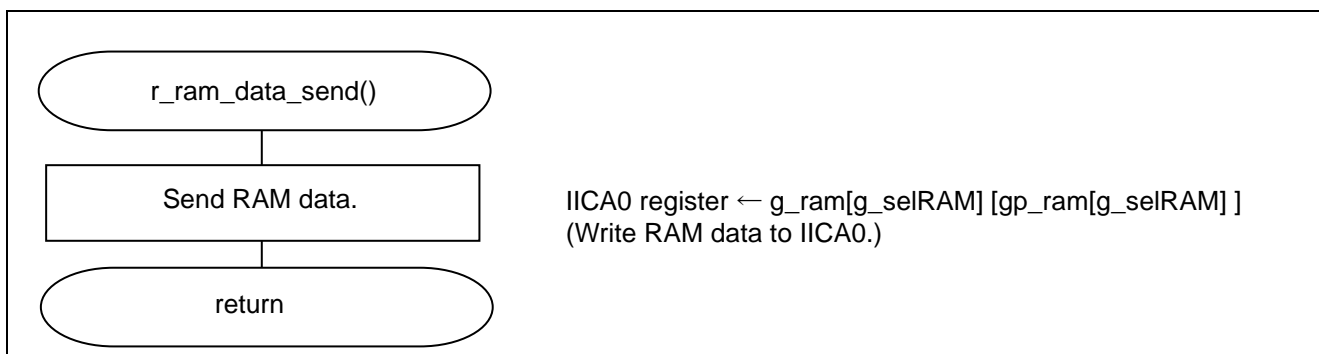
5. Sample code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User's Manual: Hardware (R01UH0896)
RL78 family user's manual software (R01US0015)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Apr.01.21	—	First Edition
1.01	May.18.21	6	Updated the Operation Confirmation Conditions

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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