RL78/G23

ELCL Manchester Decoder Function

Introduction

This application note describes how to use the logic and event link controller (ELCL) to decode Manchester code. By using ELCL, the functions realized by software can be realized by hardware, and resources (ROM, RAM, etc.) can be reduced.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note describes how to decode Manchester code by using ELCL.

There are two standards in the Manchester Code: the G.E.Thomas method, shown in Figure 1-1, and IEEE 802.3 compliance, shown in Figure 1-2. The G.E.Thomas method transmits the logical value "0" by a transition from Low to High, and "1" by a transition from High to Low. According to IEEE 802.3 transmits the logical value "0" the transition from High to Low, and "1" by a transition from Low to High.

This application note describes how to decode the G.E.Thomas method.

Figure 1-1 Manchester code (G.E.Thomas method)

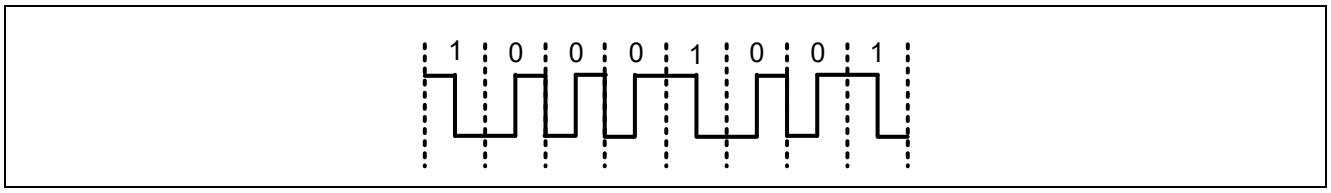


Figure 1-2 Manchester code (IEEE 802.3 compliant)

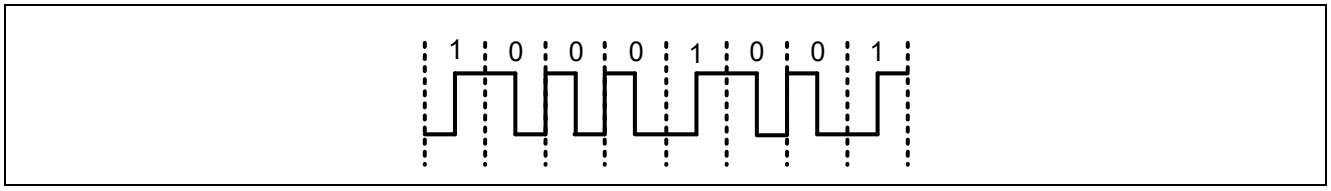


Figure 1-3 shows the Manchester code decoding system configuration using ELCL. The Manchester code received by INTPUT A is decoded to the clock line and data line. The clock line is connected to SCK0n of Serial Array Unit 0 (SAU0) via channels 0 and 1 of Timer Array Unit 0 (TAU0) and the data line is connected to SI0n of SAU0.

Figure 1-3 System Configuration

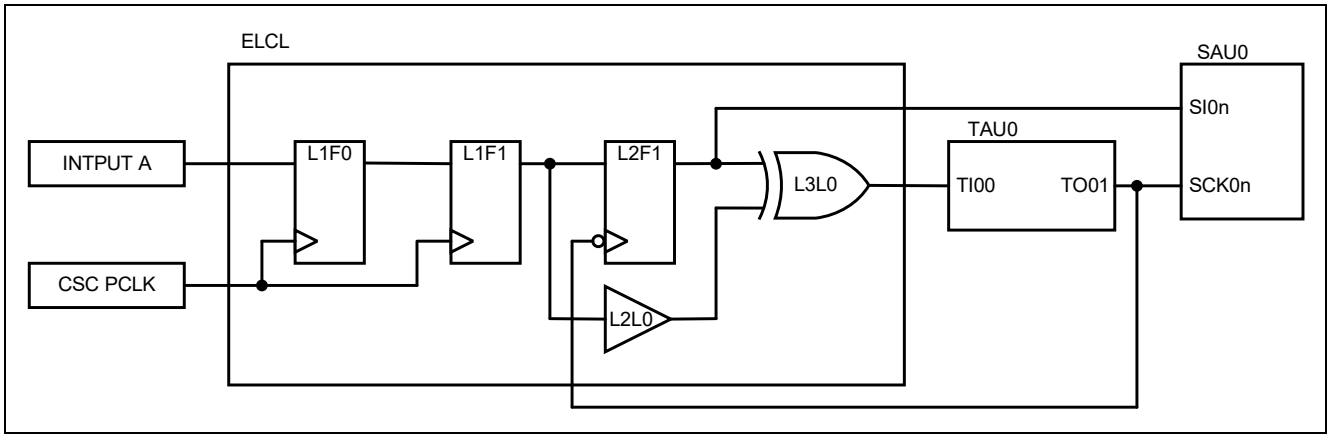


Figure 1-4 shows the timing chart.

The TAU0 channel is used by setting it to the one-shot pulse output function, and the SAU is used by setting it to the continuous transfer mode.

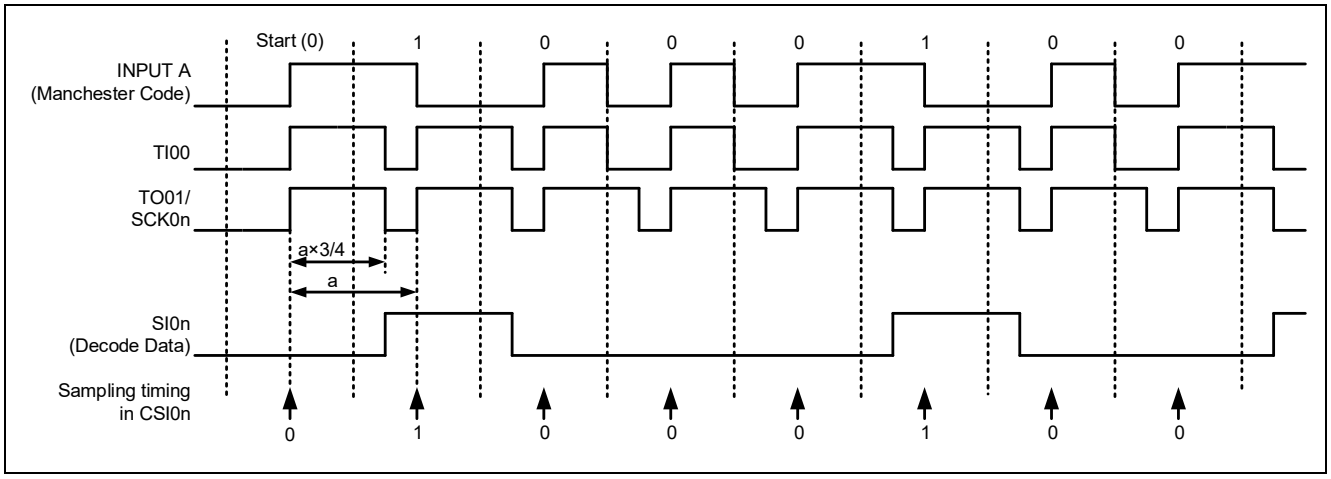
The period a for SCK0n is generated by TAU0. It is necessary to set TDR00 (delay) and TDR01 (one-shot pulse width) so that the change timings of the Manchester code, SCK0n cycle, and TAU0 do not overlap.

When changing the default settings of this sample code and using it, make sure that the following conditions are met.

TDR00: 0 (set “2” when using the Smart Configurator)

TDR01: a x 3/4 (round up after the decimal point)

Figure 1-4 Timing chart

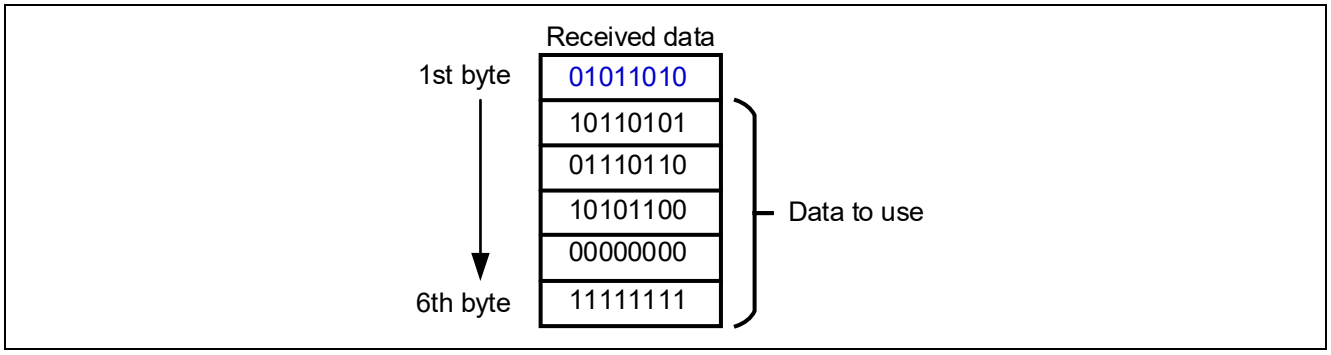


In this application note, the first byte may not be received correctly, so the first byte is treated as invalid data and the second and subsequent bytes are treated as valid data. When decoding the Manchester code using this application note, enter the code to be decoded after any data other than "FFH" and "00H" in the first byte.

Figure 1-5 shows a concrete example. In the example, the data size is 5 bytes, but there is no particular limit.

This is example that the data of 5 bytes is sent in the order "D5H, 76H, ACH, 00H, FFH". Before "D5H" is sent, "5AH" should be sent to recognize the first data. Then a total data of 6 bytes is sent. After receiving 6 bytes of data, 2 to 6 bytes are considered valid data.

Figure 1-5 Example of adding "5AH" to the first byte



2. Conditions for Operation Confirmation

The sample code with this application note runs properly under the condition below.

Table 2-1 Operation Confirmation Conditions

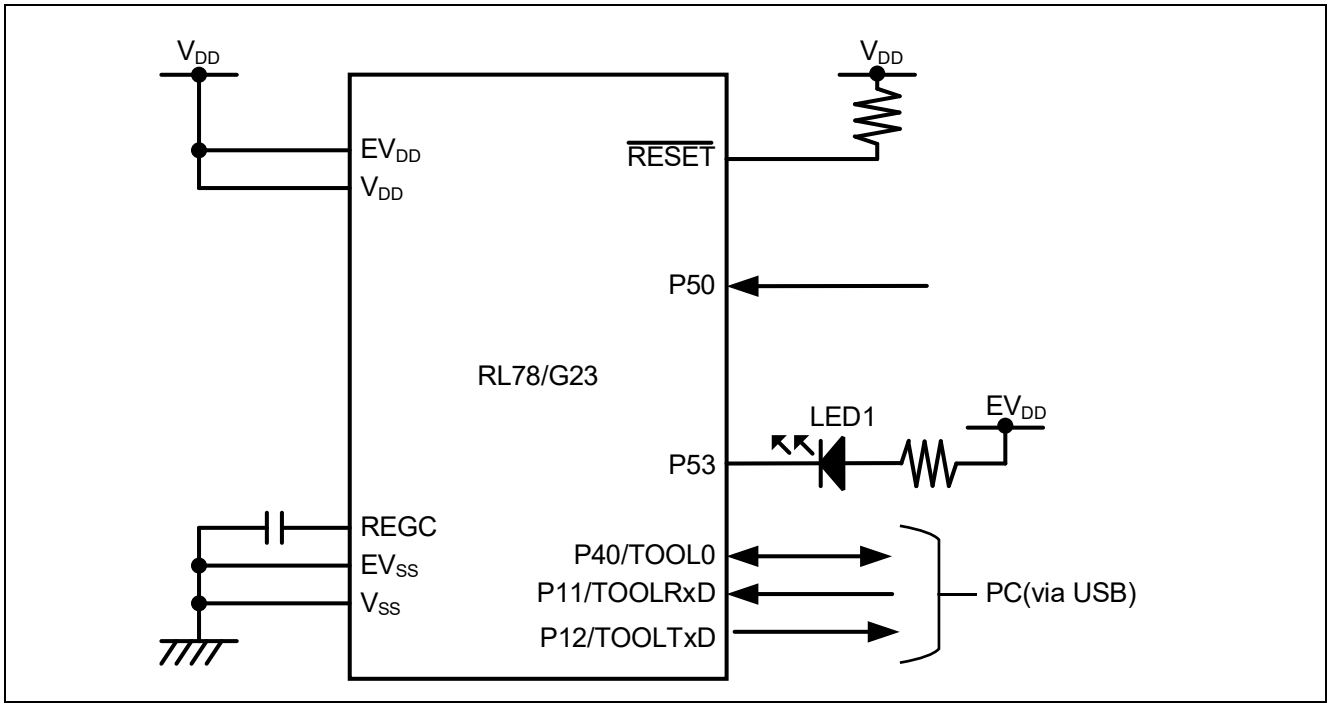
Items	Contents
MCU	RL78/G23 (R7F100GLG)
Operating frequencies	• High-speed on-chip oscillator clock: 16 MHz • CPU/peripheral hardware clock: 16 MHz
Operating voltage	• 3.3V • LVD0 operations (V_{LVD0}) : Reset mode Rising edge TYP.1.90V Falling edge TYP.1.86V
Integrated development environment (CS+)	CS+ for CC V8.07.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.11 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio 2022-01 (22.01.0) from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.11 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 v4.21.1 from IAR Systems
C compiler (IAR)	
Smart Configurator	V.1.2.0
Board support package (r_bsp)	V.1.13
Emulator	CS＋, e^2 studio: COM port IAR: E2 Emulator Lite
Board	RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)

3. Hardware

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration in this application.

Figure 3-1 Hardware Configuration



Caution 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

Caution 2. Connect the EV_{SS} pin to V_{SS} and the EV_{DD} pin to V_{DD}.

Caution 3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD0}) that is specified as LVD.

3.2 Used Pins

Table 3-1 List of Pins and Functions shows list of used pins and assigned functions.

Table 3-1 List of Pins and Functions

Pin name	Input/Output	Function
P53	Output	LED1 lights (Low Active)
P50	Input	Manchester code input

Caution. In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software

4.1 Overview of the sample program

In this sample code, the Manchester code received from P50 is decoded by ELCL, and CSI00 receives the decoded data and clock.

(1) Initial settings of SAU0 and TAU0.
(2) Prepares to receive CSI00 (setting of the storage area) and enables the interrupt.
(3) Waits for the Manchester code to be received.
(4) After receiving 6 bytes of data and transferring it to the storage area, the receive completion interrupt is generated.
(5) Turns on LED1.

Figure 4-1 shows the system configuration of the sample code, and Figure 4-2 shows the timing chart.

Select P50 as the ELCL input signal and TI00 or SI00 as the ELCL output signal.

Figure 4-1 System configuration of the sample code

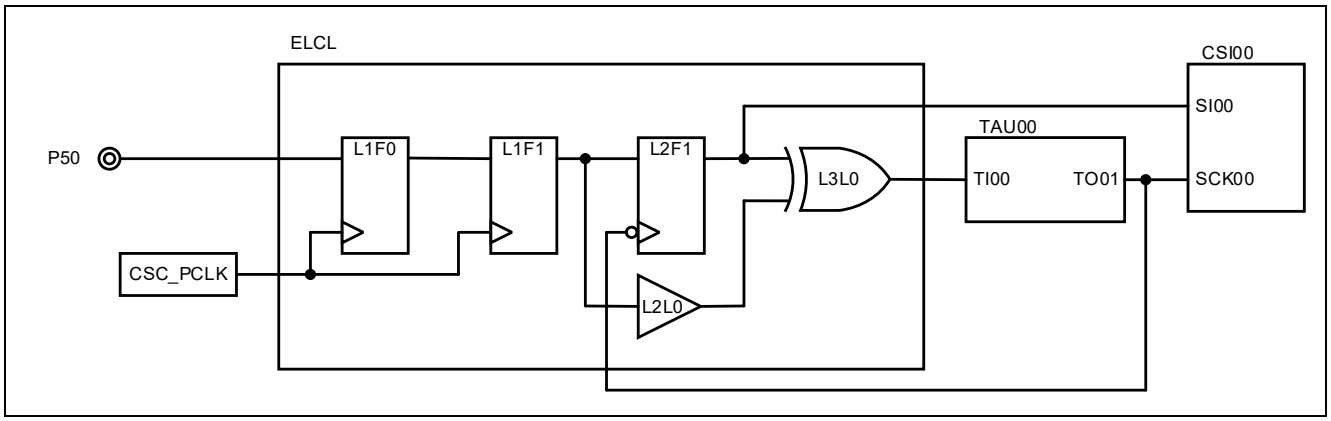
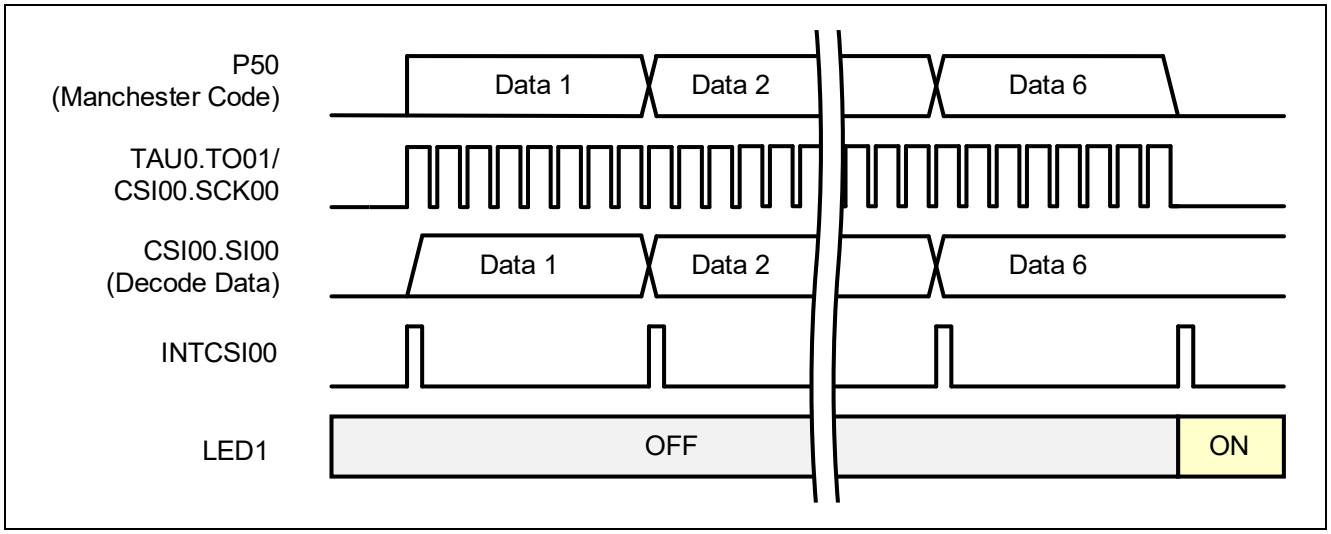


Figure 4-2 Timing chart of the sample code



4.2 Folder Configuration

Table 4-1 shows folder configuration of source file and header files using by sample code except the files generated by integrated development environment and the files in the bsp environment.

Table 4-1 Folder configuration

Folder/File configuration	Outline	Created by Smart configurator
¥r01an5616_elcl_manchester<DIR> Note 3	Root folder of this sample code	
¥src<DIR>	Folder for program source	
main.c	Sample code source file	
¥smc_gen<DIR>	Folder created by Smart Configurator	√
¥Config_ManchesterDecoder<DIR>	Folder for ELCL program	√
Config_ManchesterDecoder.c	Source file for ELCL	√
Config_ManchesterDecoder.h	Source file for ELCL	√
Config_ManchesterDecoder_user.c	Interrupt source file for ELCL	√
¥Config_PORT<DIR>	Folder for PORT program	√
Config_PORT.c	Source file for PORT	√
Config_PORT.h	Header file for PORT	√
Config_PORT_user.c	Interrupt source file for PORT	√Note 1
¥Config_CSI00<DIR>	Folder for CSI00 program	√
Config_CSI00.c	Source file for CSI00	√
Config_CSI00.h	Header file for CSI00	√
Config_CSI00_user.c	Interrupt source file for CSI00	√Note 2
¥Config_TAU0_0<DIR>	Folder for TAU0 program	√
Config_TAU0_0.c	Folder for TAU0 program	√
Config_TAU0_0.h	Folder for TAU0 program	√
Config_TAU0_0_user.c	Folder for TAU0 program	√Note 1
¥general<DIR>	Folder for initialize or common program	√
¥r_bsp<DIR>	Folder for BSP program	√
¥r_config<DIR>	Folder for program	√

Note. <DIR> means directory.

Note 1. Not used in this sample code.

Note 2. Added the interrupt handling routine to the file generated by the Smart Configurator.

Note 3. The IAR version of the sample code contains r01an5616_elcl_manchester.ipcf. For the ipcf file, refer to "RL78 Smart Configurator User Guide: IAR (R20AN0581)".

4.3 Option Byte Settings

Table 4-2 shows the option byte settings.

Table 4-2 Option Byte Settings

Address	Setting Value	Contents
000C0H/040C0H	1110 1111B (EFH)	Operation of Watchdog timer is stopped (counting is stopped after reset)
000C1H/040C1H	1111 1110B (FEH)	LVD0 operating mode: reset mode Detection voltage: Rising edge 1.90V Falling edge 1.86V
000C2H/040C2H	1110 1001B (E9H)	Flash operating mode: HS mode High-speed on-chip oscillator clock: 16MHz
000C3H/040C3H	1000 0101B (85H)	On-chip debugging is enabled

4.4 Constants

Table 4-3 shows the constants that are used in this sample code.

Table 4-3 Constants used in the sample code

Constant Name	Setting Value	Contents	File
LED1	P5_bit.no3	P53	Config_CSI00_user.c
LED_ON	0	Setting value for turning on the LED	Config_CSI00_user.c
BUFFER_SIZE	6	Receive buffer size	main.c

4.5 Variables

Global variables are not used in this sample code.

4.6 Functions

Table 4-4 shows the functions used in the sample code. However, the unchanged functions generated by the Smart Configurator are excluded.

Table 4-4 Functions

Function name	Outline	Source file
main	Main process	main.c
r_Config_CSI00_callback_receiveend	CSI00 reception complete callback process	Config_CSI00_user.c

4.7 Function Specifications

This part describes function specifications of the sample code.

[Function name] main

Outline	Main process
Header	r_smc_entry.h
Declaration	void main (void);
Description	This function initializes the ELCL, sets the receive area, and sets the interrupt. It shifts to the reception standby state and starts the operation of TAU0.
Arguments	None
Return value	None
Remarks	None

[Function name] r_Config_CSI00_callback_receiveend

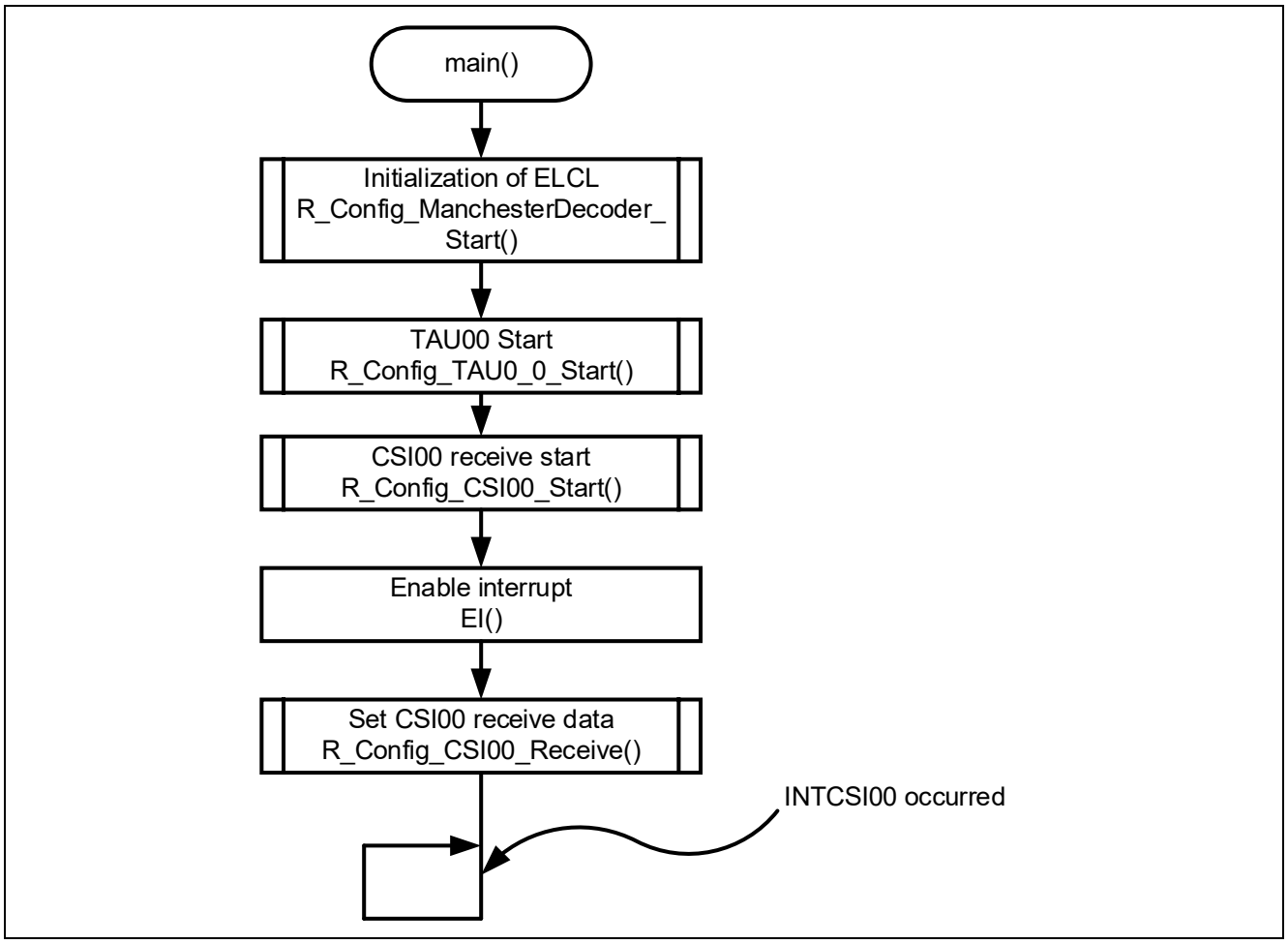
Outline	CSI00 reception complete callback process
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_CSI00.h
Declaration	static void r_Config_CSI00_callback_receiveend (void);
Description	This function lights LED1 after reception is complete.
Arguments	None
Return value	None
Remarks	None

4.8 Flow Charts

4.8.1 Main Process

Figure 4-3 shows flowchart of main process.

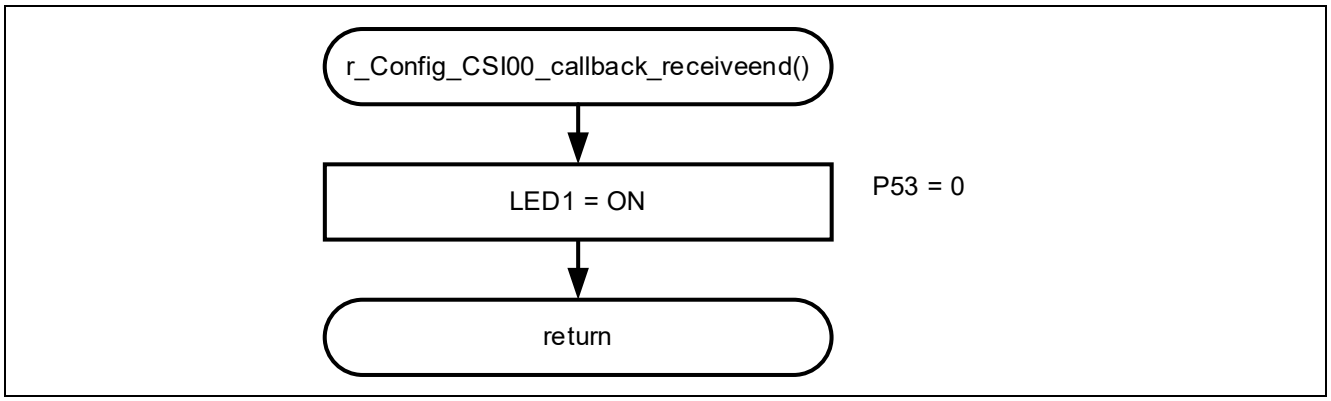
Figure 4-3 Main process



4.8.2 CSI00 reception complete callback process

Figure 4-4 shows flowchart of CSI00 reception complete callback process.

Figure 4-4 CSI00 reception complete callback process



5. Application example

In addition to the sample code, this application note contains the following Smart Configurator configuration files

r01an5616_elcl_manchester.scfg

The following is a description of the file and examples of settings and notes for use.

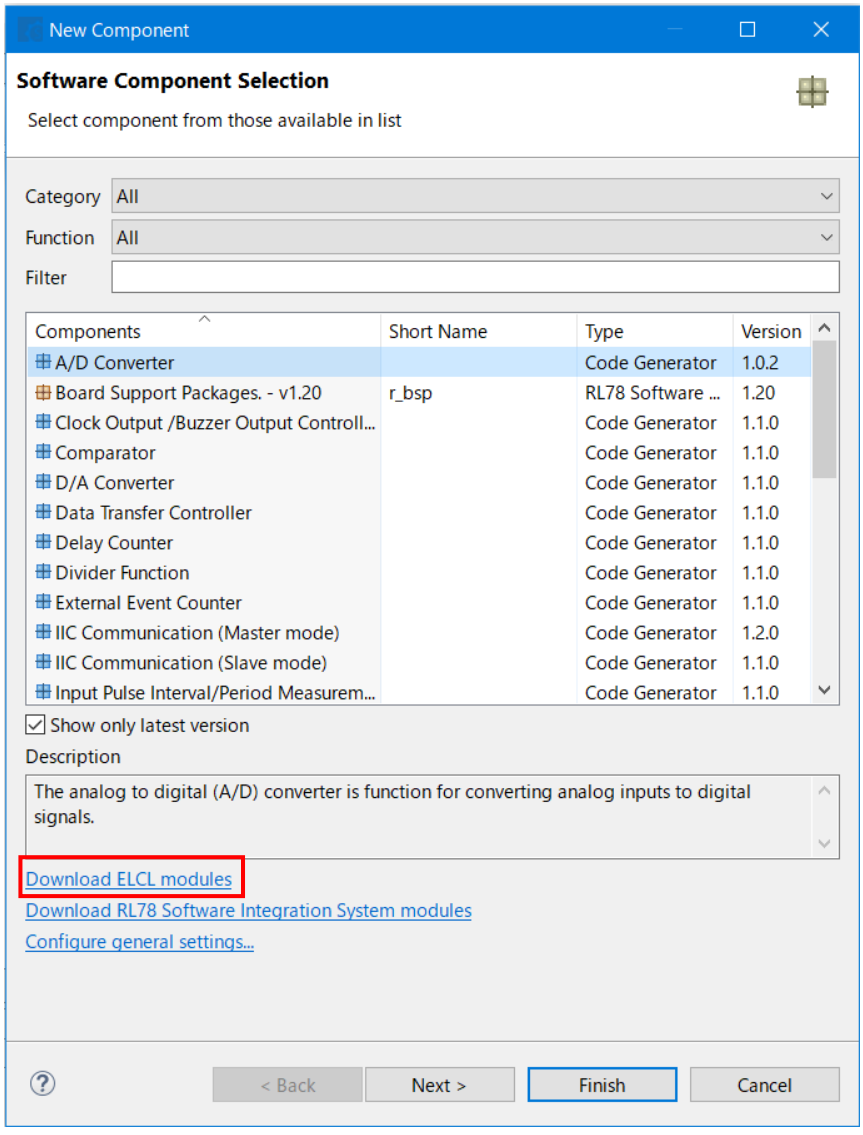
5.1 Setting up the ELCL components

To use the ELCL component, you need to install the ELCL content file.

The procedure is shown below.

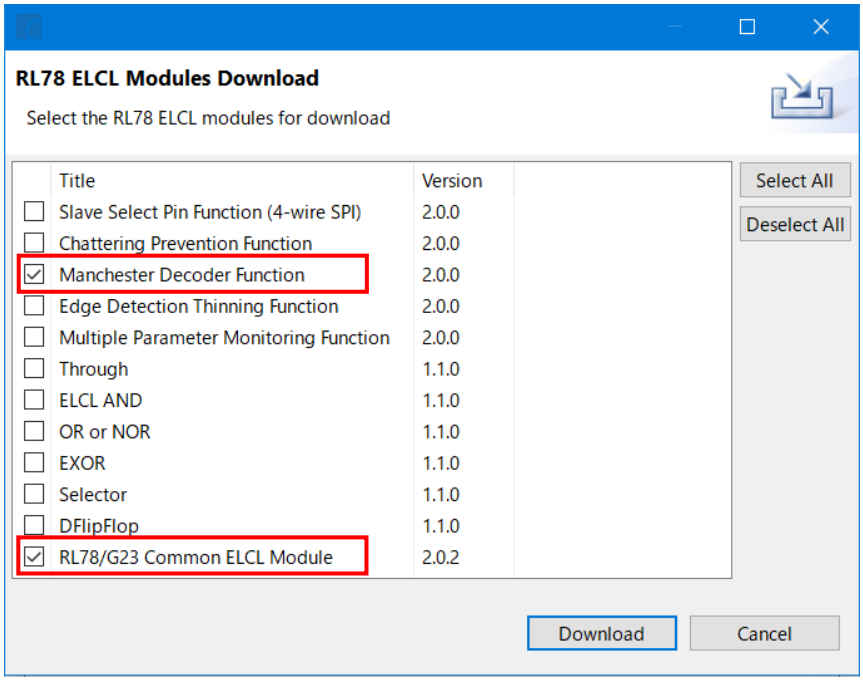
1. Start the Smart Configurator.
2. Click on the "Components" tag, and then click "Add component".
3. When the "New Component" window shown in Figure 5-1 opens, click on "Download ELCL modules".

Figure 5-1 Add component



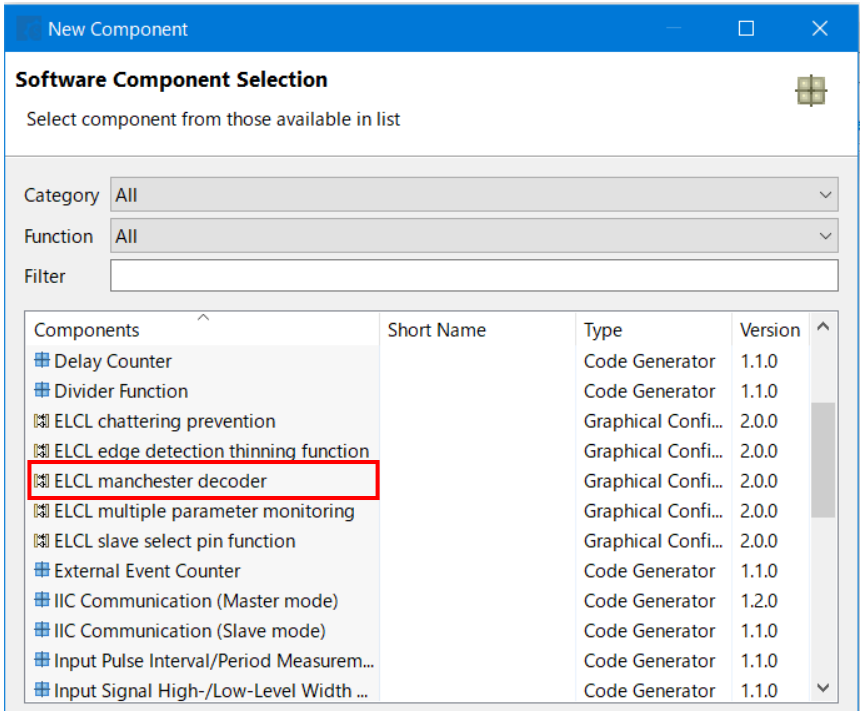
4. Select "Manchester Decoder Function" and download it. Please download the common setting file "RL78/G23 Common ELCL Module" as well.

Figure 5-2 Download the module



5. After the download is complete, make sure that "ELCL manchester decoder" is available for selection.

Figure 5-3 Select the module



5.2 r01an5616_elcl_manchester.scfg

This is the Smart Configurator configuration file used in the sample code. It contains all the features configured in the Smart Configurator. The sample code settings are as follows.

Table 5-1 Parameters of Smart Configurator (1/2)

Tag name	Component	Contents
Clocks	-	Operation mod: High-speed main mode 2.4 (V)~5.5 (V) EV_{DD} setting: $1.8V \leqq EV_{DD0} < 5.5V$ High-speed on-chip oscillator: 16MHz f_{IHP}: 16MHz f_{CLK} Note 3 : 16MHz (High-speed on-chip oscillator) f_{SXP}: 32.768kHz (Low-speed on-chip oscillator)
System	-	On-chip debug operation setting: COM port Note 1 Pseudo-RRM/DMM function setting: Used Start/Stop function setting: Unused Trace function setting: Used Security ID setting: Use security ID Security ID : 0x00000000000000000000 Security ID authentication failure setting: Do not erase flash memory data
Components	r_bsp	Start up select : Enable (use BSP startup) Control of invalid memory access detection : Disable RAM guard space (GRAM0-1) : Disabled Guard of control registers of port function (GPORT) : Disabled Guard of registers of interrupt function (GINT) : Disabled Guard of control registers of clock control function, voltage detector, and RAM parity error detection function (GCSC) : Disabled Data flash access control (DFLEN) : Disables Initialization of peripheral functions by Code Generator/Smart Configurator : Enable API functions disable : Enable Parameter check enable : Enable Setting for starting the high-speed on-chip oscillator at the times of release from STOP mode and of transitions to SNOOZE mode : High-speed Enable user warm start callback (PRE) : Unused Enable user warm start callback (POST) : Unused Watchdog Timer refresh enable : Unused
	Config_LVD0	Operation mode setting: Reset mode Voltage detection setting: Reset generation level (V_{LVD0}): 1.86 (V)

Table 5-2 Parameters of Smart Configurator (2/2)

Tag name	Component	Contents
Components	Config_TAU0_0	Components: One-shot Pulse Output Resource: TAU0_0 Operation clock: CK00 Clock source: f_{CLK} One-shot trigger setting: External trigger Input source: ELCL TI00input edge selection: Rising edge Delay time: 2 count Interrupt setting: unused One-shot slave select setting: Channel 1 slave One-shot slave setting: 10 count Note 2 Initial output value: 0 Output level: Active-high Interrupt setting (INTTM01) : unused
	Config_Manchester Decoder	Components: ELCL manchester decoder Input signal selector: P50 Output signal selector: SAU0 Channel0 Data Input
	Config_PORT	Components: Port Port selection: PORT5 P53: Out (Output 1)
	Config_CSI00	Components: SPI (CSI) Communication Operation mode: Reception Resource: CSI00 Transfer clock mode: External clock (slave) Transfer direction setting: Continuous transfer mode Data length setting: 8 bits Transfer direction setting: MSB Specification of data timing: Type 4 Interrupt setting: Level 3 Callback function setting: Reception end, Overrun error

Note 1. When using IAR, use the following settings.
On-chip debug operation setting: Use emulator
Emulator setting: E2 Emulator Lite

Note 2. This is the setting when the baud rate is 1000 kbps.
An example of recommended settings for each baud rate is shown below.

Baud rate (kbps)	Delay (count)	One-shot pulse width (count)
500	2	22
800	2	13
1000	2	10

Note 3. f_{CLK} must be 16MHz or less.

5.2.1 Clocks

Set the clock used in the sample code.

5.2.2 System

Set the on-chip debug of the sample code.

"Control of on-chip debug operation" and "Security ID authentication failure setting" affect "On-chip debugging is enabled" in "Table 4-2 Option Byte Settings". Note that changing the settings.

5.2.3 r_bsp

Set the startup of the sample code.

5.2.4 Config_LVD0

Set the power management of the sample code.

Affects "Setting of LVD0" in "Table 4-2 Option Byte Settings". Note that changing the settings.

5.2.5 Config_TAU0_0

Set the TAU0_0 of the sample code.

In the sample code, it is used to generate the SCK0 of CSI00. The optimal SCK0 is generated by setting values of "Delay" and "One-shot Pulse Width" in the Smart Configurator. When using a value other than the recommended setting example, please check the operation.

5.2.6 Config_ManchesterDecoder

Initialize and output the ELCL of the sample code.

The sample code uses P50 as the pin to receive the Manchester code and CSI00 as the output destination.

For details, refer to "5.4 Component "ELCL manchester decoder"".

5.2.7 Config_PORT

Set the port of the sample code.

In the sample code, P53 is used to control LED1.

5.2.8 Config_CSI00

Set the CSI00 of the sample code. Use "Type 4" for data transmission/reception timing setting.

5.2.9 Point for Caution when generating Smart Configurator code

In this application note, the TO01, SCK00 and SI00 pins are not used as external pins, but are connected to the ELCL internally. In the default configuration of the Smart Configurator, these pins are set as external pins. Make the following settings to prevent from unintended behavior.

5.2.9.1 TO01 settings

When TAU00 and TAU01 are set according to Table 5-1, since "Enabled" is selected for TO01 as an external terminal, make the following settings.

(1) Starts the Smart Configurator and selects the [Pins] page.
(2) Selects [Pins Function].
(3) Selects [TAU01] from the [Hardware Resource] list.
(4) Unchecks the [Enabled] checkbox on TO01.

5.2.9.2 SCK00 and SI00 settings

When SAU00 are set according to Table 5-1, since "Enabled" is selected for SCK00 and SI00 as an external terminal, make the following settings.

(1) Starts the Smart Configurator and selects the [Pins] page.
(2) Selects [Pins Function].
(3) Selects [SAU00] from the [Hardware Resource] list.
(4) Unchecks the [Enabled] checkbox on SCK00 and SI00.

5.3 Component "ELCL manchester decoder"

Figure 5-4 shows the component “ELCL manchester decoder” and Table 5-3 shows the options for this component.

Figure 5-4 Component "ELCL manchester decoder"

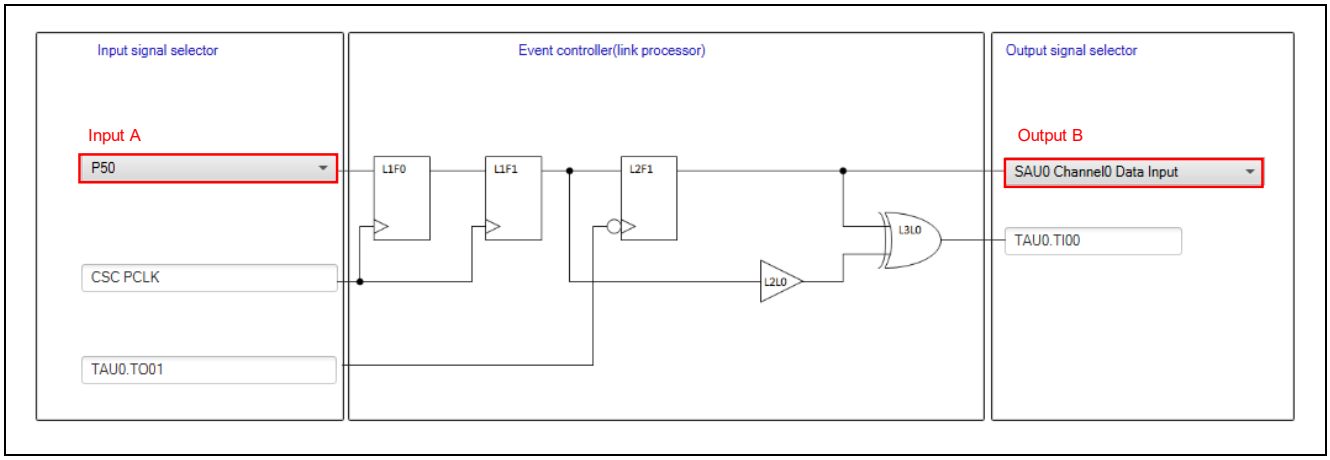


Table 5-3 Choices of component "ELCL manchester decoder"

Item	Choices	Description
Input A	P10	Select the Manchester code input terminal
	P11	
	P12	
	P20	
	P50	
	P51	
	P120	
	P137	
Output B	SAU0 Channel0 Data Input	Select the output destination
	SAU0 Channel1 Data Input	

5.3.1 Setting the ELCL Register

Table 5-4 to Table 5-8 show the initial settings of the ELCL register, and Figure 5-5 to Figure 5-9 show the ELCL configuration at that time. Refer to Figure 4-1 for the overall ELCL configuration.

Table 5-4 ELCL register settings (Inputs)

Register Symbol	Register Name	Setting	Description
ELISEL0	Input signal select register 0	05H	Input pin P50 is selected
ELISEL1	Input signal select register 1	1CH	Output from flip-flop 0 of logic cell block L1 in the ELCL is selected
ELISEL9	Input signal select register 9	08H	Output from TAU0 channel 1 is selected
ELISEL10	Input signal select register 10	1BH	CSC PCLK is selected

Figure 5-5 Setting of ELCL input

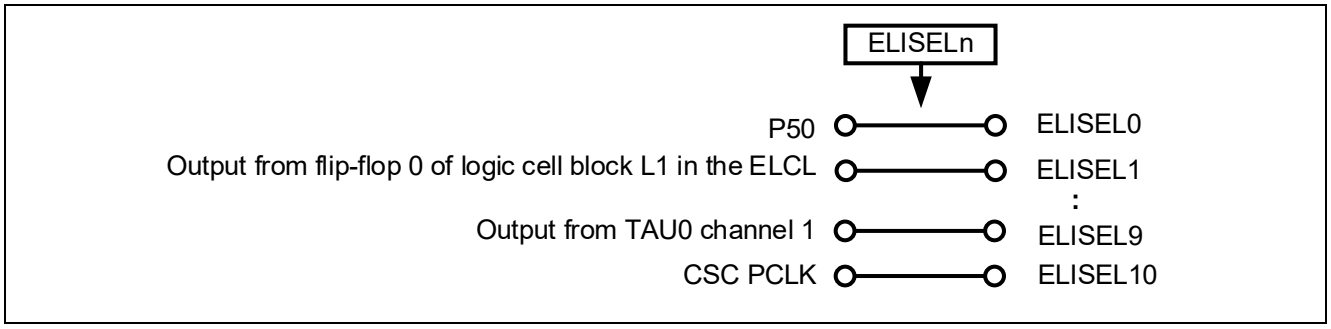


Table 5-5 ELCL register settings (Logic cell block L1)

Register Symbol	Register Name	Setting	Description
ELL1SEL0	Event link L1 signal select register 0	01H	Select the signal selected by ELISEL0 as the link target of L1
ELL1SEL1	Event link L1 signal select register 1	02H	Select the signal selected by ELISEL1 as the link target of L1
ELL1SEL6	Event link L1 signal select register 6	05H	Select the signal selected by ELISEL10 as the link target of L1
ELL1LNK0	Event link L1 output select register 0	08H	Link target selected by ELL1SEL0 to input of flip-flop 0 in logic cell block L1
ELL1LNK1	Event link L1 output select register 1	09H	Link target selected by ELL1SEL1 to input of flip-flop 1 in logic cell block L1
ELL1LNK6	Event link L1 output select register 6	03H	Link target selected by ELL1SEL6 to clock of flip-flop 0 and 1 in logic cell block L1
ELL1CTL	Logic cell block L1 control register	C0H	Enable use of logic cell block L1 flip-flops 0 and 1

Figure 5-6 Setting of logic cells L1

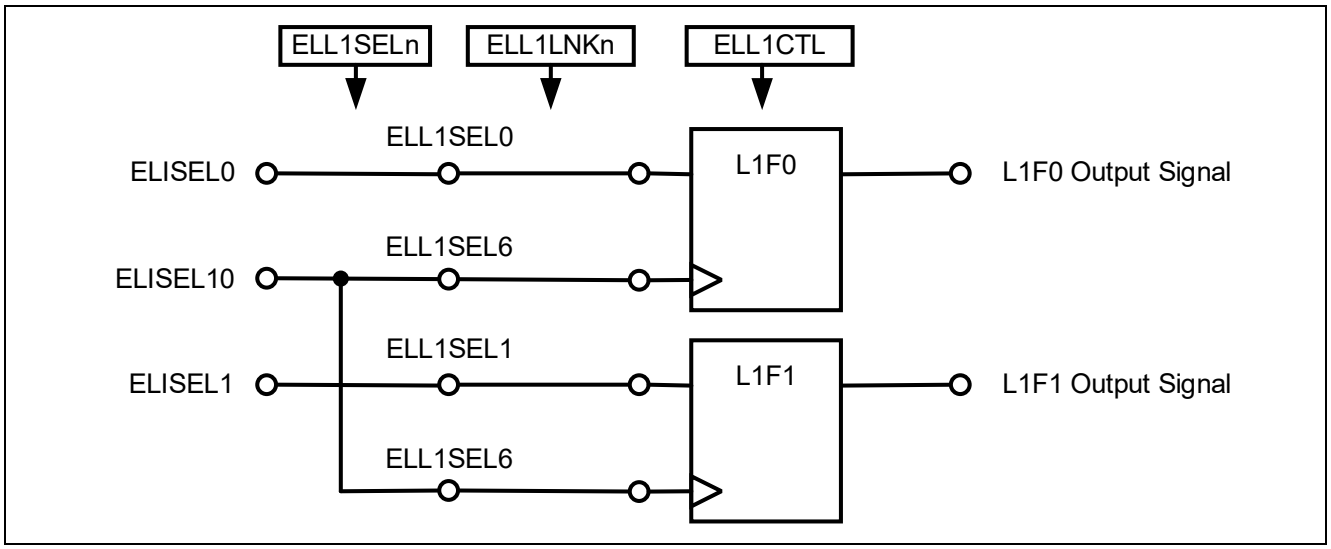


Table 5-6 ELCL register settings (Logic cell block L2)

Register Symbol	Register Name	Setting	Description
ELL2SEL0	Event link L2 signal select register 0	11H	Output signal 4 in logic cell block L1 is selected as the link target of L2
ELL2SEL1	Event link L2 signal select register 1	11H	Output signal 4 in logic cell block L1 is selected as the link target of L2
ELL2SEL6	Event link L2 signal select register 6	84H	Select the signal selected by ELISEL9 as the link target of L2 (Negative logic)
ELL2LNK0	Event link L2 output select register 0	01H	Link target selected by ELL2SEL0 to input 0 of logic cell 0 in logic cell block L2
ELL2LNK1	Event link L2 output select register 1	09H	Link target selected by ELL2SEL1 to input of flip-flop 1 in logic cell block L1
ELL2LNK6	Event link L2 output select register 6	02H	Link target selected by ELL2SEL6 to clock of flip-flop 1 in logic cell block L2
ELL2CTL	Logic cell block L2 control register	80H	Enable use of logic cell block L2 flip-flops 1, logic cell 0 selects Pass-through circuit

Figure 5-7 Setting of logic cells L2

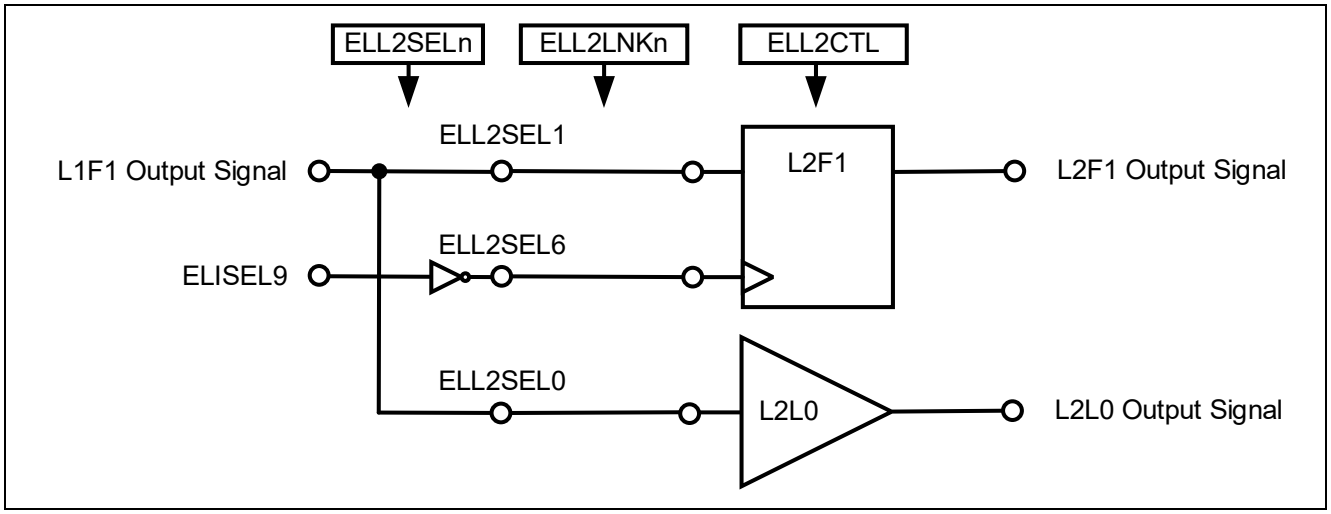


Table 5-7 ELCL register settings (Logic cell block L3)

Register Symbol	Register Name	Setting	Description
ELL3SEL0	Event link L3 signal select register 0	11H	Output signal 4 in logic cell block L2 is selected as the link target of L3
ELL3SEL1	Event link L3 signal select register 1	0DH	Output signal 0 in logic cell block L2 is selected as the link target of L3
ELL3LNK0	Event link L3 output select register 0	01H	Link target selected by ELL3SEL0 to input 0 of logic cell 0 in logic cell block L3
ELL3LNK1	Event link L3 output select register 1	02H	Link target selected by ELL3SEL1 to input 1 of logic cell 0 in logic cell block L3
ELL3CTL	Logic cell block L3 control register	03H	Logic cell 0 selects EX-OR circuit

Figure 5-8 Setting of logic cells L3

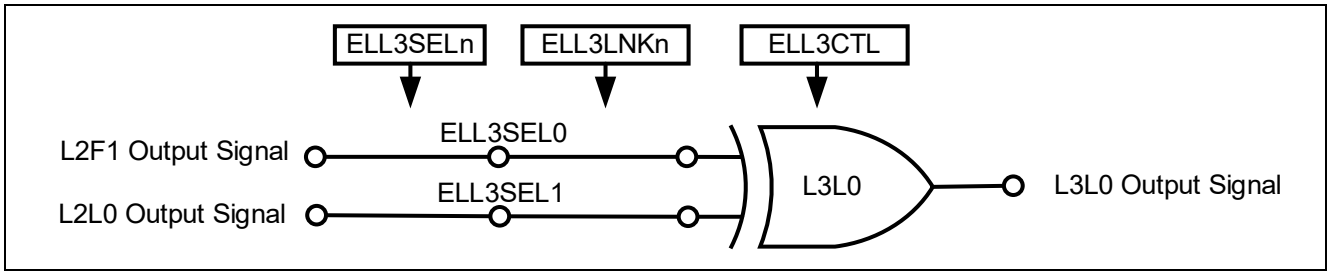
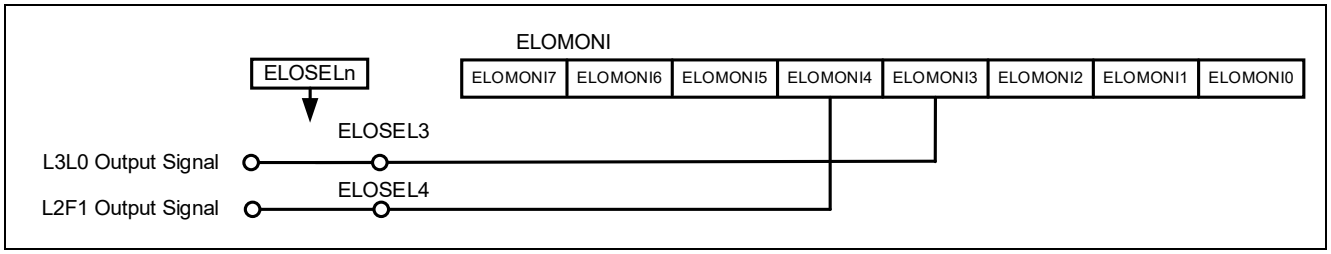


Table 5-8 ELCL register settings (Outputs)

Register Symbol	Register Name	Setting	Description
ELOSEL3	Output signal select register 3	0BH	Select the output signal [0] from logic cell block L3.
ELOSEL4	Output signal select register 4	0AH	Select the output signal [4] from logic cell block L2.

Figure 5-9 Settings of ELCL output



6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference

RL78/G23 User's Manual: Hardware (R01UH0896E)

RL78 Family User's Manual: Software (R01US0015E)

RL78 Smart Configurator User's Guide : CS+ (R20AN0580E)

RL78 Smart Configurator User's Guide : e^2 studio (R20AN0579E)

RL78 Smart Configurator User's Guide : IAREW (R20AN0581E)

(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update / Technical News

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Revision History

Rev	Date	Description	
		Page	Summary
1.00	Apr.13.21	-	First edition
2.00	Mar.24.22	5	Table 2-1 Operation Confirmation Conditions Operating voltage Rising edge TYP.1.875V -> 1.90V Falling edge TYP.1.835V -> 1.86V
		5	Updated tool version Table 2-1 Operation Confirmation Conditions Integrated development environment (CS+) : E8.05.00f -> V8.07.00 C compiler (CS+) : V1.09.00 -> V1.11 Integrated development environment (e^2 studio) : 2021-01 (21.01.0) -> 2022-01 (22.1.0) C compiler (e^2 studio) : V1.09.00 -> V1.11 Integrated development environment (IAR) : V4.20.1 -> V4.21.1 Smart Configurator : V.1.0.0 -> V.1.2.0 Board support package (r_bsp) : V.1.0.0 -> V.1.13
		5,6, 17-18	Changed due to COM port support Table 2-1 Operation Confirmation Conditions Emulator: E2 Emulator Lite -> CS＋, e^2 studio: COM port IAR: E2 Emulator Lite Figure 3-1 Hardware Configuration Added P11/TOOLRxD and P12/TOOLTxD Table 5-1 Parameters of Smart Configurator (1/2) Note 1 added
		6,10, 17-18	Changes according to the operating conditions of the user manual Table 2-1 Operation Confirmation Conditions Operating frequencies High-speed on-chip oscillator clock:32MHz -> 16 MHz CPU/peripheral hardware clock: 32MHz -> 16 MHz Table 4-2 Option Byte Settings Setting Value 1110 1000B(E8H) -> 1110 1001B(E9H) Contents High-speed on-chip oscillator clock:32MHz -> 16MHz Table 5-1 Parameters of Smart Configurator (1/2) Clocks Component High-speed on-chip oscillator: 32MHz -> 16 MHz fIHP: 32MHz -> 16 MHz fCLK: 32000kHz -> 16MHz (High-speed on-chip oscillator) Table 5-2 Parameters of Smart Configurator (2/2) Updated an example of recommended settings for each baud rate Added Note3
		9	Updated the folder structure in Table 4-1 due to the sample program update. Added Note 3 due to the update of the IAR version sample code.

Rev	Date	Description	
		Page	Summary
2.00	Mar.24.22	10	Table 4-2 Option byte setting Detection voltage Rise 1.875V / Fall 1.835V -> Rise 1.90V / Fall 1.86V
		12	Changes due to IAR version sample code update 4.7 Function specifications [function name] main, Header e^2 studio, CS+ : r_smc_entry.h IAR : ior7f100g.h, ior7f100g_ext.h, r_cg_macrodriver.h, Config_SMS.h, Config_ITL000_ITL001.h -> r_smc_entry.h
		13, 15-16, 21	Updated some figures as follows due to the component "ELCL manchester decoder" update. Figure 4-3 Main process Function name: R_Config_ManchesterDecoder_Create () -> R_Config_ManchesterDecoder_Start () Figure 5-1 Add component Figure 5-2 Download the module Figure 5-3 Select the module Figure 5-4 Component "ELCL manchester decoder" Figure update
		16,18-19, 21	Updated the component name to the latest. ELCL Manchester Decoder Function -> ELCL manchester decoder
		17	Table 5-1 Parameters of Smart Configurator Clock: f_{SXL} -> f_{SXP} Component Config_LVD0 Reset generation voltage (V_{LVD0}): 1.835 (V) -> 1.86 (V)
		18	Table 5-2 Parameters of Smart Configurator Component Config_ManchesterDecoder Output signal selector: SAU0 -> SAU0 Chamel0 Data Input
		18	Table 5-2 Parameters of Smart Configurator Component: CSI interface -> SPI (CSI) Communication
		21	Updated the contents in Table 5-3 with the component "ELCL manchester decoder" update. Added choices for Input A and Output B
		27	Added of RL78 Smart Configurator User's Guide 7. Reference RL78 Smart Configurator User's Guide: CS+ (R20AN0580E) RL78 Smart Configurator User's Guide: e² studio (R20AN0579E) RL78 Smart Configurator User's Guide: IAREW (R20AN0581E)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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