RL78/G23

Beginner's Guide to Essential Configuration Functions

Introduction

The RL78/G23 microcontroller has functions that must be configured when using it. This document explains how to configure these functions using the Smart Configurator, which can automatically generate the initial settings for the microcontroller.

For information on connecting external circuits to operate the RL78/G23 microcontroller, please refer to the RL78/G23 Hardware Design Guide (R01AN7300EJ).

List of functions that must be configured

- Flash operation mode at startup.
- High-speed on-chip oscillator frequency at startup.
- Oscillation settings for each clock source.
- On-chip debug operation enable/disable.
- On-chip debug security ID settings.
- Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication.
- Allocation of debug monitor area and debug stack area.
- Voltage detector 0.
- Watchdog timer.
- RAM initialization.
- Stack pointer initialization.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Functions That Must Be Configured

Table 1-1 shows the functions that must be configured and the methods for setting them with the Smart Configurator (SC).

Table 1-1 Functions That Must Be Configured and Their Descriptions

Function and Configuration	Description	Setting Method in SC
Flash operation mode at startup	The flash operation mode should be set based on the power supply voltage and the frequency of the high-speed on-chip oscillator to ensure efficient operation of the microcontroller. Incorrect settings may lead to improper operation of the microcontroller.	Refer to 'Clock Settings' on page 6.
High-speed on-chip oscillator frequency at startup	When the microcontroller is powered on, the CPU operates using the high-speed on-chip oscillator. The frequency can be selected from 1, 2, 3, 4, 6, 8, 12, 16, 24, or 32 MHz, and it must be set according to the flash operation mode and the power supply voltage.	Refer to 'Clock Settings' on page 6.
Oscillation settings for each clock source	The microcontroller can use either the built-in on-chip oscillator or an external crystal oscillator. At startup, the CPU clock is provided by the high-speed on-chip oscillator, and other clocks do not oscillate in the initial state. To use these for the CPU clock, oscillator settings must be configured in the software.	Refer to 'Clock Settings' on page 6.
On-chip debug operation enable/disable	Configure the permission for on-chip debugging operations when using the E2 or E2 Lite on-chip debugging emulator. When enabling debugging operations, it is necessary to configure it along with a security ID to prevent third parties from reading the flash data.	Refer to 'System Settings' on page 7.
On-chip debug security ID settings	You set any 10-byte ID code for the on-chip debugging security ID. When configuring the setting to allow on-chip debugging operations, please use a security ID that is not easily guessable by third parties.	Refer to 'System Settings' on page 7.
Allocation of memory space when using on-chip debugging functions	At the start of on-chip debugging, ID authentication is performed. Based on the result of this authentication, you can set whether or not to erase the flash memory data. Please configure this according to your security policy.	Refer to 'System Settings' on page 7.
Allocation of debug monitor area and debug stack area	The microcontroller uses the debug monitor area and debug stack area to communicate with and enable debugging functions using the E2 and E2 Lite on-chip debugging emulators. If these areas are not allocated, on-chip debugging operations may not function correctly due to data being overwritten by user programs.	Refer to 'System Settings' on page 7.
Voltage detector 0 (LVD0)	LVD0 compares the supply voltage (V_{DD}) with the detection voltage (V_{LVD0}) and generates an internal reset or interrupt request signal. The microcontroller must remain in a reset state until the supply voltage is within the operational voltage range. If LVD0 is not enabled, the microcontroller may operate outside the operational voltage range and could malfunction.	Refer to 'Voltage detector (resource: LVD0) component' on page 8.
Watchdog timer (WDT)	The watchdog timer is used to detect program malfunctions. Please configure the watchdog timer according to your system requirements.	Refer to 'Watchdog timer component' on page 8.
RAM initialization	Upon release from reset, the RAM area is in an undefined state, so be sure to initialize any RAM areas before use. Reading from uninitialized RAM areas may result in an internal reset due to RAM parity errors.	The declared variables are automatically initialized by the processing of the cstart.asm file generated by SC.
Stack pointer initialization	Upon release from reset, the stack pointer is in an undefined state. Be sure to initialize it before using the stack, and ensure that sufficient stack space is allocated to avoid overwriting data in the RAM area.	The stack pointer is automatically initialized by the processing of the cstart.asm file generated by SC.

2. How to Configure Required Functions Using the Smart Configurator

The Smart Configurator is a tool that automatically generates the initial setup program for the RL78 microcontroller. This guide explains how to configure functions using the Smart Configurator, which simplifies the setup of microcontroller functions. The Smart Configurator is compatible with the following integrated development environments: e2studio, CS+, and IAR Embedded Workbench.

Additionally, download and install the Smart Configurator from our website. After installation, you can start the Smart Configurator from the Start menu.

- The website where the Smart Configurator is available:

  https://www.renesas.com/us/en/software-tool/rl78-smart-configurator

2.1 Clock Settings

The clock settings configure the following functions. Setting the CPU/peripheral hardware clock and low-speed peripheral clocks generates code according to the settings.

- Flash operation mode at startup

  Example setting: High-speed main mode

- High-speed on-chip oscillator frequency at startup

  Example setting: 32 MHz

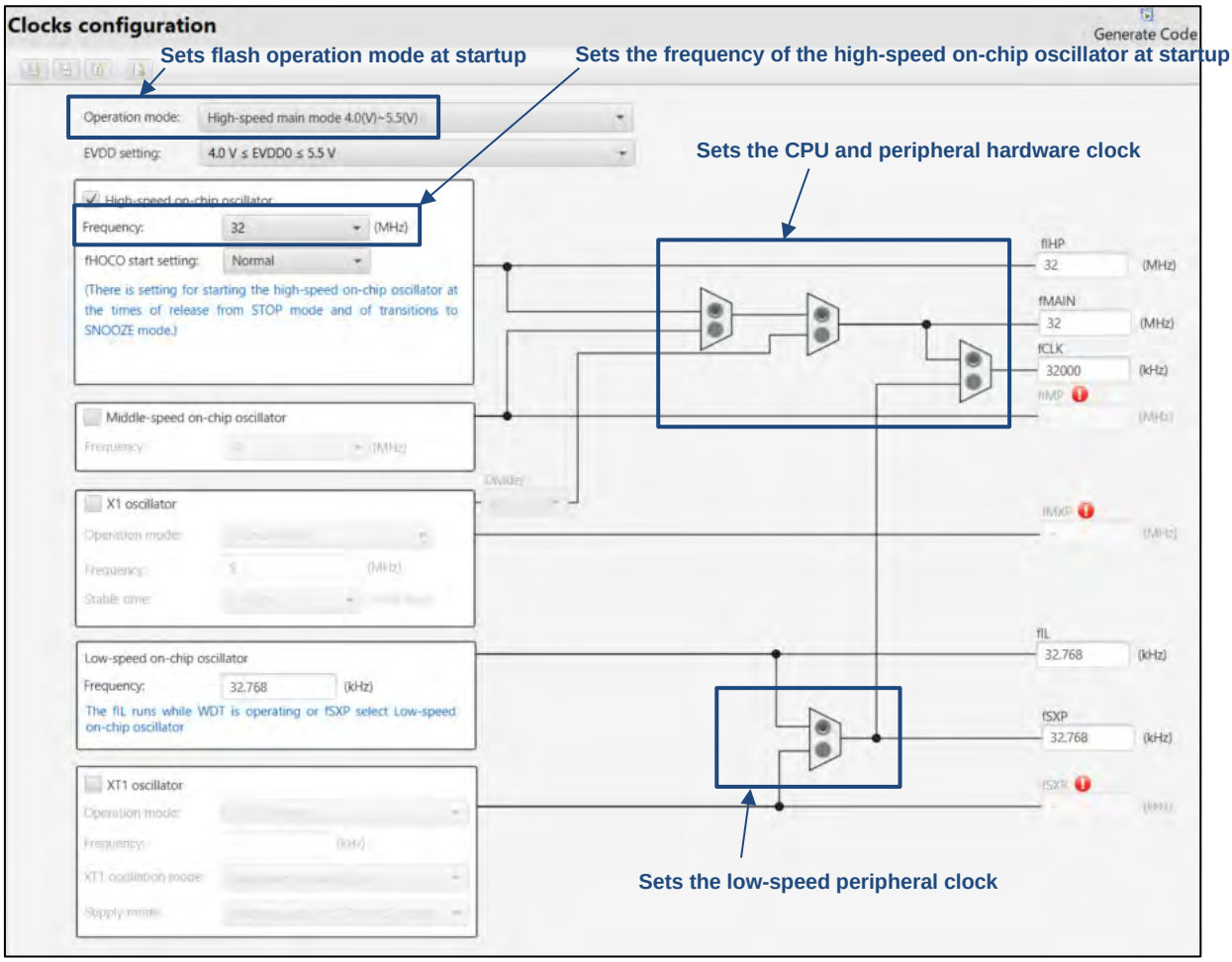
- CPU/peripheral hardware clock

  Example setting: High-speed on-chip oscillator

- Low-speed peripheral clock

  Example setting: Low-speed on-chip oscillator

Figure 2-1 Clock Settings



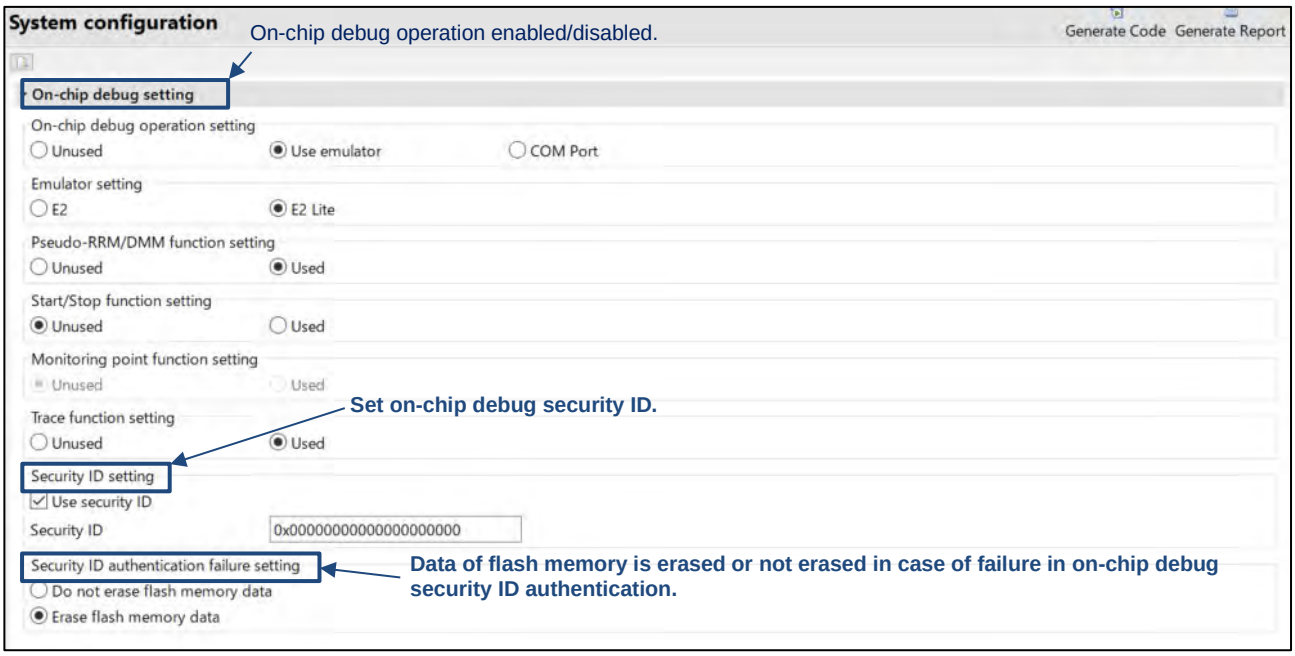
2.2 System Settings

The system settings configure the following functions:

When “Use Emulator” and “COM Port” are selected in the “On-Chip Debug Operation Settings” on the System Settings screen, the debug monitor area is automatically allocated.

- On-chip debug operation enabled/disabled
- Set on-chip debug security ID
- Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication
- Allocate debug monitor area and debug stack area

Figure 2-2 System Settings

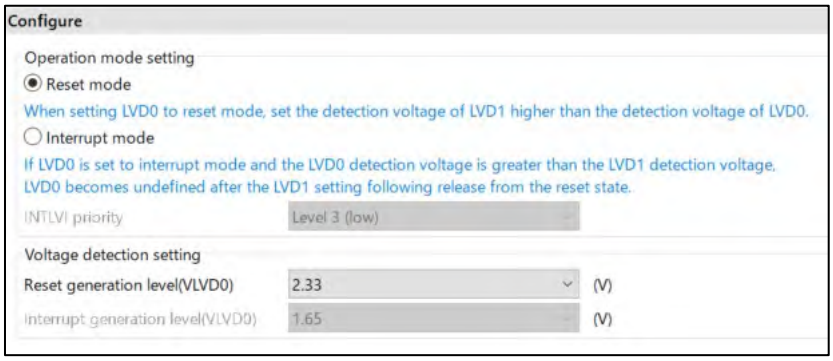


2.3 Voltage Detector Component Settings

Add the voltage detector (resource: LVD0) component. Set the voltage detector 0 (LVD0) in the user option byte. If the component is not added, the voltage detector 0 (LVD0) will be set to off.

Example setting：reset mode (voltage detection = 2.33V)

Figure 2-3 Voltage Detector Component Settings



2.4 Watchdog Timer Component Settings

Add a watchdog timer component. Set the watchdog timer in the user option byte. If the component is not added, the watchdog timer will be set to off.

Example setting (1)：Not used

(The watchdog timer is turned off when no components are added.)

Example setting (2)：

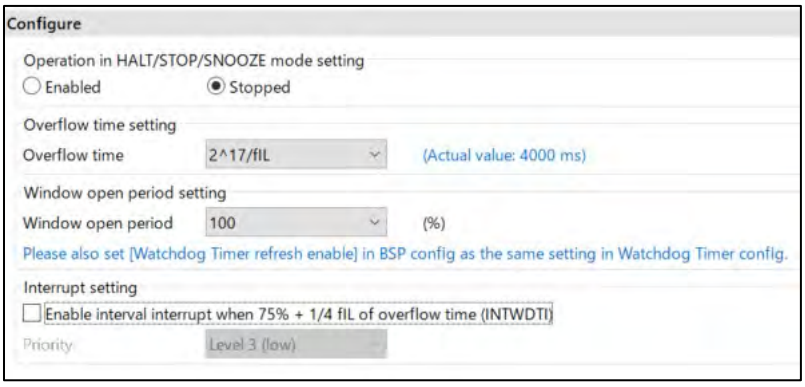
Operation setting in HALT/STOP/SNOOZE mode: Not used

Window open period: 100%.

Overflow time: 2^17/f_{IL}

Interrupt setting: No interval interrupt generated

Figure 2-4 Watchdog Timer Component Settings



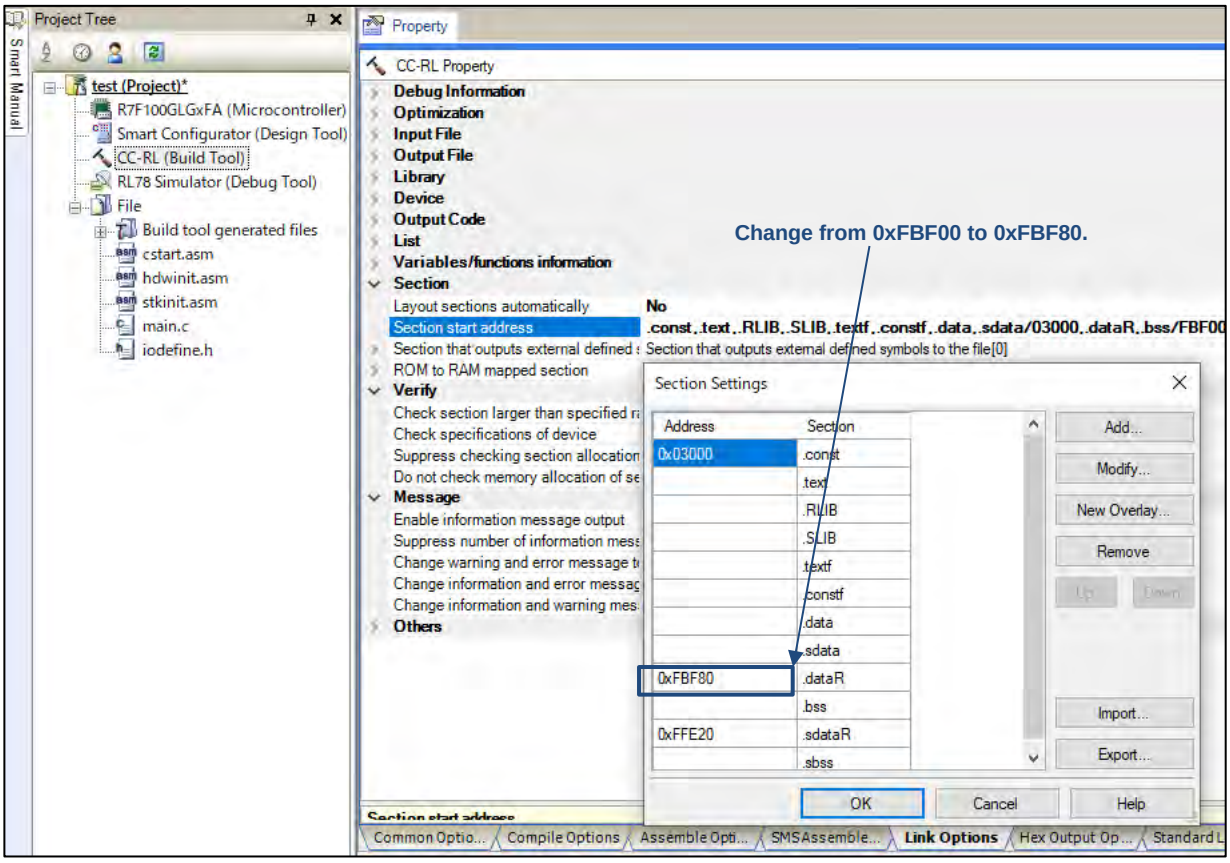
2.5 Allocation of Memory Space When Using On-chip Debugging Functions

The debug control area for self-programming (128 bytes) is an optional setting in the integrated development environment (IDE) that allows you to change the range of the RAM area used by the user and allocate this area. When performing self-programming with the on-chip debugging function, reserve 128 bytes of the RAM for the debug control area.

- Integrated Development Environment CS+

Set up a section in the Linking Options. First, set “Automatically place sections” to “No.” Next, open the section settings under “Starting Address of Section” and change the starting address of the RAM area by adding 0x80 (128) to the starting address of RAM.

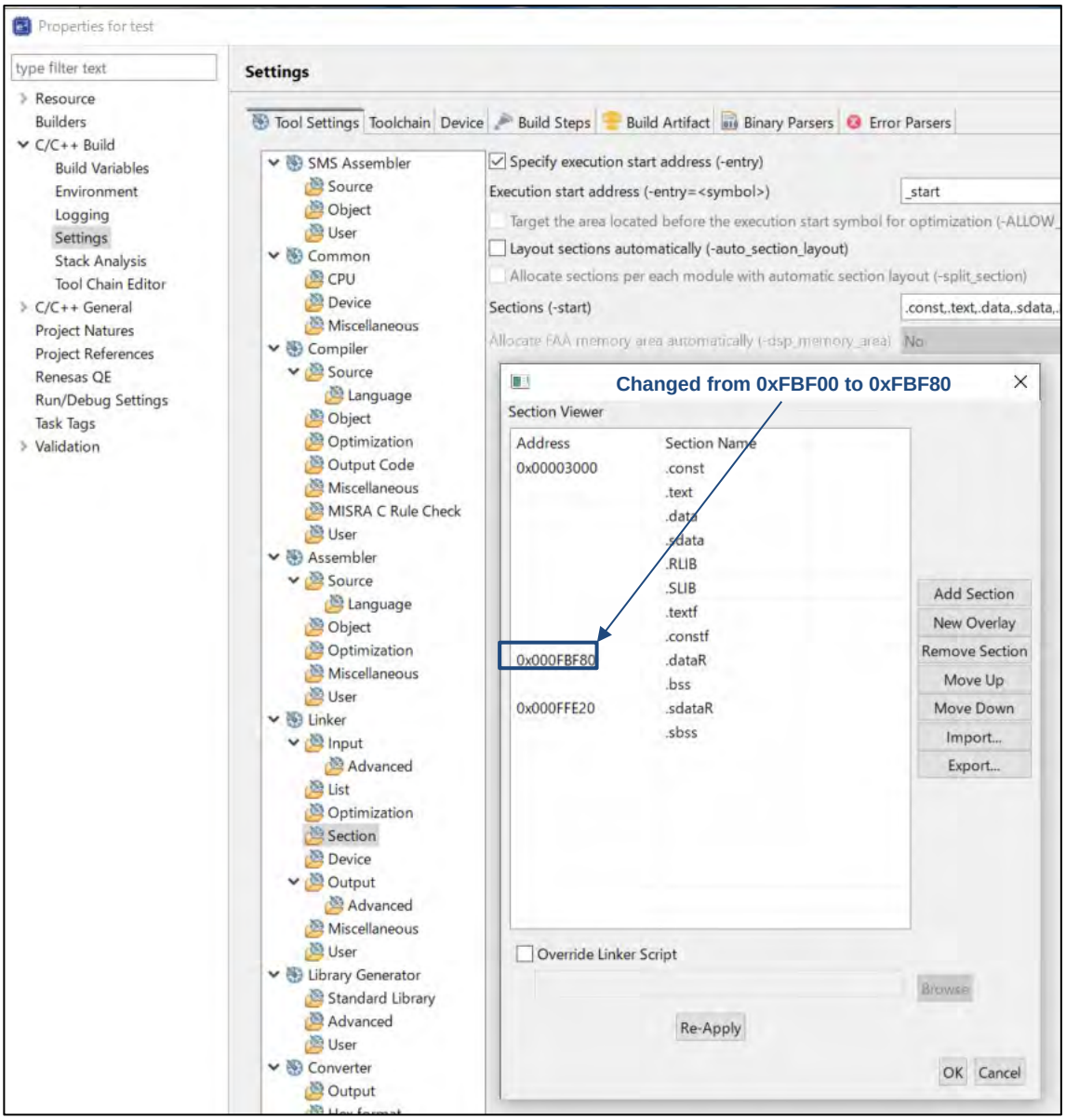
Figure 2-5 Section settings (for R7F100GLG)



- Integrated Development Environment e2studio

Configure linker sections. First, uncheck “Layout sections automatically.” Next, open the Section Viewer from “Sections” and change the starting address of the RAM area by adding 0x80 (128) to the starting address of RAM.

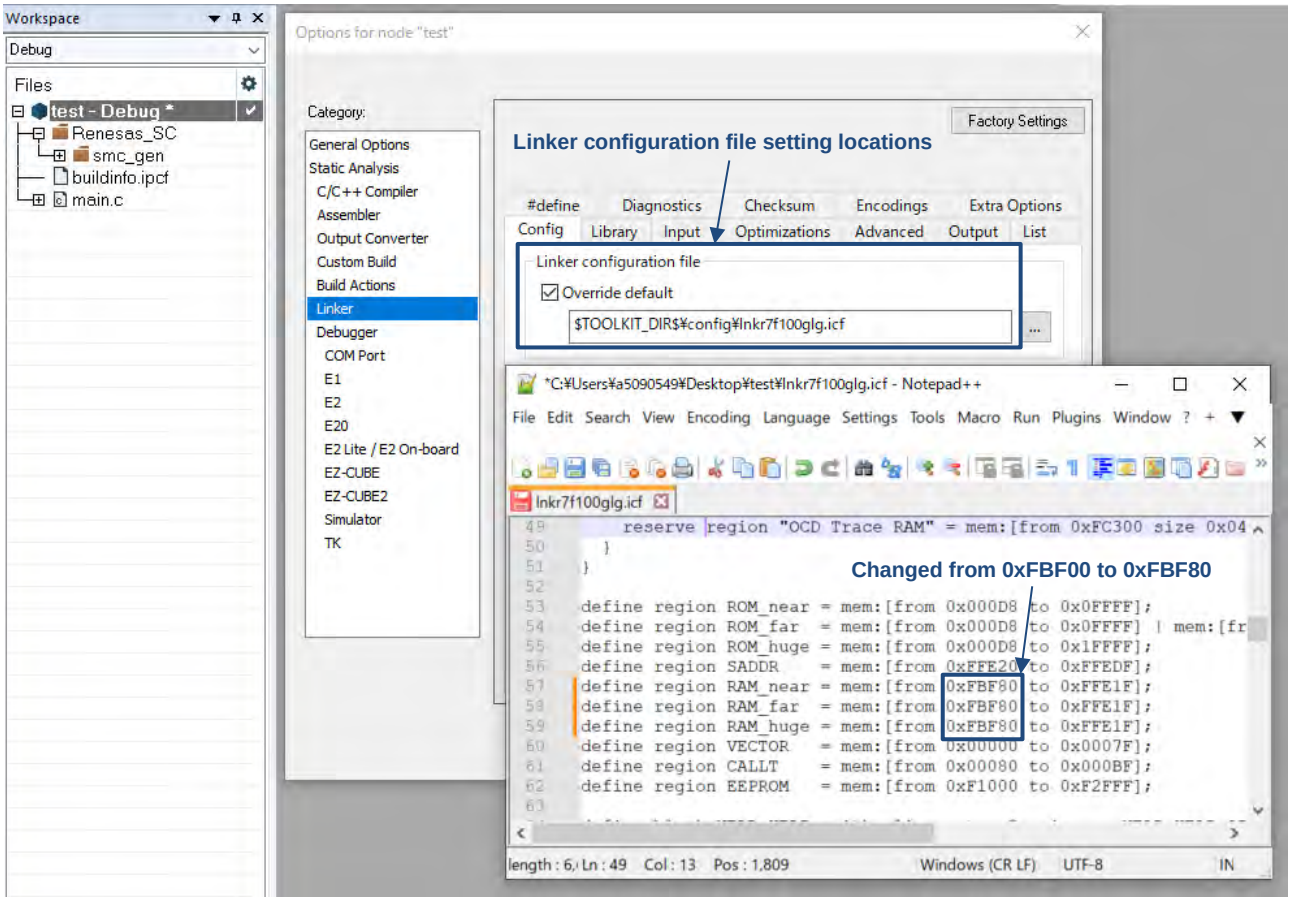
Figure 2-6 Section Viewer (for R7F100GLG)



- Integrated Development Environment IAR Embedded Workbench

Modify the linker configuration file. First, check "Default Override". Next, copy the linker configuration file and save it in the project folder. Specify the path to the copied linker configuration file. Open the copied linker configuration file, add 0x80 (128) to the start address of the RAM, and update the starting address of the RAM region.

Figure 2-7Linker configuration file (for R7F100GLG)



3. How to Verify That the Function is Set

The functions listed below can be verified from the link map file (.map file). Please configure the linker options in the Integrated Development Environment (IDE) to output the link map file.

For other functions, please verify their operation through on-chip debugging.

- User option bytes
- On-chip debug option byte
- Security settings for on-chip debugging
- Allocation of memory space when using on-chip debugging functions

Figure 3-1 Link map file (.map file) (1/2)

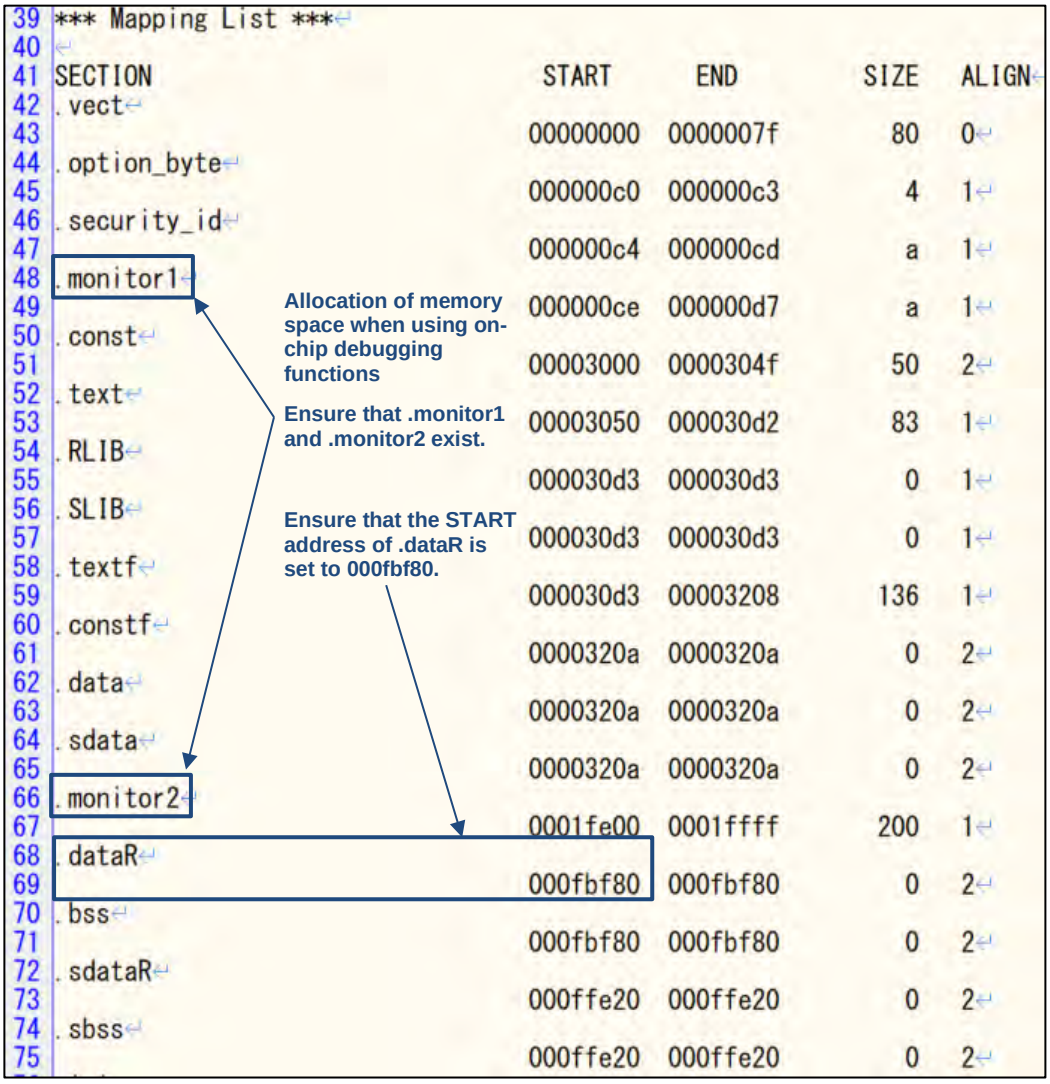
```
*** Options ***
-subcommand=DefaultBuild¥test.clnk
-Input=DefaultBuild¥main.obj
-Input=DefaultBuild¥r_cg_systeminit.obj
-Input=DefaultBuild¥hdwinit.obj
-Input=DefaultBuild¥r_bsp_init.obj
-Input=DefaultBuild¥stkinit.obj
-Input=DefaultBuild¥cstart.obj
-Input=DefaultBuild¥r_bsp_common.obj
-Input=DefaultBuild¥r_bsp_common_ccrl.obj
-Input=DefaultBuild¥mcu_clocks.obj
-Input=DefaultBuild¥Pin.obj
-SECURITY_ID=00000000000000000000
-DEVICE=C:¥Program Files (x86)¥Renesas Electronics¥CS+¥CC¥Device¥RL78¥Devicefile¥DR7F100GLG.DVF
-DEBug
-NOCOmpress
-NOOPtimize
-OUtput=DefaultBuild¥test.abs
-OCDBG=84
-DEBUG_MONITOR=1FE00-1FFFF
-USER_OPT_BYTE=EF3AE8
-OCDTR
-LISt=DefaultBuild¥test.map
-AUTO_SECTION_LAYOUT
-ROm=.data=.dataR
-ROm=.sdata=.sdataR
-NOMessage
-MEMory=High
-NOLOgo
-LIBrary=DefaultBuild¥test.lib
-end
```

On-Chip Debug Security Settings

On-Chip Debug Option Byte Settings

User Option Byte Settings

Figure 3-2 Link map file (.map file) (2/2)



4. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896)
RL78 family user's manual software (R01US0015)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Appendix

This section describes the functions of the RL78 microcontroller.

1. User Option Bytes

The RL78 microcontroller automatically refers to the option bytes and sets the specified function at power-on or reset startup. When using the product, be sure to set the following functions by using the option bytes.

Table 1-1 User Option Bytes

option bytes area		function
User option bytes	000C0H	・Watchdog timer (WDT)
	000C1H	・Voltage Detector 0 (LVD0)
	000C2H	・Flash operation mode ・Frequency of the high-speed on-chip oscillator

1.1 Watchdog Timer

1.1.1 Overview of the Watchdog Timer

The watchdog timer is used to detect program malfunctions. If a malfunction is detected, an internal reset signal is generated. Writing "ACH" to the WDTE register clears the watchdog timer counter and restarts the counting process.

The following conditions are considered a program malfunction:

- The watchdog timer counter overflows
- A 1-bit manipulation instruction is used to write to the watchdog timer enable register (WDTE).
- A value other than “ACH” is written to the WDTE register
- Writing to the WDTE register proceeds while the window is closed

1.1.2 Setting the Watchdog Timer

The functions of the watchdog timer and the bits to be set are shown below.

Figure 1-1 Format of User Option Byte (000C0H)

7	6	5	4	3	2	1	0
WDTINT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON

Bit	Bit Name	Bit Description
7	WDTINT	0: Interval interrupt of watchdog timer is not used 1: Interval interrupt of watchdog timer is used (An interval interrupt is generated when 75% of the overflow time + 1/4 f_{IL} is reached.)
6-5	WINDOW [1:0]	00B: Setting prohibited 01B: Watchdog timer window open period: 50% 10B: Setting prohibited 11B: Watchdog timer window open period: 100%
4	WDTON	0: Watchdog counter operation disabled (counting stopped after reset) 1: Watchdog counter operation enabled (counting started after reset)
3-1	WDCS [2:0]	Watchdog timer over-flow time select bits (Count source: f_{IL}) 000B: $2^7/f_{IL}$、001B: $2^8/f_{IL}$、010B: $2^9/f_{IL}$、011B: $2^{10}/f_{IL}$、 100B: $2^{12}/f_{IL}$、101B: $2^{14}/f_{IL}$、110B: $2^{15}/f_{IL}$、111B: $2^{17}/f_{IL}$
0	WDSTBYON	0: Counter operation stopped in HALT / STOP / SNOOZE mode 1: Counter operation enabled in HALT / STOP / SNOOZE mode

1.1.3 Notes on Setting the Watchdog Timer

The following are notes on setting the watchdog timer.

- Oscillator characteristics of f_{IL} (Low-speed on-chip oscillator clock frequency) is (TYP.) 32.768 kHz. To clear the watchdog timer counter, perform within the range of the oscillator characteristics of f_{IL}.
- The window open period is 100% when WDSTBYON = 0, regardless the value of the WINDOW1 and WINDOW0 bits.
- The invalid memory access detection function is always enabled when the WDTON bit is 1, regardless of the setting of the IAWEN bit of IAWCTL register.

1.2 Voltage Detector 0 (LVD0)

1.2.1 Overview of the Voltage Detector 0 (LVD0)

The voltage detector has LVD0 set by option byte and LVD1 set by software; LVD0 has the following functions

- LVD0 compares the supply voltage (V_{DD}) with the detection voltage (V_{LVD0}), and generate an internal reset or internal interrupt signal.
- The option byte allows you to select the detection voltage (V_{LVD0}) for LVD0 from among 6 voltages.
- Operable in STOP mode.
- The reset mode detects $V_{DD} \geq V_{LVD0}$ to generate an internal reset. It also detects $V_{DD} < V_{LVD0}$ to generate an internal reset, and the reset state continues until $V_{DD} \geq V_{LVD0}$.
- In interrupt mode, immediately after a reset occurs, the internal reset of the LVD continues in the reset state until $V_{DD} \geq V_{LVD0}$. The internal reset of LVD is released when $V_{DD} \geq V_{LVD0}$ is detected. After the internal reset of LVD is released, an interrupt request signal (INTLVI) is generated by detecting $V_{DD} < V_{LVD0}$ or $V_{DD} \geq V_{LVD0}$.

1.2.2 Setting the Voltage Detector 0 (LVD0)

The functions of the voltage detector 0 (LVD0) and the bits to be set are shown below.

Figure 1-2 Format of User Option Byte (000C1H)

7	6	5	4	3	2	1	0
LVD0EN	LVD0SEL	1	1	1	LVD0V2	LVD0V1	LVD0V0

Bit	Bit Name	Bit Description
7	LVD0EN	0: Stop operation 1: Enable operation
6	LVD0SEL	0:Interrupt mode 1:Reset mode
5-3	—	Be sure to set these bits to 111B.
2-0	LVD0V[2:0]	111B:Rise 1.69V, Fall 1.65V 110B: Rise 1.90V, Fall 1.86V 101B: Rise 2.38V, Fall 2.33V 100B: Rise 2.67V, Fall 2.62V 011B: Rise 2.97V, Fall 2.91V 010B: Rise 3.96V, Fall 3.88V 001B: Setting prohibited 000B: Setting prohibited

1.2.3 Notes on Setting the Voltage Detector 0 (LVD0)

The following are notes on setting the voltage detector 0 (LVD0).

- When setting the LVD0EN bit to 0, be sure to connect a reset circuit to the RESET pin.
- When the LVD0SEL bit is set to 0, the reset voltage at the falling edge of the power supply is V_{PDR} (Typ. 1.50V). In this case the V_{PDR} will be out of the specified operation voltage for this product. After the occurrence of an interrupt (INTLVI), disable other interrupt factors as long as the power supply voltage is within the valid operation range and shift to STOP mode. The operating voltage range depends on the setting of the user option byte (000C2H/040C2H).
- There is a delay of up to 300us in the detection of LVD. During the falling edge of the supply voltage, the detector threshold voltage should be set so that a reset condition occurs before the supply voltage falls outside the operating voltage range, accounting for this delay.
- After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 37.4 AC Characteristics. This is done by utilizing LVD0 or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing LVD0 or controlling the externally input reset signal before the voltage falls below the operating range.

1.3 Flash Operating Modes and High-speed On-chip Oscillator Frequency

1.3.1 Overview of Flash Operating Modes and High-speed On-chip Oscillator Frequency

The operating voltage, operating timing, and operating current of the internal circuit are optimized using flash operation modes. Select an appropriate flash operation mode according to the operating voltage range and clock frequencies of the MCU.

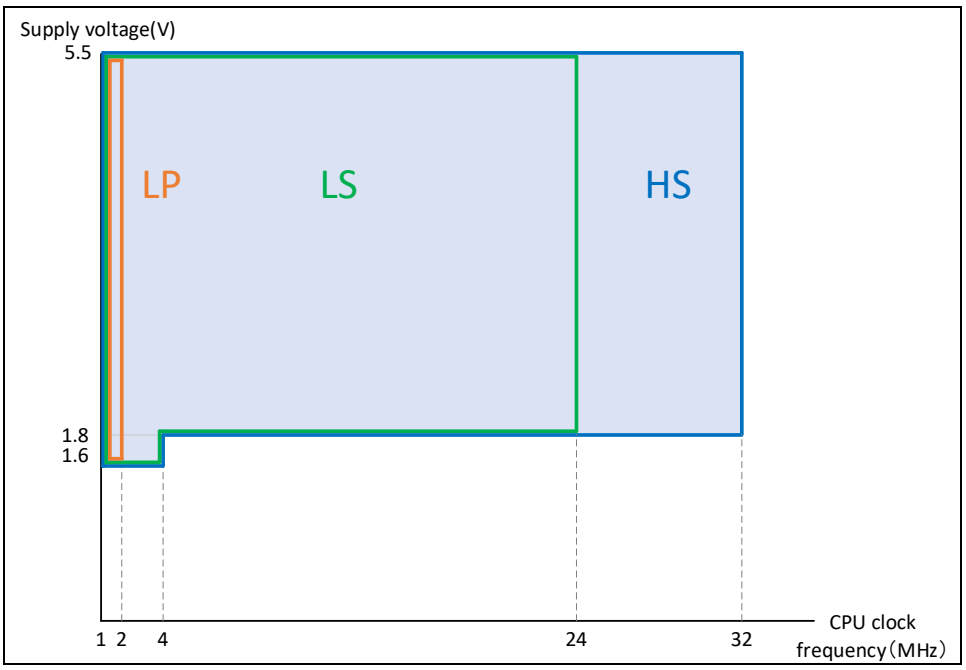
The flash operation mode set by the option byte is used immediately after a reset is released.

Table 1-2 Flash Operation Mode

Flash Operation Mode	Recommended operating range		Description
HS (high-speed main) mode	1.6V to 1.8V	1 to 4MHz (Rewriting of the flash memory is not possible Note.)	High-speed CPU operation (up to 32 MHz) is possible in this mode. Suitable when CPU processing capacity is required. The suitable operating range in HS mode is when the supply voltage is 1.8 V ≤ V_{DD} ≤ 5.5 V and the operating frequency is 24 MHz < f_{CLK} ≤ 32 MHz.
	1.6V to 1.8V	1 to 2MHz	
	1.8V to 5.5V	1 to 32MHz	
LS (low-speed main) mode	1.6V to 1.8V	1 to 4MHz (Rewriting of the flash memory is not possible Note.)	The operating current and CPU operation processing (up to 24 MHz) are well-balanced in this mode. The suitable operating range in LS mode is when the supply voltage is 1.8 V ≤ V_{DD} ≤ 5.5 V and the operating frequency is 2 MHz <f_{CLK} ≤ 24 MHz, or when the supply voltage is 1.6 V ≤ V_{DD} < 1.8 V and the operating frequency is 2 MHz < f_{CLK} ≤ 4 MHz
	1.6V to 1.8V	1 to 2MHz	
	1.8V to 5.5V	1 to 4MHz	
LP (low-power main) mode	1.6V to 5.5V	1 to 4MHz (Rewriting of the flash memory is not possible Note.)	The CPU operates at 1 to 2 MHz in this mode. Low operating current is realized at 1 to 2 MHz. The suitable operating range in LP mode is when the supply voltage is 1.6 V ≤ V_{DD} ≤ 5.5 V and the operating frequency is 1 MHz ≤ f_{CLK} ≤ 2 MHz.
SUB mode	1.6V to 5.5V	32.768kHz (Rewriting of the flash memory is not possible Note.)	Operation is driven by the subsystem clock. This mode enables low-power operation.

Note Flash memory cannot be rewritten by self-programming.

Figure 1-3 Operating Range of Each Flash Operating Mode



1.3.2 Setting the Flash Operating Mode and High-speed On-chip Oscillator Frequency

The bits for setting the flash operating mode and the high-speed on-chip oscillator frequency are shown below.

Figure 1-4 Format of User Option Byte (000C2H)

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

Bit	Bit Name	Bit Description
7-6	CMODE[1:0]	00: Setting prohibited 01: LP (low-power main) mode 10: LS (low-speed main) mode 11: HS (high-speed main) mode
5-4	—	Be sure to set these bits to 10B.
3-0	FRQSEL[3:0]	High-speed on-chip oscillator frequency setting 1000: 32 MHz 0000: 24 MHz 1001: 16 MHz 0001: 12MHz 1010: 8 MHz 0010: 6 MHz 1011: 4 MHz 0011: 3 MHz 1100: 2 MHz 1101: 1 MHz Other than above: Setting prohibited

2. On-chip Debug Option Byte

The 000C3H area of the on-chip debug option byte stores settings for on-chip debug operation control and handling of flash memory data in the event of a failure in authenticating the on-chip debug security ID.

Table 2-1 On-chip Debug Option Byte

Option byte area		Function
On-chip Debug Option Byte	000C3H	・Control of on-chip debug operation ・Processing of flash memory data when security ID authentication fails

2.1 On-Chip Debug Operation Control and Flash Memory Data Handling in Case of Security ID Authentication Failure

2.1.1 Overview of On-Chip Debug Operation Control and Flash Memory Data Handling in Case of Security ID Authentication Failure

The RL78/G23 has on-chip debugging functionality for use in the development and evaluation of user systems. The on-chip debug option byte determines whether on-chip debug operation is permitted or prohibited when an on-chip debugger is connected. The on-chip debug function is also equipped with a security ID authentication function. If the security ID authentication fails, the on-chip debug operation cannot be executed. It can also be configured to erase all flash memory if security ID authentication fails.

2.1.2 Flash Memory Data Handling Settings in Case of Security ID Authentication Failure

Figure 2-1 Format of On-chip Debug Option Byte (000C3H)

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	0	OCDERSD

Bit	Bit Name	Bit Description
7	OCDENSET	0: Disables on-chip debugging. 1: Enables on-chip debugging.
6-1	—	Be sure to set these bits to 000010B.
0	OCDERSD	0: Erases data of flash memory in case of failures in authenticating on-chip debug security ID. 1: Does not erase data of flash memory in case of failures in authenticating on-chip debug security ID.

2.1.3 Notes on Setting Flash Memory Data Handling in Case of Security ID Authentication Failure

The following notes should be observed when configuring the flash memory data handling in the event of a security ID authentication failure.

- To enable on-chip debugging, set “On-chip debug security ID”.
- When enabling 'On-chip Debug Operation', ensure that the area for the debugging monitor program is reserved.

3. Security Settings for On-chip Debugging

When using the on-chip debug function, in addition to setting the on-chip debug option byte, you must also configure the on-chip debug security ID.

To prevent third parties from reading the contents of the memory, the on-chip debug function provides an on-chip debug security ID setting area in 000C4H to 000CDH.

Table 3-1 Security ID Code for On-chip Debugging

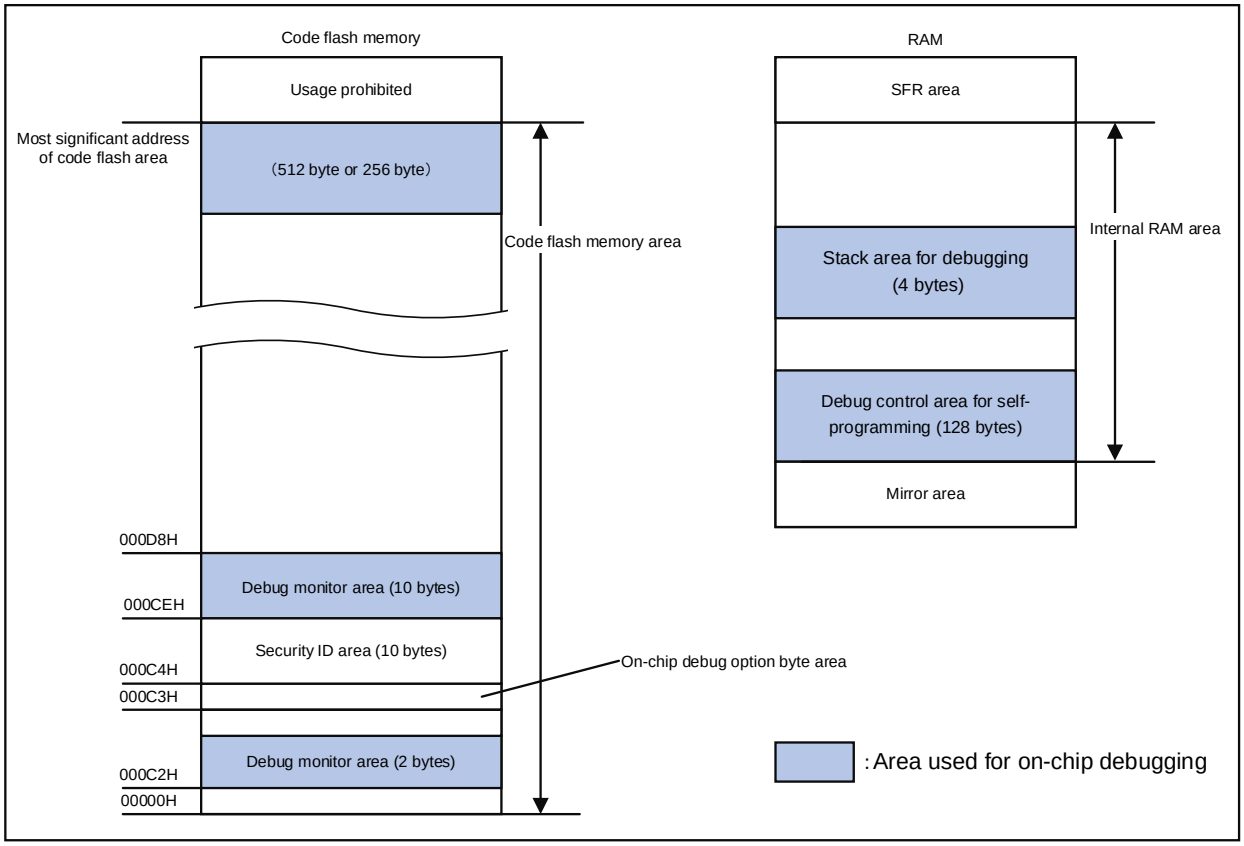
Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID code. The setting FFFFFFFFFFFFFFFFFFFFH is not allowed.
040C4H to 040CDH	

4. Allocation of Memory Space When Using On-chip Debugging Functions

To enable communication between the RL78 microcontroller and the E2 or E2 Lite on-chip debugging emulator, or to use any on-chip debugging functions, it is necessary to allocate memory space in advance. Please allocate the required memory space by configuring the options and sections in the Integrated Development Environment. Since the on-chip debug function uses 512 bytes below the highest address of the code flash memory, ensure that your user program is sized so that it does not use this area.

The area shown in Figure 4-1 is reserved for the debug monitor program and cannot be used for placing user programs or data.

Figure 4-1 Memory space where debug monitor programs are located



4.1 Notes on Allocating Memory Space When Using On-Chip Debugging Functions

The following are notes on allocating memory space.

- If the real-time RAM monitor (RRM) and dynamic memory modification (DMM) functions are not used, the required memory space is reduced to 256 bytes.
- During debugging, the reset vector is relocated to the address of the monitor program.
- Since the debug stack area is allocated immediately below the main stack area in use, its address changes based on the main stack usage. Therefore, 4 additional bytes are consumed for the stack area, and in the case of self-programming, 12 additional bytes are required.
- The on-chip debugger uses 128 bytes of RAM for breakpoints during self-programming. Please refer to the applicable product user's manual for details.

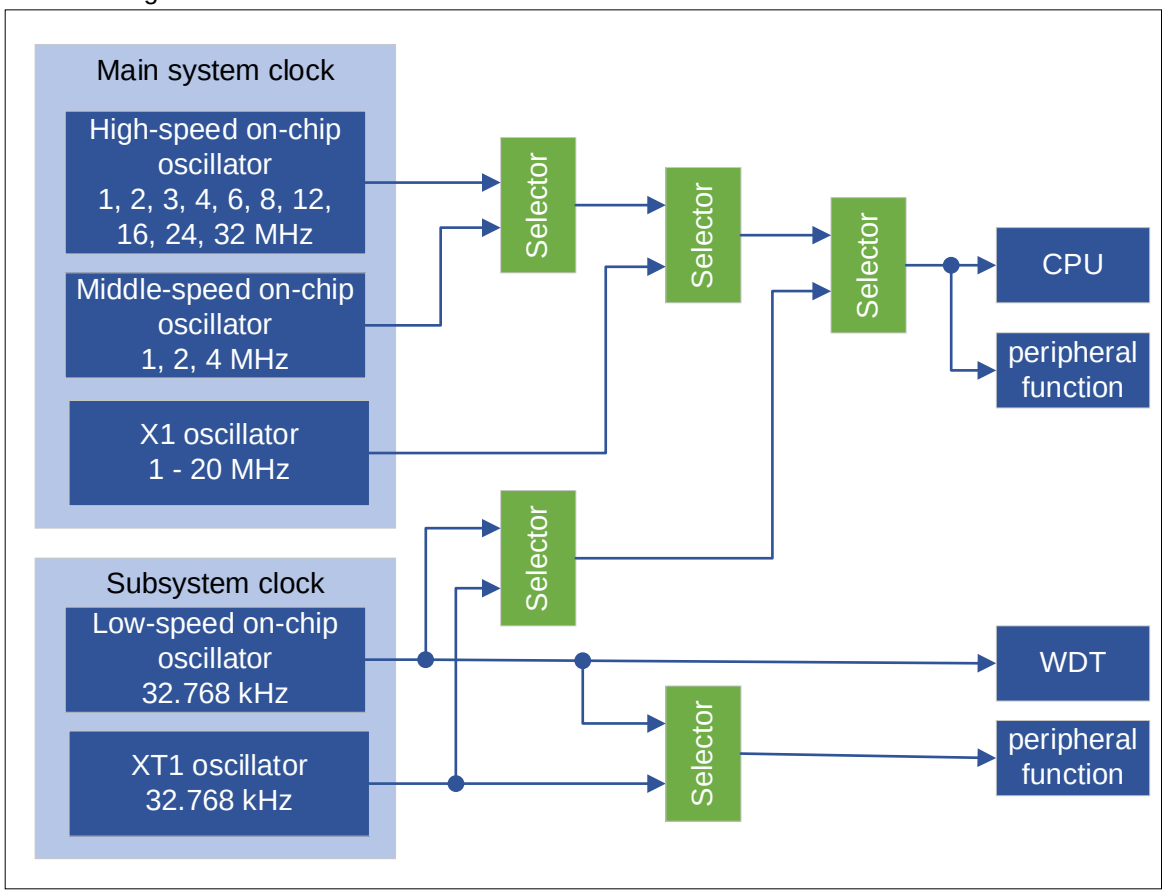
5. CPU/peripheral hardware clock (f_{CLK})

During power-up or startup from a reset, the high-speed on-chip oscillator clock is automatically selected for the CPU/peripheral hardware clock (f_{CLK}). The CPU and peripheral functions will operate using the high-speed on-chip oscillator clock. If other clocks are to be used, you need to change the clock settings.

5.1 Overview of System Clock and Clock Generation Circuit

The following types of system clocks and clock generation circuits are available:

Figure 5-1 Configuration of the Clock Generation Circuit



(1) Main system clock

1) High-speed on-chip oscillator clock

The frequency of oscillation can be selected from among f_{IH} = 32, 24, 16, 12, 8, 6, 4, 3, 2, or 1 MHz (typ.) by using an option byte (000C2H). After release from the reset state, the CPU always starts operating with this high-speed on-chip oscillator clock.

2) Middle-speed on-chip oscillator clock

The frequency of oscillation can be selected from among f_{IM} = 4, 2, or 1 MHz (typ.) by using the MOCODIV bits (bits 0, 1 of the MOCODIV register).

3) High-Speed System Clock

the X1 oscillation circuit oscillates to produce a clock at f_X = 1 to 20 MHz by connecting a resonator to the X1 pin and X2 pin. If the X1 clock oscillation frequency is between 10 MHz and 20 MHz, the AMPH bit in the CMC register must be set to 1. If using the X1 oscillation circuit, please request oscillation evaluation from the crystal oscillator manufacturer for the implementation circuit.

(2) Subsystem clock

1) Low-speed on-chip oscillator

This circuit oscillates to produce a clock at f_{IL} = 32.768 kHz (typ.). When the WDT is enabled (WDTON=1), f_{IL} will operate. If the low-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock, the operation of the A/D converter and the serial interface IICA cannot be guaranteed.

2) Subsystem clock X

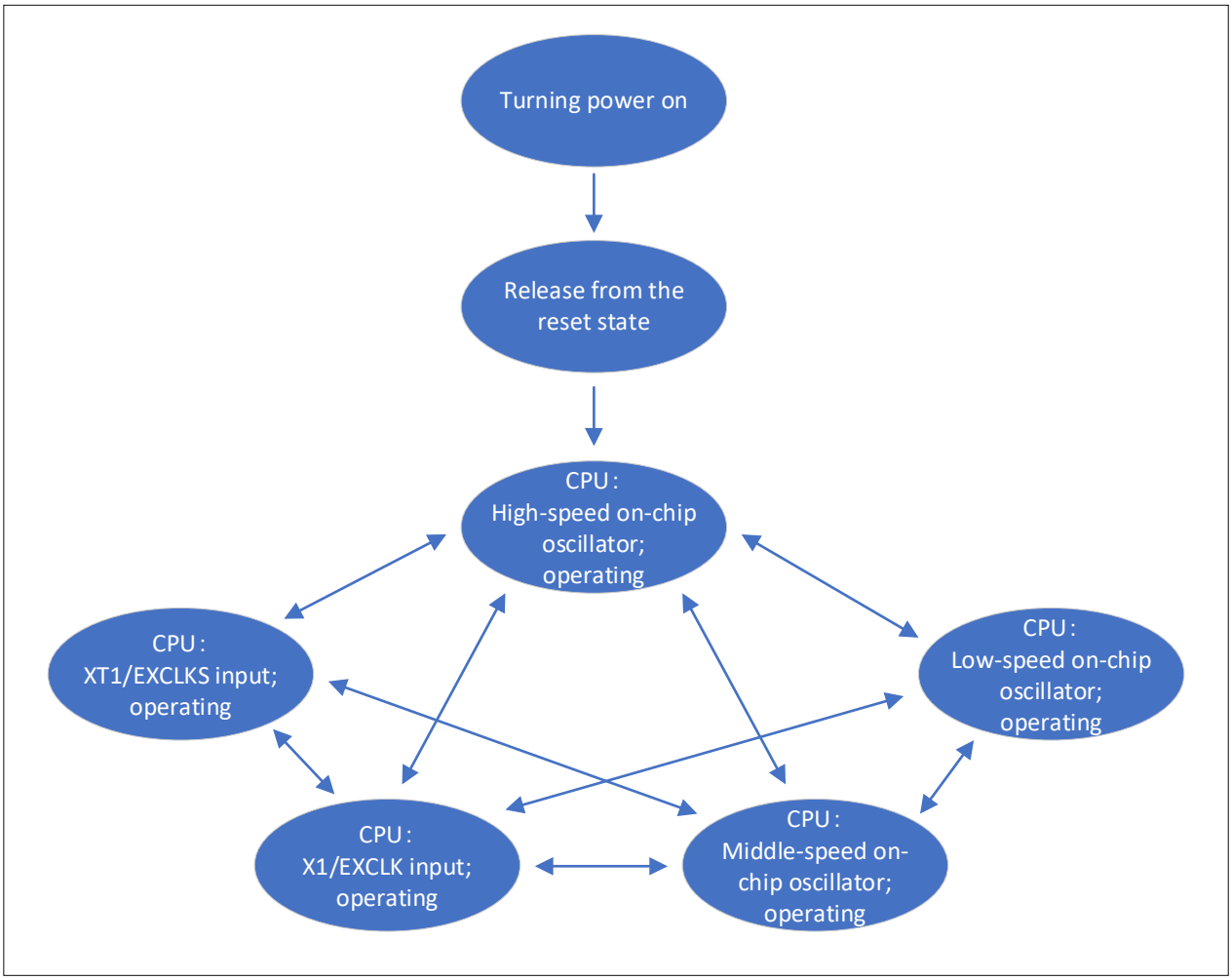
This circuit oscillates to produce a clock at f_{XT} = 32.768 kHz by connecting a 32.768-kHz resonator to XT1

pin and XT2 pin. If the subsystem clock X is selected for the CPU/peripheral hardware clock, the operation of the A/D converter and the serial interface IICA cannot be guaranteed. The XT1 oscillation circuit has oscillation modes including normal oscillation, low power consumption oscillation 1, low power consumption oscillation 2, and low power consumption oscillation 3. The gain and operating current of the XT1 oscillation circuit decrease in the order of low power consumption oscillation 1 > low power consumption oscillation 2 > low power consumption oscillation 3. If using the XT1 oscillation circuit, please request oscillation evaluation from the crystal oscillator manufacturer for the implementation circuit.

5.2 Changing the CPU/Peripheral Hardware Clock (f_{CLK})

For information on how to change the CPU/peripheral hardware clock (f_{CLK}), please refer to the application note RL78/G23 CPU Clock Changing and Standby Settings (R01AN5546EJ).

Figure 5-2 State Transitions of the CPU Clock



6. Low-speed peripheral clock

During power-up or startup from a reset, no clock is supplied to the low-speed peripheral clock. If using real-time clocks or similar peripherals, the user needs to enable the subsystem clock or the low-speed on-chip oscillator. Please refer to the application note RL78/G23 CPU Clock Changing and Standby Settings (R01AN5546EJ).

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep 6, 2024	-	First edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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