RL78/G23

32-Bit Interval Timer (8-bit counter mode)

Introduction

This application note describes how to use the 32-bit interval timer channels in 8-bit counter mode. Using this mode, the application reverses LED indications based on the settings of the compare match detection flags when a timer interrupt occurs. The application also changes the timer interrupt generation intervals based on the number of times the switch has been previously pressed.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Overview of Specifications

In this application note, the application uses timer interrupts generated by the 32-bit interval timer (INTITL) and interrupts received by the edge-detecting interrupt input pin (INTP0).

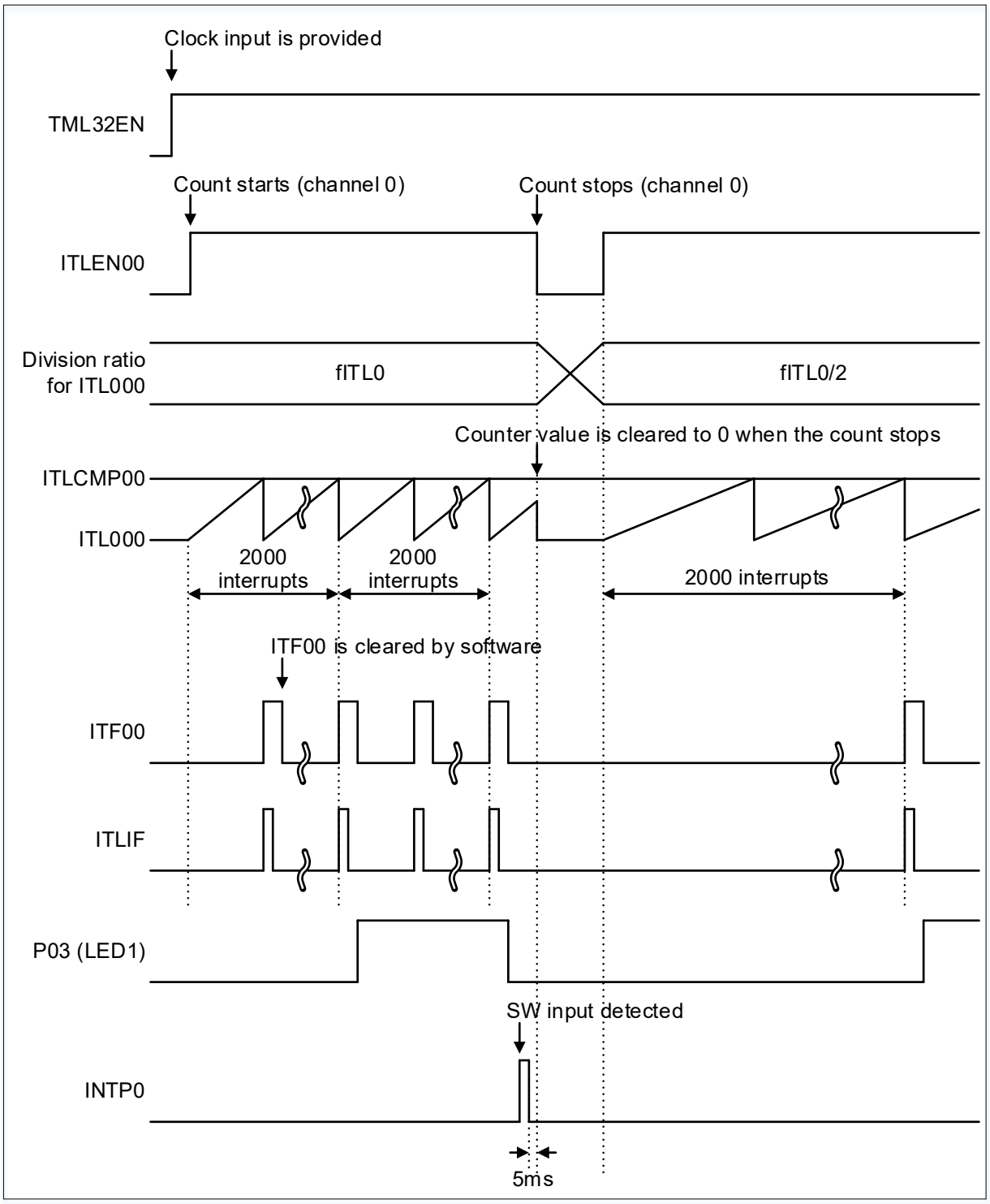
When an INTITL timer interrupt occurs, the application checks the compare match detection flags (ITF00 to ITF03) and reverses the indications of the LEDs associated with the flags. In addition, the application changes the frequency division ratios for the timer channels to modify the timer interrupt generation intervals based on the number of times the switch (SW) has been previously pressed.

Table 1-1 lists the peripheral functions to be used and their uses, Figure 1-1 gives an overview of the relationship between the timer and interrupts, and Figure 1-2 gives an overview of the timer interrupt operation.

Table 1-1 Peripheral Functions Used and Their Uses

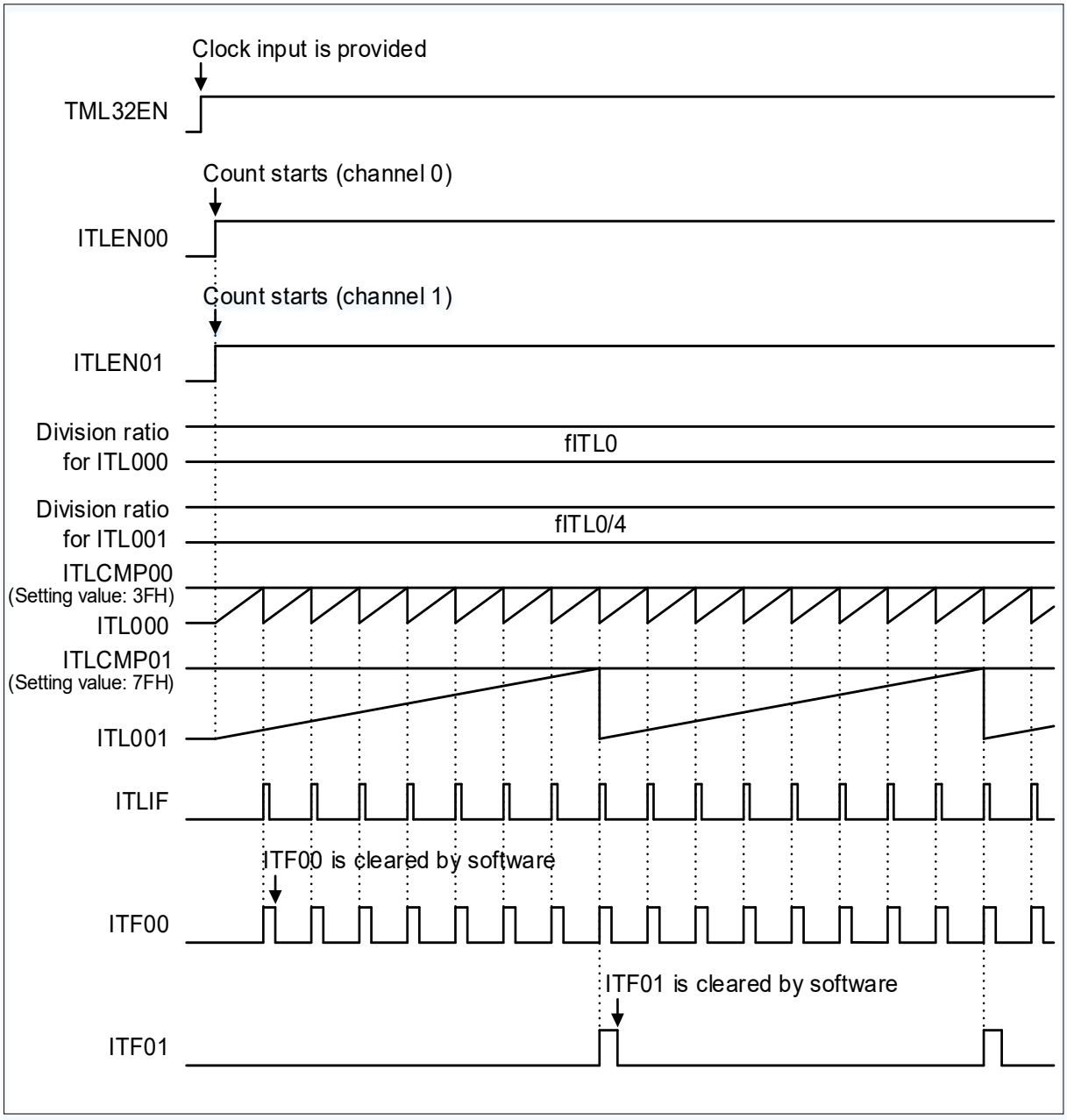
Peripheral Function	Use
32-bit interval timer	Sets the interval of the 32-bit interval timer.
External interrupt	Used as a interrupt generated on pin input edge detection (INTP0) by switch input. Receives switch input interrupts on the edge-detecting interrupt input pin (INTP0).
Port output	Controls the LEDs (LED1 to LED4) connected to P03, P02, P43, and P42 pins.

Figure 1-1 Overview of the Relationship Between the Timer and Interrupts (Operation Example of Channel 0 in 8-bit Counter Mode)



Caution This timing chart is for channel 0. For channels 1 to 3, check their setting values and replace the names of the relevant registers with the appropriate ones.

Figure 1-2 Overview of the Timer Interrupt Operation (8-bit Counter Mode)



Caution This timing chart is for channels 0 and 1. For channels 2 and 3, check their setting values and replace the names of the relevant registers with the appropriate ones.

1.2 Outline of Operation

This section describes how to set the 8-bit counter mode for the 32-bit interval timer.

After the mode is set, the timer interrupt (INTITL) processing for the interval timer counts the number of compare matches for each timer channel. When any of the counts reaches 2000, the CPU reverses the corresponding LED indication. Another processing changes the frequency division ratios for the timer channels, as shown in Table 1-2, based on the number of times the switch has been previously pressed (the operation number increments as the number of switch presses increases).

Table 1-2 LED On/Off Interval Changes

Operation	Frequency division ratios for timer channels			
	Channel 0 (P03)	Channel 1 (P02)	Channel 2 (P43)	Channel 3 (P42)
(1)	fITL0	fITL0/4	fITL0/16	fITL0/64
(2)	fITL0/2	fITL0/8	fITL0/32	fITL0/128
(3)	fITL0/4	fITL0/16	fITL0/64	fITL0
(4)	fITL0/8	fITL0/32	fITL0/128	fITL0/2
(5)	fITL0/16	fITL0/64	fITL0	fITL0/4
(6)	fITL0/32	fITL0/128	fITL0/2	fITL0/8
(7)	fITL0/64	fITL0	fITL0/4	fITL0/16
(8)	fITL0/128	fITL0/2	fITL0/8	fITL0/32

Operations (1) to (8) cycle each time the switch is pressed.

（1） Initialize the I/O ports.
- P03, P02, P43, and P42 pins: Set as output ports (to be used for LED on/off control).
- P137 / INTP0 pin: Set as an input port (to be used for switch input).

（2） Initialize the 32-bit interval timer.
- Place the timer in 8-bit counter mode.
- Set the compare values (INTCMP0n) for channels 0 to 4.
  ITLCMP000 = 3FH
  ITLCMP001 = 7FH
  ITLCMP012 = BFH
  ITLCMP013 = FFH
- Enable timer interrupts by the 32-bit interval timer (INTITL).

（3） Initialize the edge-detecting external interrupt pin.
- Set the falling edge as the valid edge for the INTP0 pin.
- Enable INTP0 interrupts.

（4） Execute a HALT instruction and wait for a timer interrupt (INTITL).

（5） When a timer interrupt (INTITL) cancels HALT mode, the number of compare matches (the number of interrupts) for each timer channel is counted.

（6） When any of the timer interrupt counts reaches 2000, the indication of the applicable LED is reversed.

（7） The INTP0 interrupt processing increments the number of switch inputs (the number of INTP0 interrupts) and changes the frequency division ratio for each timer channel as shown in Table 1-2.

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

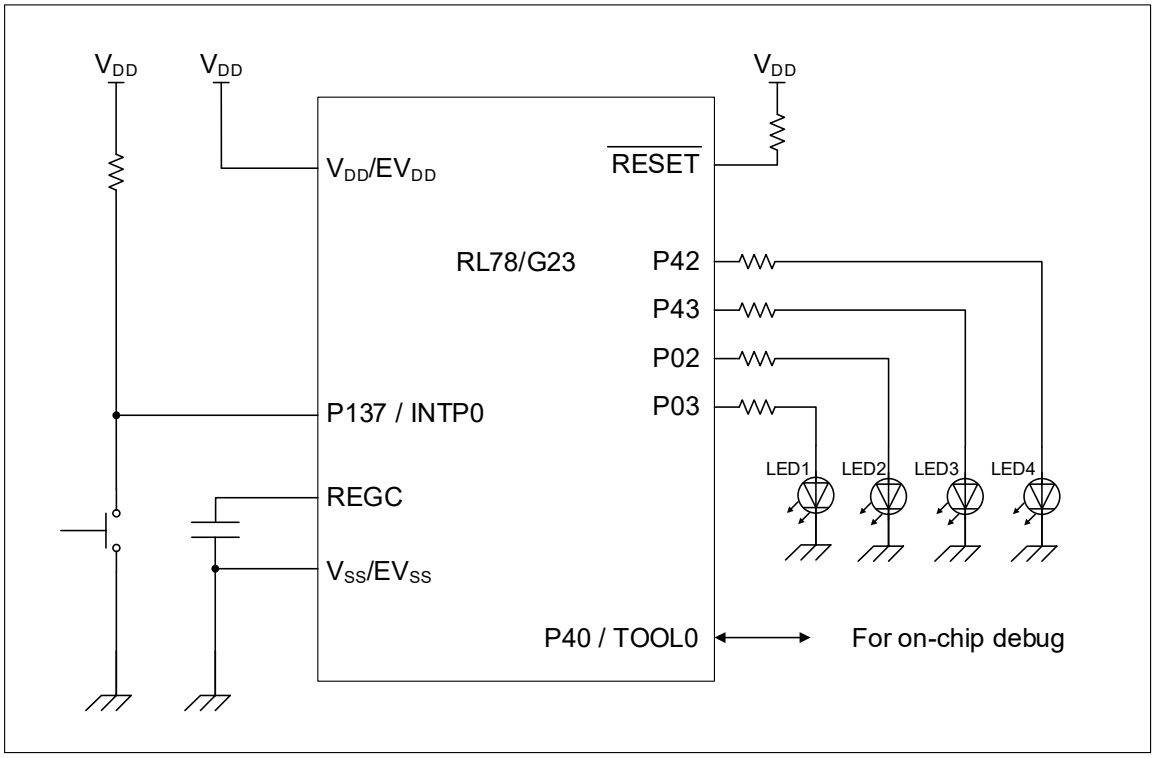
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23-64p Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	High-speed on-chip oscillator clock (f_{IH}): 32 MHz
Operating voltage	5.0 V (can be operated at 2.0 V to 5.5 V) LVD0 operations (V_{LVD0}): Reset mode At rising edge TYP. 1.90V (1.84 V to 1.95 V) At falling edge TYP. 1.86V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ for CC E8.05.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.10.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2021-04 (21.4.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.10.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.1 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.1.2260 from IAR Systems Corp.
Smart configurator (SC)	V1.0.1 from Renesas Electronics Corp.
Board support package (BSP)	V1.00 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to V_{DD} or V_{SS} through a resistor).

Note 2. Connect any pins whose name begins with EV_{SS} to V_{SS}, and any pins whose name begins with EV_{DD} to V_{DD}, respectively.

Note 3. V_{DD} must not be lower than the reset release voltage (V_{LVD0}) that is specified for the LVD0.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Function
P03	Output	LED1 control
P02	Output	LED2 control
P43	Output	LED3 control
P42	Output	LED4 control
P137 / INTP0	Input	Input pin for the switch (SW) (external interrupt request input pin)

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 040C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 040C1H	11111110B	LVD0 detection voltage: reset mode At rising edge TYP. 1.90V (1.84 V to 1.95 V) At falling edge TYP. 1.86V (1.80 V to 1.91 V)
000C2H / 040C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 040C3H	10000100B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2 Constants

Constant Name	Setting Value	Description
IT_COUNT	2000	Timer interrupt count for reversing LED indications
WAITCOUNT_32M	8000	Wait count for 5 ms when the MCU operates in HS mode at 32 MHz

4.3 List of Variables

Table 4-3 lists global variables.

Table 4-3 Global Variables

Type	Variable Name	Description	Function Used
uint16_t	g_transition_status	Transition status variable	r_Config_INTC_intp0_interrupt
uint16_t	g_itldiv_table	Frequency division ratio table for each timer counter	r_Config_INTC_intp0_interrupt
uint16_t	g_inttm00_counter	Timer interrupt counter for channel 0	R_Config_ITL000_Callback_Shared_Interrupt
uint16_t	g_inttm01_counter	Timer interrupt counter for channel 1	R_Config_ITL000_Callback_Shared_Interrupt
uint16_t	g_inttm02_counter	Timer interrupt counter for channel 2	R_Config_ITL000_Callback_Shared_Interrupt
uint16_t	g_inttm03_counter	Timer interrupt counter for channel 3	R_Config_ITL000_Callback_Shared_Interrupt

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function Name	Outline
UserInit()	Initial settings by the user in main processing
R_Config_ITL000_Callback_Shared_Interrupt()	Interrupt processing for interval timer channel 0
R_Config_ITL001_Callback_Shared_Interrupt()	Interrupt processing for interval timer channel 1
R_Config_ITL012_Callback_Shared_Interrupt()	Interrupt processing for interval timer channel 2
R_Config_ITL013_Callback_Shared_Interrupt()	Interrupt processing for interval timer channel 3
r_Config_INTC_intp0_interrupt()	External interrupt processing.

4.5 Specification of Functions

The function specifications of the sample code are shown below.

UserInit()	
Outline	Initial settings by the user in main processing
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_itl_common.h, Config_INTC.h, Config_ITL000.h, Config_ITL001.h, Config_ITL012.h, Config_ITL013.h
Declaration	void UserInit (void)
Description	Initialization required for running the application
Argument	None
Return Value	None

R_Config_ITL000_Callback_Shared_Interrupt()	
Outline	Interrupt processing for interval timer channel 0
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_ITL000.h
Declaration	void R_Config_ITL000_Callback_Shared_Interrupt (void)
Description	Reverses the LED1 indication each time the number of channel 0 interrupts reaches 2000.
Argument	None
Return Value	None

R_Config_ITL001_Callback_Shared_Interrupt()	
Outline	Interrupt processing for interval timer channel 1
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_ITL001.h
Declaration	void R_Config_ITL001_Callback_Shared_Interrupt (void)
D v escription	Reverses the LED2 indication each time the number of channel 1 interrupts reaches 2000.
Argument	None
Return Value	None

R_Config_ITL012_Callback_Shared_Interrupt()	
Outline	Interrupt processing for interval timer channel 2
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_ITL012.h
Declaration	void R_Config_ITL012_Callback_Shared_Interrupt (void)
Description	Reverses the LED3 indication each time the number of channel 2 interrupts reaches 2000.
Argument	None
Return Value	None

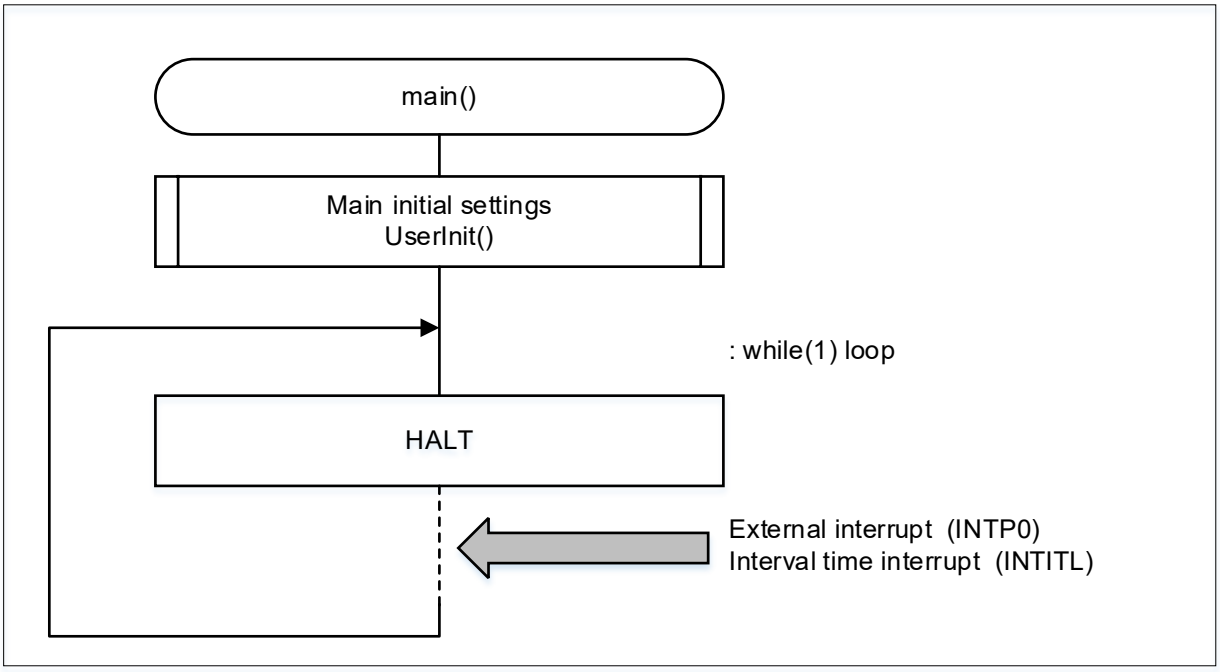
R_Config_ITL013_Callback_Shared_Interrupt()	
Outline	Interrupt processing for interval timer channel 3
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_ITL013.h
Declaration	void R_Config_ITL013_Callback_Shared_Interrupt (void)
Description	Reverses the LED4 indication each time the number of channel 3 interrupts reaches 2000.
Argument	None
Return Value	None

r_Config_INTC_intp0_interrupt()	
Outline	External interrupt processing
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_INTC.h, r_cg_itl.h, r_cg_itl_common.h, Config_ITL000h, Config_ITL001.h, Config_ITL012.h, Config_ITL013.h
Declaration	static void __near r_Config_INTC_intp0_interrupt (void)
Description	Changes the frequency division ratio for each interval timer channel when the switch is pressed.
Argument	None
Return Value	None

4.6 Flowcharts

Figure 4-1 shows the flowchart of the main processing in this application note.

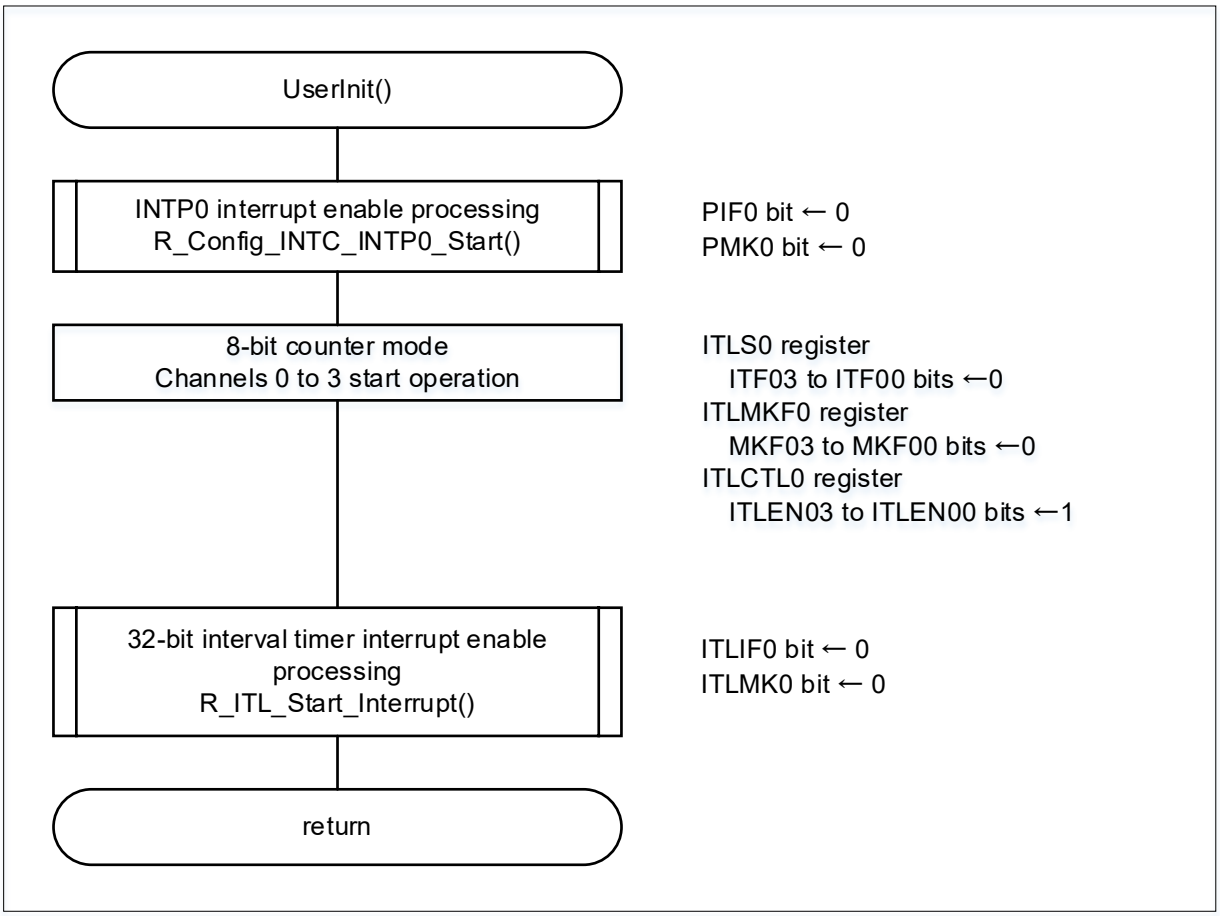
Figure 4-1 Main Processing



4.6.1 Initial Settings by the User in Main Processing

Figure 4-2 shows the flowchart of the initial settings by the user in main processing.

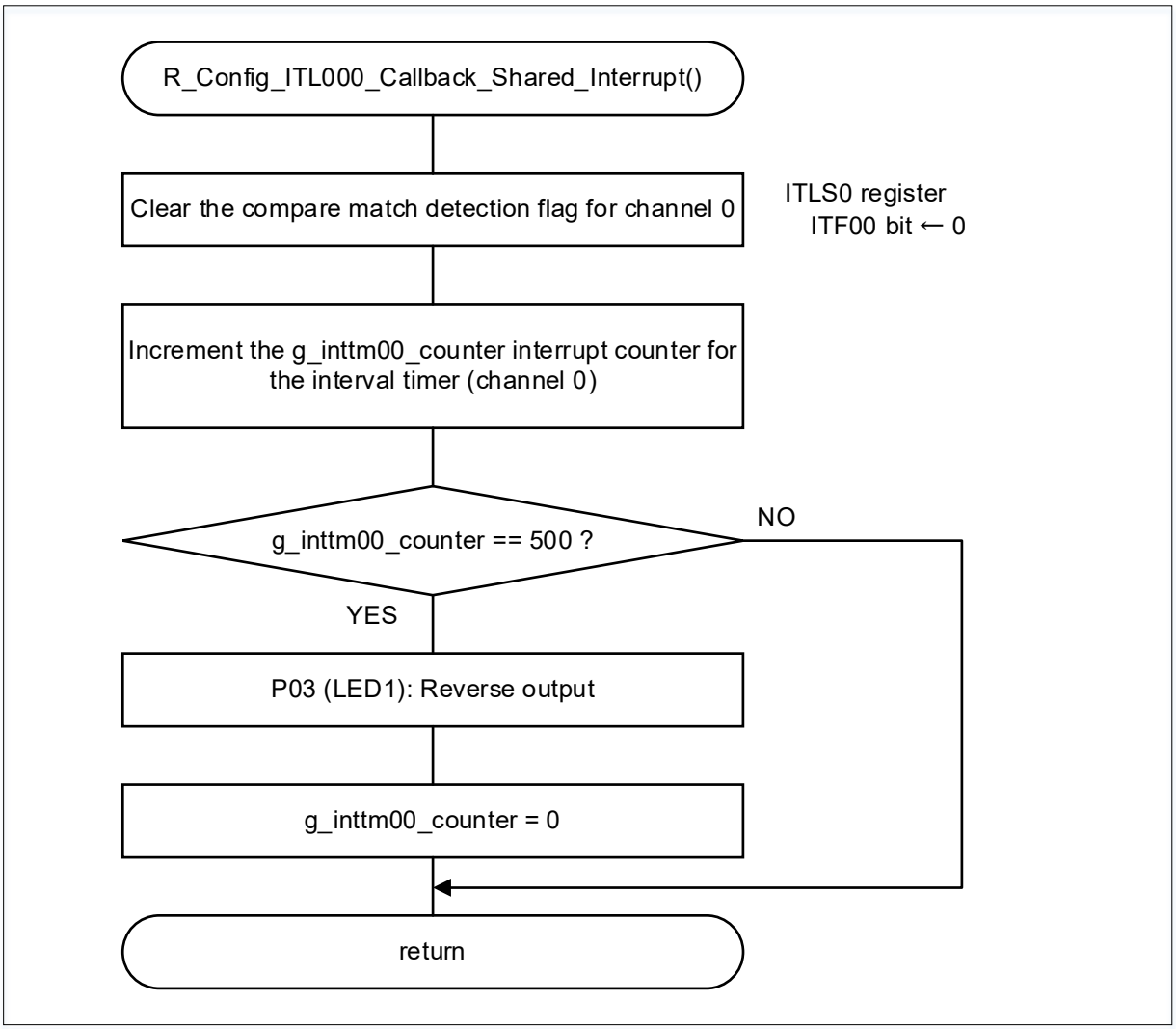
Figure 4-2 Initial Settings by the User in Main Processing



4.6.2 Interrupt Processing for Interval Timer Channel 0

Figure 4-3 shows the flowchart of the interrupt processing for interval timer channel 0.

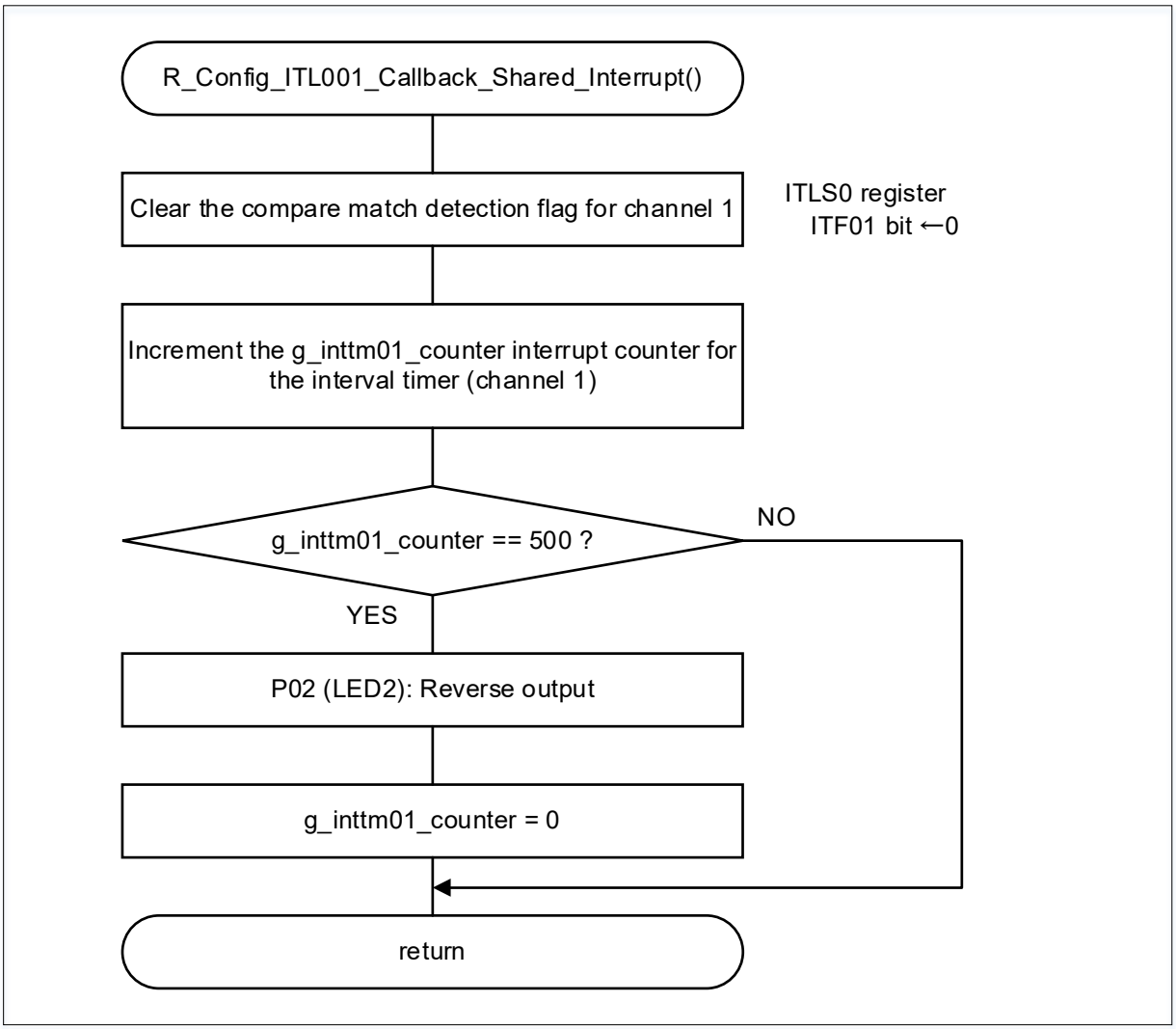
Figure 4-3 Interrupt Processing for Interval Timer Channel 0



4.6.3 Interrupt Processing for Interval Timer Channel 1

Figure 4-4 shows the flowchart of the interrupt processing for interval timer channel 1.

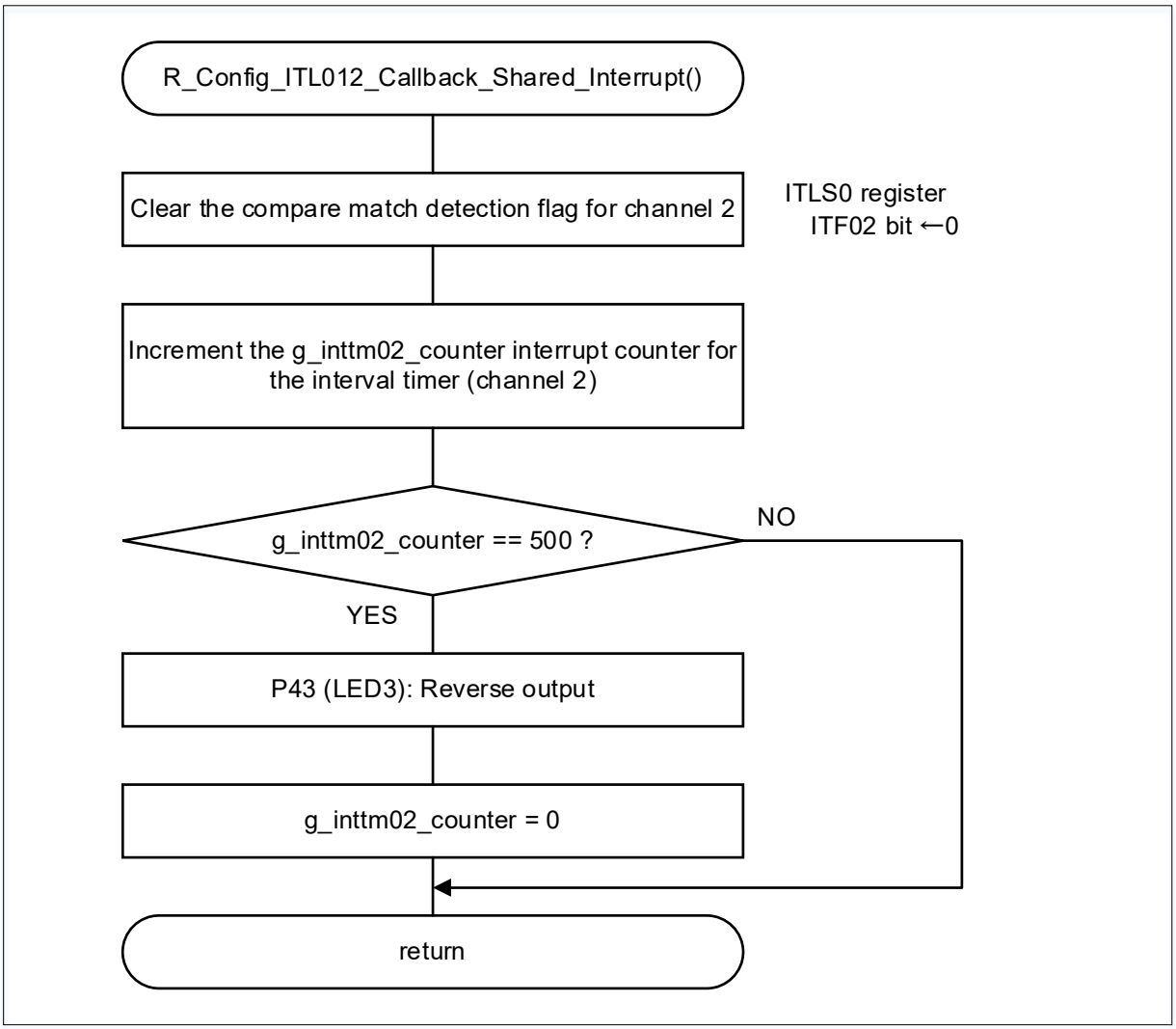
Figure 4-4 Interrupt Processing for Interval Timer Channel 1



4.6.4 Interrupt Processing for Interval Timer Channel 2

Figure 4-5 shows the flowchart of the interrupt processing for interval timer channel 2.

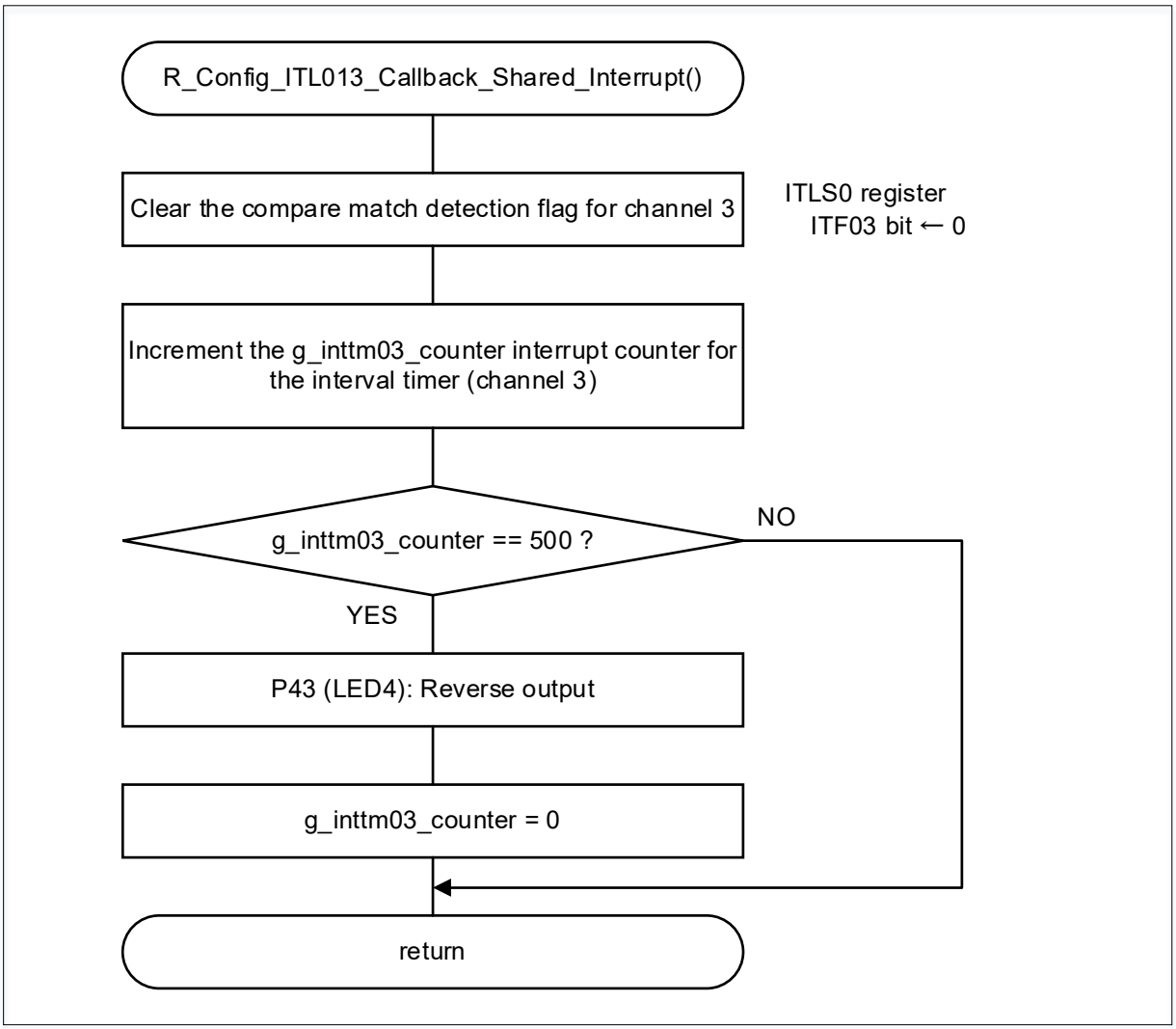
Figure 4-5 Interrupt Processing for Interval Timer Channel 2



4.6.5 Interrupt Processing for Interval Timer Channel 3

Figure 4-6 shows the flowchart of the interrupt processing for interval timer channel 3.

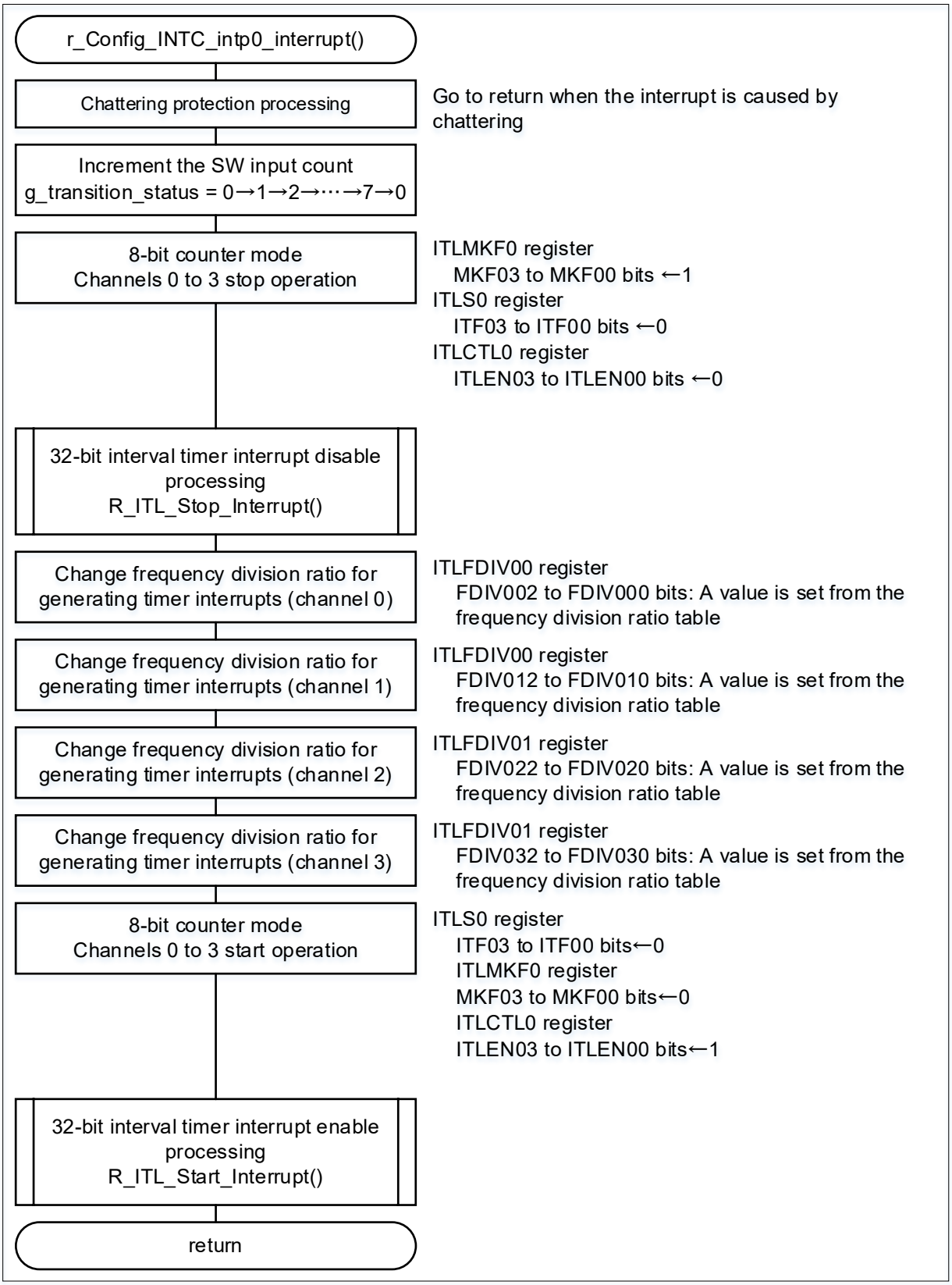
Figure 4-6 Interrupt Processing for Interval Timer Channel 3



4.6.6 External Interrupt (INTP0) Processing

Figure 4-7 shows the flowchart of the external interrupt (INTP0) processing.

Figure 4-7 External Interrupt (INTP0) Processing



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896J)
RL78 family user's manual software (R01US0015J)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2021.04.13	—	First Edition
1.01	2021.07.12	7	Updated the Operation Confirmation Conditions
1.02	2021.08.18	—	Fix the sample code

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   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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