RL78/G22

A/D Converter (Software Trigger and Scan Conversion Modes)

Introduction

This application note describes how to convert an analog voltage to a digital voltage by using the RL78/G22 A/D converter (software trigger, scan mode, and sequential conversion mode).

In this application note, A/D conversion result data is converted and stored in the internal RAM.

Target Device

RL78/G22

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Overview of Specifications

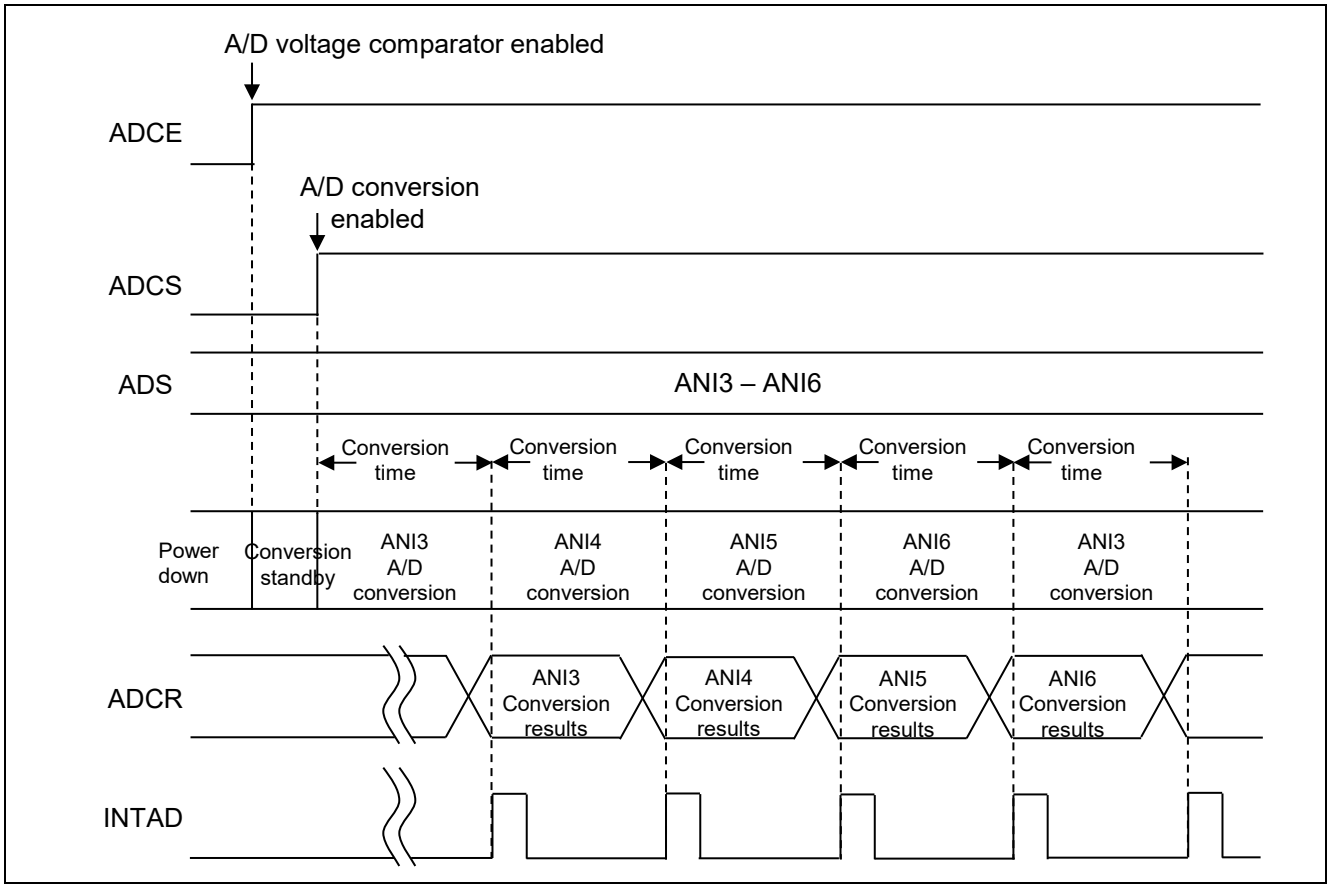
This application note shows an example of using the software trigger, scan mode, and sequential conversion mode of the A/D converter. The A/D converter converts the analog signal input level of the P23 / ANI3 to P26 / ANI6 pins to digital values. Then, A/D conversion result data is converted and stored in the internal RAM.

Table 1- 1 shows the Peripheral Function and Use. Figure 1-1 shows the conversion operation of the A/D converter.

Table 1- 1 Peripheral Function and Use

Peripheral function	Use
A/D converter	Converts the analog signal input level of the P23 / ANI3 to P26 / ANI6 pins.

Figure 1-1 Outline of the A/D Converter Conversion Processing



1.2 Outline of Operation

This sample code uses the software trigger, scan mode, and sequential conversion mode of the A/D converter to convert analog voltages that are input on ANI3 to ANI6 pins to digital voltages. The sample code enters the HALT mode to wait for termination of A/D conversion. After A/D conversion terminates, the A/D conversion result is shifted to the right by 6 bits and stored in the internal RAM.

The following describes the major settings.

(1) Initial settings of the A/D converter

Specify the initial settings according to Table 1- 2.

Table 1- 2 Initial Setting Conditions of the A/D Converter

Register name	Set value	Description
ADM0	40H	Conversion time setting Conversion time mode: Standard mode 1 Conversion time: 1216 /f_{CLK} (38 µs) A/D conversion channel selection: Scan mode
ADM1	00H	A/D conversion mode: Scan mode A/D conversion start condition: Software trigger mode
ADM2	00H	Resolution setting: 10-bit resolution Reference volage source setting V_{REF} (+) : V_{DD} V_{REF} (-) : V_{SS}
ADUL	FFH	Upper limit of conversion result comparison: FFH
ADLL	00H	Lower limit of conversion result comparison: 00H
PMCA2	FFH	Set the P23 / ANI3 to P26 / ANI6 pins to analog input.
PM2	FFH	Set the P23 / ANI3 to P26 / ANI6 pins to input.
ADS	03H	Analog input channels: ANI3 to ANI6
-	-	Use the A/D conversion end interrupt request signal (INTAD).

(2) Main processing

- The sample code sets the ADCS bit of the ADM0 register to 1 (A/D conversion start) to start A/D conversion, and then enters the HALT mode by executing the HALT instruction to wait for an A/D conversion end interrupt.
- After A/D conversion terminates, the A/D conversion result for the input analog signal on the ANI3 pin is transferred to the ADCR register, and then an A/D conversion end interrupt is generated.
- When the HALT mode is released by the A/D conversion end interrupt, the A/D conversion result is read from the ADCR register, shifted to the right by 6 bits, and then stored in the internal RAM.
- The analog input channel changes as follows by the scan mode function:
  ANI3 -> ANI4 -> ANI5 -> ANI6 -> ANI3 (the sequence from ANI3 to ANI6 subsequently repeats)
- The sample code enters the HALT mode to wait for an A/D conversion end interrupt.
  When an A/D conversion end interrupt is generated, the processing described above is performed.

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

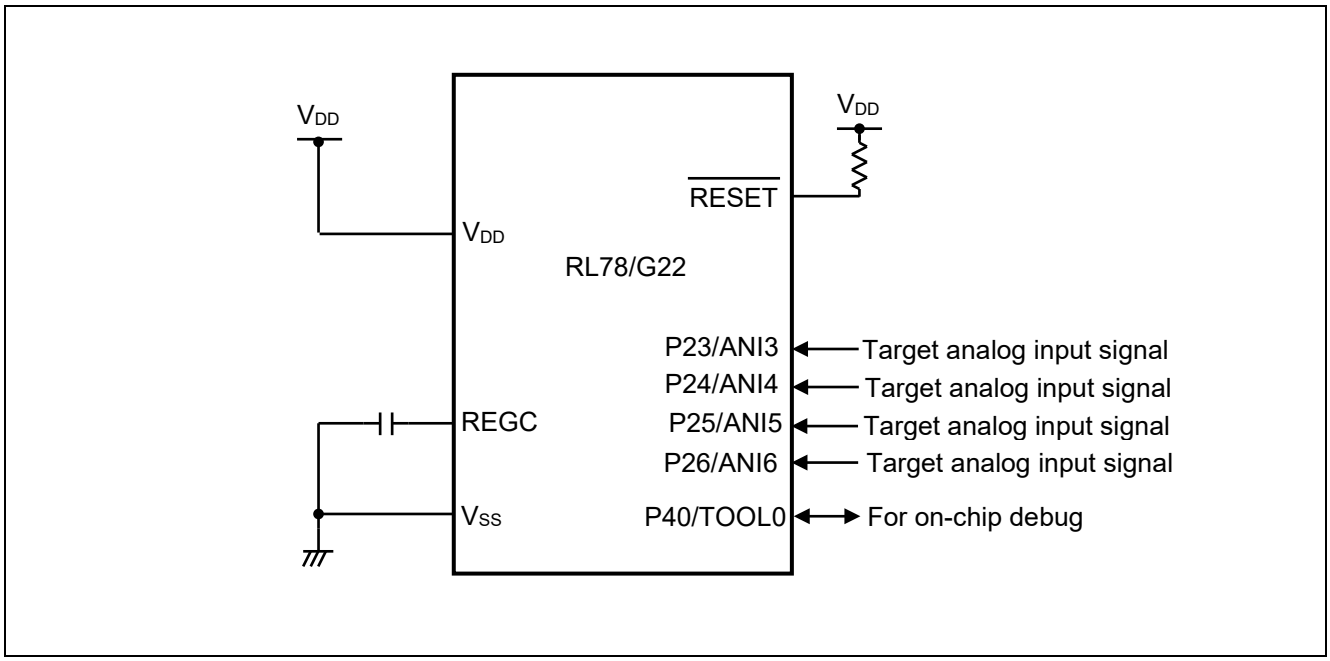
Item	Description
MCU used	RL78/G22 (R7F100GLG)
Board used	RL78/G22-64p Fast Prototyping Board (RTK7RLG220CLG000BJ)
Operating frequency	・ High-speed on-chip oscillator clock (f_{IH}): 32 MHz ・ CPU/peripheral hardware clock: 32 MHz
Operating voltage	3.3 V (can be operated at 1.8 V to 5.5 V) LVD0 operations (V_{LVD0}): Reset mode At rising edge TYP. 1.90V (1.84 V～1.95 V) At falling edge TYP. 1.86V (1.80 V～1.91 V)
Integrated development environment (CS+)	CS+ for CC E8.10.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.01 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2023-01 (23.1.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.12.01 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.3 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.3.2447 from IAR Systems Corp.
Smart configurator (SC)	V1.5.0 from Renesas Electronics Corp.
Board support package (BSP)	V1.40 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to V_{DD} or V_{SS} through a resistor).

Note 2. V_{DD} must not be lower than the reset release voltage (V_{LVD0}) that is specified for the LVD0.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Function
P23 / ANI3	Input	A/D converter analog input port
P24 / ANI4	Input	A/D converter analog input port
P25 / ANI5	Input	A/D converter analog input port
P26 / ANI6	Input	A/D converter analog input port

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H/020C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H/020C1H	11111110B	LVD0 detection voltage: reset mode At rising edge TYP. 1.90V (1.84 V～1.95 V) At falling edge TYP. 1.86V (1.80 V～1.91 V)
000C2H/020C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H/020C3H	10000100B	Enables on-chip debugging

4.2 List of Variables

Table 4-2 lists global variables.

Table 4-2 Global Variables

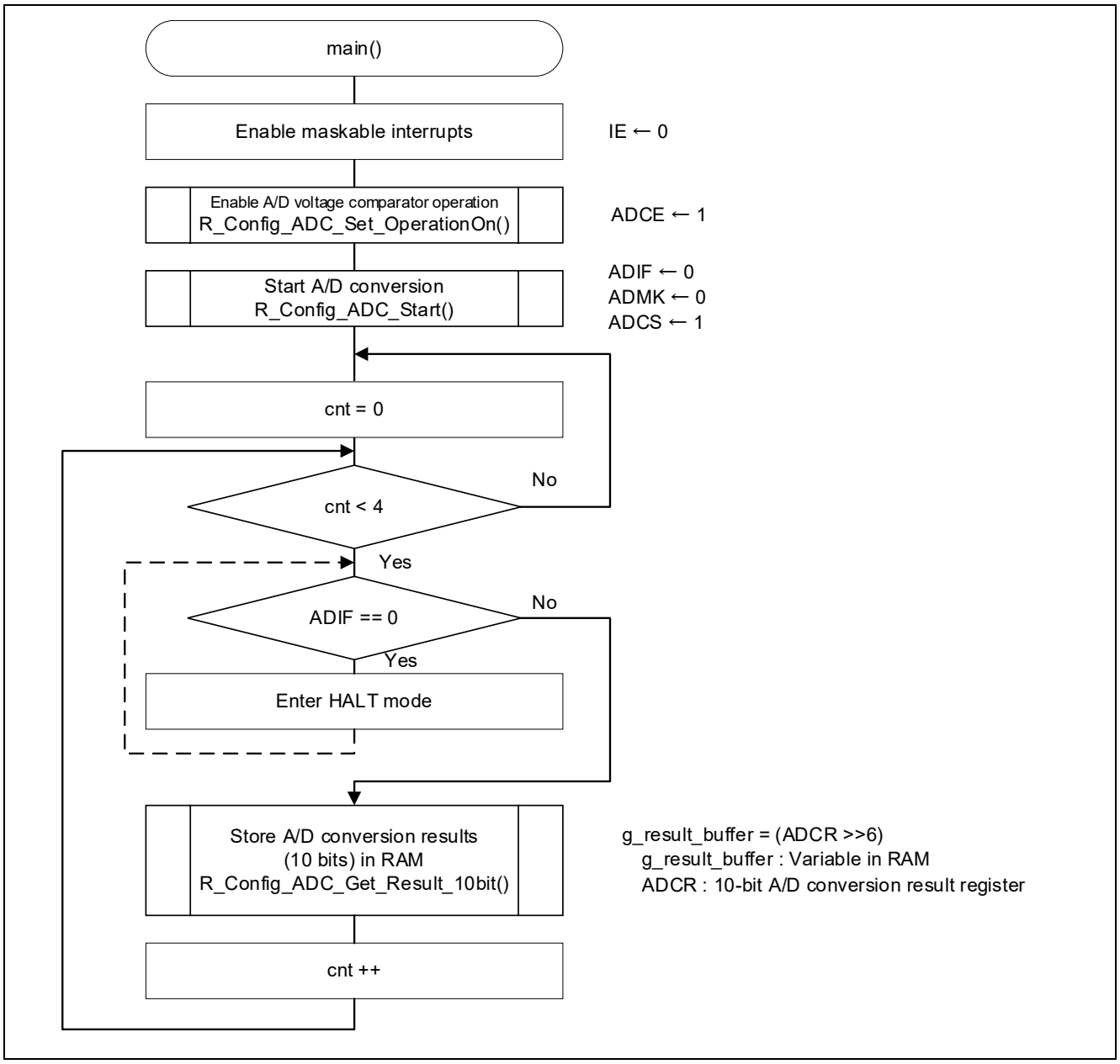
Type	Variable Name	Description	Function Used
unsigned short	g_result_buffer	A/D conversion result storage area	main()

4.3 Flowchart

4.3.1 Main Processing Function

Figure 4-1shows the flowchart of the main processing.

Figure 4-1 Main Processing Function



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G22 User's Manual: Hardware (R01UH0896J)
RL78 family user's manual software (R01US0015J)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.02. 20	-	First Edition
1.01	2023.08. 04	5	Operation Confirmation Conditions update

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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