RL78/G1H, RAA604S00

Electrical Characteristics of 915-MHz-Band +30dBm RF Transceiver (FCC Part 15.247)

Introduction

This document shows the measurement results with RF transceiver (RL78/G1H+front-end module) at 915MHz band.
The front-end module consists of SW(switch), PA(power amplifier) and LNA(low noise amplifier).
The target regulation is "FCC Part 15.247" and the frequency band is 902MHz to 928MHz.

Although this document describes the RL78/G1H, the same system configuration is possible for the RAA604S00.

Note: The contents of this document are provided as an example for reference and do not guarantee the signal quality in systems. When implementing this example into an existing system, thoroughly evaluate the product in the overall system and apply the contents of this document at your own responsibility.

Target Device for Operation Check

The data shown in this document is measured with the following microcomputer.

Microcomputer: RL78/G1H Family

Contents

1. System Configuration

Figure 1 shows the system configuration using RL78/G1H and front-end module. Table 1 shows examples of front-end module specifications. The evaluation described in this document uses front-end module.

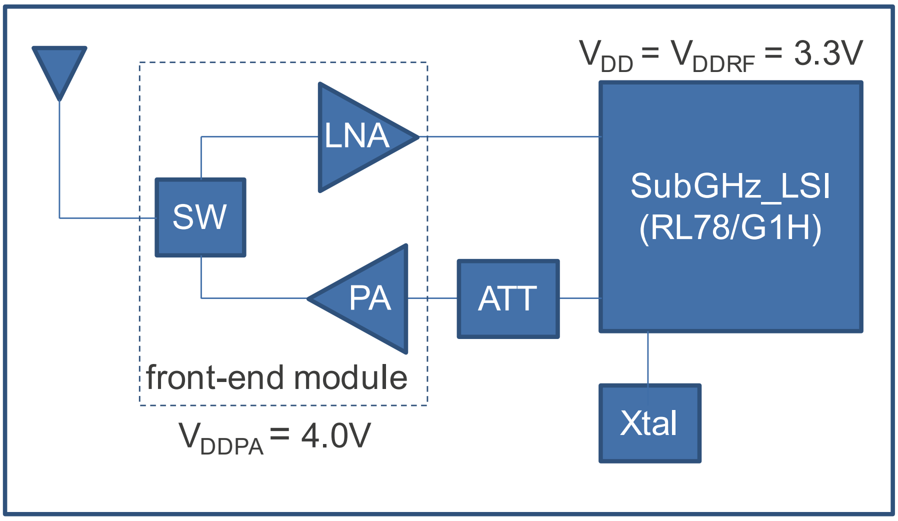


Figure 1 System Configuration

Table 1 Examples of front-end module specifications

Item	Specifications
Frequency	860 - 930 MHz
TX Output Power	+30.5 dBm (typ)
TX Gain	26 dB (min)
RX Gain	16 dB (typ)
RX Noise Figure	2 dB (typ)

2. Electrical Characteristics

2.1 Current Characteristics

Table 2 Current Characteristics (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, Temperature = Room, TX Power = +30 dBm)

Items		RF Frequency [MHz]	Gain Setting	Unit	Evaluation results	Spec
TX Mode	VDDRF (*1)	915.0	90 dec	mA	34.9	-
	VDDPA (*2)			mA	565.6	
	Total (VDDRF + VDDPA)			mA	600.5	
RX Mode	VDDRF (*1)	915.0	-	mA	5.7	-
	VDDPA (*2)			mA	6.2	
	Total (VDDRF + VDDPA)			mA	11.9	
Idle Mode	VDDRF (*1)	915.0	-	mA	1.2	-
	VDDPA (*2)			mA	6.2(*3)	
	Total (VDDRF + VDDPA)			mA	7.4(*3)	

(*1) Current of RF part in G1H. MCU part is not included, (*2) Current of the front-end module,
(*3) It depends on the control method of the front-end module.

2.2 TX Electrical Characteristics

Table 3 TX Electrical Characteristics 1 (V_{DDPA} = 4.0V, V_{DD} = V_{DDRF} = 3.3 V, Temperature = Room)

Items		RF Frequency [MHz]	Gain Setting	Unit	Evaluation results	Spec
TX Power Range	Max	915.0	104 dec	dBm	+30.5	-
	Min		0 dec	dBm	+6.3	-
	variable power range		-	dB	24.2	-
TX Power	@+30dBm	902.2	90 dec	dBm	+30.5	+30.0 (*1)
		915.0			+30.3	
		927.8			+30.2	
Harmonics	2nd	902.2	90 dec	dBm /MHz	-47.3	-
		915.0			-46.6	
		927.8			-42.0	
	3rd	902.2			-44.2	-41.2 (*1)
		915.0			-44.7	
		927.8			-44.6	

(*1) FCC 47 CFR Part15, Subpart C, Section 15.247

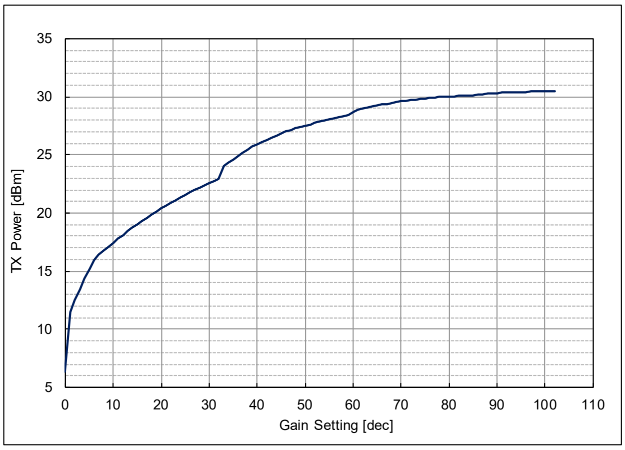


Figure 2 TX Power vs. Gain Setting (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, Temperature = Room, Frequency = 915 MHz)

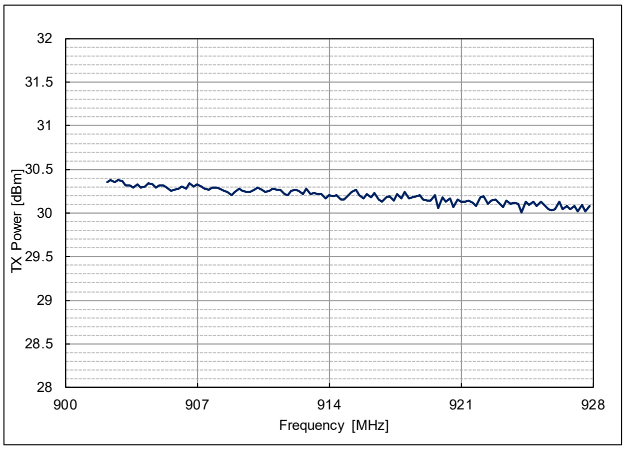


Figure 3 TX Power vs. RF Frequency (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, Temperature = Room, Gain Setting = 90)

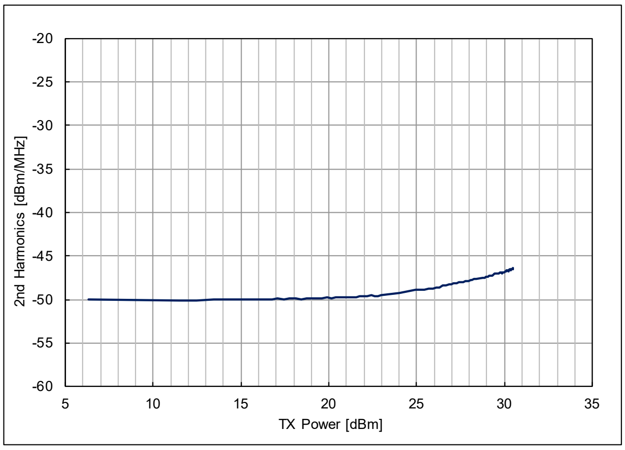


Figure 4 2nd Harmonics vs. TX Power (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, Temperature = Room, Frequency = 915 MHz)

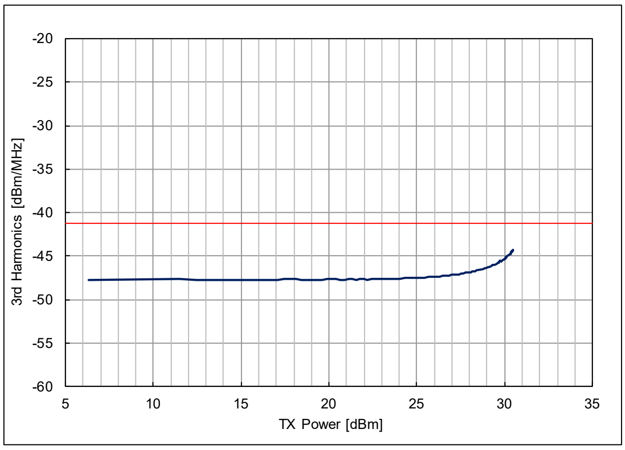


Figure 5 3rd Harmonics vs. TX Power (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, Temperature = Room, Frequency = 915 MHz)

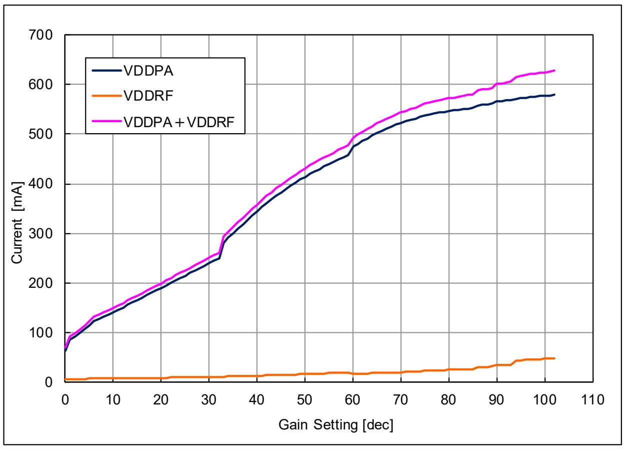


Figure 6 Current of V_{DDPA} and V_{DDRF} for TX mode vs. Gain Setting (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, Temperature = Room, Frequency = 915 MHz)

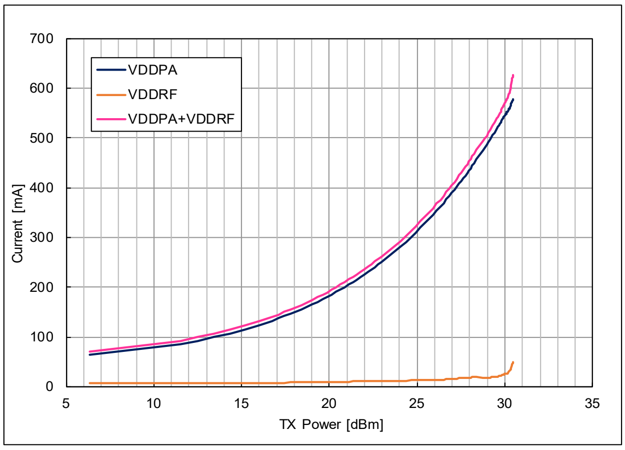


Figure 7 Current of V_{DDPA} and V_{DDRF} for TX mode vs. TX Power (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, Temperature = Room, Frequency = 915 MHz)

Table 4 TX Electrical Characteristics 2 (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, modulation index = 1, Temperature = Room, TX Power = +30 dBm)

Items	RF Frequency [MHz]	Gain Setting	Unit	Evaluation results	Spec
Occupied Bandwidth	902.2	90 dec	kHz	82.9	-
	915.0			82.5	
	927.8			82.5	
6dB Bandwidth (Digital modulation systems)	902.2	90 dec	kHz	51.6	-
	915.0			51.4	
	927.8			51.4	
20dB Bandwidth (Frequency hopping systems)	915.0	90 dec	kHz	103	250 (*1)
Adjacent Channel Power Ratio (M1_Lower, 150 kHz offset) (*2)	902.2	90 dec	dBc	-55.4	-25 (*4)
	915.0			-53.9	
	927.8			-54.3	
Adjacent Channel Power Ratio (M1_Upper, 150 kHz offset) (*2)	902.2			-55.8	-25 (*4)
	915.0			-55.2	
	927.8			-54.5	
Adjacent Channel Power Ratio (M2_Lower, 300 kHz offset) (*2)	902.2	90 dec	dBc	-64.0	-35 (*4)
	915.0			-62.7	
	927.8			-60.9	
Adjacent Channel Power Ratio (M2_Upper, 300 kHz offset) (*2)	902.2			-63.3	-35 (*4)
	915.0			-63.6	
	927.8			-61.7	
Deviation Offset	902.2	90 dec	% rms	3.02	30 (*3)
	915.0			3.00	
	927.8			3.01	
Zero Crossing Error	902.2	90 dec	% pk	-1.55	±12.5 (*3)
	915.0			-1.65	
	927.8			1.58	
Frequency tolerance (*5)	915.0	90 dec	ppm	0.59	±20 (*3)

(*1) FCC 47 CFR Part15, Subpart C, Section 15.247
(*2) IEEE.802.15.4g
M1: 1.5*R*(h+1), M2: 3*R*(h+1), R(symbol rate): 50kbps, h(modulation index): 1
(*3) Wi-SUN, (*4) IEEE.802.15.4g
(*5) This characteristic depends on the temperature variation of a crystal resonator.

Table 5 TX Electrical Characteristics 3 (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, modulation index = 1, Temperature = Room, TX Power = +30 dBm)

Items		RF Frequency [MHz]	Gain Setting	Unit	Evaluation results	Spec
Unwanted emissions	30 kHz-88 MHz	902.2	90 dec	dBm /100 kHz	-63.4	-55.2 (*1)
		915.0			-63.0	
		927.8			-63.3	
	88 MHz-216 MHz	902.2		dBm /100 kHz	-59.8	-51,7 (*1)
		915.0			-59.4	
		927.8			-59.4	
	216 MHz-614 MHz	902.2		dBm /100 kHz	-55.3	-49.2 (*1)
		915.0			-55.8	
		927.8			-54.8	
	960 MHz-1722.2 MHz	902.2		dBm / MHz	-45.2	-41.2 (*1)
		915.0			-45.8	
		927.8			-45.2	
	2200 MHz-5460 MHz	902.2		dBm / MHz	-44.2	-41.2 (*1)
		915.0			-44.4	
		927.8			-44.3	
	7250 MHz-9200 MHz	902.2		dBm / MHz	-47.9	-41.2 (*1)
		915.0			-51.1	
		927.8			-56.8	
Tx out of band emission (Band edge)	LOWER 870-902MHz	902.2	90 dec	dBc	-44.3	-20 (*2)
		915.0			-68.3	
		927.8			-68.1	
	UPPER 928-960MHz	902.2		dBc	-68.8	-20 (*2)
		915.0			-68.6	
		927.8			-44.7	

(*1) In the FCC standard, spurious emissions are specified by electric field intensity (V / m). Since this document is the result of the wired condition, the value converted to the power value (dBm) is used.
Power(dBm)@3m = $10*\log(300E^2)$, E = electric field intensity (V / m)

(*2) FCC 47 CFR Part15, Subpart C, Section 15.247

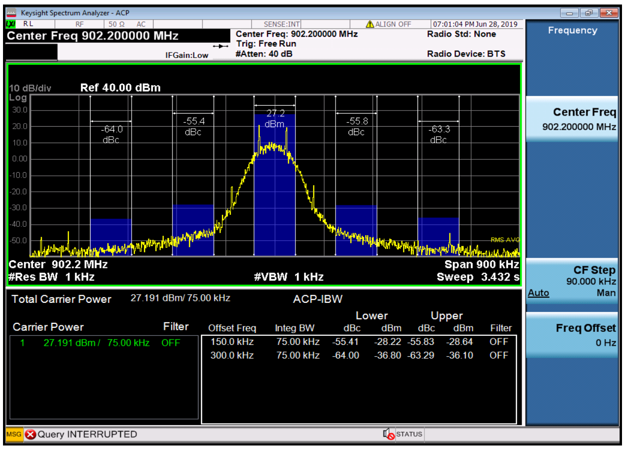


Figure 8 Transmit Spectrum
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, mod index = 1, Frequency = 902.2 MHz, Gain Setting = 90, Temperature = Room)

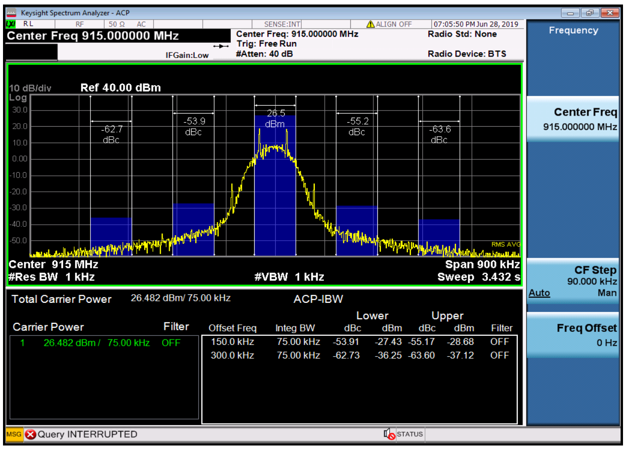


Figure 9 Transmit Spectrum
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, mod index = 1, Frequency = 915.0 MHz, Gain Setting = 90, Temperature = Room)

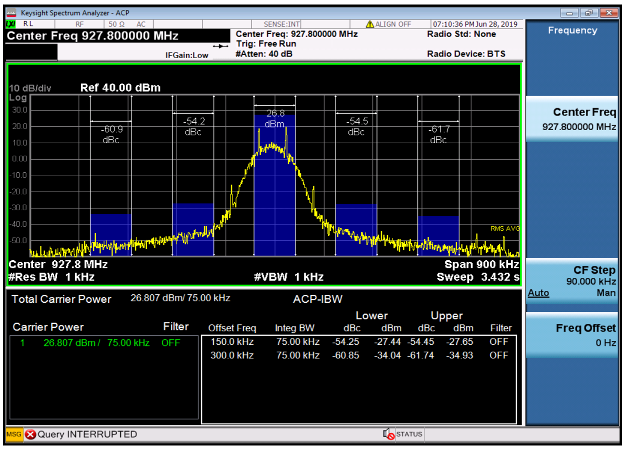


Figure 10 Transmit Spectrum
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, mod index = 1, Frequency = 927.8 MHz, Gain Setting = 90, Temperature = Room)

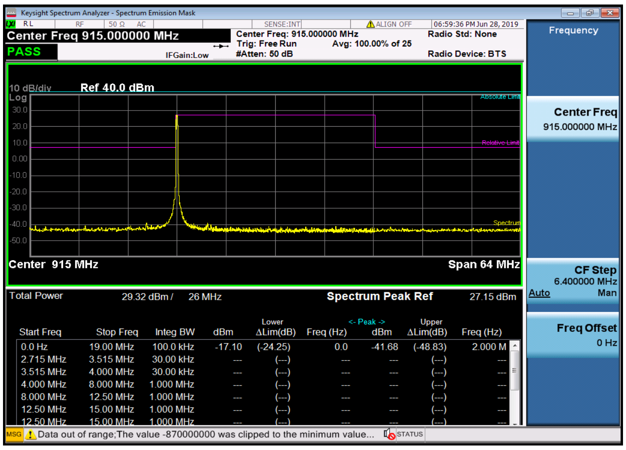


Figure 11 TX Out Of Band Emissions for Operational Frequency Band
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, mod index = 1, Frequency = 902.2 MHz, Gain Setting = 90, Temperature = Room)

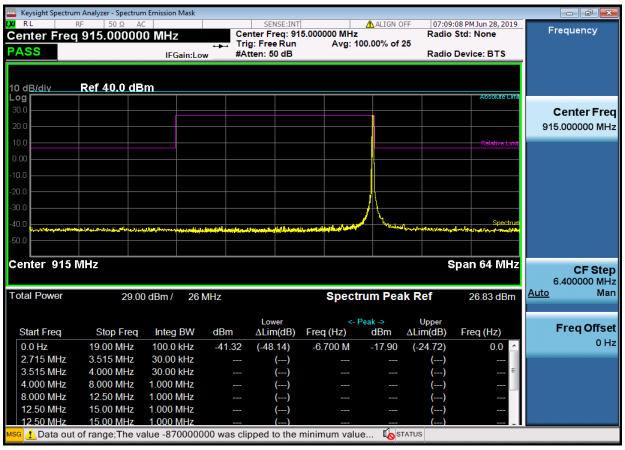


Figure 12 TX Out Of Band Emissions for Operational Frequency Band
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, mod index = 1, Frequency = 927.8 MHz, Gain Setting = 90, Temperature = Room)

Figure 13 TX Spurious emission
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, mod index = 1, Frequency = 915.0 MHz, Gain Setting = 90, Temperature = Room)

Table 6 TX Electrical Characteristics 4 (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, modulation index = 0.5, Temperature = Room, TX Power = +30 dBm)

Items	RF Frequency [MHz]	Gain Setting	Unit	Evaluation results	Spec
Occupied Bandwidth	902.4	90 dec	kHz	158.6	-
	915.2			158.5	
	927.6			159.1	
6dB Bandwidth (Digital modulation systems)	902.4	90 dec	kHz	102.7	-
	915.2			102.5	
	927.6			102.4	
20dB Bandwidth (Frequency hopping systems)	915.0	90 dec	kHz	185	250 (*1)
Adjacent Channel Power Ratio (M1_Lower, 337.5 kHz offset) (*2)	902.4	90 dec	dBc	-53.9	-20 (*4)
	915.2			-54.0	
	927.6			-53.7	
Adjacent Channel Power Ratio (M1_Upper, 337.5 kHz offset) (*2)	902.4			-54.3	-20 (*4)
	915.2			-54.7	
	927.6			-54.1	
Adjacent Channel Power Ratio (M2_Lower, 675 kHz offset) (*2)	902.4	90 dec	dBc	-61.4	-35 (*4)
	915.2			-61.4	
	927.6			-61.1	
Adjacent Channel Power Ratio (M2_Upper, 675 kHz offset) (*2)	902.4			-61.7	-35 (*4)
	915.2			-61.8	
	927.6			-61.0	
Deviation Offset	902.4	90 dec	% rms	3.71	±30 (*3)
	915.2			3.68	
	927.6			3.64	
Zero Crossing Error	902.4	90 dec	% pk	1.86	±12.5 (*3)
	915.2			-2.31	
	927.6			-2.60	
Frequency tolerance (*5)	915.2	90 dec	ppm	0.59	±20 (*3)

(*1) FCC 47 CFR Part15, Subpart C, Section 15.247
(*2) IEEE.802.15.4g
M1: 1.5*R*(h+1), M2: 3*R*(h+1), R(symbol rate): 150kbps, h(modulation index):0.5
(*3) Wi-SUN, (*4) IEEE.802.15.4g
(*5) This characteristic depends on the temperature variation of a crystal resonator.

Table 7 TX Electrical Characteristics 5 (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, modulation index = 0.5, Temperature = Room, TX Power = +30 dBm)

Items		RF Frequency [MHz]	Gain Setting	Unit	Evaluation results	Spec
Unwanted emissions	30 kHz-88 MHz	902.4	90 dec	dBm /100 kHz	-62.9	-55.2 (*1)
		915.2			-63.0	
		927.6			-63.6	
	88 MHz-216 MHz	902.4		dBm /100 kHz	-58.0	-51,7 (*1)
		915.2			-60.1	
		927.6			-59.0	
	216 MHz-614 MHz	902.4		dBm /100 kHz	-56.0	-49.2 (*1)
		915.2			-56.6	
		927.6			-54.9	
	960 MHz-1722.2 MHz	902.4		dBm / MHz	-45.5	-41.2 (*1)
		915.2			-45.7	
		927.6			-46.3	
	2200 MHz-5460 MHz	902.4		dBm / MHz	-44.1	-41.2 (*1)
		915.2			-44.4	
		927.6			-44.3	
	7250 MHz-9200 MHz	902.4		dBm / MHz	-58.4	-41.2 (*1)
		915.2			-50.9	
		927.6			-56.6	
Tx out of band emission (Band edge)	LOWER 870-902MHz	902.4	90 dec	dBc	-48.7	-20 (*2)
		915.2			-68.0	
		927.6			-67.8	
	UPPER 928-960MHz	902.4		dBc	-68.6	-20 (*2)
		915.2			-68.2	
		927.6			-48.6	

(*1) In the FCC standard, spurious emissions are specified by electric field intensity (V / m). Since this document is the result of the wired condition, the value converted to the power value (dBm) is used.
Power(dBm)@3m = $10*\log(300E^2)$, E = electric field intensity (V / m)

(*2) FCC 47 CFR Part15, Subpart C, Section 15.247

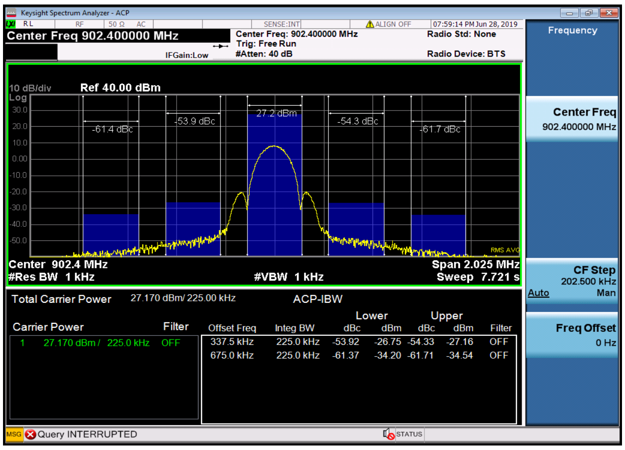


Figure 14 Transmit Spectrum
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, mod index = 0.5, Frequency = 902.4 MHz, Gain Setting = 90, Temperature = Room)

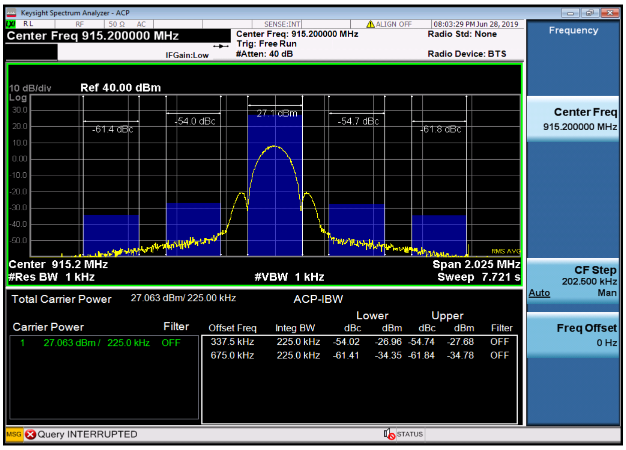


Figure 15 Transmit Spectrum
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, mod index = 0.5, Frequency = 915.2 MHz, Gain Setting = 90, Temperature = Room)

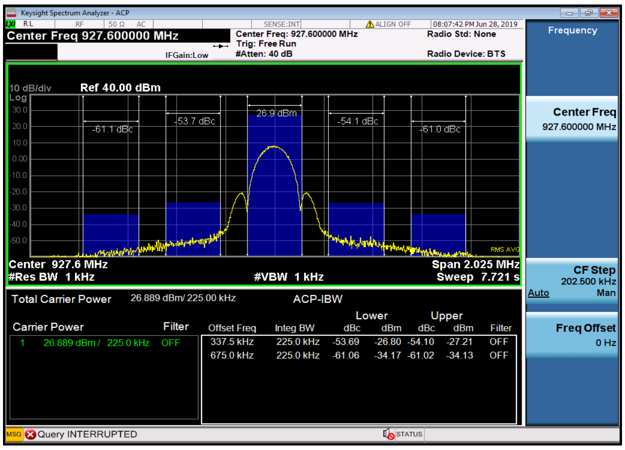


Figure 16 Transmit Spectrum
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, mod index = 0.5, Frequency = 927.6 MHz, Gain Setting = 90, Temperature = Room)

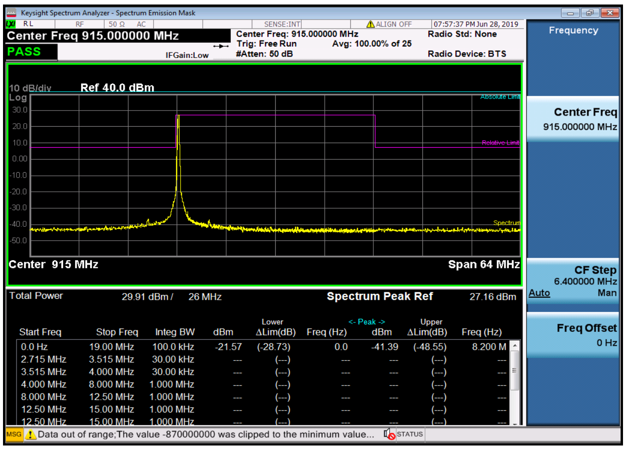


Figure 17 TX Out Of Band Emissions for Operational Frequency Band
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, mod index = 0.5, Frequency = 902.4 MHz, Gain Setting = 90, Temperature = Room)

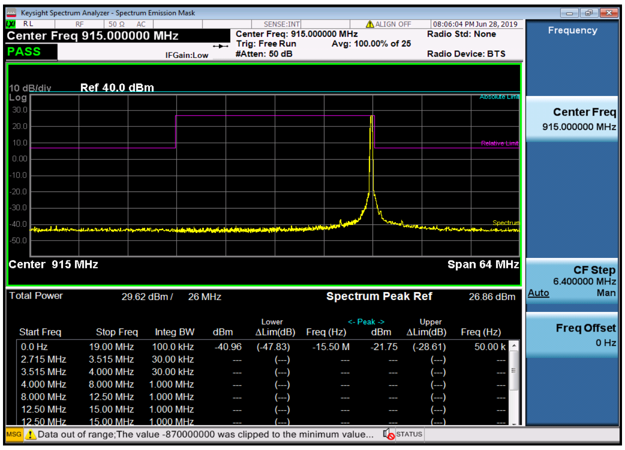


Figure 18 TX Out Of Band Emissions for Operational Frequency Band
(V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, mod index = 0.5, Frequency = 927.6 MHz, Gain Setting = 90, Temperature = Room)

2.3 RX Electrical Characteristics

Table 8 RX Electrical Characteristics (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, modulation index = 1, Temperature = Room)

Items			RF Frequency [MHz]	Unit	Evaluation results	Spec
Receiver sensitivity	PER < 1 % PSDU Length 20 octets		902.2	dBm	-109	-91 (*1)
			915.0		-109	
			927.8		-109	
	BER < 0.1 %		902.2	dBm	-112	-
			915.0		-112	
			927.8		-112	
Maximum Input level	PER < 1 % PSDU Length 20 octets		902.2	dBm	> -10	-
			915.0		> -10	
			927.8		> -10	
	BER < 0.1 %		902.2	dBm	> -10	-
			915.0		> -10	
			927.8		> -10	
Frequency tolerance	PER < 1 % PSDU Length 20 octets	Max	915.0	ppm	+82	±61 (*1)
		Min			-78	
Adjacent channel rejection	-200 kHz	BER < 0.1 % (*3)	915.0	dB	50	-
	+200 kHz				51	
	-200 kHz	PER < 10 % (*4) Length 250 octets			36	10 (*2)
	+200 kHz				36	
Alternate channel rejection	-400 kHz	BER < 0.1 % (*3)	915.0	dB	51	-
	+400 kHz				52	
	-400 kHz	PER < 10 % (*4) Length 250 octets			48	30 (*2)
	+400 kHz				48	
Blocking	-2 MHz	BER < 0.1 % (*3)	915.0	dB	50	-
	+2 MHz				51	
	-10 MHz				63	-
	+10 MHz				63	
	-60 MHz				67	-
	+60 MHz				65	
Image rejection	-1.0 MHz		915.0	dB	27	-
Spurious emission	9 kHz - 1 GHz		902.2	dBm /100 kHz	-82.2	-
			915.0		-82.0	
			927.8		-82.1	
	1 GHz - 6 GHz		902.2	dBm /1 MHz	-68.6	-
			915.0		-68.5	
			927.8		-68.7	

(*1) IEEE.802.15.4g, (*2) Wi-SUN
(*3) The level of the desired signal: DUT sensitivity +3 dB
(*4) The level of the desired signal: -88 dBm

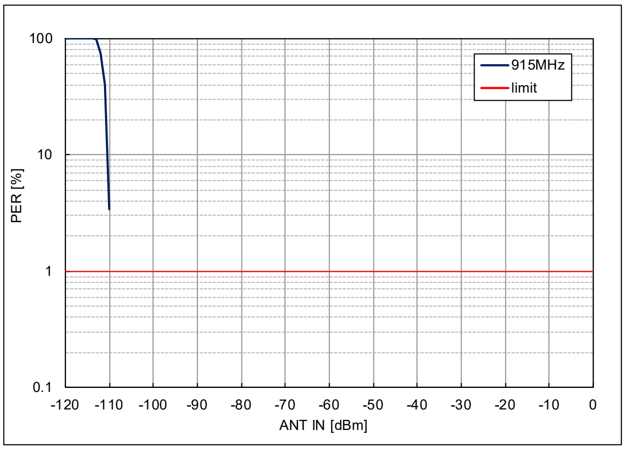


Figure 19 Packet Error Rate vs. RF Input Level (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, RF Frequency = 915 MHz, RF Input Level = -120 dBm to -3 dBm, Data Length = 20 B, mod index = 1, Temperature = Room)

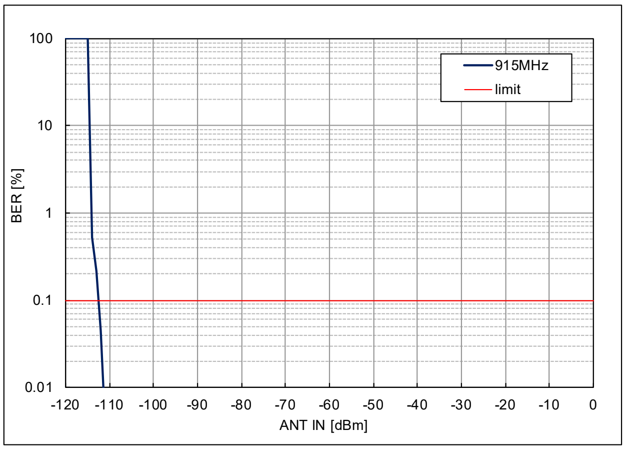


Figure 20 Bit Error Rate vs. RF Input Level (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, RF Frequency = 915 MHz, RF Input Level = -120 dBm to -3 dBm, Data Length = 20 B, mod index = 1, Temperature = Room)

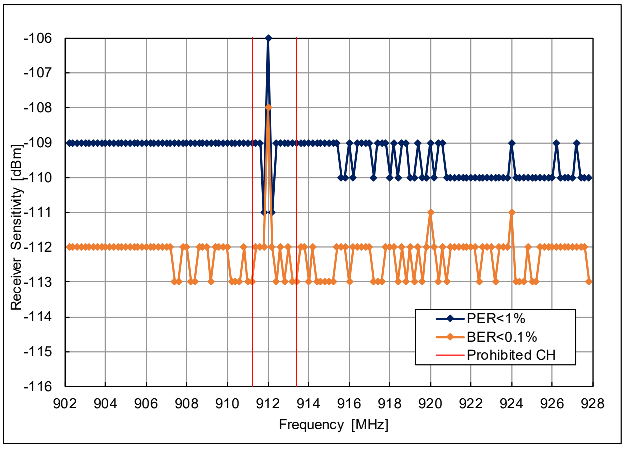


Figure 21 Receiver Sensitivity vs. RF Frequency (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, Data Length = 20 B, mod index = 1, Temperature = Room)

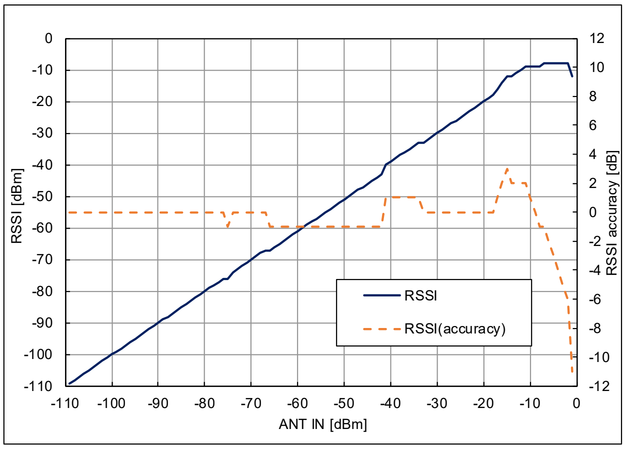


Figure 22 RSSI Accuracy vs. RF Input Level (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, RF Frequency = 915 MHz, mod index = 1, Temperature = Room) This RSSI value includes LNA gain correction (17dB).

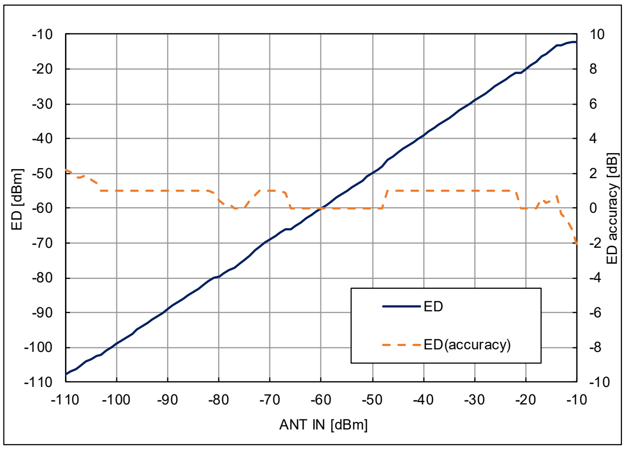


Figure 23 ED Accuracy vs. RF Input Level (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, RF Frequency = 915 MHz, mod index = 1, Temperature = Room) This ED value includes LNA gain correction (17dB).

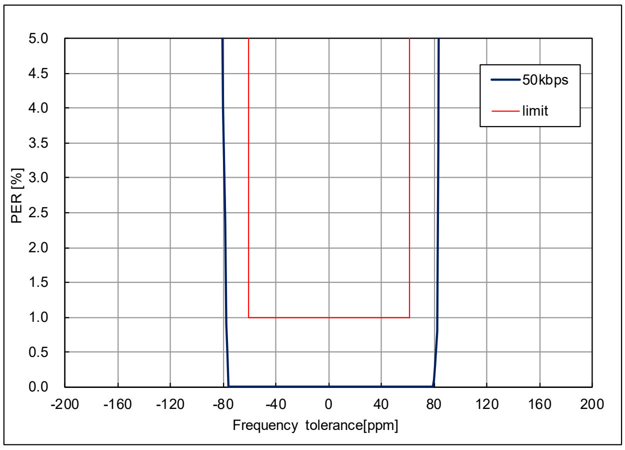


Figure 24 Packet Error Rate vs. RF Frequency tolerance (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, RF Frequency = 915 MHz, RF Input Level = DUT sensitivity +3 dB, Data Length = 20 B, mod index = 1, Temperature = Room)

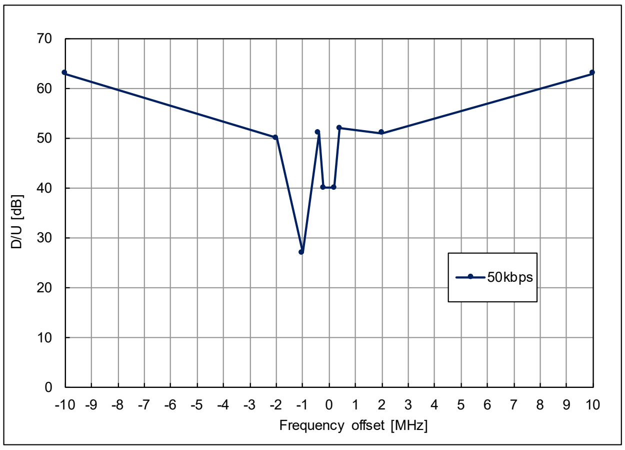


Figure 25 Desire/Unwanted Signal Ratio vs. RF Frequency offset (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 50kbps, RF Frequency = 915 MHz, RF Input Level = DUT sensitivity +3 dB, mod index = 1, Temperature = Room)

Table 9 RX Electrical Characteristics (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, modulation index = 0.5, Temperature = Room)

Items			RF Frequency [MHz]	Unit	Evaluation results	Spec
Receiver sensitivity	PER < 1 % PSDU Length 20 octets		902.4	dBm	-104	-86 (*1)
			915.2		-104	
			927.6		-104	
	BER < 0.1 %		902.4	dBm	-106	-
			915.2		-107	
			927.6		-107	
Maximum Input level	PER < 1 % PSDU Length 20 octets		902.4	dBm	> -10	-
			915.2		> -10	
			927.6		> -10	
	BER < 0.1 %		902.4	dBm	> -10	-
			915.2		> -10	
			927.6		> -10	
Frequency tolerance	PER < 1 % PSDU Length 20 octets	Max	915.2	ppm	+112	±91.2 (*1)
		Min			-118	
Adjacent channel rejection	-400 kHz	BER < 0.1 % (*3)	915.2	dB	36	-
	+400 kHz				38	
	-400 kHz	PER < 10 % (*4) Length 250 octets			34	10 (*2)
	+400 kHz				36	
Alternate channel rejection	-800 kHz	BER < 0.1 % (*3)	915.2	dB	53	-
	+800 kHz				54	
	-800 kHz	PER < 10 % (*4) Length 250 octets			36	30 (*2)
	+800 kHz				38	
Blocking	-2 MHz	BER < 0.1 % (*3)	915.2	dB	59	-
	+2 MHz				58	
	-10 MHz				59	-
	+10 MHz				58	
	-60 MHz				62	-
	+60 MHz				61	
Image rejection	-1.0 MHz		915.2	dB	31	-
Spurious emission	9 kHz - 1 GHz		902.4	dBm /100 kHz	-82.0	-
			915.2		-82.3	
			927.6		-82.3	
	1 GHz - 6 GHz		902.4	dBm /1 MHz	-68.1	-
			915.2		-68.8	
			927.6		-68.5	

(*1) IEEE.802.15.4g, (*2) Wi-SUN
(*3) The level of the desired signal: DUT sensitivity +3 dB
(*4) The level of the desired signal: -83 dBm

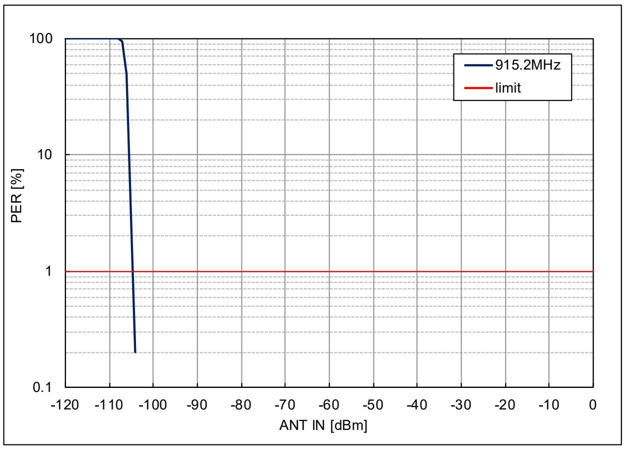


Figure 26 Packet Error Rate vs. RF Input Level (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, RF Frequency = 915.2 MHz, RF Input Level = -120 dBm to -3 dBm, Data Length = 20 B, mod index = 0.5, Temperature = Room)

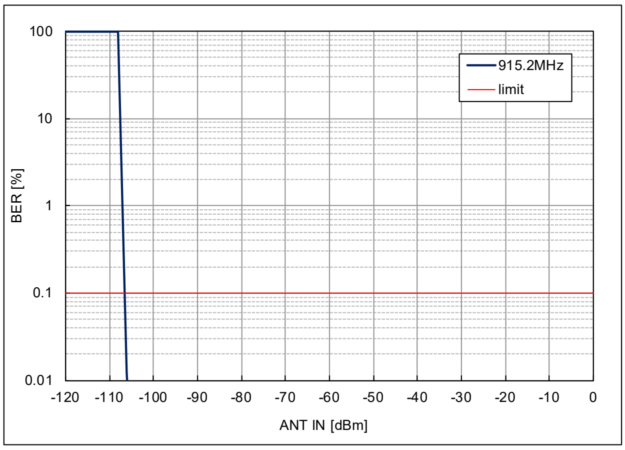


Figure 27 Bit Error Rate vs. RF Input Level (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, RF Frequency = 915.2 MHz, RF Input Level = -120 dBm to -3 dBm, Data Length = 20 B, mod index = 0.5, Temperature = Room)

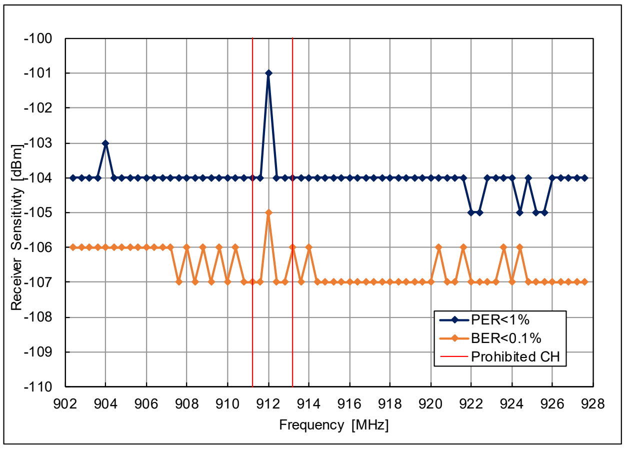


Figure 28 Receiver Sensitivity vs. RF Frequency (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, Data Length = 20 B, mod index = 0.5, Temperature = Room)

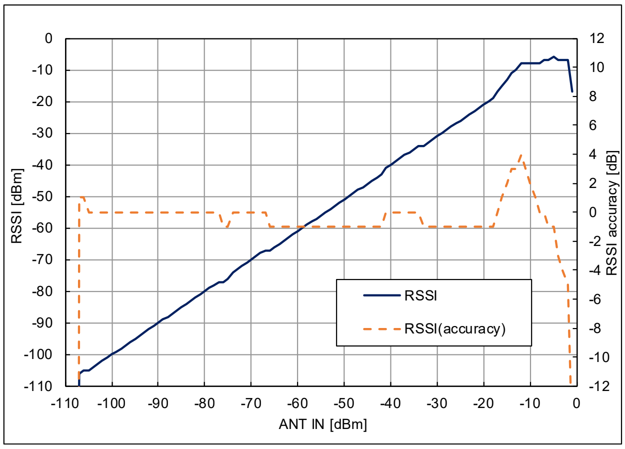


Figure 29 RSSI Accuracy vs. RF Input Level (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, RF Frequency = 915.2 MHz, mod index = 0.5, Temperature = Room) This RSSI value includes LNA gain correction (17dB).

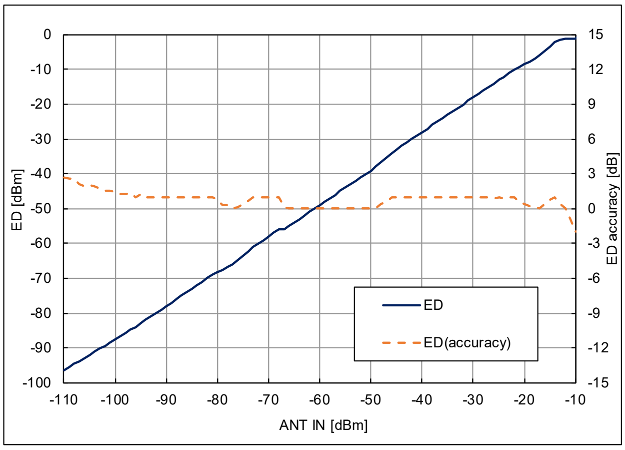


Figure 30 ED Accuracy vs. RF Input Level (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, RF Frequency = 915.2 MHz, mod index = 0.5, Temperature = Room) This ED value includes LNA gain correction (17dB).

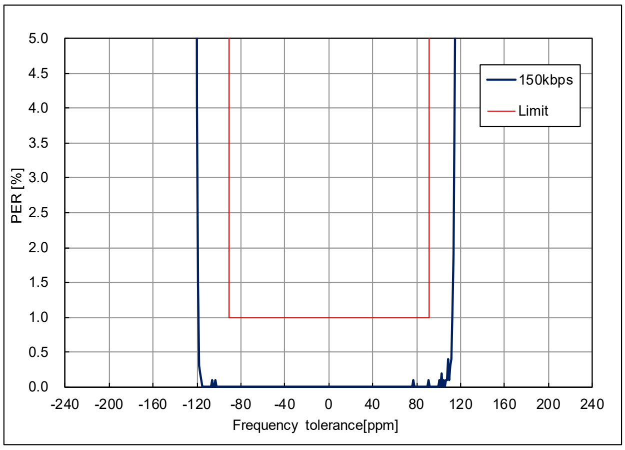


Figure 31 Packet Error Rate vs. RF Frequency tolerance (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, RF Frequency = 915.2 MHz, RF Input Level = DUT sensitivity +3 dB, Data Length = 20 B, mod index = 0.5, Temperature = Room)

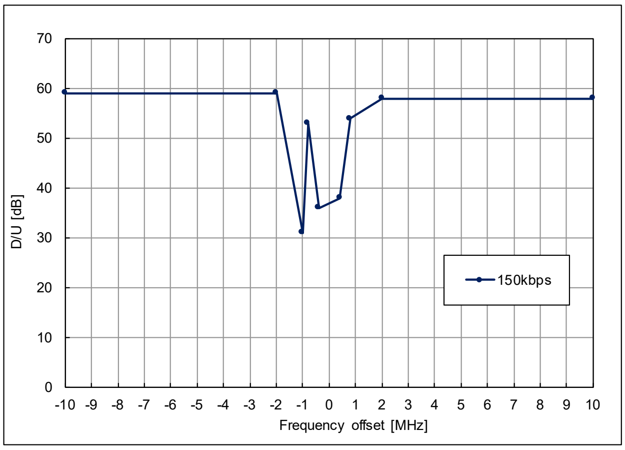


Figure 32 Desire/Unwanted Signal Ratio vs. RF Frequency offset (V_{DDPA} = 4.0 V, V_{DD} = V_{DDRF} = 3.3 V, 150kbps, RF Frequency = 915.2 MHz, RF Input Level = DUT sensitivity +3 dB, mod index = 0.5, Temperature = Room)

3. Characteristics of FHSS operation

This chapter describes typical characteristics of FHSS operation.

The signal conditions used for measurement are shown below.

Preamble=8byte, Data Length=20byte, Transmit Interval=2ms, Channel switching=random

Table 10 Characteristics of FHSS operation

Items		Unit	Result	Spec
20dB Bandwidth	50kbps	kHz	103	< 250
	150kbps		185	
Carrier Frequency Separation	50kbps	kHz	200	≧ 20dB Bandwidth
	150kbps		400	
Number of Hopping Frequencies	50kbps	ch	129	≧ 50
	150kbps		64	
Average Time of Occupancy	50kbps	ms	116	≦ 400 @ 20s
	150kbps		123	

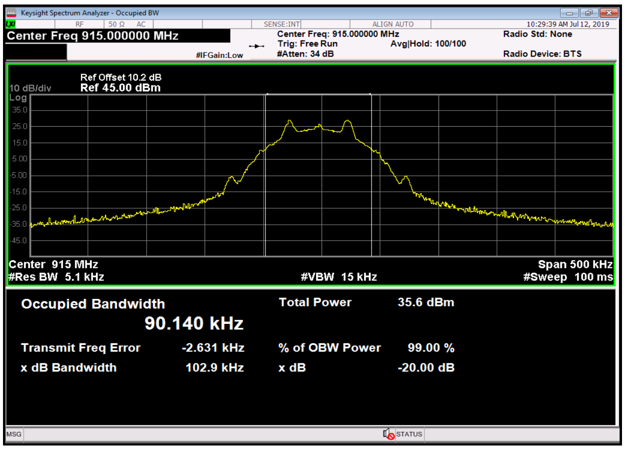


Figure 33 20dB Bandwidth (50kbps)

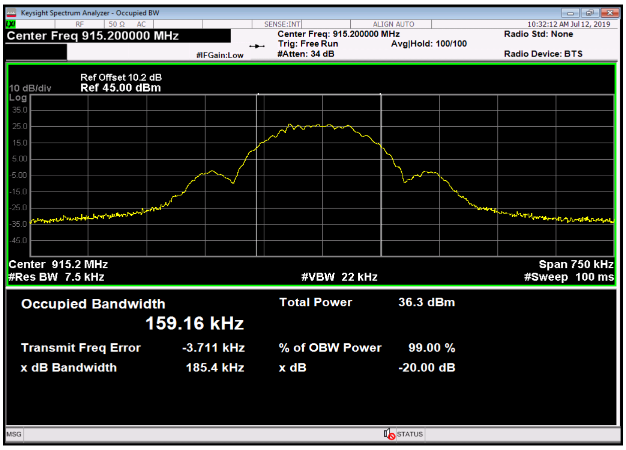


Figure 34 20dB Bandwidth (150kbps)

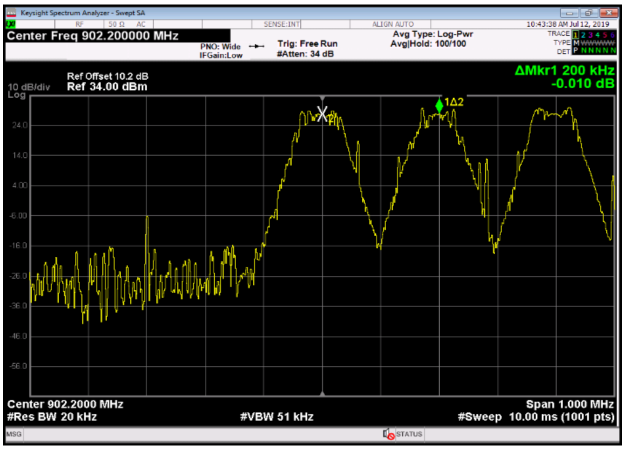


Figure 35 Carrier Frequency Separation (50kbps)

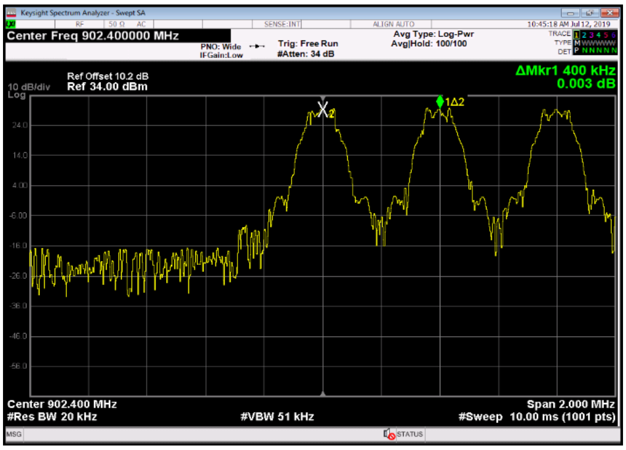


Figure 36 Carrier Frequency Separation (150kbps)

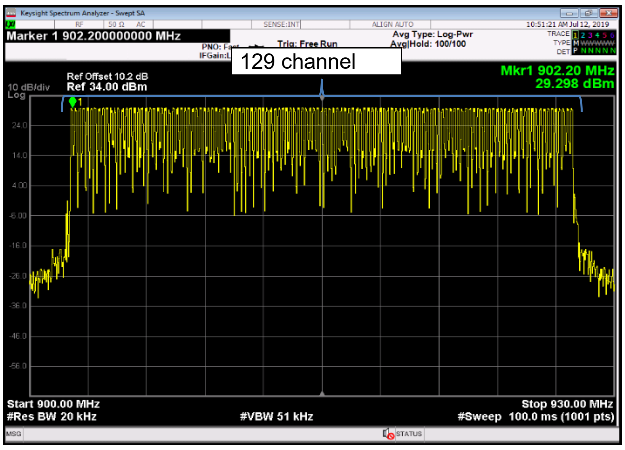


Figure 37 Number of Hopping Frequency (50kbps)

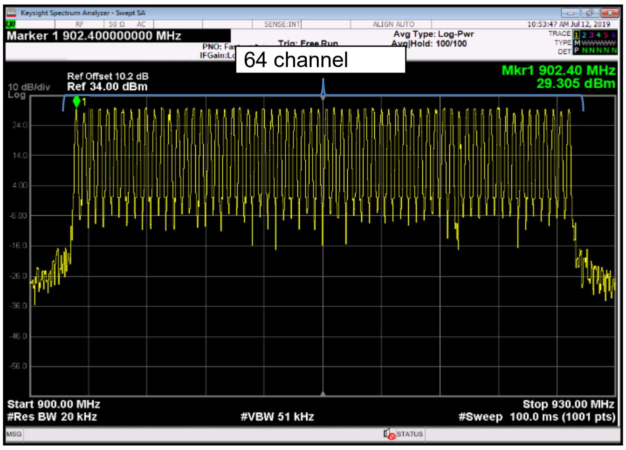


Figure 38 Number of Hopping Frequency (150kbps)

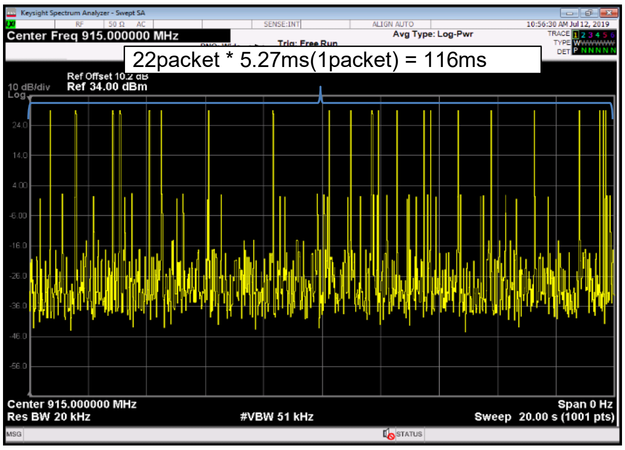


Figure 39 Average Time of Occupancy (50kbps)

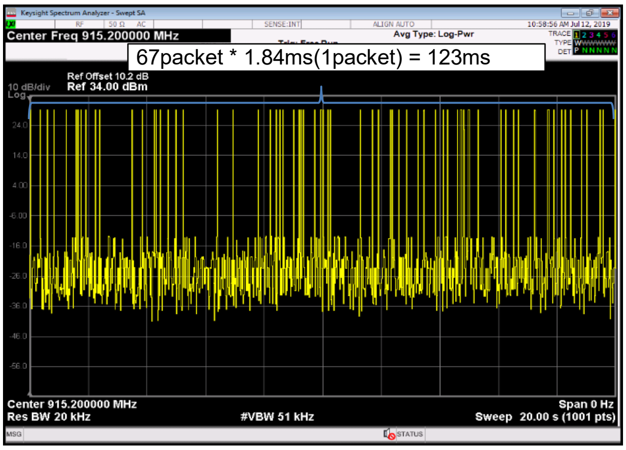
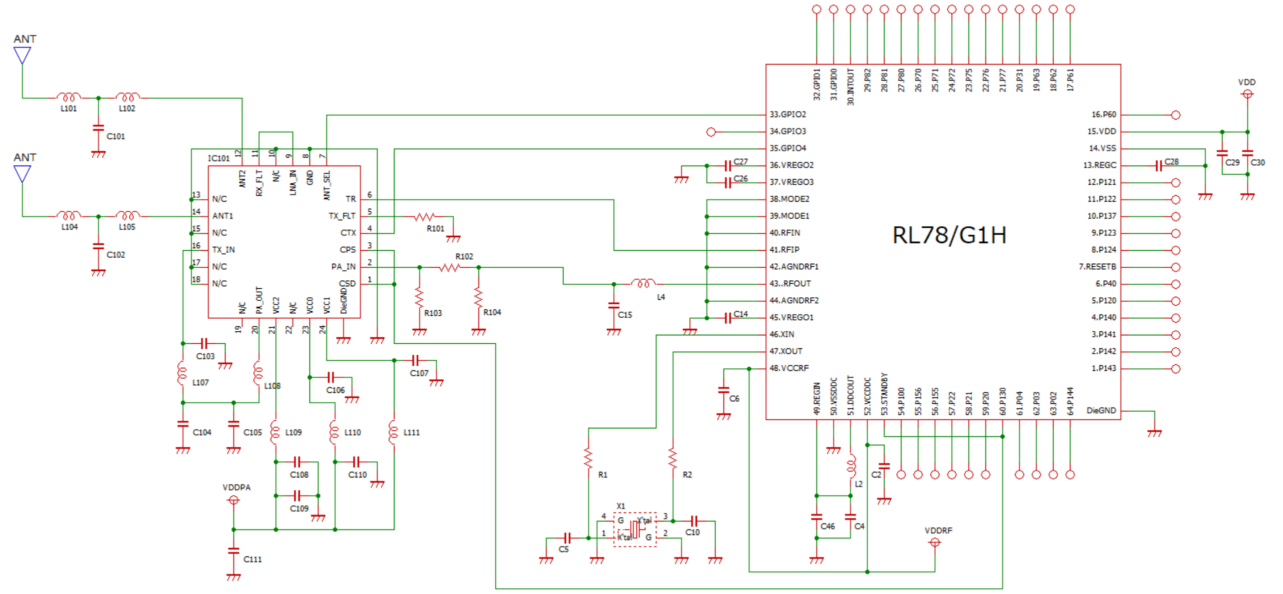


Figure 40 Average Time of Occupancy (150kbps)

4. Example of Peripheral Circuit



V_{DD} : Current of MCU part (15pin)

V_{DDRF} : Current of RF part (48pin + 52pin)

V_{DDPA} : Current of External PA / LNA

Figure 41 Example of Peripheral Circuit

Table 11 BOM Lists

Part	Description	Parts number	Part	Description	Parts number
C2	1 uF	GRM155B31C105KA12D	C109	1000 pF	GRM1552C1H102JA01
C4	1 uF	GRM155B31C105KA12D	C110	0.01 uF	GRM155B31H103KA88
C5	9 pF (*1)	GRM1552C1H9R0CA01D	C111	4.7 uF	GRM188B30J475KE18
C6	2.2 uF	GRM155R60G225ME15D			
C10	9 pF (*1)	GRM1552C1H9R0CA01D	L2	10 uH	MLZ1608M100WT
C14	1 uF	GRM155B31C105KA12D	L4	4.7 nH	LQW15AN4N7C00
C15	5.6 pF	GRM1552C1H5R6CA01D	L101	6.8 nH	MLG1005S6N8J
C26	1 uF	GRM155B31C105KA12D	L102	6.8 nH	MLG1005S6N8J
C27	1 uF	GRM155B31C105KA12D	L104	6.8 nH	MLG1005S6N8J
C28	1 uF	GRM155B31C105KA12D	L105	6.8 nH	MLG1005S6N8J
C29	1 uF	GRM155B31C105KA12D	L107	5.6 nH	MLG1005S5N6S
C30	Not mounted		L108	1.3 nH	MLG1005S1N3S
C46	47 pF	C1005CH1H470J	L109	6.8 nH	MLG1005S6N8J
C101	3.3 pF	GJM1555C1H3R3BB01	L110	4.7 nH	MLG1005S4N7S
C102	3.3 pF	GJM1555C1H3R3BB01	L111	3.3 nH	MLG1005S3N3S
C103	2.4 pF	GJM1555C1H2R4BB01			
C104	1.8 pF	GJM1555C1H1R8BB01	R1	SHORT	
C105	8.2 pF	GJM1555C1H8R2CB01	R2	SHORT	
C106	22 pF	GRM1552C1H220JZ01	R101	51 Ω	RK73H1ET51R0F
C107	100 pF	GRM1552C1H101JA01	R102	36 Ω	RK73H1ET36R0F
C108	33 pF	GRM1552C1H330JZ01	R103	150 Ω	RK73H1ET1500F

Part	Description	Parts number	Part	Description	Parts number
R104	150 Ω	RK73H1ET1500F	X1	Crystal resonator 48 MHz	XRCMD48M000FXQ60R0
IC101	Front-end module (SW+PA+LNA)	SE2435L			

(*1) This provides a load capacitance for the crystal resonator and its value depends on the parasitic capacitance of the combination of the crystal resonator and the board on which it is mounted.

5. Appendix

The typical characteristics described in this document are results of wired condition.
In the FCC certification test, spurious emissions are measured using an antenna.

Therefore, it is necessary to be aware that even though the spurious characteristics are satisfied with the wired condition, the characteristics can not be satisfied by the wireless condition.

In RL78/G1H and RAA604S00, a low-pass filter is configured with an external matching circuit to attenuate harmonics of transmission.
However, the place where the radio wave is radiated is not limited to the antenna, it may be radiated from the board pattern or the LSI itself.
Especially, the higher order harmonics become easier to radiate from the board pattern because the wavelength is short.

When spurious emissions are a problem in the wireless condition using the antenna, it is recommended to shield the RF circuit with metal case to suppress radiation from other than the antenna.

When shielding the RF circuit, connect the outer periphery of the metal case to the board GND as much as possible.
It is necessary to connect the outer periphery of the metal case to the board GND at intervals of at least $\lambda / 2$, and if the distance is large, the shielding effect may not be obtained.
For example, when shielding harmonics of about 10 GHz ($\lambda = 3$ cm), connect the outer periphery of the metal case and board GND at intervals of 1.5 cm or less.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug 21, 2019	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Contact information

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