RL78/G1E Group

Low-Power Control of Analog Block (Intermittent Operation)

R01AN1128EJ0110
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Introduction

This application note describes how to apply the low-power control for the sensor measurement by using the stanby function (HALT mode) of the microcontroller block and the power-off function of the analog block incorporated in the RL78/G1E (R5F10FMx).

Operation Verified Devices

RL78/G1E (R5F10FMx (x = C, D, or E))

When this application note is applied to other microcontrollers, make the necessary changes according to the specifications of the microcontroller and verify them thoroughly.

Contents

1. Specifications

This application note describes the example of the low-power control introducing the intermittent operation to the sensor measurement with the RL78/G1E (R5F10FMx).

In this application note, using the example of the system to measure the illuminance with the photodiode (BS520E0F made by Sharp Corporation) connected to the RL78/G1E (R5F10FMx), it is explained how to shift the microcontroller block and the analog block incorporated in the RL78/G1E (R5F10FMx) from the normal operation mode to the stanby mode, how to make a comeback to the normal operation mode, and how to use the CPU/peripheral function, the analog peripheral function after a comeback.

Figure 1.1 shows an overview of the control flow used in this application note.

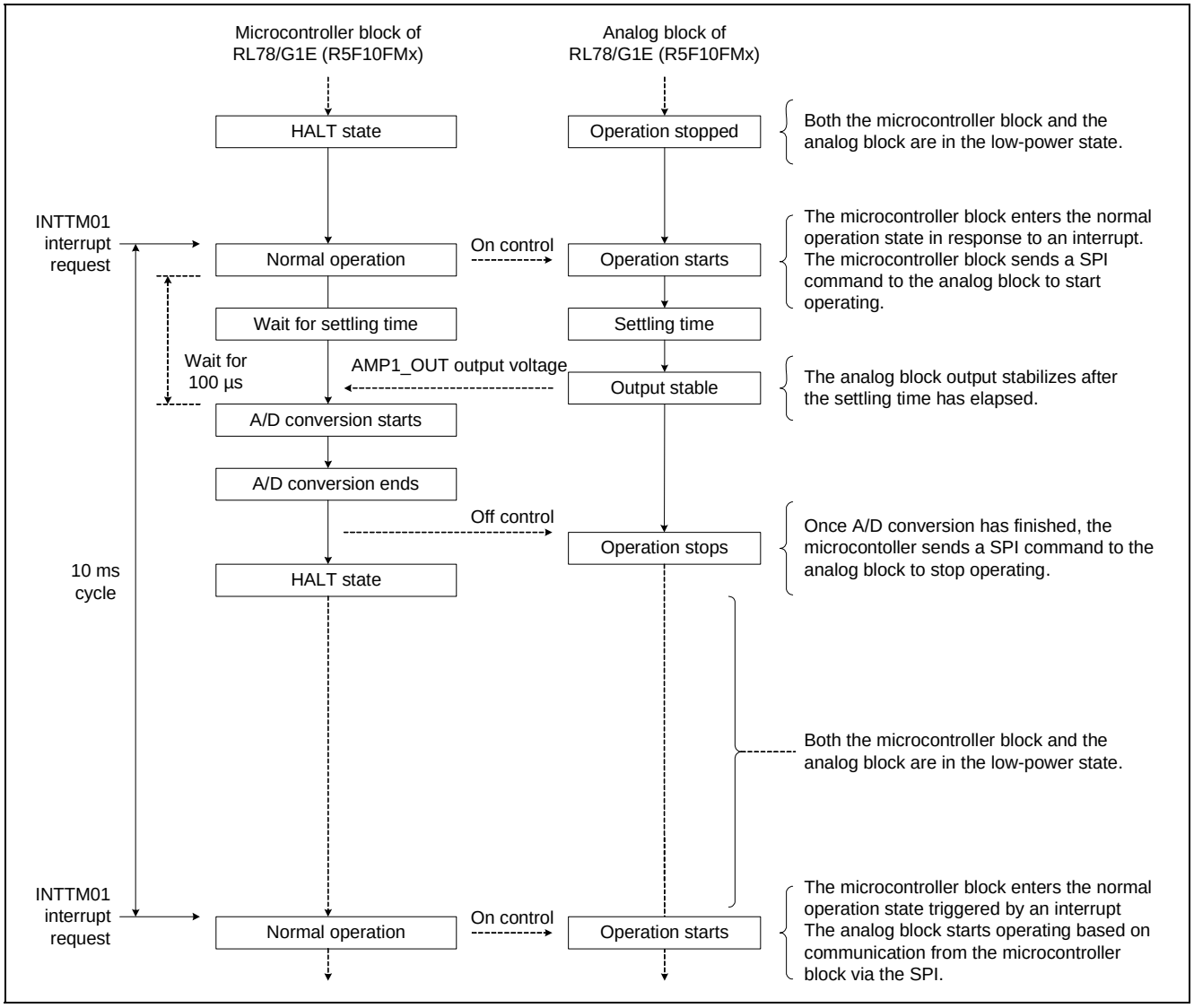


Figure 1.1 Control Flow

2. Conditions for Verifying Operation

The operation of the sample code shown in this application note has been verified under the conditions shown below.

Table 2.1 Conditions for Verifying Operation

Item	Description
Microcontroller used	RL78/G1E (R5F10FME)
Operating frequency	High-speed on-chip oscillator (high-speed OCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	V_{DD}, DV_{DD}, AV_{DD1}, AV_{DD2}, AV_{DD3}: 5.0 V AV_{DD}: 3.3 V LVD detection voltage (V_{LVIH}): 4.06 V when rising, 3.98 V when falling
External devices used	Photodiode (BS520E0F made by Sharp Corporation)
Integrated development environment	CubeSuite+ V1.01.01 [31 Jan 2012] made by Renesas Electronics
C compiler	CA78K0R V1.30 made by Renesas Electronics

3. Related Application Notes

Related application notes are shown below. Also refer to these documents when using this application note.

- RL78/G13 Low-Power Operation (R01AN0465E) Application Note
- RL78/G1E Example Measurement Using a Current Sensor (R01AN1055E) Application Note
- RL78/G1E Sample Code for Performing SPI Communication with Analog Block (R01AN1130E) Application Note

4. Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration described in this application note.

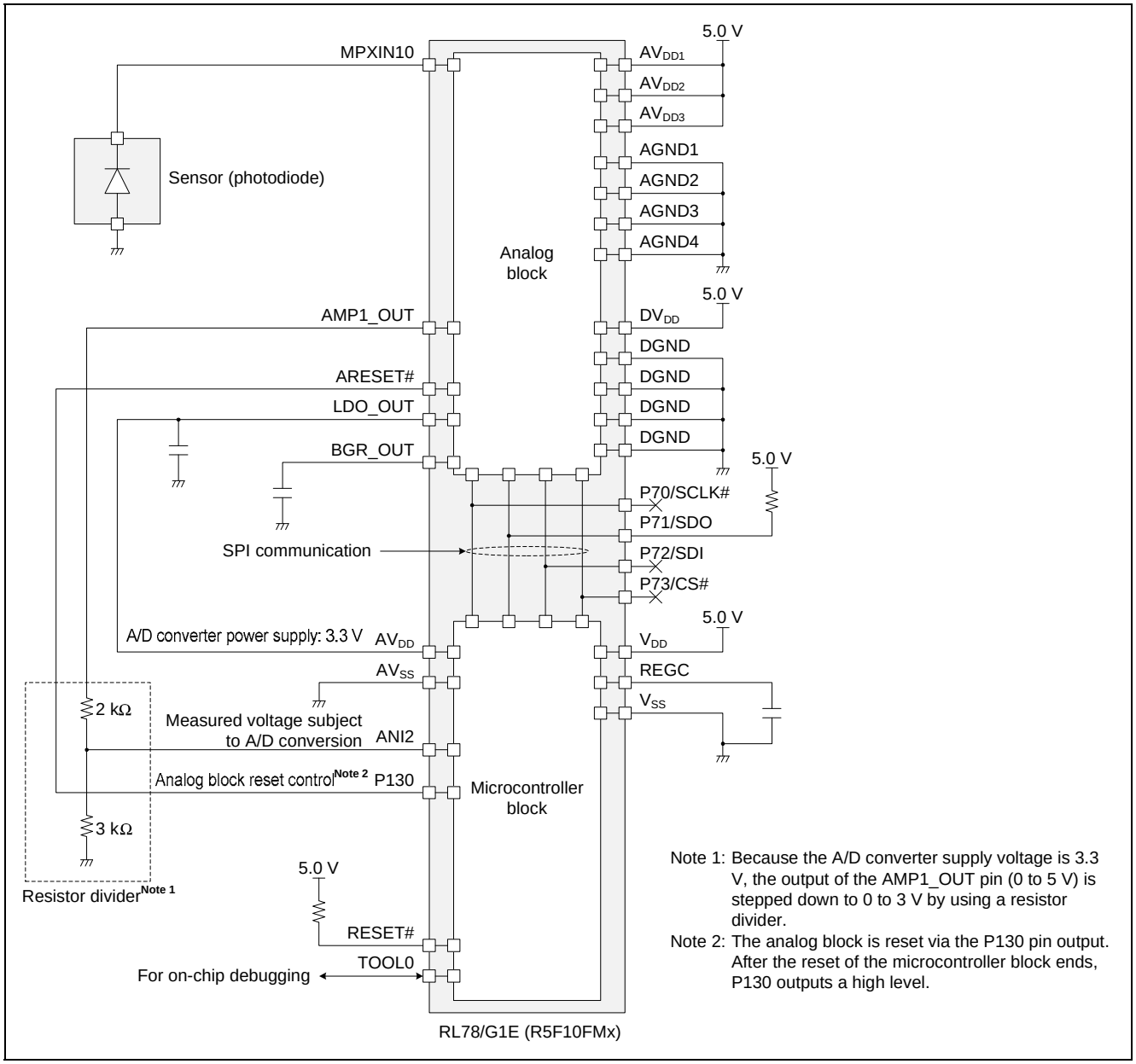


Figure 4.1 Hardware Configuration

Caution This circuit diagram is simplified to show an overview of the circuit connections. When designing an actual circuit, connect pins appropriately so as to satisfy the electrical specifications. (Connect unused input-only ports individually to V_{DD} or V_{SS} via a resistor.)

4.2 Circuits Used

Table 4.1 shows the RL78/G1E (R5F10FMx) peripheral circuits used in this application note and their applications.

Table 4.1 RL78/G1E (R5F10FMx) Peripheral Circuits and Their Applications

RL78/G1E (R5F10FMx) Peripheral Circuit		Application
Analog block	Configurable amplifier	Used as a transimpedance amplifier that converts the output current from a sensor (photodiode) to a single-ended voltage and amplifies it.
	D/A converter	Generates a bias voltage for the configurable amplifier (used as a transimpedance amplifier).
	Variable output voltage regulator	Generates the power supply voltage for the A/D converter.
	SPI	Controls SPI communication with the microcontroller block of the RL78/G1E (R5F10FMx).
Microcontroller block	A/D converter	Converts the voltage output from the configurable amplifier (used as a transimpedance amplifier) to a digital value.
	High-speed on-chip oscillator (high-speed OCO)	Generates the 32 MHz clock used as the main system clock.
	Serial array unit 1 (channel 1)	Controls SPI communication with the analog block by using the 3-wire serial I/O (CSI21).
	I/O ports	Controls the reset of the analog block, and the chip select signal (CS) used to control SPI communication with the analog block.
	Timer array unit 0 (channel 1)	The timer to generate the signal which cancels the HALT mode.
	Timer array unit 0 (channel 3)	The timer to generate the settling time that the system must wait until the output of configurable amplifier Ch1 (used as a transimpedance amplifier) and the D/A converter stabilizes.

4.3 Pins Used

Table 4.2 shows the RL78/G1E (R5F10FMx) pins used in this application note and their features.

Table 4.2 RL78/G1E (R5F10FMx) Pins Used and Their Features

Pin Name	I/O	Description
MPXIN10	Input	This is an inverted input pin of the configurable amplifier Ch1 (used as a transimpedance amplifier) in the analog block. This pin is connected to the sensor (Photodiode).
AMP1_OUT	Output	This is an output pin of the configurable amplifier Ch1 (used as a transimpedance amplifier) in the analog block. This pin is connected to the ANI2 pin of the A/D converter in the microcontroller block via a resistor divider.
ANI2	Input	This is an analog input pin of the A/D converter in the microcontroller block. This pin is connected to the AMP1_OUT pin in the analog block via a resistor divider.
P130	Output	P130 is an output-only pin in the microcontroller block. This pin is connected to the ARESET# pin in the analog block and is used to control the analog reset feature of the analog block.

5. Features of the Analog Block

See *6.2 Settings of Analog Block Registers* on p. 14 for details.

5.1 Procedure for Setting the Variable Output Voltage Regulator

The variable output voltage regulator incorporated in the RL78/G1E (R5F10FMx) is a series regulator which outputs the variable voltage from 2.0 to 3.3 V by a 0.1 V step with the setting of control registers. In this application note, the output voltage from the variable output voltage regulator is set to be 3.3 V and is used as the power supply voltage of the A/D converter.

Figure 5.1 shows the connection between the variable output voltage regulator in the analog block and the A/D converter in the microcontroller block incorporated in the RL78/G1E (R5F10FMx).

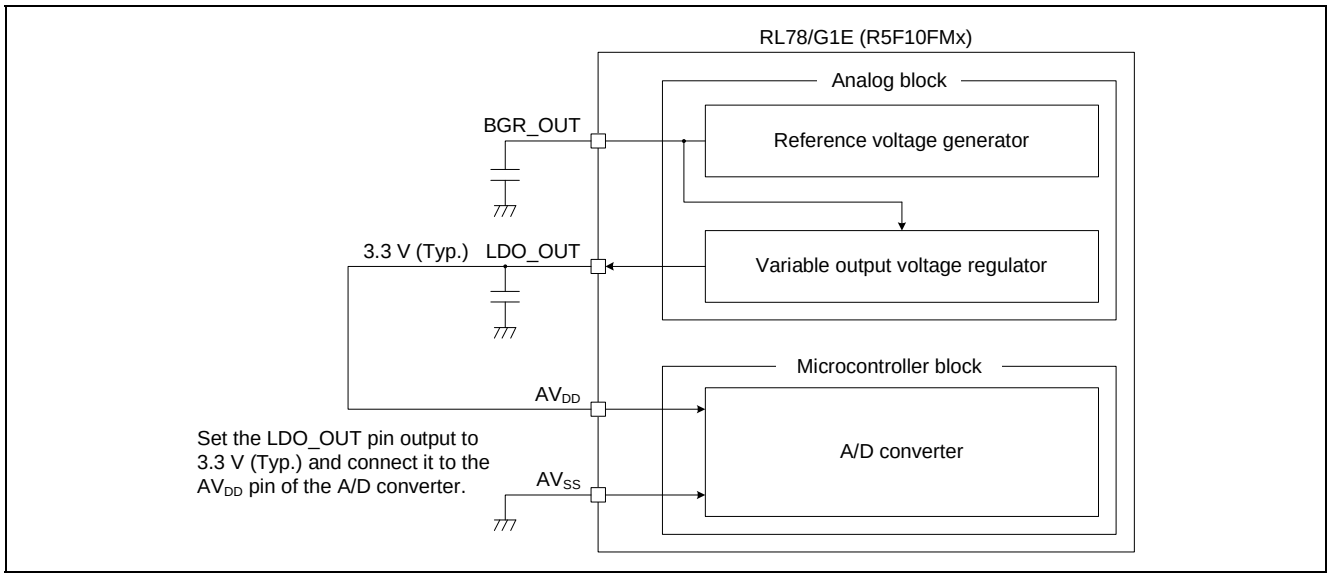


Figure 5.1 Connection Between Variable Output Voltage Regulator and A/D Converter

Follow the procedure below to start the variable output voltage regulator (LDO_OUT = 3.3 V (Typ.)) and reference voltage generator in the analog block of the RL78/G1E (R5F10FMx)).

<1> Set LDO3 to 1, LDO2 to 1, LDO1 to 0, and LDO0 to 1 in the LDO control register (LDOC) to specify 3.3 V (Typ.) as the voltage output from the variable output voltage regulator.
<2> Set LDOOF to 1 in power control register 2 (PC2) to enable operation of the variable output voltage regulator and reference voltage generator.

By executing the above steps, the variable output voltage regulator and reference voltage generator start operating and 3.3 V (Typ.) is output from the LDO_OUT pin.

Follow the procedure below to stop the variable output voltage regulator and reference voltage generator.

<1> Set LDOOF to 0 in power control register 2 (PC2) to stop operation of the variable output voltage regulator and reference voltage generator.

By executing the above step, the variable output voltage regulator and reference voltage generator stop operating and 0 V is output from the LDO_OUT pin.

In this application note, the output voltage from the variable output voltage regulator in the analog block is used as the power supply voltage of the A/D converter in the microcontroller block, so the variable output voltage regulator is never stopped once they start operating.

5.2 Procedure for Setting the Configurable Amplifiers

A configurable amplifier can change its circuit configuration and its circuit features and characteristics with the setting of control registers included in the analog block. In this application note, the configurable amplifier Ch1 is connected to the photodiode and is used as a transimpedance amplifier to convert an output current from the photodiode to a single-ended voltage. The output pin (AMP1_OUT) of the configurable amplifier Ch1 is connected to the analog input pin (ANI2) of the A/D converter outside the packages.

Figure 5.2 shows the connection among the photodiode, the configurable amplifier Ch1 and the A/D converter.

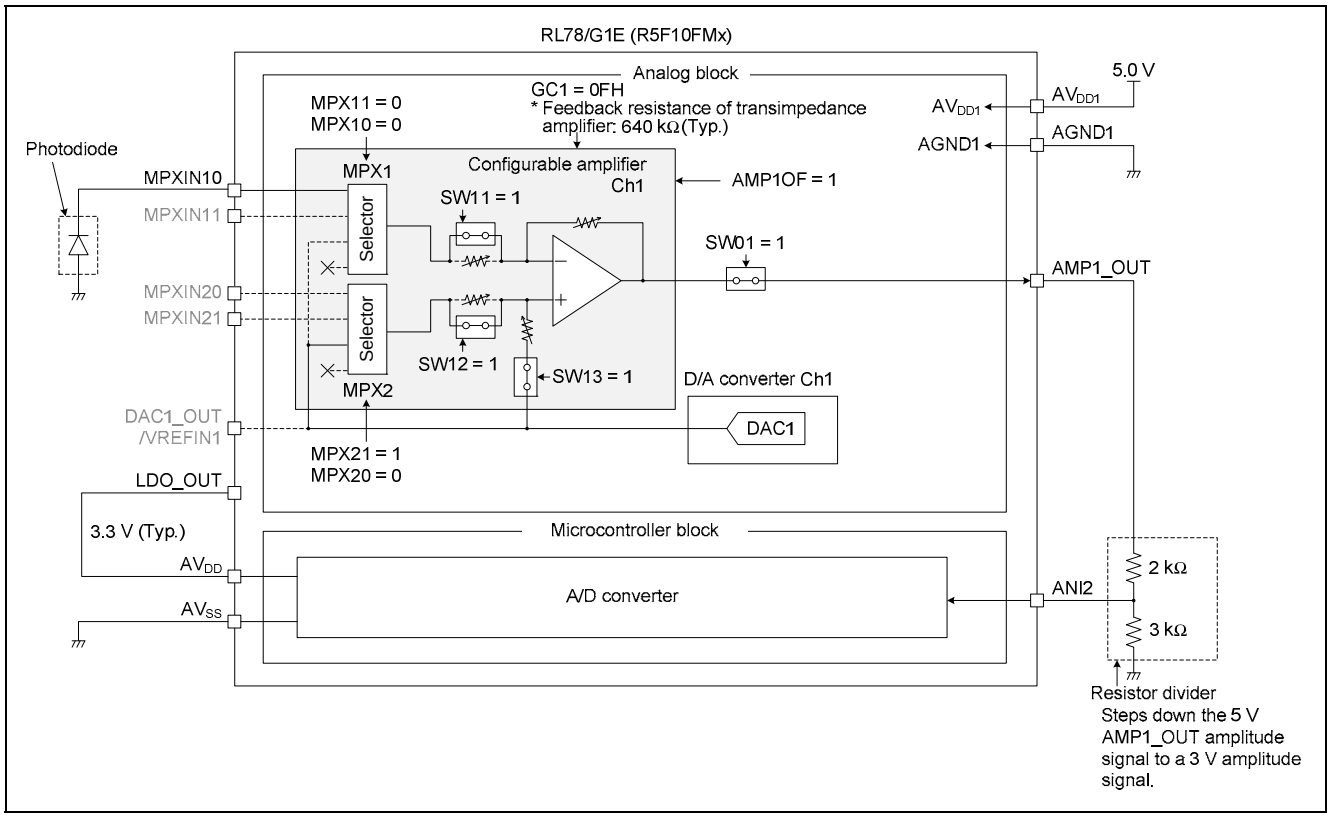


Figure 5.2 Connection Between Configurable Amplifier Ch1 and Photodiode, and Between Configurable Amplifier Ch1 and A/D Converter

Follow the procedure below to start configurable amplifier Ch1 (used as a transimpedance amplifier).

<1> Set SW11 to 1, SW12 to 1, and SW13 to 1 in configuration register 1 (CONFIG1) to specify that configurable amplifier Ch1 is used as a transimpedance amplifier.
<2> Set MPX11 to 0 and MPX10 to 0 in MPX setting register 1 (MPX1) to specify the MPXIN10 pin as the source of inverted input to configurable amplifier Ch1.
<3> Set MPX21 to 1 and MPX20 to 0 in MPX setting register 1 (MPX1) to specify the D/A converter Ch1 output signal or the VREFIN1 pin as the source of non-inverted input to configurable amplifier Ch1.
<4> Set CC1 to 0 and CC0 to 0 in the AMP operation mode control register (AOMC) to specify high-speed mode as the operation mode of configurable amplifier channels Ch1 to Ch3.
<5> Set AMP14 to 0, AMP13 to 1, AMP12 to 1, AMP11 to 1, and AMP10 to 1 in gain control register 1 (GC1) to specify 640 kΩ as the feedback resistance (Typ.) of configurable amplifier Ch1 (used as a transimpedance amplifier).
<6> Set SW01 to 1 in configuration register 2 (CONFIG2) to turn on SW01.
<7> Set AMP1OF to 1 in power control register 1 (PC1) to enable operation of configurable amplifier Ch1.

By executing the above steps, configurable amplifier Ch1 (used as a transimpedance amplifier) starts operating.

Follow the procedure below to stop configurable amplifier Ch1 (used as a transimpedance amplifier).

<1> Set AMP1OF to 0 in power control register 1 (PC1) to stop operation of configurable amplifier Ch1.

By executing the above step, configurable amplifier Ch1 (used as a transimpedance amplifier) stops operating.

In this application note, the operation of configurable amplifier Ch1 (used as a transimpedance amplifier) is stopped after its output voltage, which is a voltage that has been stepped down by using a resistor divider, has been A/D converted by the A/D converter in the microcontroller block.

5.3 Procedure for Setting the D/A Converter

In this application note, D/A converter Ch1 in the analog block is used to generate a bias voltage for configurable amplifier Ch1 (used as a transimpedance amplifier).

Follow the procedure below to start D/A converter Ch1.

<1> Set VRT1 to 0 and VRT0 to 0 in the DAC reference voltage control register (DACRC) to specify "$AV_{DD1} \times 5/10$" as the upper limit of the reference voltage (VRT) for the D/A converter.

<2> Set VRB1 to 0 and VRB0 to 0 in the DAC reference voltage control register (DACRC) to specify AGND1 as the lower limit of the reference voltage (VRB) for the D/A converter.

<3> Specify the analog voltage to be output to DAC control register 1 (DAC1C).

- In this application note, D/A converter Ch1 is used to generate a bias voltage for configurable amplifier Ch1 (used as a transimpedance amplifier). Set the DAC1C register to 19H to specify 0.49 V as the voltage output from the DAC1_OUT pin. (Note that the value set to the DAC1C register is a reference value. The user needs to evaluate the system to determine the actual values.)
- DAC1_OUT = ((reference voltage upper limit − reference voltage lower limit) × 2 × m/255) + 2 × reference voltage lower limit

  $= ((AV_{DD1} \times 5/10 - AGND1) \times 2 \times 25/255) + 2 \times AGND1$

  $= ((5 \times 5/10 - 0) \times 2 \times 25/255) + 2 \times 0$

  $= 0.49$ V

  * $AV_{DD1} = 5$ V
  * AGND1 = 0 V
  * m (DAC1C register value) = 25 (19H)

<4> Set DAC1OF to 1 in power control register 1 (PC1) to enable operation of D/A converter Ch1.

By executing the above steps, D/A converter Ch1 starts operating.

Follow the procedure below to stop D/A converter Ch1.

<1> Set DAC1OF to 0 in power control register 1 (PC1) to stop operation of D/A converter Ch1.

By executing the above step, D/A converter Ch1 stops operating.

In this application note, the operation of configurable amplifier Ch1 (used as a transimpedance amplifier) is stopped after its output voltage, which is a voltage that has been stepped down by using a resistor divider, has been A/D converted by the A/D converter in the microcontroller block. Due to this, the operation of D/A converter is also stopped.

5.4 Analog Block Settling Time

5.4.1 Settling time of the variable output voltage regulator

When operation of the variable output voltage regulator is started (by setting LDOOF to 1 in power control register 2 (PC2)) after having been stopped (by setting LDOOF to 0 in PC2), a settling time (t_{SET}) is required for the output of the variable output voltage regulator to stabilize.

The required settling time of the variable output voltage regulator is shown in **Table 5.1** below, based on the electrical specifications described in the *RL78/G1E Hardware User's Manual*.

Table 5.1 Settling Time of Variable Output Voltage Regulator

(−40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, LDOOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Settling time	t_{SET}	–	–	–	5	ms

Caution The rating in Table 5.1 applies to when a 4.7 µF (recommended value) capacitor is connected to the LDO_OUT pin and a 0.1 µF (recommended value) capacitor is connected to the BGR_OUT pin.

5.4.2 Settling time of the configurable amplifier (used as transimpedance amplifier)

When operation of the configurable amplifier is started (by setting AMPnOF (n = 1 to 3) to 1 in power control register 1 (PC1)) after having been stopped (by setting AMPnOF (n = 1 to 3) to 0 in PC1), a settling time (T_S) is required for the output of the amplifier to stabilize.

The settling time of the configurable amplifier (used as a non-inverting amplifier) is measured from the end of SPI command (the data that changes the setting of the AMPnOF (n = 1 to 3) bit from 0 to 1 is latched) until the output voltage from the configurable amplifier (AMPn_OUT (n = 1 to 3)) is within ±0.1% of the final output voltage.**Figure 5.3** shows the settling time.

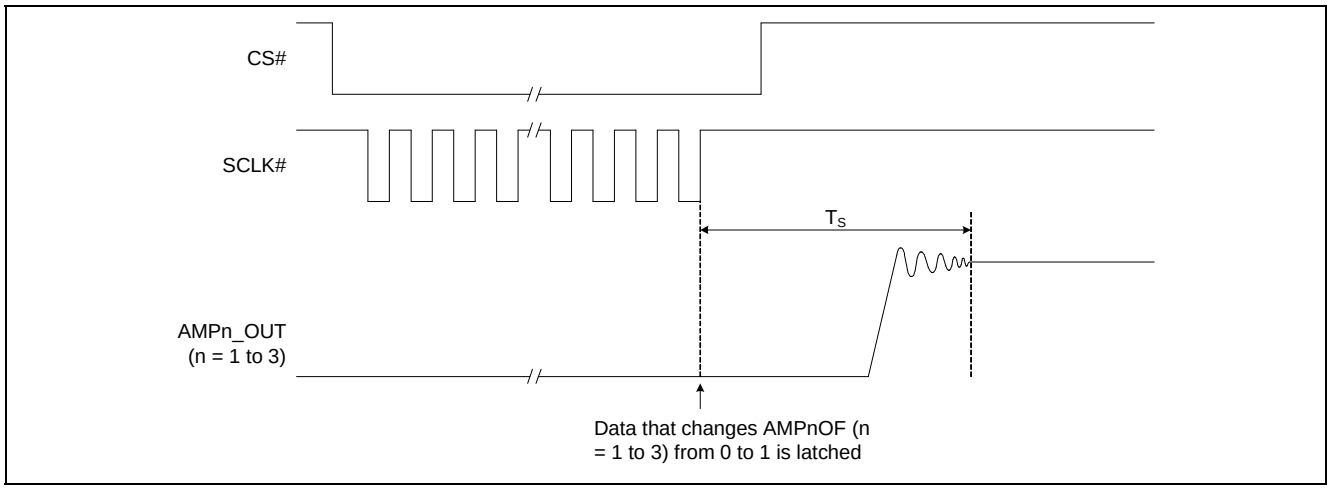


Figure 5.3 Settling Time of Configurable Amplifier (Used as Transimpedance Amplifier)

The required settling time of the configurable amplifier when used as a transimpedance amplifier is shown in **Table 5.2** below, based on the electrical specifications described in the *RL78/G1E Hardware User's Manual*.

Table 5.2 Settling Time of Configurable Amplifier (Used as Transimpedance Amplifier)

(−40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, AMP1OF = AMP2OF = AMP3OF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Settling time	T_S	High-speed mode (CC1, CC0 = 0, 0) Feedback resistance: 20 kΩ	–	–	9	μs

5.4.3 D/A converter settling time

When operation of the D/A converter is started (by setting DACnOF (n = 1 to 4) to 1 in power control register 1 (PC1)) after having been stopped (by setting DACnOF (n = 1 to 4) to 0 in PC1), a settling time (t_{SET}) is required for the output of the D/A converter to stabilize.

The settling time of the D/A converter is measured from the end of SPI command (the data that changes the setting of the DACnOF (n = 1 to 4) bit from 0 to 1 is latched) until the output voltage from the D/A converter (DACn_OUT (n = 1 to 4)) is within ±1.0% of the final output voltage.

The required settling time of the D/A converter is shown in **Table 5.3** below, based on the electrical specifications described in the *RL78/G1E Hardware User's Manual*.

Table 5.3 D/A Converter Settling Time

(−40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, DAC1OF = DAC2OF = DAC3OF = DAC4OF = 1)

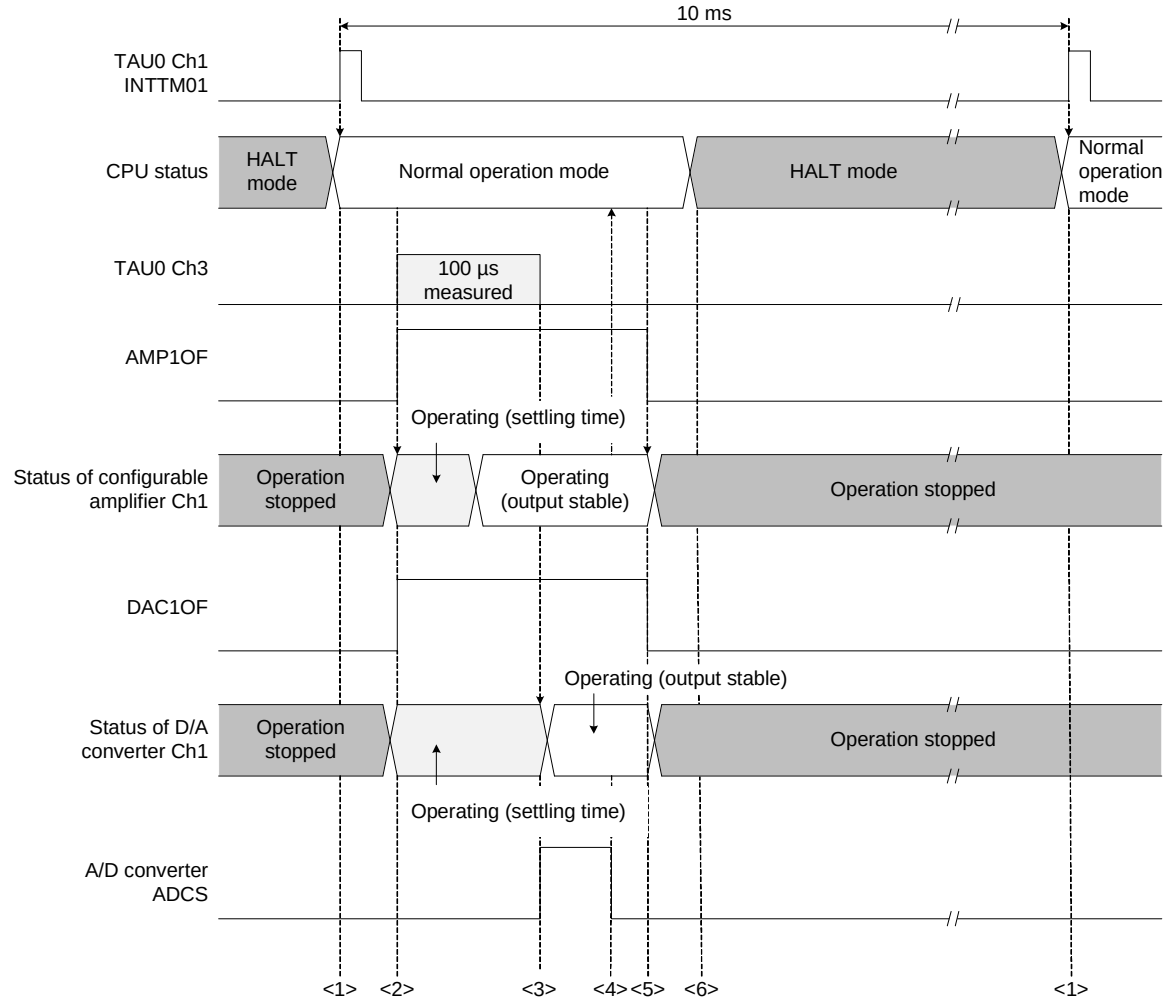
Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Settling time	t_{SET}	–	–	–	100	μs

6. Software

6.1 Timing Chart

In this application note, configurable amplifier Ch1 (used as a transimpedance amplifier) and D/A converter Ch1 are used. It is therefore necessary to program the system to wait for at least 100 us between when the AMP1OF and DAC1OF bits are set to 1 in the PC1 register and the start of A/D conversion, to accord with the D/A converter's settling time, which is the longer of the two.

A timing chart showing the intermittent operation described in this application note is shown below.



Remark

INTTM01: Interrupt triggered by the completion of counting by channel 1 of timer array unit 0 or capture interrupt

AMP1OF: Bit 0 of power control register 1 (PC1). Controls the operation of configurable amplifier Ch1.
- 0: Stop operation of configurable amplifier Ch1.
- 1: Enable operation of configurable amplifier Ch1.

DAC1OF: Bit 4 of power control register 1 (PC1). Controls the operation of D/A converter Ch1.
- 0: Stop operation of D/A converter Ch1.
- 1: Enable operation of D/A converter Ch1.

ADCS: Bit 7 of A/D converter mode register 0 (ADM0)
- 0: Stop conversion (When read: Conversion stopped or in the standby status)
- 1: Enable conversion (When read: Conversion in progress (software trigger mode))

Figure 6.1 Timing Chart for Intermittent Operation

<1> The microcontroller block exits the HALT mode upon occurrence of the interrupt request triggered by the completion of counting by channel 1 of timer array unit 0 (INTTM01).

<2> Operation of configurable amplifier Ch1 (used as a transimpedance amplifier) and D/A converter Ch1 in the analog block is started via the 3-wire serial I/O of channel 1 of serial array unit 1 (CSI21) in the microcontroller block (by setting the AMP1OF and DAC1OF bits to 1 in the PC1 register).

<3> The system waits for 100 us, which is the settling time of configurable amplifier Ch1 (used as a transimpedance amplifier) and D/A converter Ch1 in the analog block, and which is counted by using the interval timer of channel 3 of timer array unit 0 in the microcontroller block. Once the 100 us wait time has elapsed, the A/D converter in the microcontroller block enters software trigger mode and A/D conversion of the data input from the ANI2 pin is started (by setting the ADCS bit to 1 in A/D converter mode register 0 (ADM0)).

<4> When the A/D converter in the microcontroller block finishes A/D converting the data, the conversion result is read out.

<5> Operation of configurable amplifier Ch1 (used as a transimpedance amplifier) and D/A converter Ch1 in the analog block is stopped via CSI21 in the microcontroller block (by setting the AMP1OF and DAC1OF bits to 0 in the PC1 register).

<6> The microcontroller block enters HALT mode.

6.2 Settings of Analog Block Registers

This section describes the settings of the SPI control registers in the analog block of the RL78/G1E (R5F10FMx) used in this application note. This section omits descriptions of the SPI control registers not used in this application note. (They are used with their default values.)

Caution For how to specify the SPI control register settings, see the *RL78/G1E Hardware User's Manual*.

(1) Configuration register 1 (CONFIG1)

Set all the switches of configurable amplifier Ch1 to "transimpedance amplifier" mode.

Address: 00H After reset: 00H R/W Set value: 70H

Symbol	7	6	5	4	3	2	1	0
CONFIG1	0	SW11	SW12	SW13	0	SW21	SW22	SW23
Set value	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**

(2) Configuration register 2 (CONFIG2)

Turn on the output switches of configurable amplifier Ch1.

Address: 01H After reset: 00H R/W Set value: 02H

Symbol	7	6	5	4	3	2	1	0
CONFIG2	0	SW31	SW32	SW33	0	SW02	SW01	SW00
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

(3) MPX setting register 1 (MPX1)

Specify the MPXIN10 pin as the source of inverted input to configurable amplifier Ch1, and the D/A converter Ch1 output signal or the VREFIN1 pin as the source of non-inverted input to configurable amplifier Ch1.

Address: 03H After reset: 00H R/W Set value: 20H

Symbol	7	6	5	4	3	2	1	0
MPX1	MPX11	MPX10	MPX21	MPX20	MPX31	MPX30	MPX41	MPX40
Set value	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**

(4) Gain control register 1 (GC1)

Set the feedback resistance of configurable amplifier Ch1 (used as a transimpedance amplifier) to 640 kΩ (Typ.).

Address: 06H After reset: 00H R/W Set value: 0FH

Symbol	7	6	5	4	3	2	1	0
GC1	0	0	0	AMPG14	AMPG13	AMPG12	AMPG11	AMPG10
Set value	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**

(5) AMP operation mode control register (AOMC)

Set the operating mode of configurable amplifier Ch1 to “high-speed mode”.

Address: 09H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
AOMC	0	0	0	0	0	0	CC1	CC0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

(6) LDO control register (LDOC)

Set the output voltage of the variable output voltage regulator to 3.3 V (Typ.).

Address: 0BH After reset: 0DH R/W Set value: 0DH

Symbol	7	6	5	4	3	2	1	0
LDOC	0	0	0	0	LDO3	LDO2	LDO1	LDO0
Set value	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**

(7) DAC reference voltage control register (DACRC)

Set the upper (VRT) and lower (VRB) limits of the reference voltage for the D/A converter to $AV_{DD1} \times 5/10$ and AGND1, respectively.

Address: 0CH After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
DACRC	0	0	0	0	VRT1	VRT0	VRB1	VRB0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

(8) DAC control register 1 (DAC1C)

Set the analog voltage to be output to the DAC1_OUT pin to 0.49 V.

Address: 0DH After reset: 80H R/W Set value: 19H

Symbol	7	6	5	4	3	2	1	0
DAC1C	DAC17	DAC16	DAC15	DAC14	DAC13	DAC12	DAC11	DAC10
Set value	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**

(9) Power control register 1 (PC1)

Enable or stop operation of configurable amplifier Ch1 and D/A converter Ch1.

Address: 11H After reset: 00H R/W Set value: **H

Symbol	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	0	AMP3OF	AMP2OF	AMP1OF
Set value	**0**	**0**	**0**	*****	**0**	**0**	**0**	*****

Remark: * = Write 1 to this bit to enable operation of configurable amplifier Ch1 and D/A converter Ch1, and 0 to stop operation.

(10) Power control register 2 (PC2)

Enable operation of the variable output voltage regulator and reference voltage generator.

Address: 12H After reset: 00H R/W Set value: 02H

Symbol	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

6.3 Settings of Microcontroller Block Registers

The register settings specified for the microcontroller block of the RL78/G1E (R5F10FMx) are shown below. This section omits descriptions of the SPI control registers not used in this application note. (They are used with their default values.)

Caution For how to specify the microcontroller block register settings, see the *RL78/G1E Hardware User's Manual*.

(1) User option bytes

(a) User option byte (000C0H/010C0H)

Disable operation of the watchdog timer counter.

Address: 000C0H/010C0H Set value: EEH

Symbol	7	6	5	4	3	2	1	0
	WDTINT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON
Set value	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

(b) User option byte (000C1H/010C1H)

Set the LVD operation mode to "reset mode", and the LVD detection level (V_{LVIH}) when the voltage is rising to 4.06 V and when the voltage is falling to 3.98 V.

Address: 000C1H/010C1H Set value: 73H

Symbol	7	6	5	4	3	2	1	0
	VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0
Set value	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**

(c) User option byte (000C2H/010C2H)

Set the flash operation mode to "HS (high speed main) mode" and select 32 MHz as the high-speed on-chip oscillator frequency.

Address: 000C2H/010C2H Set value: E8H

Symbol	7	6	5	4	3	2	1	0
	CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0
Set value	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**

(d) On-chip debug option byte (000C3H/010C3H)

Enable on-chip debugging and specify that the flash memory data is erased if security ID authorization fails.

Address: 000C3H/010C3H Set value: 84H

Symbol	7	6	5	4	3	2	1	0
	OCDENSET	0	0	0	0	1	0	OCDERSD
Set value	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**

(2) Clock generator

(a) Clock operation mode control register (CMC)

Set the operation mode of the high-speed system clock pin to "input port".

Address: FFFA0H After reset: 00H R/W Set value: 10H

Symbol	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	0	0	0	0	0	AMPH
Set value	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

(b) Clock operation status control register (CSC)

Set the operation mode of the high-speed system clock (in input port mode) to "input port" and the operation mode of the high-speed on-chip oscillator to "high-speed on-chip oscillator operating".

Address: FFFA1H After reset: C0H R/W Set value: C0H

Symbol	7	6	5	4	3	2	1	0
CSC	MSTOP	1	0	0	0	0	0	HIOSTOP
Set value	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**

(c) System clock control register (CKC)

Select the high-speed on-chip oscillator clock (f_{MAIN}) as the main system clock (f_{IH}).

Address: FFFA4H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
CKC	CLS	0	MCS	MCM0	0	0	0	0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

(d) Operation speed mode control register (OSMC)

Select the low-speed on-chip oscillator clock as the interval timer operation clock.

Address: F00F3H After reset: 00H R/W Set value: 10H

Symbol	7	6	5	4	3	2	1	0
OSMC	0	0	0	WUTMMCK0	0	0	0	0
Set value	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

(e) Peripheral enable register 0 (PER0)

Enable the input clock supply to the A/D converter, serial array unit 1, and timer array unit 0.

Address: F00F0H After reset: 00H R/W Set value: 29H

Symbol	7	6	5	4	3	2	1	0
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN
Set value	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**

(3) Serial array unit 1

(a) Serial mode register 11 (SMR11)

Specify the operation clock specified by the SPS1 register (CK10) as the operation clock for channel 1 (f_{MCK}), the divided operation clock (f_{MCK}) specified by the CKS11 bit as the transfer clock for channel 1 (f_{TCLK}), CSI mode as the channel 1 operation mode, and the transfer end interrupt or buffer empty interrupt as the channel 1 interrupt source.

Address: F0152H, F0153H After reset: 0020H R/W Set value: 002*H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMR11	CKS11	CCS11	0	0	0	0	0	STS11	0	SIS110	1	0	0	MD112	MD111	MD110
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	*****

Remark: * = Switch the transfer end interrupt (= 0) and buffer empty interrupt (= 1) by using software.

(b) Serial communication operation setting register 11 (SCR11)

Specify "transmission/reception" as the channel 1 operation mode, "Type 1" as the data and clock phase in CSI mode, "MSB first" as the data transfer order, and "8 bits" as the transfer data length.

Address: F015AH, F015BH After reset: 0087H R/W Set value: C007H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR11	TXE11	RXE11	DAP11	CKP11	0	EOC11	PTC111	PTC110	DIR11	0	0	SLC110	0	1	1	DLS110
Set value	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**

(c) Serial data register 11 (SDR11)

Specify "$f_{MCK}/32$" as the transfer clock generated by dividing the operation clock (f_{MCK}). The lower 8 bits (bits 7 to 0) function as a transmission/reception buffer register.

Address: FFF4AH, FFF4BH After reset: 0000H R/W Set value: 1E**H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDR11	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	*****	*****	*****	*****	*****	*****	*****	*****

Remark: * = Functions as a transmission/reception buffer register.

(d) Serial channel stop register 1 (ST1)

Specify whether the trigger to stop operation of channel 1 is the "no trigger operation" or "clear the SE11 bit to 0 to stop the communication operation".

Address: F0164H, F0165H After reset: 0000H R/W Set value: 000*H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ST11	ST10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*****	**0**

Remark: * = Write 1 to this bit only when finishing serial communication.

(e) Serial clock select register 1 (SPS1)

Specify "32 MHz when f_{CLK} = 32 MHz" as the operation clock (CK10).

Address: F0166H, F0167H After reset: 0000H R/W Set value: 0000H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPS1	0	0	0	0	0	0	0	0	PRS113	PRS112	PRS111	PRS110	PRS103	PRS102	PRS101	PRS100
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

(f) Serial output register 1 (SO1)

Set the serial clock output of channel 1 to "1" and the serial data output to "0".

Address: F0168H, F0169H After reset: 0F0FH R/W Set value: 0301H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	0	0	CKO11	CKO10	0	0	0	0	0	0	SO11	SO10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

(g) Serial output enable register 1 (SOE1)

Specify whether to enable the serial output of channel 1 during serial communication.

Address: F016AH, F016BH After reset: 0000H R/W Set value: 000*H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE11	SOE10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*****	**0**

Remark: * = Write 1 to this bit to start serial communication and 0 to stop serial communication.

(h) Serial channel start register 1 (SS1)

Specify that the trigger to start operation of channel 1 is "clear the SE11 bit to 1 and enter the communication wait status".

Address: F0162H, F0163H After reset: 0000H R/W Set value: 000*H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SS11	SS10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*****	**0**

Remark: * = Write 1 to this bit only when starting serial communication.

(4) Ports

(a) Port mode registers

Select the Pmn pin I/O mode (m = 0 to 2, 4, 6, 7, 14, 15; n = 0 to 7).

Address: FFF20H After reset: FFH R/W Set value: 9FH

Symbol	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00
Set value	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**1**

Address: FFF21H After reset: FFH R/W Set value: BFH

Symbol	7	6	5	4	3	2	1	0
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10
Set value	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**

Address: FFF22H After reset: FFH R/W Set value: 1FH

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
Set value	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**

Address: FFF24H After reset: FFH R/W Set value: F7H

Symbol	7	6	5	4	3	2	1	0
PM4	1	1	1	1	PM43	PM42	PM41	PM40
Set value	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**

Address: FFF26H After reset: FFH R/W Set value: F0H

Symbol	7	6	5	4	3	2	1	0
PM6	1	1	1	1	PM63	PM62	PM61	PM60
Set value	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**

Address: FFF27H After reset: FFH R/W Set value: 02H

Symbol	7	6	5	4	3	2	1	0
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

Address: FFF2EH After reset: FFH R/W Set value: FDH

Symbol	7	6	5	4	3	2	1	0
PM14	1	1	1	1	1	1	PM141	PM140
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**

Address: FFF2H After reset: FFH R/W Set value: E0H

Symbol	7	6	5	4	3	2	1	0
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150
Set value	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**

(b) Port registers

Control the Pmn pin output data (m = 0 to 2, 4, 7, 13, 14; n = 0 to 5 and 7).

Address: FFF00H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
P0	0	0	0	P04	P03	P02	P01	P00
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Address: FFF01H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
P1	0	0	P15	P14	P13	P12	P11	P10
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Address: FFF02H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
P2	0	0	0	P24	P23	P22	P21	P20
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Address: FFF04H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
P4	0	0	0	0	0	P42	P41	P40
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Address: FFF07H After reset: 00H R/W Set value: 0*H

Symbol	7	6	5	4	3	2	1	0
P7	0	0	0	0	P73	P72	P71	P70
Set value	**0**	**0**	**0**	**0**	*****	**1**	**0**	**1**

Address: FFF0DH After reset: Undefined R/W Set value: 01H

Symbol	7	6	5	4	3	2	1	0
P13	P137	0	0	0	0	0	0	P130
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Address: FFF0EH After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
P14	0	0	0	0	0	0	0	P140
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Remark: * = Write 0 or 1 to switch the output level according to the status.

(c) Port mode control register 7 (PMC7)

Specify whether the P70 pin is used as a digital I/O pin or an analog input pin.

Address: FFF67H After reset: FFH R/W Set value: FEH

Symbol	7	6	5	4	3	2	1	0
PMC7	1	1	1	1	1	1	1	PMC70
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**

(5) A/D converter

(a) A/D converter mode register 0 (ADM0)

Enable A/D conversion, specify "select" as the A/D conversion channel selection mode, enable operation of the A/D voltage comparator, and set the A/D conversion time to 54 μs (12-bit A/D conversion, no stabilization wait (hardware trigger no-wait mode), AV_{DD} = 2.7 to 3.6 V, f_{CLK} = 32 MHz).

Address: FFF30H After reset: 00H R/W Set value: *1H

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Set value	*	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Remark: * = Write 1 to this bit only when starting A/D conversion.

(b) A/D converter mode register 1 (ADM1)

Specify software trigger mode as the A/D conversion trigger mode and one-shot conversion mode as the A/D conversion operation mode.

Address: FFF32H After reset: 00H R/W Set value: 20H

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
Set value	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**

(c) A/D converter mode register 2 (ADM2)

Specify AV_{DD} as the positive reference voltage supply of the A/D converter, AV_{SS} as the negative reference voltage supply of the A/D converter, the generation of an interrupt signal (INTAD) if the conversion result upper/lower limit check results in ADLL register value ≤ ADCR register value ≤ ADUL register value, disable the SNOOZE mode, and set the A/D conversion resolution to "12 bits".

Address: F0010H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

(d) Conversion result comparison upper limit setting register (ADUL)

Set the A/D conversion result comparison upper limit to FFH.

Address: F0011H After reset: FFH R/W Set value: FFH

Symbol	7	6	5	4	3	2	1	0
ADUL	ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

(e) Conversion result comparison lower limit setting register (ADLL)

Set the A/D conversion result comparison lower limit to 00H.

Address: F0012H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

(f) Analog input channel specification register (ADS)

Specify ANI2 as the A/D conversion channel (in select mode (ADMD = 0)).

Address: FFF31H After reset: 00H R/W Set value: 02H

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

(g) A/D port configuration register (ADPC)

Specify "analog input" (not "digital I/O") as the I/O mode of the P24/ANI4, P23/ANI3, P22/ANI2, P21/ANI1, and P20/ANI0 pins.

Address: F0076H After reset: 00H R/W Set value: 00H

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	0	ADPC2	ADPC1	ADPC0
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

(6) Timer array unit 0

(a) Timer channel stop register 0 (TT0)

Specify “no trigger operation” as the trigger to stop operation of channel 3 and “operation is stopped (stop trigger is generated)” as that of channel 1.

Address: F01B4H, F01B5H After reset: 0000H R/W Set value: 000*H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT0	0	0	0	0	TTH03	0	TTH01	0	TT07	TT06	TT05	TT04	TT03	TT02	TT01	TT00
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*****	**0**	*****	**0**

Remark: * = Write 1 to this bit during timer operation to stop the timer operation.

(b) Timer clock selection register 0 (TPS0)

Specify "32 MHz (f_{CLK} = 32 MHz)" as the CK00 operation clock and "4 MHz (f_{CLK} = 32 MHz)" as the CK01 operation clock.

Address: F01B6H, F01B7H After reset: 0000H R/W Set value: 0030H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPS0	0	0	PRS031	PRS030	0	0	PRS021	PRS020	PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**

(c) Timer mode registers 1 and 3 (TMR01, TMR03)

Set timer mode registers 1 and 3 as follows:

- Set the operation clock of channel 1 (f_{MCK}) to "operation clock CK01 set by TPS0".
- Set the operation clock of channel 3 (f_{MCK}) to "operation clock CK00 set by TPS0"
- Set the count clock of channels 3 and 1 (f_{TCLK}) to "operation clock (f_{MCK}) specified by the CKS0n0 and CKS0n1 (n = 1 to 3) bits".
- Specify that channels 3 and 1 are used as 8-bit timers (not 16-bit timers).
- Specify "only software trigger start is valid (other trigger sources are unselected)" as the start trigger and capture trigger for channels 3 and 1.
- Specify the interval timer as the operation mode of channels 3 and 1.
- Specify "timer interrupt is not generated when counting is started (timer output does not change, either)" as the count start and interrupt setting for channels 3 and 1.

Address: F0192H, F0193H After reset: 0000H R/W Set value: 8000H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR01	CKS011	CKS010	0	CCS01	SPLIT01	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
Set value	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Address: F0196H, F0197H After reset: 0000H R/W Set value: 0000H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR03	CKS031	CKS030	0	CCS03	SPLIT03	STS032	STS031	STS030	CIS031	CIS030	0	0	MD033	MD032	MD031	MD030
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

(d) Timer data registers 1 and 3 (TDR01, TDR03)

Specify the interval in the interval mode of channels 1 and 3 of timer array unit 0.

Address: FFF1AH, FFF1BH After reset: 0000H R/W Set value: 9C3FH

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR01	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**

Address: FFF66H, FFF67H After reset: 0000H R/W Set value: 001FH

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR03	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**

(e) Timer channel start register 0 (TS0)

Specify that the trigger to start operation of channel 1 and channel 3 is the setting of the TE01 and TE03 bits to 1, enabling counting.

Address: F01B2H, F01B3H After reset: 0000H R/W Set value: 000*H

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS0	0	0	0	0	TSH03	0	TSH01	0	TS07	TS06	TS05	TS04	TS03	TS02	TS01	TS00
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*****	**0**	*****	**0**

Remark: * = Write 1 to this bit only when starting the timer.

6.4 Functions

Table 6.1 Functions

File Name	Function Name	Overview
main.c	main	main function
	R5F10FMx_LDO_Enable	Analog block LDO initialization function
	R5F10FMx_Analog_Init	Analog block initialization function
	R5F10FMx_Analog_Start	Analog block operation start function
	R5F10FMx_Analog_Stop	Analog block operation stop function
r_systeminit.c	R_Systeminit	MCU initialization function
	hdwinit	System initialization function
r_cg_cgc.c	R_CGC_Create	Clock generator initialization function
r_cg_port.c	R_PORT_Create	Port initialization function
r_cg_serial.c	R_SAU1_Create	SAU1 initialization function
	R_CSI21_Create	CSI21 initialization function
	R_CSI21_Start	CSI21 operation start function
	R_CSI21_Stop	CSI21 operation stop function
	R_CSI21_Send_Receive	CSI21 transmission/reception function
r_cg_serial_user.c	r_csi21_interrupt	INTCSI21 interrupt service function
	r_csi21_callback_receiveend	CSI21 reception completion function
	r_csi21_callback_error	CSI21 error handling function
	SPI_ControlRegister_Read	SPI control register read function
	SPI_ControlRegister_Write	SPI control register write function
	SPI_ControlRegister_Write_Verify	SPI control register write verify function
	SPI_ControlRegister_Read_Bit	SPI control register bit read function
	SPI_ControlRegister_Write_Bit	SPI control register bit write function
	SPI_ControlRegister_Write_Verify_Bit	SPI control register bit write verify function
r_cg_adc.c	R_ADC_Create	ADC initialization function
	R_ADC_Start	ADC operation start function
	R_ADC_Stop	ADC operation stop function
	R_ADC_Set_OperationOn	ADC comparator operation enable function
	R_ADC_Set_OperationOff	ADC comparator operation stop function
	R_ADC_Get_Result	A/D conversion result read function
r_cg_adc_user.c	ADC_Control	A/D conversion control function
r_cg_timer.c	R_TAU0_Create	TAU0 initialization function
	R_TAU0_Channel1_Start	TAU0 Ch1 counter operation start function
	R_TAU0_Channel1_Stop	TAU0 Ch1 counter operation stop function
	R_TAU0_Channel3_Start	TAU0 Ch3 counter operation start function
	R_TAU0_Channel3_Stop	TAU0 Ch3 counter operation stop function
r_cg_timer_user.c	r_tau0_channel1_interrupt	TAU0 Ch1 interrupt service function
	TAU0_WAIT_1us	1-µs unit wait function

6.5 Function Specifications

The specifications of the major functions used in this application note are described below. For details about using the SPI to communicate with the analog block, see *Sample Code for Performing SPI Communication with Analog Block (R01AN1130E)*.

(1) `main` function

Declaration	`void main(void)`
Overview	`Main` routine function
Parameters	None
Return value	None
Description	• Initializes the variable output voltage regulator in the analog block. • Initializes timer array unit 0 in the microcontroller block. • Executes processing to make the system wait for the output of the variable output voltage regulator in the analog block to stabilize. • Initializes the A/D converter in the microcontroller block. • Initializes the circuits (configurable amplifier Ch1 and D/A converter Ch1) in the analog block. • Starts counting using channel 1 in timer array unit 0 in the microcontroller block. • Starts operation of the circuits (configurable amplifier Ch1 and D/A converter Ch1) in the analog block. • Waits for the 100 µs settling time. • Controls A/D conversion performed by the A/D converter in the microcontroller block. • Stops operation of the circuits (configurable amplifier Ch1 and D/A converter Ch1) in the analog block. • Shifts the microcontroller block to HALT mode.

(2) Analog block LDO initialization function (`R5F10FMx_LDO_Enable`)

Declaration	`static uinu8_t R5F10FMx_LDO_Enable(void)`
Overview	Analog block LDO initialization function
Parameters	None
Return value	0: Successful 1: Communication with the analog block failed
Description	• Initializes the variable output voltage regulator in the analog block. - Sets the variable output voltage regulator voltage to 3.3 V and enables the variable output voltage regulator and the reference voltage generator.

(3) Analog block initialization function (`R5F10FMx_Analog_Init`)

Declaration	`static uinu8_t R5F10FMx_Analog_Init(void)`
Overview	Analog block initialization function
Parameters	None
Return value	0: Successful 1: Communication with the analog block failed
Description	• Initializes the circuits in the analog block. - Configures configurable amplifier CH1 (used as a transimpedance amplifier) as shown in this application note. - Sets the D/A converter Ch1 output voltage. - Enables D/A converter Ch1 and configurable amplifier Ch1.

(4) Analog block operation start function (`R5F10FMx_Analog_Start`)

Declaration	`static uinu8_t R5F10FMx_Analog_Start(void)`
Overview	Analog block operation start function
Parameters	None
Return value	0: Successful 1: Communication with the analog block failed
Description	• Starts operation of the circuits in the analog block. - Enables D/A converter Ch1 and configurable amplifier Ch1.

(5) Analog block operation stop function (`R5F10FMx_Analog_Stop`)

Declaration	`static uinu8_t R5F10FMx_Analog_Stop(void)`
Overview	Analog block operation stop function
Parameters	None
Return value	0: Successful 1: Communication with the analog block failed
Description	• Stops operation of the circuits in the analog block. - Stops operation of D/A converter Ch1 and configurable amplifier Ch1.

(6) MCU initialization function (`R_Systeminit`)

Declaration	`void R_Systeminit(void)`
Overview	MCU initialization function
Parameters	None
Return value	None
Description	• Initializes the peripheral hardware in the MCU used in this application note. - Calls the `R_PORT_Create` function to initialize the ports. - Calls the `R_CGC_Create` function to initialize the clock generator. - Calls the `R_SAU1_Create` function to initialize the 3-wire serial I/O (CSI21) of channel 1 in serial array unit 1.

(7) System initialization function (`hdwinit`)

Declaration	`void hdwinit(void)`
Overview	System initialization function
Parameters	None
Return value	None
Description	• Disables interrupts. • Calls the `R_Systeminit` function to initialize the MCU. • Enables interrupts.

(8) A/D conversion control function (`ADC_Control`)

Declaration	`void ADC_Control(void)`
Overview	A/D conversion control function
Parameters	None
Return value	None
Description	Controls A/D conversion of the voltage output from the configurable amplifier (Ch1) (voltage stepped down by using a resistor divider).

(9) 1-µs unit wait function (TAU0_WAIT_1us)

Declaration	void TAU0_WAIT_1us(uint32_t wait_1us)
Overview	1-µs unit wait function
Parameters	uint32_t wait_1us: 1-µs counter
Return value	None
Description	• Calls the R_TAU0_Channel3_Stop function to stop counting using channel 3 in timer array unit 0. • Calls the R_TAU0_Channel3_Start function to start counting using channel 3 in timer array unit 0. • Decrements the value of the wait_1us parameter for the interval of channel 3 in timer array unit 0 (1 µs) until the value becomes 0.

6.6 RAM Variables

Table 6.2 RAM Variables

Data Type	Variable Name	Description	Function That Uses This Variable
volatile uint8_t *	gp_csi21_rx_address	Address of CSI21 reception buffer	R_CSI21_Send_Receive r_csi21_interrupt
volatile uint16_t	g_csi21_rx_length	Number of bytes received at CSI21	None
volatile uint16_t	g_csi21_rx_count	CSI21 received byte counter	None
volatile uint8_t *	gp_csi21_tx_address	Address of CSI21 transmission buffer	R_CSI21_Send_Receive r_csi21_interrupt
volatile uint16_t	g_csi21_send_length	Number of bytes transmitted from CSI21	R_CSI21_Send_Receive r_csi21_interrupt
volatile uint16_t	g_csi21_tx_count	CSI21 transmitted byte counter	R_CSI21_Send_Receive r_csi21_interrupt
static uint16_t	_ad_buffer	Stores the A/D conversion result.	r_adc_interrupt ADC_Get_AD_Buffer_Value
static uint8_t	g_csi21_overrun_flag	CSI21 overrun flag	R_CSI21_Send_Receive r_csi21_callback_error SPI_ControlRegister_Read SPI_ControlRegister_Write

6.7 Flowcharts

Figure 6.2 shows an overview of the processing flow used in this application note. Flowcharts for the major functions are shown in the subsequent figures.

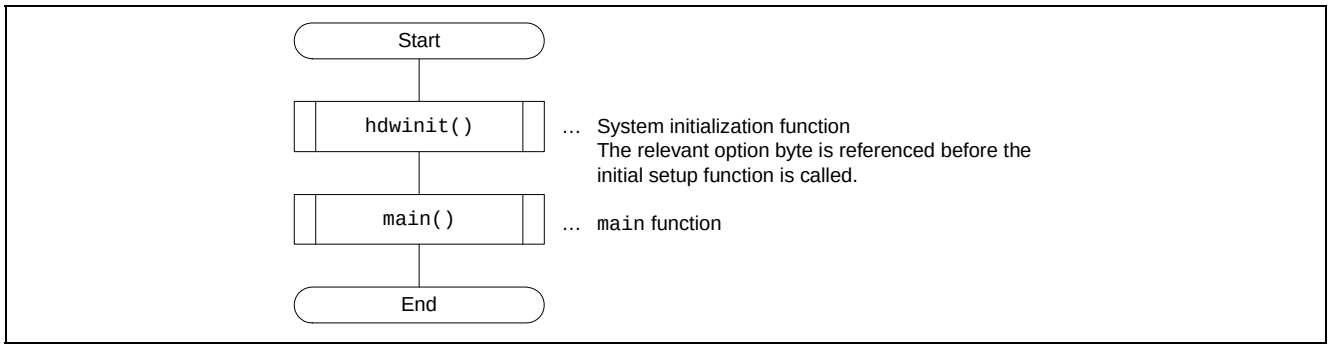


Figure 6.2 Overview of Processing Flow

(1) System initialization function (hdwinit)

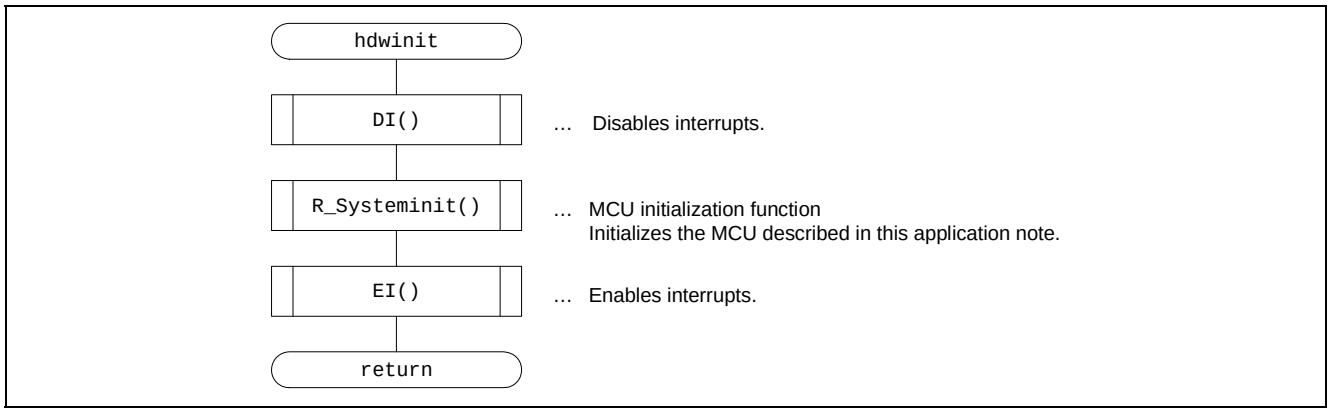


Figure 6.3 Flowchart for hdwinit Function

(2) MCU initialization function (R_Systeminit)

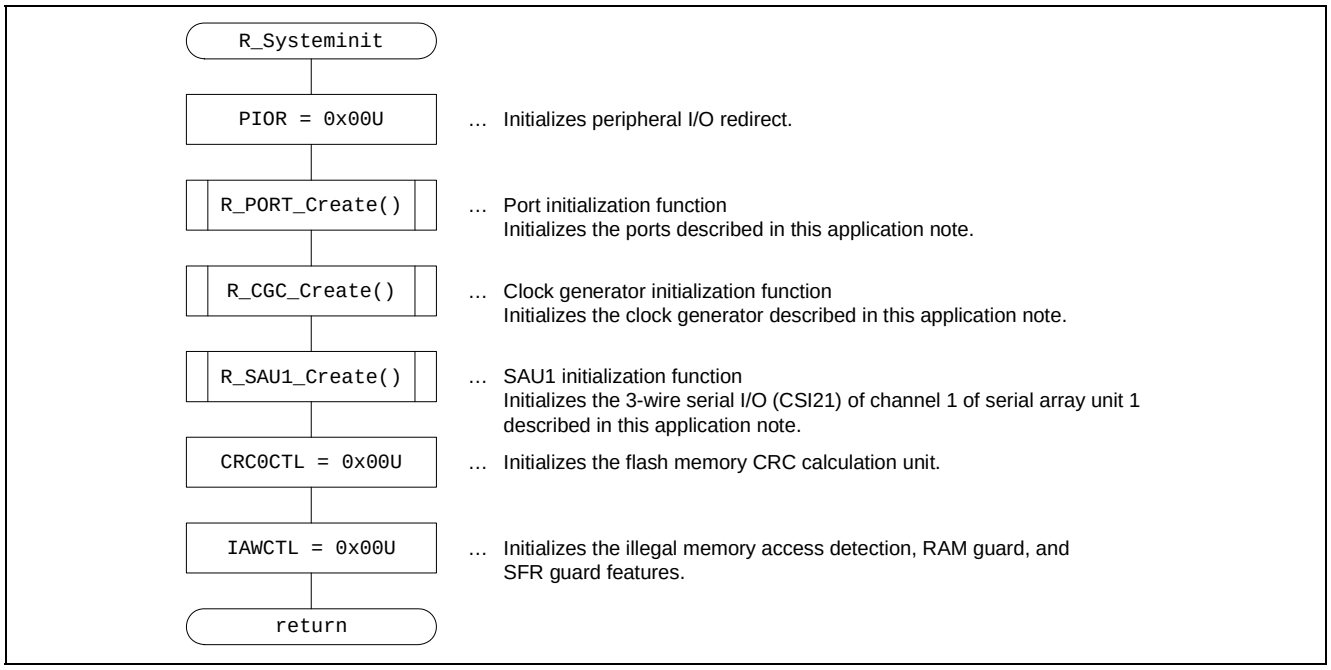


Figure 6.4 Flowchart for R_Systeminit Function

(3) `main` function (`main`)

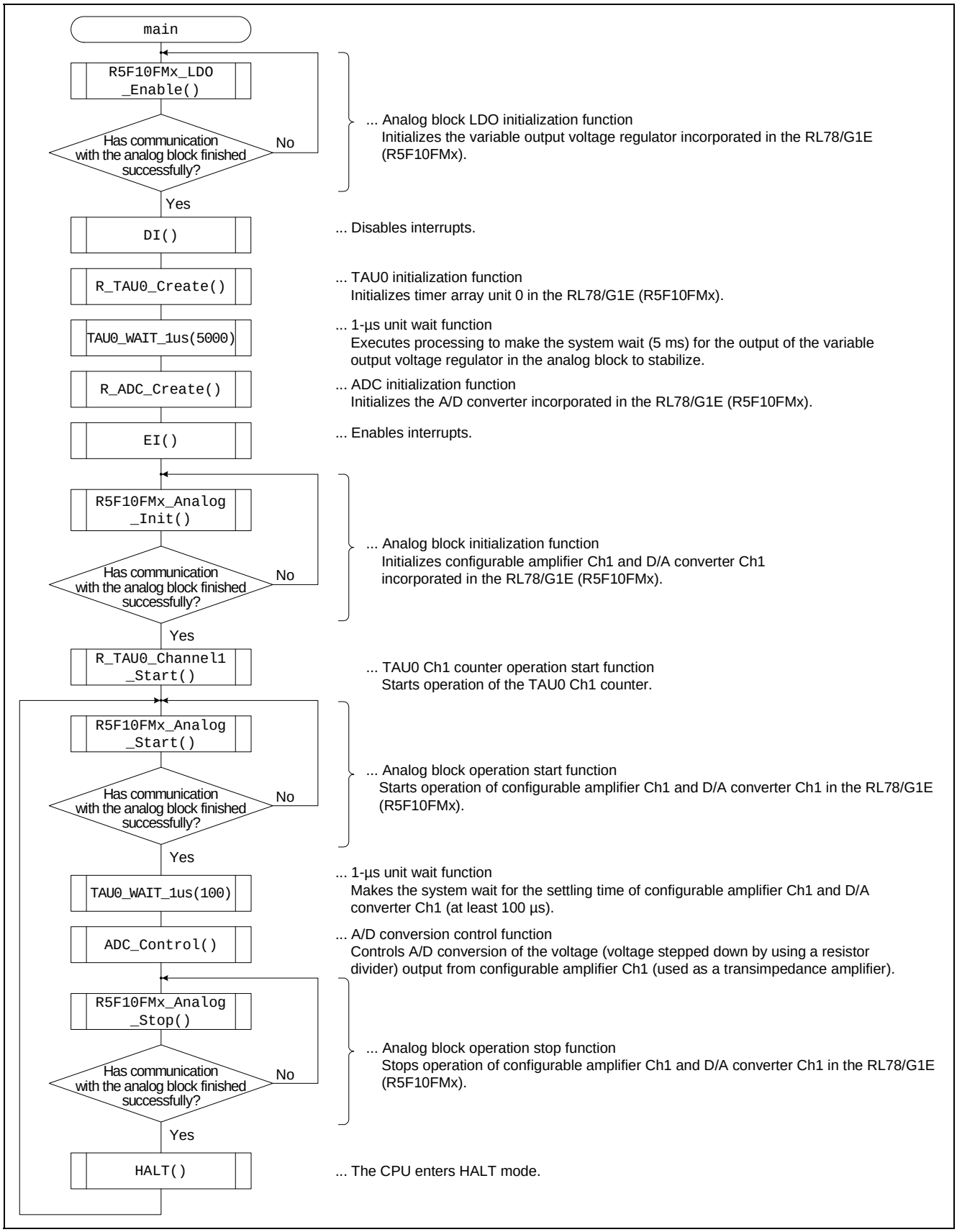


Figure 6.5 Flowchart for `main` Function

(4) Analog block LDO initialization function (R5F10FMx_LDO_Enable)

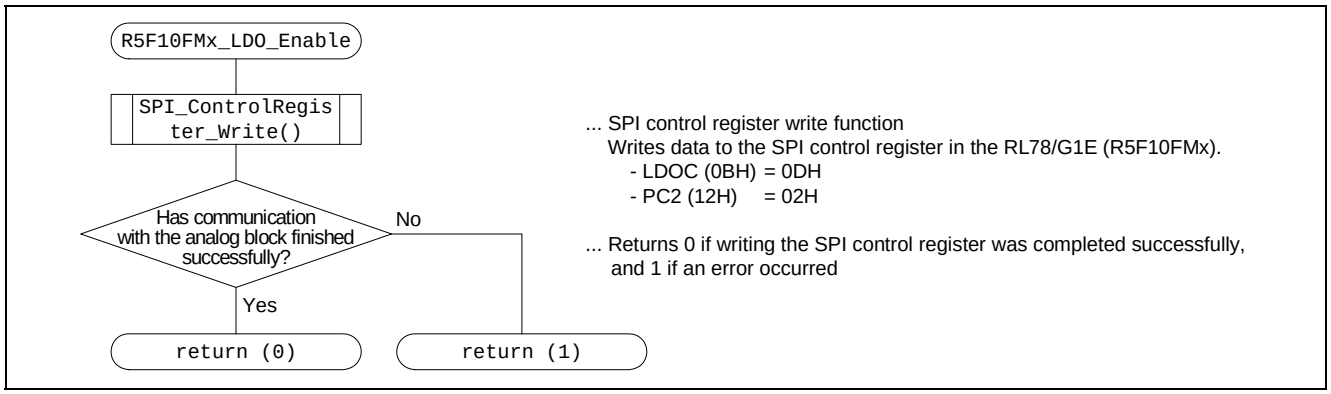


Figure 6.6 Flowchart for R5F10FMx_LDO_Enable Function

(5) Analog block initialization function (R5F10FMx_Analog_Init)

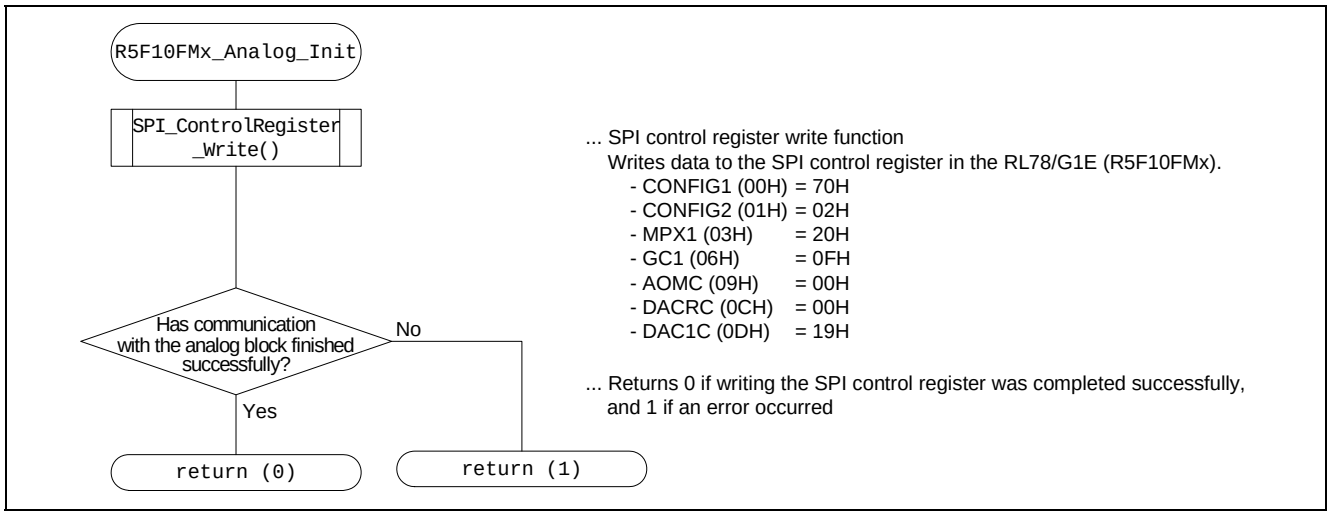


Figure 6.7 Flowchart for R5F10FMx_Analog_Init Function

(6) Analog block operation start function (R5F10FMx_Analog_Start)

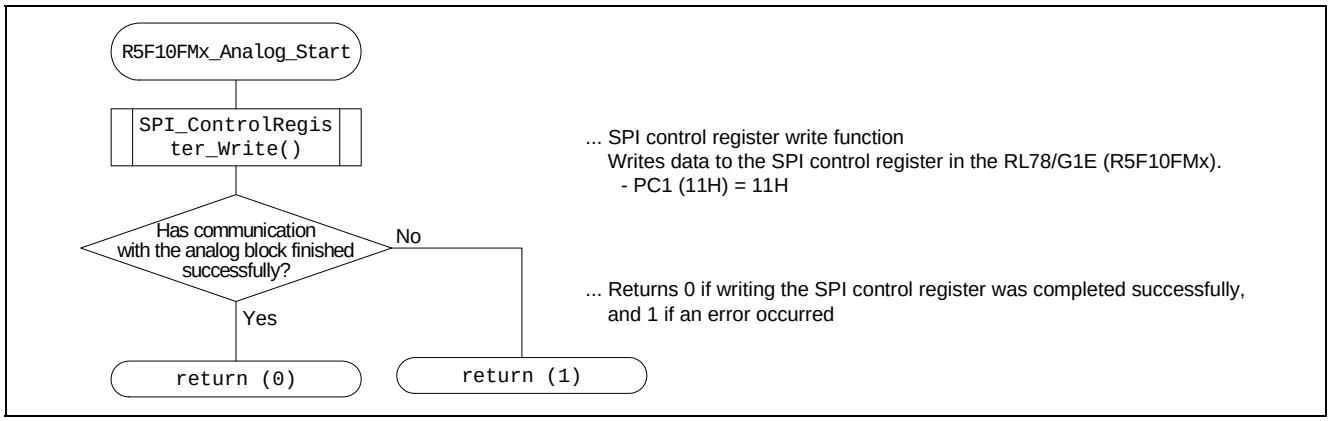


Figure 6.8 Flowchart for R5F10FMx_Analog_Start Function

(7) Analog block operation stop function (R5F10FMx_Analog_Stop)

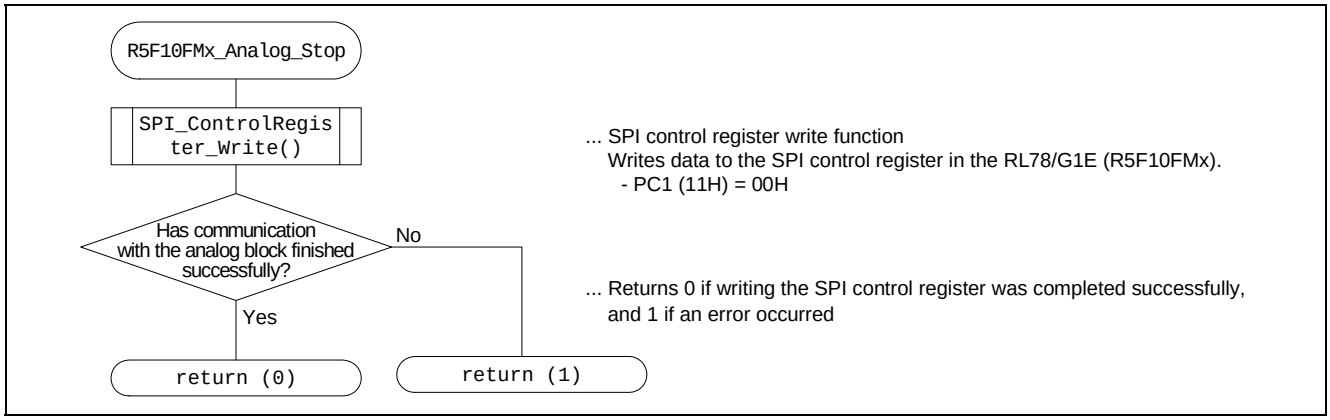


Figure 6.9 Flowchart for R5F10FMx_Analog_Stop Function

6.8 Source Files and Changes Applied to the Code Output from the Code Generator

The sample code used in this application note was created based on the code for the RL78/G1A group (R5F10ELE) output by the code generator of CubeSuite+.

The output file has been modified to apply the differences between the RL78/G1A (R5F10ELE) and RL78/G1E (R5F10FME) such as incorporated registers. **Table 6.3** and **Table 6.4** show the changes applied to the code output by the code generator. For details about the differences between the RL78/G1A (R5F10ELE) and RL78/G1E (R5F10FME), see the *RL78/G1E Hardware User's Manual*.

Table 6.3 Source Files and Changes Applied to the Code Output from the Code Generator (1/2)

File Name	Description	Changes Applied to the Code Output by the Code Generator	
		Item	Description
r_main.c	Output by the code generator	–	–
r_systeminit.c	Output by the code generator	R_systeminit function	• Commented out R_ADC_Create();. • Commented out R_TAU0_Create();.
r_cg_cgc.c	Output by the code generator	R_CGC_Create function	• Changed the value set to CMC = …;. • Commented out XSTOP = …;. • Commented out CSS = …;.
r_cg_cgc_user.c	Output by the code generator	–	–
r_cg_port.c	Output by the code generator	R_PORT_Create function	• Commented out P6 = …;. • Commented out P12 = …;. • Commented out P15 = …;. • Commented out PMC4 = …;. • Changed the value set to ADPC = …;.
r_cg_port_user.c	Output by the code generator	–	–
r_cg_serial.c	Output by the code generator	R_CSI21_Create function	• Commented out SO1 |= …;. • Commented out SO1 &= …;.
r_cg_serial_user.c	Output by the code generator	r_csi21_callback _receiveend function	• Added processing.
r_cg_adc.c	Output by the code generator	R_ADC_Create function	• Commented out PM2 |= …;. • Commented out PM15 |= …;. • Commented out PM12 |= …;. • Commented out PMC3 |= …;. • Commented out PM3 |= …;.
r_cg_adc_user.c	Output by the code generator	r_adc_interrupt function	• Added processing.
r_cg_timer.c	Output by the code generator	R_TAU0_Create function	• Commented out TOM0 &= …;. • Commented out TOL0 &= …;. • Commented out TO0 &= …;. • Commented out TOE0 &= …;.
r_cg_timer_user.c	Output by the code generator	–	–
r_cg_macrodriver.h	Output by the code generator	–	–

Table 6.4 Source Files and Changes Applied to the Code Output from the Code Generator (2/2)

File Name	Description	Changes Applied to the Code Output by the Code Generator	
		Item	Description
r_cg_userdefine.h	Output by the code generator	–	• Added the typedef and define statements.
r_cg_cgc.h	Output by the code generator	–	• Added the extern statement.
r_cg_port.h	Output by the code generator	–	• Added the extern statement.
r_cg_serial.h	Output by the code generator	–	• Added the extern statement.
r_cg_adc.h	Output by the code generator	–	• Added the extern statement.
r_cg_timer.h	Output by the code generator	–	• Added the extern statement.
lcd.c	LCD module control	–	–
lcd.h	Header file for lcd.c	–	–

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2012	—	First edition issued.
1.10	Sep. 30, 2013	—	Some descriptions are modified.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   - Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   - The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   - Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   - After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   - Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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