RL78/G14

Transferring A/D Conversion Result Using the DTC CC-RL

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Abstract

This document describes a method to use the DTC (in repeat mode) in conjunction with the A/D converter (in software trigger mode, scan mode, and one-shot conversion mode) with the RL78/G14.

Product

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This document describes an example of using the DTC (in repeat mode) in conjunction with the A/D converter (in software trigger mode, scan mode, and one-shot conversion mode). Perform A/D conversion on analog input voltage input to pins P20/ANI0 to P23/ANI3 while in scan mode, and use DTC transfer to store the A/D converted value to the RAM. Perform A/D conversion for individual pins successively. Every time A/D conversion for a pin is completed, store the converted result to the 10-bit A/D conversion result register (ADCR), activate the DTC, and transfer the A/D converted result from the ADCR register to the RAM. When A/D conversion and DTC transfer for all of the above pins are completed, an A/D conversion end interrupt request is generated.

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows the Operation Overview.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
DTC	Transfer the A/D converted result to the RAM
A/D converter	Perform A/D conversion on analog input voltage

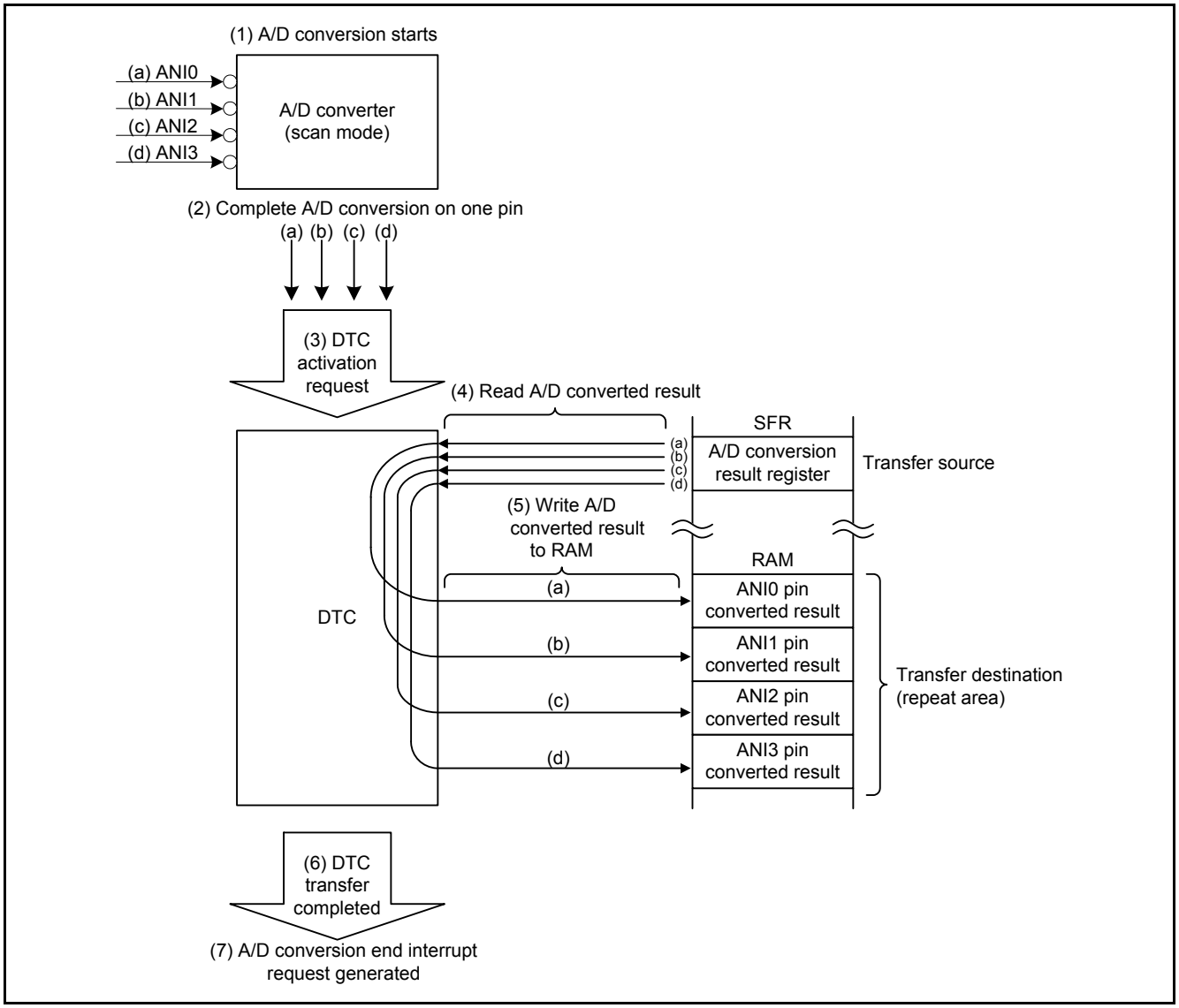


Figure 1.1 Operation Overview

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104LEA)
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}): 64 MHz (typical) • CPU/peripheral hardware clock (f_{CLK}): 32 MHz
Operating voltage	5.0 V (2.9 to 5.5 V) LVD operation (V_{LVD}): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment (CS+)	Renesas Electronics Corporation CS+ V3.01.00
C compiler (CS+)	Renesas Electronics Corporation CC-RL V1.01.00
Integrated development environment (e^2 studio)	Renesas Electronics Corporation e^2 studio V4.0.0.26
C compiler (e^2 studio)	Renesas Electronics Corporation CC-RL V1.01.00

3. Reference Application Note

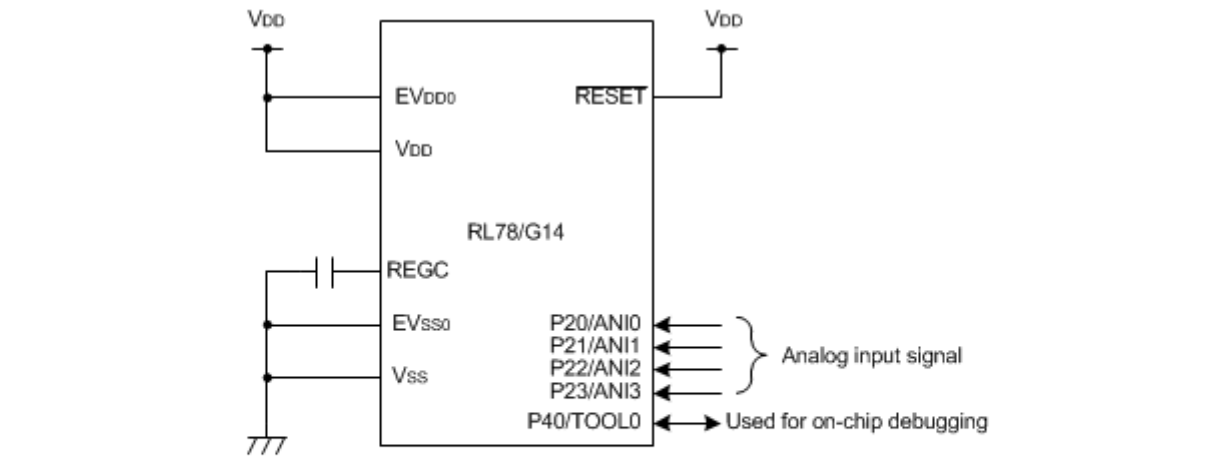
For additional information associated with this document, refer to the following application note.

- RL78/G14 How to Use the DTC for the RL78/G14 (R01AN0861E)

4. Hardware

4.1 Hardware Configuration

Figure 4.1 shows the Hardware Configuration used in this document.



Notes:
1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics. Connect input-only ports independently to VDD or VSS via resistors.
2. Connect pins with names that begin with EVSS to VSS, and pins with names that begin with EVDD to VDD.
3. Make sure to set VDD greater than the detection voltage (VLVD) specified by the LVD.

Figure 4.1 Hardware Configuration

4.2 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P20/ANI0	Input	A/D converter input (ANI0)
P21/ANI1	Input	A/D converter input (ANI1)
P22/ANI2	Input	A/D converter input (ANI2)
P23/ANI3	Input	A/D converter input (ANI3)

5. Software

5.1 Operation Overview

In this sample program, the results of four pins that are A/D converted in scan mode are stored to the RAM using DTC transfer. Set the transfer destination as a repeat area using DTC repeat mode, and store the A/D converted results of the four pins to RAM successively.

When A/D conversion of the ANI0 pin is completed, the first DTC transfer from the transfer source address (ADCR register (FFFF1EH and FFFF1FH) to the transfer destination address (ad_value[0] (FFF500H to FFF501H)) is performed. When A/D conversion of the ANI1 pin is completed, the second DTC transfer is performed. Since the transfer destination is set as a repeat area, the A/D converted result is transferred to ad_value[1] (FFF502H to FFF503H). In the same procedure, DTC transfer for the A/D converted results of pins ANI3 and ANI4 is performed. When the fourth DTC transfer is completed, an A/D conversion end interrupt is generated.

Table 5.1 lists the DTC Settings and Table 5.2 lists the A/D Converter Settings.

Table 5.1 DTC Settings

Function Name	Setting Value
	Control data 0
Transfer mode	Repeat mode
Repeat mode interrupt	Enabled
Source address control	Fixed
Destination address control	Repeat area
Chain transfer	Disabled
Transfer block size	2 bytes
Number of DTC transfers	4
Transfer source address	ADCR (FFF1EH to FFF1FH)
Transfer destination address	ad_value[0] (FF500H to FF501H) ad_value[1] (FF502H to FF503H) ad_value[2] (FF504H to FF505H) ad_value[3] (FF506H to FF507H)

Table 5.2 A/D Converter Settings

Setting Item	Setting Value
Conversion Clock (f_{AD})	f_{CLK}/64
A/D conversion modes	• A/D conversion trigger mode: Software trigger mode • A/D conversion channel selection mode: Scan mode • A/D conversion operating mode: One-shot conversion mode
Resolution	10 bits
Analog input channels	• Scan 0: ANI0 • Scan 1: ANI1 • Scan 2: ANI2 • Scan 3: ANI3
Conversion result comparison upper limit (ADUL register)	FFH
Conversion result comparison lower limit (ADLL register)	00H
Conversion result upper limit/lower limit check	INTAD is generated when ADLL register ≤ ADCR register ≤ ADUL

(1) Perform the initial setting for the A/D converter and DTC.
(2) Set the ADCS bit in the ADM0 register to 1 (conversion operation enabled) to start A/D conversion.
(3) When A/D conversion of pins ANI0, ANI1, ANI2, and ANI3 is completed, the DTC is activated.
(4) The DTC reads the A/D converted results from the ADCR register and transfers them to the RAM (ad_value[0] to ad_value[3]) corresponding to each pin.
(5) When the fourth DTC transfer is completed, an A/D conversion end interrupt is generated. The A/D converted results of ad_value[0] to ad_value[3] are shifted 6 bits in an interrupt service routine and stored to variables an0_value to an3_value.
(6) Determine if DTC activation is disabled by a program, enable DTC activation again, and start A/D conversion.
(7) Repeat steps (2) to (6).

Figure 5.1 shows an Timing Diagram of DTC Transfer and A/D Conversion.

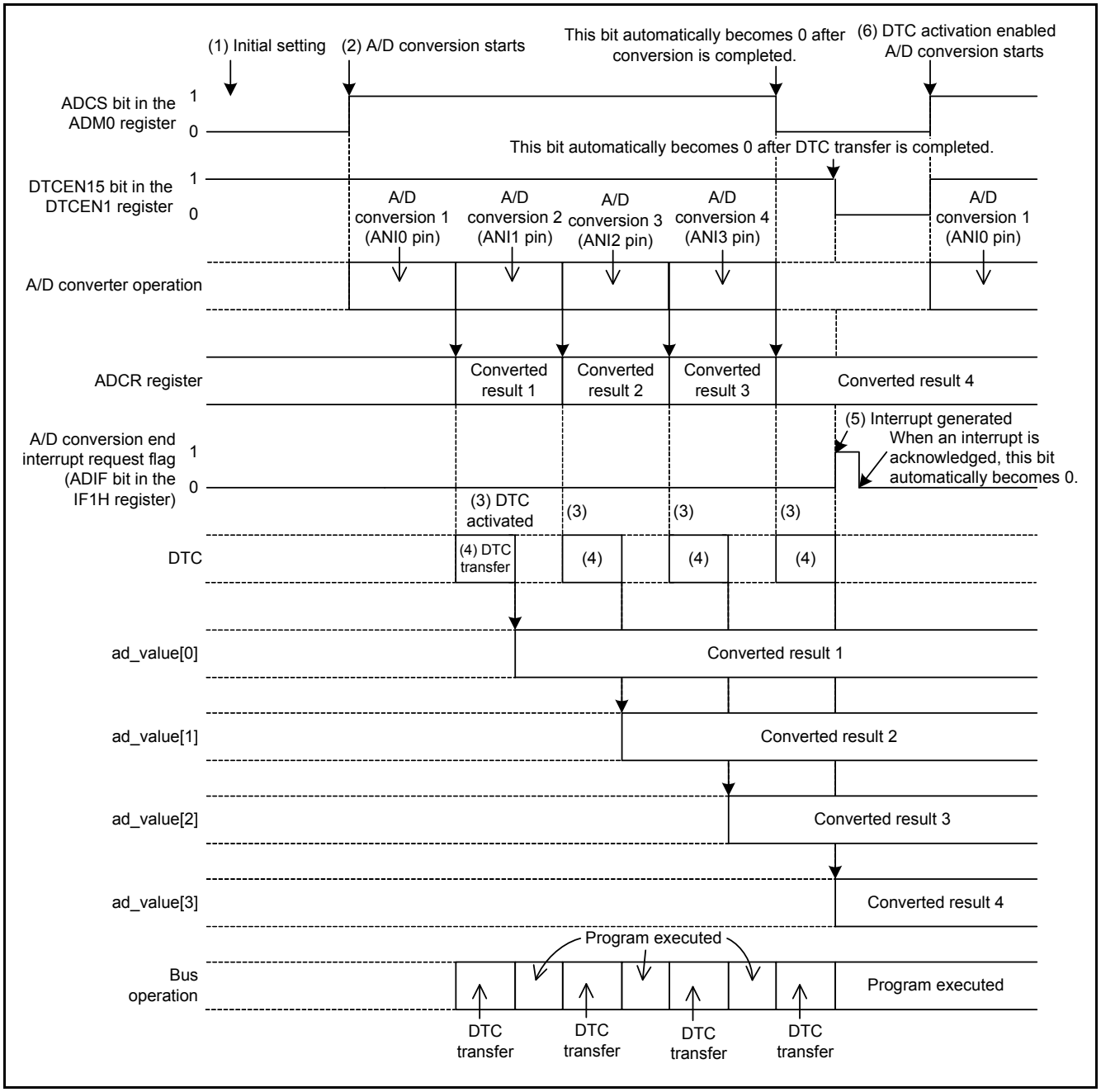


Figure 5.1 Timing Diagram of DTC Transfer and A/D Conversion

5.2 Option Byte Settings

Table 5.3 lists the Option Byte Settings. When necessary, set a value suited to the user system.

Table 5.3 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11111000B	Internal high-speed oscillation HS mode: 64 MHz
000C3H/010C3H	10000100B	On-chip debug enabled

5.3 Constant

Table 5.4 lists the Constant Used in the Sample Code.

Table 5.4 Constant Used in the Sample Code

Constant Name	Setting Value	Contents
ad_value	0FF500H	DTC transfer destination address

5.4 Variables

Table 5.5 lists the Global Variables.

Table 5.5 Global Variables

Type	Variable Name	Contents	Function Used
int16_t __near	ad_value[4]	A/D converted result storage address of ANI0 to ANI3	r_adc_interrupt
uint16_t	an0_value	Store A/D converted result of ANI0	r_adc_interrupt
uint16_t	an1_value	Store A/D converted result of ANI1	r_adc_interrupt
uint16_t	an2_value	Store A/D converted result of ANI2	r_adc_interrupt
uint16_t	an3_value	Store A/D converted result of ANI3	r_adc_interrupt

5.5 Functions

Table 5.6 lists the Functions.

Table 5.6 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	CPU initial setting
R_ADC_Create	Initial setting of A/D converter
R_DTC_Create	Initial setting of DTC
main	Main processing
R_DTCD0_Start	DTC activation
R_ADC_Start	A/D conversion start
r_adc_interrupt	A/D conversion interrupt

5.6 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	CPU initial setting
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_ADC_Create	
Outline	Initial setting of A/D converter
Header	None
Declaration	void R_ADC_Create(void)
Description	Perform the initial setting to use the A/D converter in software trigger mode, scan mode, and one-shot conversion mode
Argument	None
Return Value	None

R_DTC_Create	
Outline	Initial setting of DTC
Header	None
Declaration	void R_DTC_Create(void)
Description	Perform the initial setting to use the DTC in repeat mode.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_DTCD0_Start	
Outline	DTC activation
Header	None
Declaration	void R_DTCD0_Start(void)
Description	Enable DTC activation.
Argument	None
Return Value	None

R_ADC_Start	
Outline	A/D conversion start
Header	None
Declaration	void R_ADC_Start(void)
Description	Perform A/D conversion.
Argument	None
Return Value	None

r_adc_interrupt	
Outline	A/D conversion interrupt
Header	None
Declaration	static void __near r_adc_interrupt(void)
Description	Perform an A/D conversion interrupt service routine.
Argument	None
Return Value	None

5.7 Flowcharts

5.7.1 Overall Flowchart

Figure 5.2 shows the Overall Flowchart.

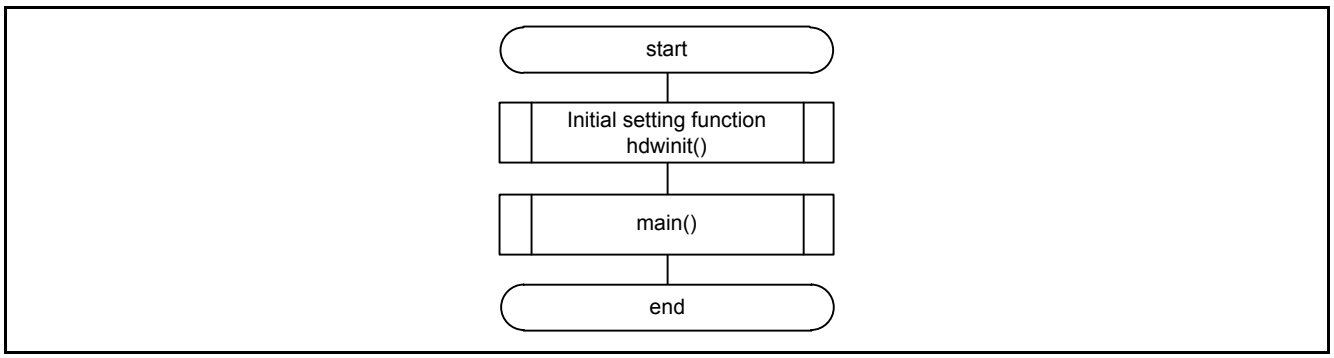


Figure 5.2 Overall Flowchart

5.7.2 Initial Setting

Figure 5.3 shows the Initial Setting.

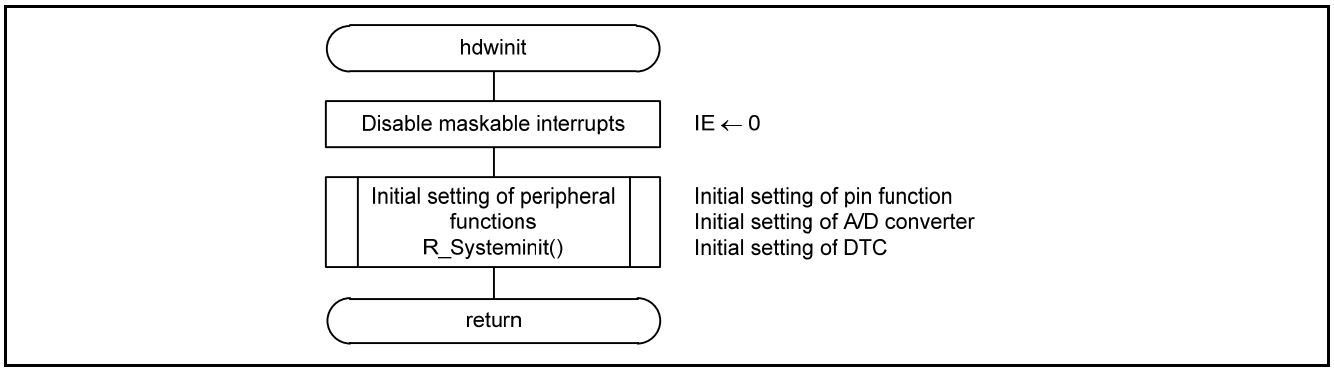


Figure 5.3 Initial Setting

5.7.3 Initial Setting of Peripheral Functions

Figure 5.4 shows the Initial Setting of Peripheral Functions.

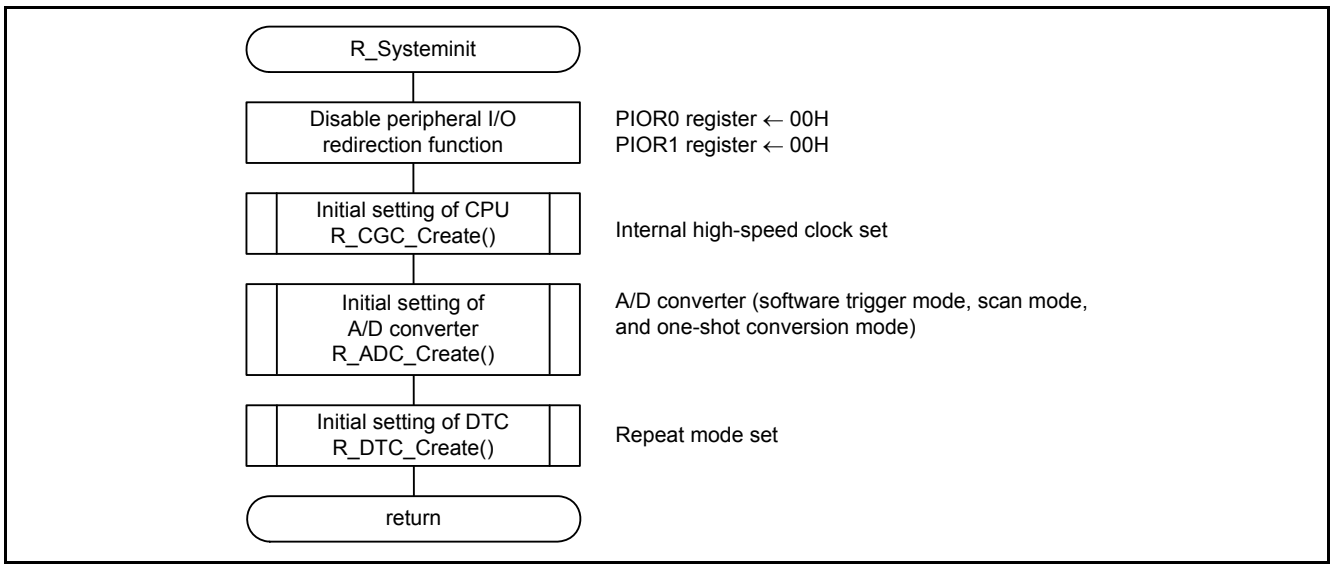


Figure 5.4 Initial Setting of Peripheral Functions

5.7.4 Initial Setting of CPU

Figure 5.5 shows the Initial Setting of the CPU.

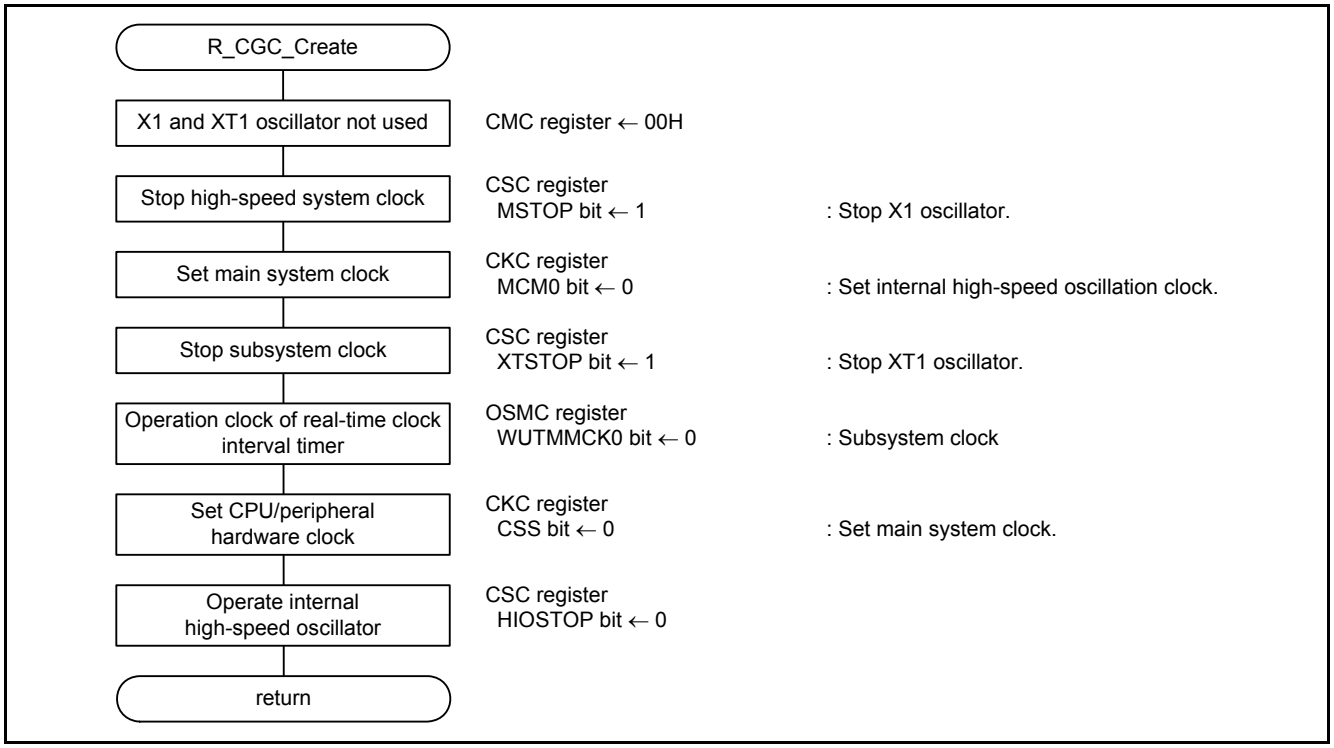


Figure 5.5 Initial Setting of the CPU

5.7.5 Initial Setting of the A/D Converter

Figure 5.6 shows the Initial Setting of the A/D Converter.

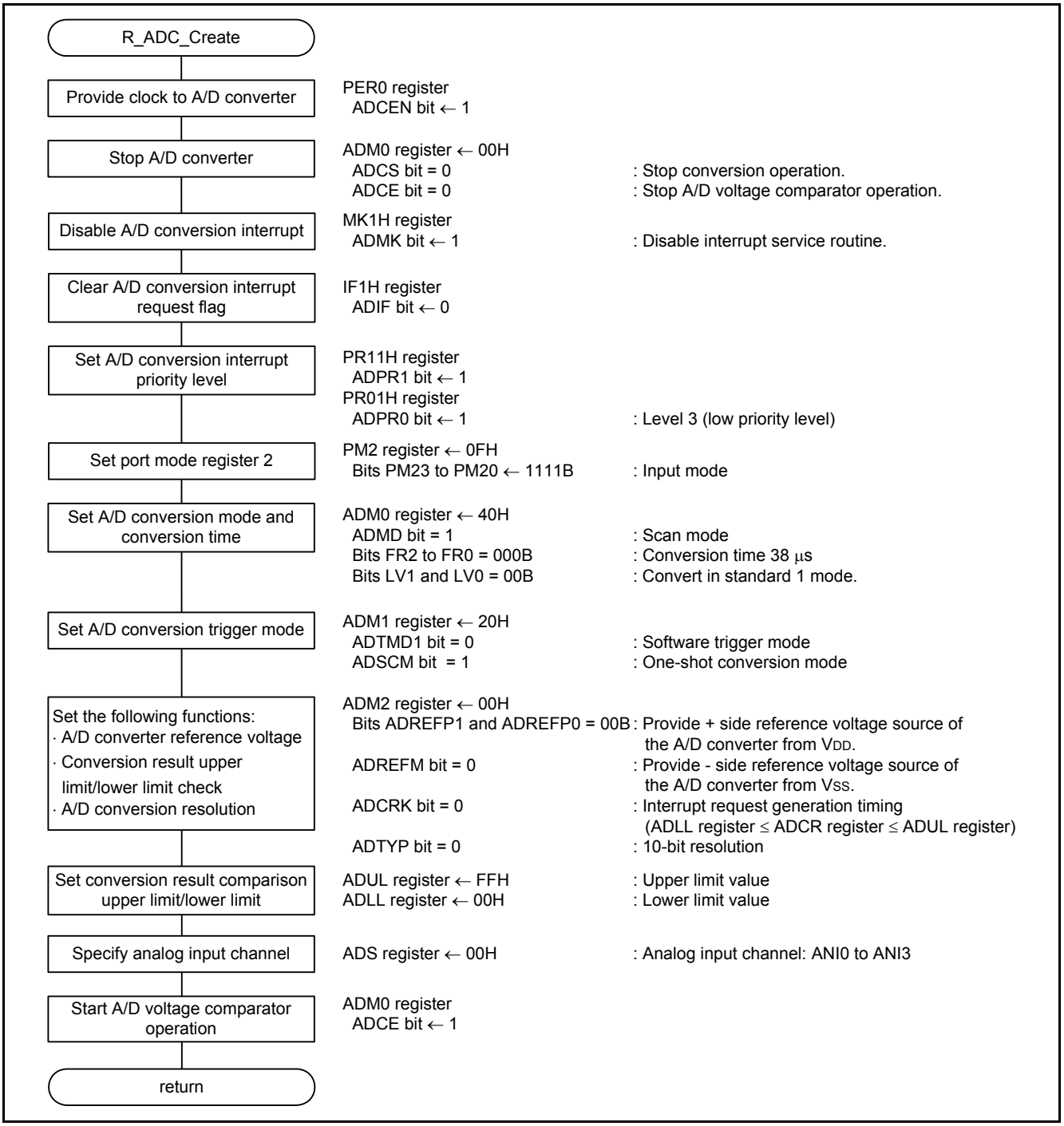


Figure 5.6 Initial Setting of the A/D Converter

Start providing a clock to the A/D converter.

- Peripheral Enable Register 0 (PER0)
  Provide a clock to the A/D converter.

Symbol	7	6	5	4	3	2	1	0
PER0	RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
Setting Value	x	x	1	x	x	x	x	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFR used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFR used by the A/D converter can be read/written.

Stop the A/D converter.

- A/D Converter Mode Register 0 (ADM0)
  Stop the A/D converter.

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Setting Value	0							0

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	Enables conversion operation [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: Stabilization wait status + conversion operation status

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable an A/D conversion interrupt.

- Interrupt Mask Flag Register (MK1H)
  Disable an A/D conversion interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
Setting Value	x	x	x	x	x	x	x	1

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Set the A/D conversion interrupt request flag

- Interrupt Request Flag Register (IF1H)
  Clear the A/D conversion interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	TIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
Setting Value	x	x	x	x	x	x	x	0

Bit 0

ADIF	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the A/D conversion interrupt priority level.

- Priority Specification Flag Registers (PR11H and PR01H)
  Set to level 3 (low priority).

Symbol	7	6	5	4	3	2	1	0
PR11H	TMPR110	TRJPR10	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
Setting Value	x	x	x	x	x	x	x	1

Symbol	7	6	5	4	3	2	1	0
PR01H	TMPR010	TRJPR00	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
Setting Value	x	x	x	x	x	x	x	1

Bit 0

ADPR1	ADPR0	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Set port mode register 2.

- Port Mode Register 2 (PM2)
  Set port mode register 2 to input mode.

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
Setting Value	x	x	x	x	1	1	1	1

Bit 3

PM23	P23 pin I/O mode selection (m = 0 to 8, 10 to 12, 14, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 2

PM22	P22 pin I/O mode selection (m = 0 to 8, 10 to 12, 14, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 1

PM21	P21 pin I/O mode selection (m = 0 to 8, 10 to 12, 14, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 0

PM20	P20 pin I/O mode selection (m = 0 to 8, 10 to 12, 14, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Set A/D conversion mode and conversion time.

- A/D Converter Mode Register 0 (ADM0)
  Set A/D conversion mode and conversion time.

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Setting Value		1	0	0	0	0	0	

Bit 6

ADMD	Specification of the A/D conversion channel selection mode
0	Select mode
1	Scan mode

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bits 5 to 1

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	38 μs	f_{CLK}/64
0	0	1								38 μs	19 μs	f_{CLK}/32
0	1	0							38 μs	19 μs	9.5 μs	f_{CLK}/16
0	1	1						38 μs	19 μs	9.5 μs	4.75 μs	f_{CLK}/8
1	0	0						28.5 μs	14.25 μs	7.125 μs	3.5625 μs	f_{CLK}/6
1	0	1						23.75 μs	11.875 μs	5.938 μs	2.9688 μs	f_{CLK}/5
1	1	0					38 μs	19 μs	9.5 μs	4.75 μs	2.375 μs	f_{CLK}/4
1	1	1				38 μs	19 μs	9.5 μs	4.75 μs	2.375 μs	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	34 μs	f_{CLK}/64
0	0	1								34 μs	17 μs	f_{CLK}/32
0	1	0							34 μs	17 μs	8.5 μs	f_{CLK}/16
0	1	1						34 μs	17 μs	8.5 μs	4.25 μs	f_{CLK}/8
1	0	0						25.5 μs	12.75 μs	6.375 μs	3.1875 μs	f_{CLK}/6
1	0	1						21.25 μs	10.625 μs	5.3125 μs	2.6563 μs	f_{CLK}/5
1	1	0					34 μs	17 μs	8.5 μs	4.25 μs	2.125 μs	f_{CLK}/4
1	1	1				34 μs	17 μs	8.5 μs	4.25 μs	2.125 μs	Setting prohibited	f_{CLK}/2
×	×	×	1	0	Low voltage 1	Setting prohibited						—
×	×	×	1	1	Low voltage 2	Setting prohibited						—

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set A/D conversion trigger mode.

- A/D Converter Mode Register 1 (ADM1)
  Select the A/D conversion trigger.

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
Setting Value	0	x	1	—	—	—	x	x

Bits 7 and 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	—	Software trigger mode
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	One-shot conversion mode

Set A/D conversion trigger mode.

- A/D Converter Mode Register 2 (ADM2)
  Set the A/D converter reference voltage, check the upper limit and lower limit conversion result, and set the resolution..

Symbol	7	6	5	4	3	2	1	0
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADCRK	AWC	0	ADTYP
Setting Value	0	0	0	—	0	x	—	0

Bits 7 and 6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage (1.44 V)
1	1	Setting prohibited

Only rewrite the values of the ADREFP1 and ADREFP0 bits after clearing ADREFP1 and ADREFP0 to 0.
However, to rewrite ADREFP1 and ADREFP0 with 1 and 0, respectively, perform the following procedure:
(1) Clear ADCE to 0.
(2) Set ADREFP1 and ADREFP0 to 1 and 0, respectively.
(3) Set ADCE to 1.
Note that a wait time (T.B.D) is required between steps (1) to (3).
When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output. Be sure to perform A/D conversion while ADISS = 0.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 5

ADREFM	Selection of the − side reference voltage source of the A/D converter
0	Supplied from VSS
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADCRK	Checking the upper limit and lower limit conversion result values
0	The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register
1	The interrupt signal (INTAD) is output when the ADCR register ≤ the ADLL register or the ADUL register ≤ the ADCR register

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	10-bit resolution
1	8-bit resolution

Set the conversion result comparison upper limit.

- Conversion Result Comparison Upper Limit Setting Register (ADUL)
  Set FFH to the conversion result comparison upper limit.

Symbol	7	6	5	4	3	2	1	0
ADUL	ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
Setting Value	1	1	1	1	1	1	1	1

Set the conversion result comparison lower limit.

- Conversion Result Comparison Lower Limit Setting Register (ADLL)
  Set 00H to the conversion result comparison lower limit.

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
Setting Value	0	0	0	0	0	0	0	0

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set analog input channels.

- Analog Input Channel Specification Register (ADS)
  Set analog input channels to ANI0 to ANI3.

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
Setting Value	x	—	—	0	0	0	0	0

Bits 3 to 0

ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel			
					Scan 0	Scan 1	Scan 2	Scan 3
0	0	0	0	0	ANI0	ANI1	ANI2	ANI3
0	0	0	0	1	ANI1	ANI2	ANI3	ANI4
0	0	0	1	0	ANI2	ANI3	ANI4	ANI5
0	0	0	1	1	ANI3	ANI4	ANI5	ANI6
0	0	1	0	0	ANI4	ANI5	ANI6	ANI7
0	0	1	0	1	ANI5	ANI6	ANI7	ANI8
0	0	1	1	0	ANI6	ANI7	ANI8	ANI9
0	0	1	1	1	ANI7	ANI8	ANI9	ANI10
0	1	0	0	0	ANI8	ANI9	ANI10	ANI11
0	1	0	0	1	ANI9	ANI10	ANI11	ANI12
0	1	0	1	0	ANI10	ANI11	ANI12	ANI13
0	1	0	1	1	ANI11	ANI12	ANI13	ANI14
Other than the above					Setting prohibited			

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the A/D voltage comparator.

- A/D Converter Mode Register 0 (ADM0)
  Start A/D voltage comparator operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Setting Value								1

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5.7.6 Initial Setting of DTC

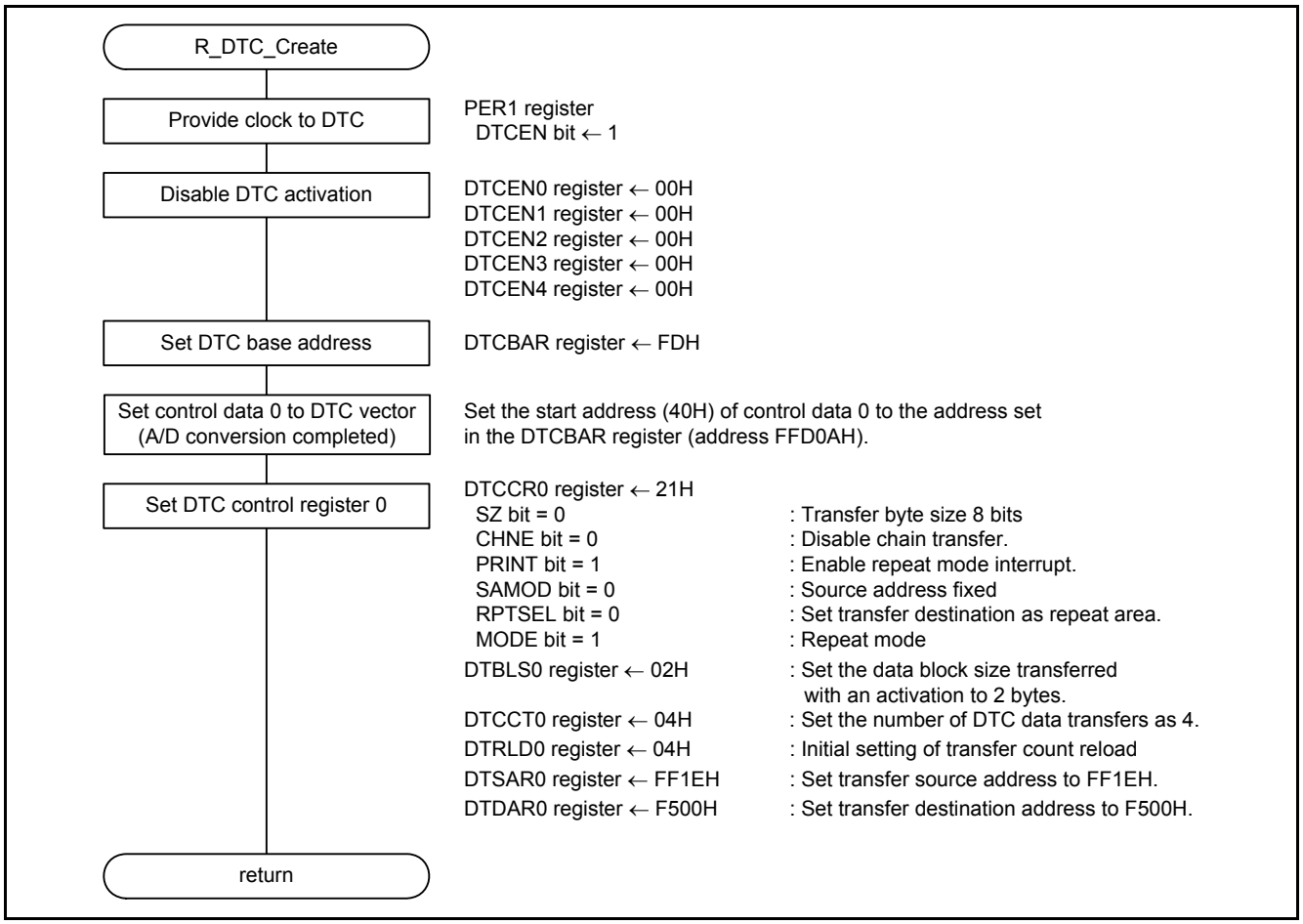


Figure 5.7 Initial Setting of the DTC

Start providing a clock to the DTC.

- Peripheral Enable Register 1 (PER1)
  Provide a clock to the DTC.

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
Setting Value	x	x	x	x	1	—	—	1

Bit 3

DTCEN	Control of DTC input clock supply
0	Stops input clock supply.
1	Enables input clock supply.

Disable DTC activation.

- DTC Activation Enable Register i (DTCENi) (i = 0 to 4)
  Disable DTC activation.

Symbol	7	6	5	4	3	2	1	0
DTCENi	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
Setting Value	0	0	0	0	0	0	0	0

Bit 7

DTCENi7	DTC activation enable i7
0	Activation disabled
1	Activation enabled
The DTCENi7 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 6

DTCENi6	DTC activation enable i6
0	Activation disabled
1	Activation enabled
The DTCENi6 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 5

DTCENi5	DTC activation enable i5
0	Activation disabled
1	Activation enabled
The DTCENi5 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 4

DTCENi4	DTC activation enable i4
0	Activation disabled
1	Activation enabled
The DTCENi4 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 3

DTCENi3	DTC activation enable i3
0	Activation disabled
1	Activation enabled
The DTCENi3 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 2

DTCENi2	DTC activation enable i2
0	Activation disabled
1	Activation enabled
The DTCENi2 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 1

DTCENi1	DTC activation enable i1
0	Activation disabled
1	Activation enabled
The DTCENi1 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 0

DTCENi0	DTC activation enable i0
0	Activation disabled
1	Activation enabled
The DTCENi0 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the DTC base address.

- DTC Base Address Register (DTCBAR)
  Set FDH to the DTC base address.

Symbol	7	6	5	4	3	2	1	0
DTCBAR	DTCBAR7	DTCBAR6	DTCBAR5	DTCBAR4	DTCBAR3	DTCBAR2	DTCBAR1	DTCBAR0
Setting Value	1	1	1	1	1	1	0	1

Set the DTC control register.

- DTC Control Register 0 (DTCCR0)
  Set DTC control register 0.

Symbol	7	6	5	4	3	2	1	0
DTCCR0	0	SZ	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
Setting Value	—	0	1	0	0	0	0	1

Bit 6

SZ	Data size selection
0	8 bits
1	16 bits

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	Interrupt generation disabled
1	Interrupt generation enabled
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	Chain transfers disabled
1	Chain transfers enabled
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 2

SAMOD	Transfer source address control
0	Fixed
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 1

RPTSEL	Repeat area selection
0	Transfer destination is the repeat area
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	Normal mode
1	Repeat mode

Set DTC block size register 0.

- DTC Block Size Register 0 (DTBLS0)
  Set 02H (2 bytes) to DTC block size register 0.

Symbol	7	6	5	4	3	2	1	0
DTBLS0	DTBLS0	DTBLS06	DTBLS05	DTBLS04	DTBLS03	DTBLS02	DTBLS01	DTBLS00
Setting Value	0	0	0	0	0	0	1	0

DTBLS0	Transfer Block Size	
	8-bit transfer	16-bit transfer
00H	256 bytes	512 bytes
01H	1 byte	2 bytes
02H	2 bytes	4 bytes
03H	3 bytes	6 bytes
• • •	• • •	• • •
FDH	253 bytes	506 bytes
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set DTC transfer count register 0.

- DTC Transfer Count Register (DTCCT0)
  Set 04H (four times) to the DTC transfer count register.

Symbol	7	6	5	4	3	2	1	0
DTCCT0	DTCCT07	DTCCT06	DTCCT05	DTCCT04	DTCCT03	DTCCT02	DTCCT01	DTCCT00
Setting Value	0	0	0	0	0	1	0	0

DTCCT0	Number of Transfers
00H	256
01H	1
02H	2
03H	3
•	•
•	•
•	•
FDH	253
FEH	254
FFH	255

Set DTC transfer count reload register 0.

- DTC Transfer Count Reload Register 0 (DTRLD0)
  Set 04H (four times) to DTC transfer count reload register 0.

Symbol	7	6	5	4	3	2	1	0
DTRLD0	DTRLD07	DTRLD06	DTRLD05	DTRLD04	DTRLD03	DTRLD02	DTRLD01	DTRLD00
Setting Value	0	0	0	0	0	1	0	0

Set DTC source address register 0.

- DTC Source Address Register 0 (DTSAR0)
  Set FF1EH to DTC source transfer source address 0.

Symbol	15	14	13	12	11	10	9	8
DTSAR0	DTS AR015	DTS AR014	DTS AR013	DTS AR012	DTS AR011	DTS AR010	DTS AR09	DTS AR08
Setting Value	1	1	1	1	1	1	1	1

Symbol	7	6	5	4	3	2	1	0
DTSAR0	DTS AR07	DTS AR06	DTS AR05	DTS AR04	DTS AR03	DTS AR02	DTS AR01	DTS AR00
Setting Value	0	0	0	1	1	1	1	0

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set DTC destination address register 0.

- DTC Destination Address Register 0 (DTDAR0)
  Set F500H to DTC destination address register 0.

Symbol	15	14	13	12	11	10	9	8
DTDAR0	DTD AR015	DTD AR014	DTD AR013	DTD AR012	DTD AR011	DTD AR010	DTD AR09	DTD AR08
Setting Value	1	1	1	1	0	1	0	1

Symbol	7	6	5	4	3	2	1	0
DTDAR0	DTD AR07	DTD AR06	DTD AR05	DTD AR04	DTD AR03	DTD AR02	DTD AR01	DTD AR00
Setting Value	0	0	0	0	0	0	0	0

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5.7.7 Main Processing

Figure 5.8 shows the Main Processing.

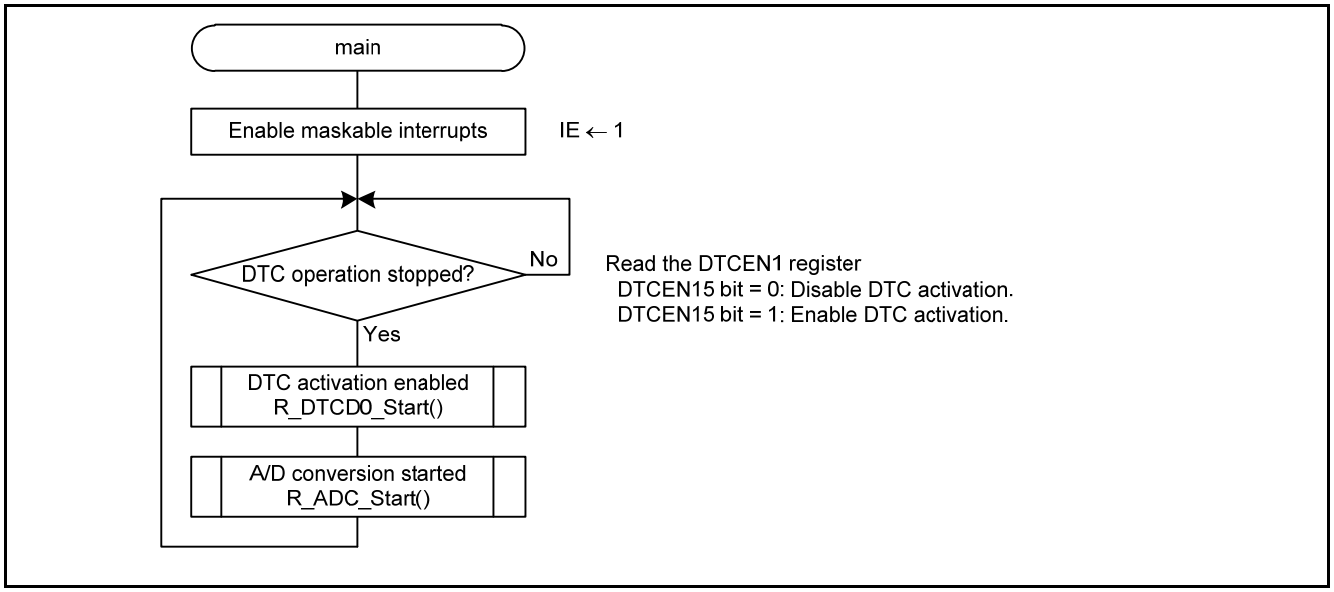


Figure 5.8 Main Processing

5.7.8 DTC Activation

Figure 5.9 shows the DTC Activation.

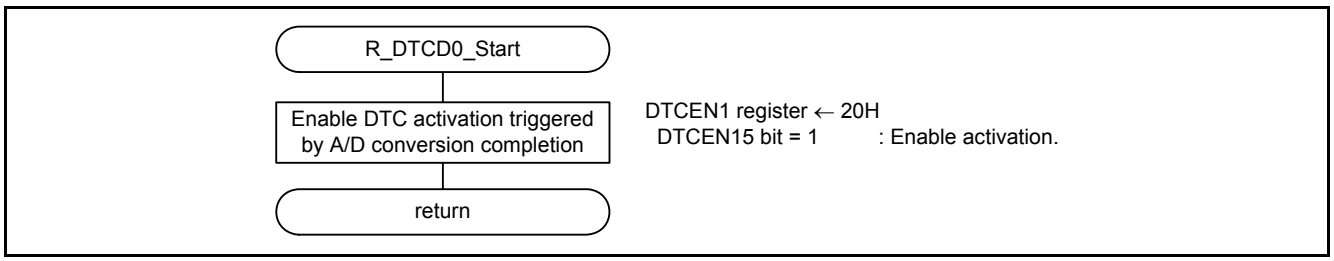


Figure 5.9 DTC Activation

Enable DTC activation.

- DTC Activation Enable Register 1 (DTCEN1)
  Enable DTC activation.

Symbol	7	6	5	4	3	2	1	0
DTCEN1	DTCEN17	DTCEN16	DTCEN15	DTCEN14	DTCEN13	DTCEN12	DTCEN11	DTCEN10
Setting Value			1					

Bit 5

DTCEN15	DTC activation enable 15
0	Activation disabled
1	Activation enabled
The DTCEN15 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5.7.9 A/D Conversion Start

Figure 5.10 shows the A/D Conversion Start.

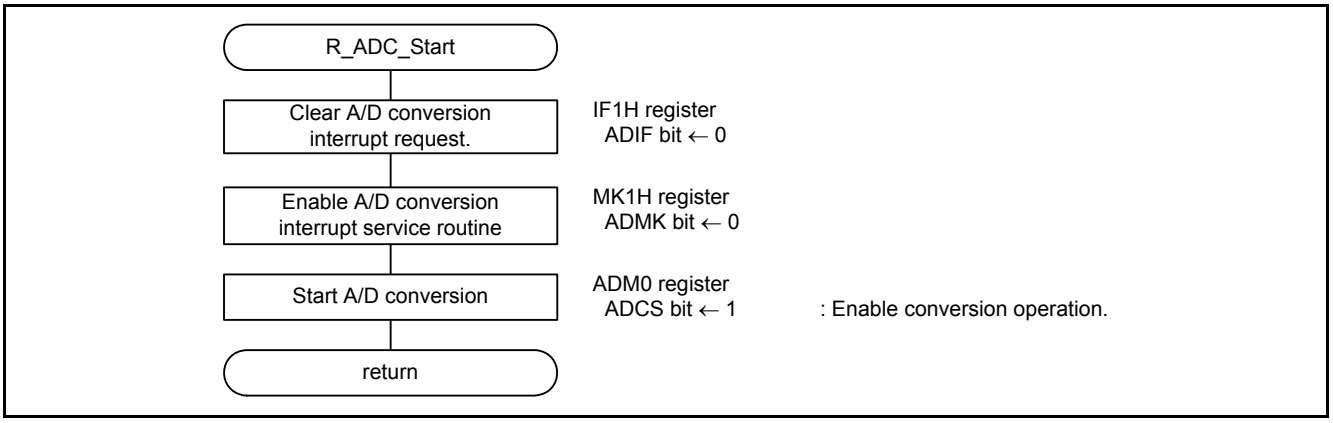


Figure 5.10 A/D Conversion Start

Set the A/D conversion interrupt request flag.

- Interrupt Request Flag Register (IF1H)
  Clear the A/D conversion interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	TIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
Setting Value	x	x	x	x	x	x	x	0

Bit 0

ADIF	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Disable A/D conversion interrupts.

- Interrupt Mask Flag Register (MK1H)
  Disable A/D conversion interrupts.

Symbol	7	6	5	4	3	2	1	0
MK1H	TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
Setting Value	x	x	x	x	x	x	x	1

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Operate the A/D converter.

- A/D Converter Mode Register 0 (ADM0)
  Start A/D converter conversion.

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Setting Value	1							

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	Enables conversion operation [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: Stabilization wait status + conversion operation status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5.7.10 A/D Conversion Interrupt

Figure 5.11 shows the A/D Conversion Interrupt.

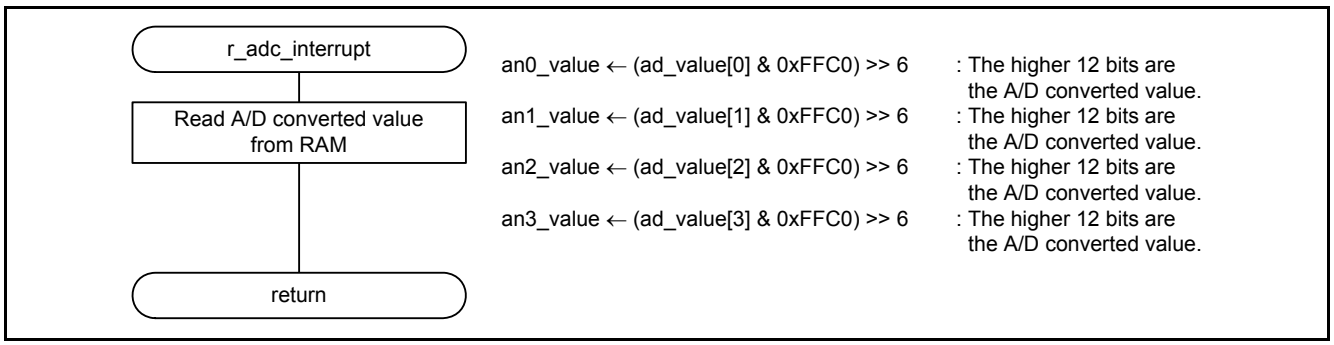


Figure 5.11 A/D Conversion Interrupt

Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware

RL78/G14 Group User's Manual: Hardware (R01UH0186E)
RL78 Family User's Manual: Software (R01US0015E)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

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REVISION HISTORY	RL78/G14 Transferring A/D Conversion Result Using the DTC

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 01, 2015	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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