RL78/G14

Setting the D/A Converter's Normal Mode

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Abstract

This document describes a method to output analog voltage using the D/A converter in the RL78/G14 Group MCU.

Products

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Output analog voltage from the ANO0 pin using the D/A converter. Output for the analog voltage starts at 0.0 V and the output level changes every millisecond in the following order:
0.0 V → 1.0 V → ··· 4.0 V → 5.0 V → 0.0 V → 1.0 V ···

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows the Analog Voltage Output Waveform.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
D/A converter 0 (hereinafter referred to as DAC0)	Output the analog voltage
Timer array unit 0 (hereinafter referred to as TAU0)	Generate a period to change the analog voltage

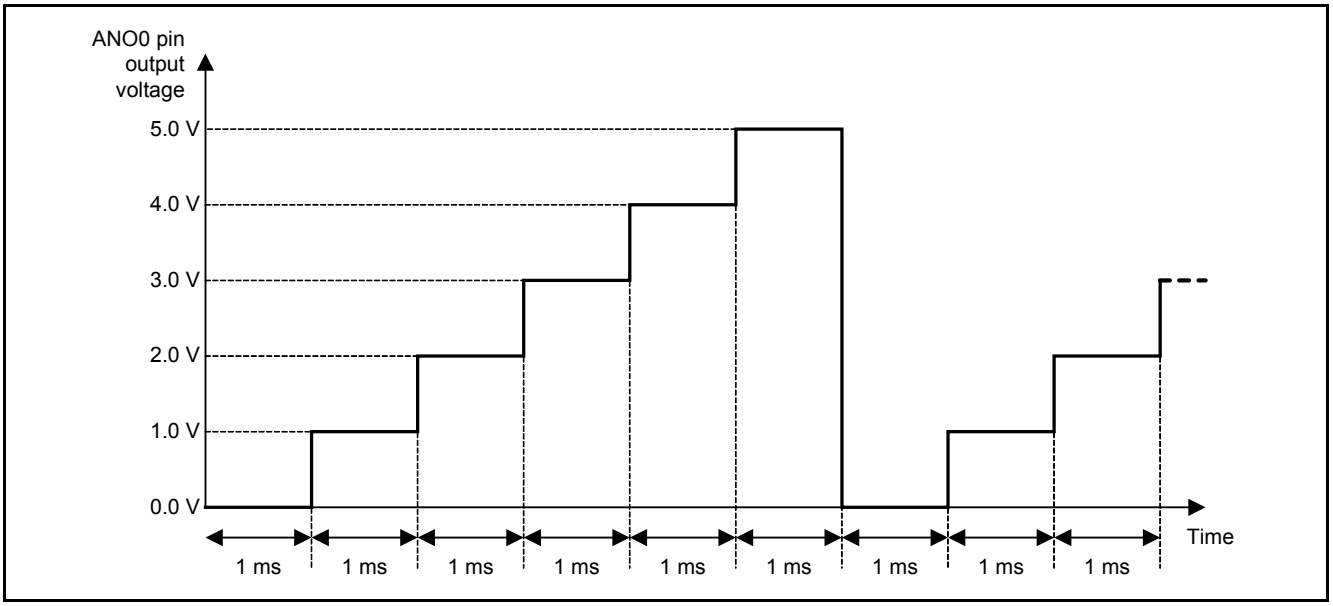


Figure 1.1 Analog Voltage Output Waveform

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

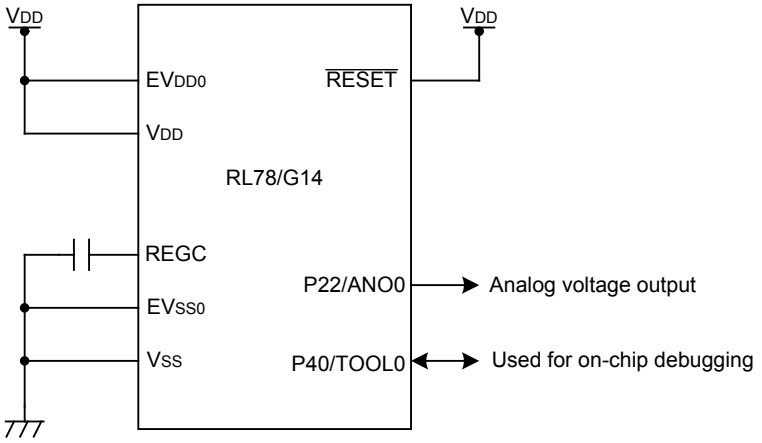
Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104PJA)
Operating frequencies	• Internal high-speed oscillator clock (f_{HOCO}): 16 MHz (typical) • CPU/peripheral hardware clock (f_{CLK}): 16 MHz
Operating voltage	5.0 V (2.9 to 5.5 V) LVD operation (V_{LVH}): Reset mode rising edge 2.81 V/falling edge 2.75 V
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V1.02.00
C compiler	Renesas Electronics Corporation CA78K0R V1.40
RL78/G14 code library	Renesas Electronics Corporation CodeGenerator for RL78/G14 V1.01.01

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows the Hardware Configuration used in this document.



Notes:
1. The above image is simplified to show a connection overview. When making a circuit, perform pin processing accurately and design it to satisfy the electrical characteristics. Connect dedicated input ports to VDD or VSS via a resistor individually.
2. When a pin name starts with EVSS, connect it to VSS, when a pin name starts with EVDD, connect it to VDD.
3. Set VDD to the release reset voltage (VLVIH) set in the LVD or higher.

Figure 3.1 Hardware Configuration

3.2 Pin Used

Table 3.1 lists the Pin Used and Its Function.

Table 3.1 Pin Used and Its Function

Pin Name	I/O	Function
P22/ANO0	Output	Output the analog voltage

4. Software

4.1 Operation Overview

Output the analog voltage from the ANO0 pin using DAC0. The analog output voltage immediately after DAC0 conversion operation is enabled is 0.0 V.
Use TAU0 channel 0 (hereinafter referred to as TAU00) in interval timer mode and generate interrupts every millisecond. Rewrite the DACS0 register value in the count completion interrupt service routine of TAU00 to change the analog output voltage. Use the value stored in the D/A conversion value table for the DACS0 register and output the analog output voltage repeatedly in the following order:
0.0 V → 1.0 V → ··· 4.0 V → 5.0 V → 0.0 V → 1.0 V ···

The D/A conversion value table lists D/A conversion values to output 0.0 V, 1.0 V, 2.0 V, 3.0 V, 4.0 V, and 5.0 V as the analog output voltage when V_{DD} is 5.0 V. Use the value calculated based on the following calculating formula for the D/A conversion value.

Analog output voltage of the D/A converter (VANO0) = reference voltage for the D/A converter (V_{DD}) × (DACS0) ÷ 256

Settings of DAC0 and TAU00 are shown below.

DAC0 settings:
- Use normal mode for the operation mode.
- Use the ANO0 pin.

TAU00 settings:
- Use interval timer mode for the operation mode.
- Set 1 ms for the interrupt period.
- Use the TAU00 count completion interrupt.
- Use f_{CLK} (16 MHz) for the count source.

(1) Initial settings
Perform initial settings of DAC0 and TAU00. Set the D/A conversion value to the DACS0 register to output 0.0 V from the ANO0 pin.

(2) Enable the D/A conversion operation.
The analog voltage which was D/A converted for the DACS0 register value is output from the ANO0 pin.

(3) Start the TAU00 count.
Start counting 1 ms.

(4) TAU00 count completion interrupt
Set the D/A conversion value to the DACS0 register.

Figure 4.1 shows the Timing Diagram.

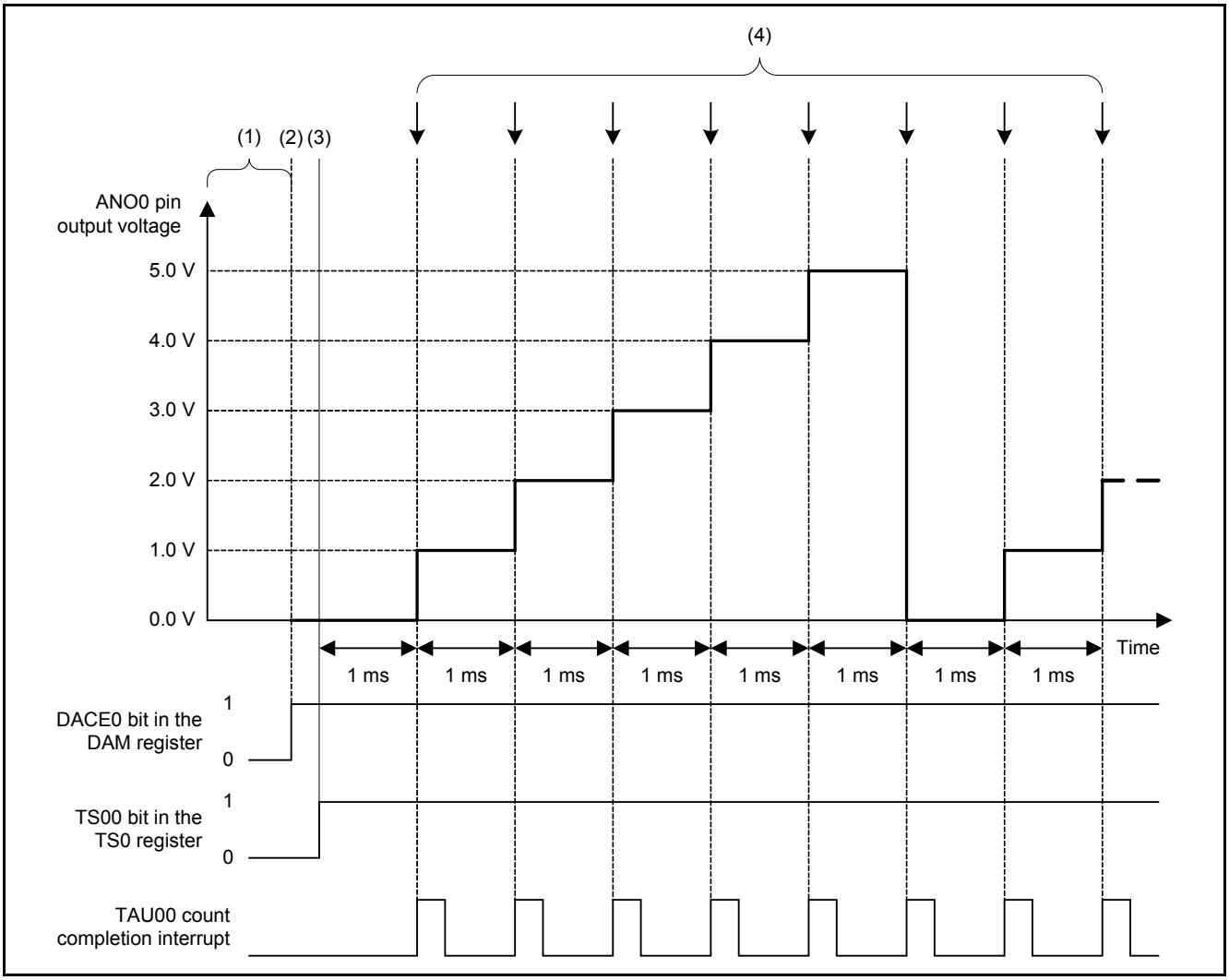


Figure 4.1 Timing Diagram

4.2 Option-Setting Memory

Table 4.1 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

Table 4.1 Option-Setting Memory Configured in the Sample Code

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11101001B	Internal high-speed oscillation HS mode: 16 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

4.3 Variables

Table 4.2 lists the Global Variables.

Table 4.2 Global Variables

Type	Variable Name	Contents	Functions Used
uint8_t	da_data[]	D/A conversion value table	da_out_change
uint8_t	da_cnt	D/A conversion value counter	da_out_change

4.4 Functions

Table 4.3 lists the Functions.

Table 4.3 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	Initial setting of the CPU clock
R_TAU0_Create	Initial setting of TAU0
R_DAC_Create	Initial setting of the D/A converter
main	Main processing
R_DAC0_Start	DAC0 conversion start setting
R_TAU0_Channel0_Start	TAU00 operation enable setting
r_tau0_channel0_interrupt	TAU00 interrupt
da_out_change	D/A conversion value switch processing
R_DAC0_Set_ConversionValue	DAC0 conversion value setting

4.5 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	Initial setting of the CPU clock
Header	r_cg_cgc.h
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU clock.
Argument	None
Return Value	None

R_TAU0_Create	
Outline	Initial setting of TAU0
Header	r_cg_timer.h
Declaration	void R_TAU0_Create(void)
Description	Perform the initial setting to use TAU00 as an interval timer.
Argument	None
Return Value	None

R_DAC_Create	
Outline	Initial setting of the D/A converter
Header	r_cg_dac.h
Declaration	void R_DAC_Create(void)
Description	Perform the initial setting to use DAC0 in normal mode.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_DAC0_Start	
Outline	DAC0 conversion start setting
Header	r_cg_dac.h
Declaration	void R_DAC0_Start(void)
Description	Start D/A conversion.
Argument	None
Return Value	None

R_TAU0_Channel0_Start	
Outline	TAU00 operation enable setting
Header	r_cg_timer.h
Declaration	void R_TAU0_Channel0_Start(void)
Description	Start TAU00 count.
Argument	None
Return Value	None

r_tau0_channel0_interrupt	
Outline	TAU00 interrupt
Header	None
Declaration	void r_tau0_channel0_interrupt(void)
Description	Perform TAU00 interrupt service routine.
Argument	None
Return Value	None

da_out_change	
Outline	D/A conversion value switch processing
Header	r_cg_userdefine.h
Declaration	void da_out_change(void)
Description	Change the output analog voltage value.
Argument	None
Return Value	None

R_DAC0_Set_ConversionValue		
Outline	DAC0 conversion value setting	
Header	r_cg_dac.h	
Declaration	void R_DAC0_Set_ConversionValue(uint8_t reg_value)	
Description	Set the D/A conversion value to the DACS0 register.	
Argument	reg_value	D/A conversion value
Return Value	None	

4.6 Flowcharts

4.6.1 Overall Flowchart

Figure 4.2 shows the Overall Flowchart.

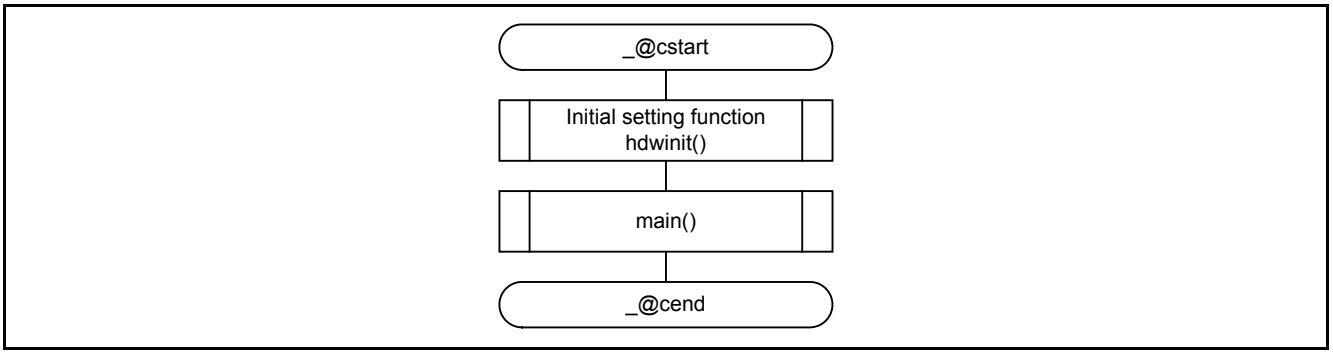


Figure 4.2 Overall Flowchart

4.6.2 Initial Setting

Figure 4.3 shows the Initial Setting.

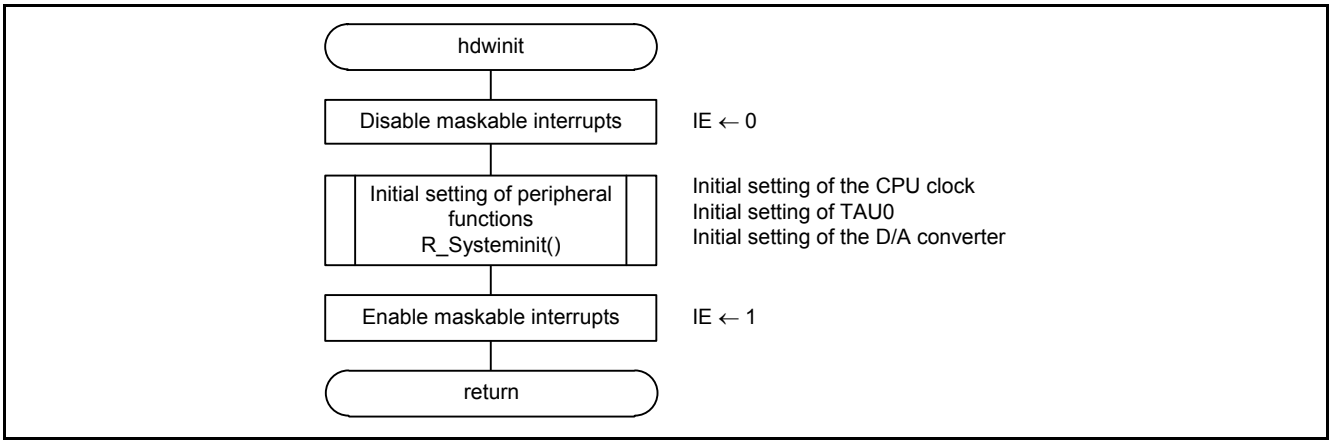


Figure 4.3 Initial Setting

4.6.3 Initial Setting of Peripheral Functions

Figure 4.4 shows the Initial Setting of Peripheral Functions.

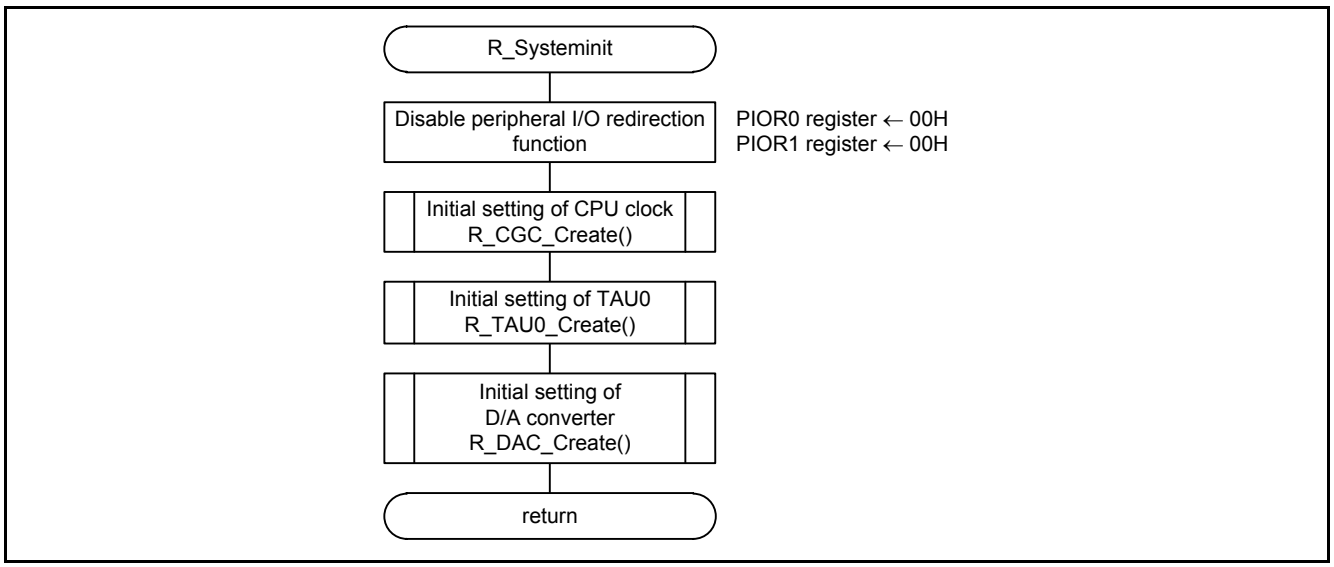


Figure 4.4 Initial Setting of Peripheral Functions

4.6.4 Initial Setting of the CPU Clock

Figure 4.5 shows the Initial Setting of the CPU Clock.

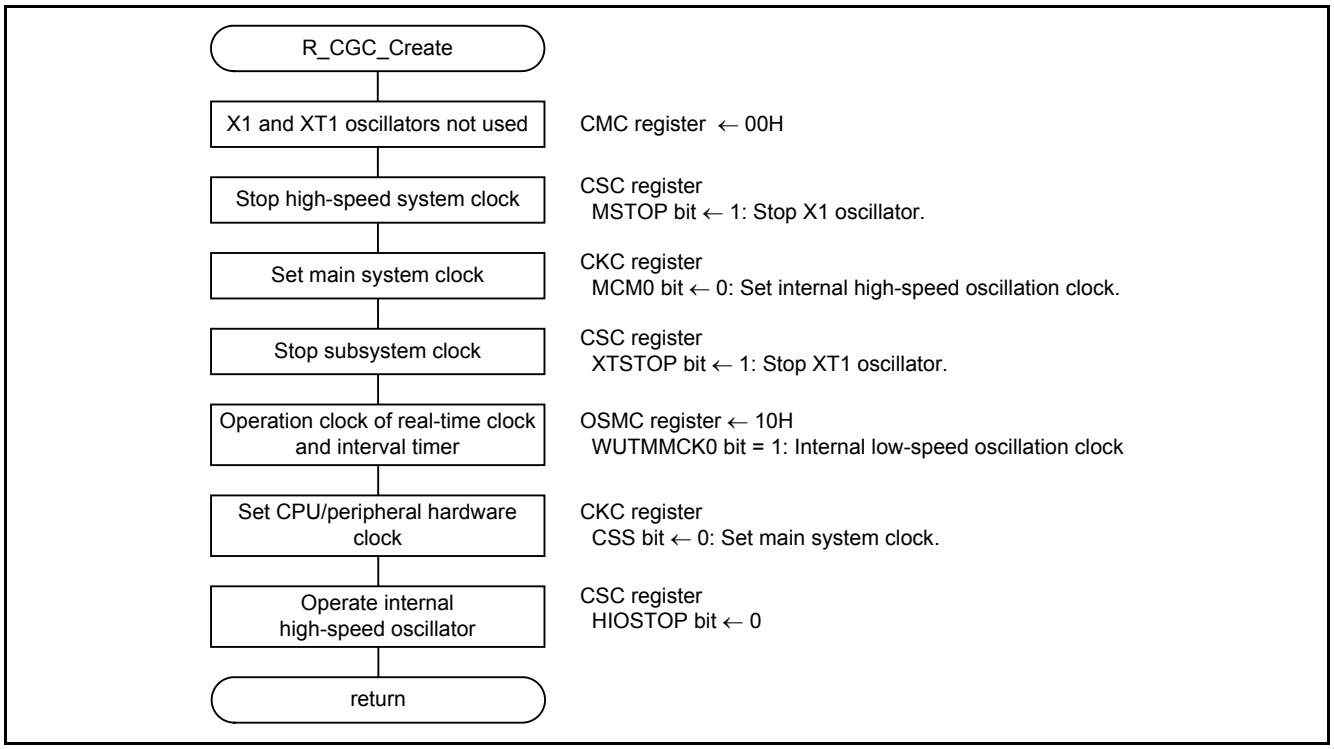


Figure 4.5 Initial Setting of the CPU Clock

4.6.5 Initial Setting of TAU0

Figure 4.6 shows the Initial Setting of TAU0.

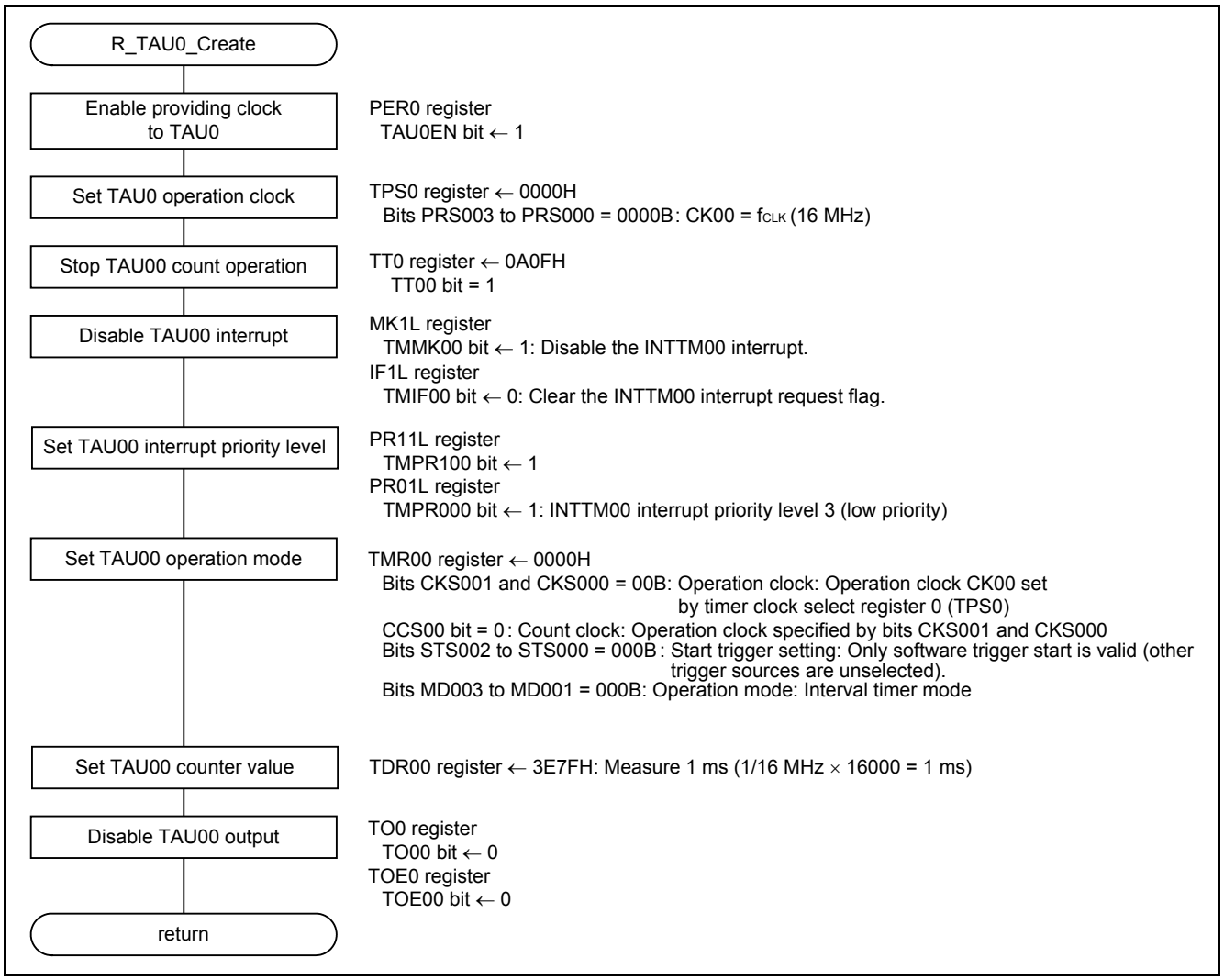


Figure 4.6 Initial Setting of TAU0

Enable providing a clock to TAU0.

• Peripheral Enable Register 0 (PER0)

Symbol	7	6	5	4	3	2	1	0
PER0	RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	**TAU0EN**
Setting Value	x	x	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	**Enables input clock supply.** **• SFR used by timer array unit 0 can be read and written.**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set an operation clock of TAU0.

- Timer Clock Select Register 0 (TPS0)

Set 16 MHz for the operation clock.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPS0	0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	**PRS 003**	**PRS 002**	**PRS 001**	**PRS 000**
Setting Value	—	—	×	×	—	—	×	×	×	×	×	×	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Stop the TAU00 count operation.

- Timer Channel Stop Register 0 (TT0)

Set 16 MHz for the operation clock.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT0	0	0	0	0	TTH03	0	TTH01	0	0	0	0	0	TT03	TT02	TT01	**TT00**
Setting Value	—	—	—	—	×	—	×	—	—	—	—	—	×	×	×	**1**

Bit 0

TT00	Operation stop trigger of channel 0
0	No trigger operation
1	**Operation is stopped (stop trigger is generated). This bit is the trigger to stop operation of the lower 8-bit timer for TT01 and TT03 when channel 1 or 3 is in the 8-bit timer mode.**

Disable the TAU00 interrupt.

- Interrupt Mask Flag Register (MK1L)

Symbol	7	6	5	4	3	2	1	0
MK1L	TMMK03	TMMK02	TMMK01	**TMMK00**	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
Setting Value	x	x	x	**1**	x	x	x	x

Bit 4

TMMK00	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

• Interrupt Request Flag Register (IF1L)

Symbol	7	6	5	4	3	2	1	0
IF1L	TMIF03	TMIF02	TMIF01	**TMIF00**	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
Setting Value	x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Set the TAU00 interrupt priority level.

• Priority Specification Flag Register (PR11L, PR01L)

Symbol	7	6	5	4	3	2	1	0
PR11L	TMPR103	TMPR102	TMPR101	**TMPR100**	IICAPR10	SREPR11 TMPR103H	SRPR11 CSIPR111 IICPR111	STPR11 CSIPR110 IICPR110
Setting Value	x	x	x	**1**	x	x	x	x

Symbol	7	6	5	4	3	2	1	0
PR01L	TMPR003	TMPR002	TMPR001	**TMPR000**	IICAPR00	SREPR01 TMPR003H	SRPR01 CSIPR011 IICPR011	STPR01 CSIPR010 IICPR010
Setting Value	x	x	x	**1**	x	x	x	x

Bit 4

TMPR100	TMPR000	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set TAU00 operation mode.

- Timer Mode Register (TMR00)
  Operation clock (fMCK): CK00
  Count clock (fTCLK): fMCK
  Start trigger: Only software trigger start is valid.
  Operation mode: Interval timer mode (A timer interrupt is not generated when counting is started.)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMR00	**CKS 001**	**CKS 000**	0	**CCS 00**	0	**STS 002**	**STS 001**	**STS 000**	CIS 001	CIS 000	0	0	**MD 003**	**MD 002**	**MD 001**	**MD 000**
Setting Value	**0**	**0**	—	**0**	—	**0**	**0**	**0**	×	×	—	—	**0**	**0**	**0**	**0**

Bits 15 and 14

CKS 001	CKS 000	Selection of operation clock (fMCK) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)
Operation clock (fMCK) is used by the edge detector. A count clock (fTCLK) and a sampling clock are generated depending on the setting of the CCS00 bit. The operation clocks CK02 and CK03 can only be selected for channels 1 and 3.		

Bit 12

CCS 00	Selection of count clock (fTCLK) of channel 0
0	**Operation clock (fMCK) specified by the CKS000 and CKS001 bits**
1	Valid edge of input signal input from the TI00 pin
Count clock (fTCLK) is used for the timer/counter, output controller, and interrupt controller.	

Bits 10 to 8

STS 002	STS 001	STS 000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bits 3 to 1

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	**0**	**0**	**1/0**	**Interval timer mode**	**Interval timer** / Square wave output / Divider function / PWM output (master)	**Counting down**
0	1	1	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting up
Other than above				Setting prohibited		
The operation of the MD000 bit varies depending on each operation mode (see table below).						

Bit 0

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD 000	Setting of starting counting and interrupt
• **Interval timer mode (0, 0, 0)** • Capture mode (0, 1, 0)	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the TAU00 count value.

• Timer Data Register (TDR00)

Set 3E7FH to the counter and measure 1 ms.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDR00	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Disable the TAU00 output.

• Timer Output Register (TO0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO0	0	0	0	0	0	0	0	0	0	0	0	0	TO03	TO02	TO01	**TO00**
Setting Value	—	—	—	—	—	—	—	—	—	—	—	—	×	×	×	**0**

Bit 0

TO00	Timer output of channel 0
0	**Timer output value is “0”.**
1	Timer output value is “1”.

• Timer Output Enable Register (TOE0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	**TOE00**
Setting Value	—	—	—	—	—	—	—	—	—	—	—	—	×	×	×	**0**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**Timer output is disabled.** **Timer operation is not applied to the TO00 bit and the output is fixed.** **Writing to the TO00 bit is enabled.**
1	Timer output is enabled. Timer operation is applied to the TO00 bit and an output waveform is generated. Writing to the TO00 bit is ignored.

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.

Initial values of individual bits

x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.6.6 Initial Setting of the D/A Converter

Figure 4.7 shows the Initial Setting of the D/A Converter.

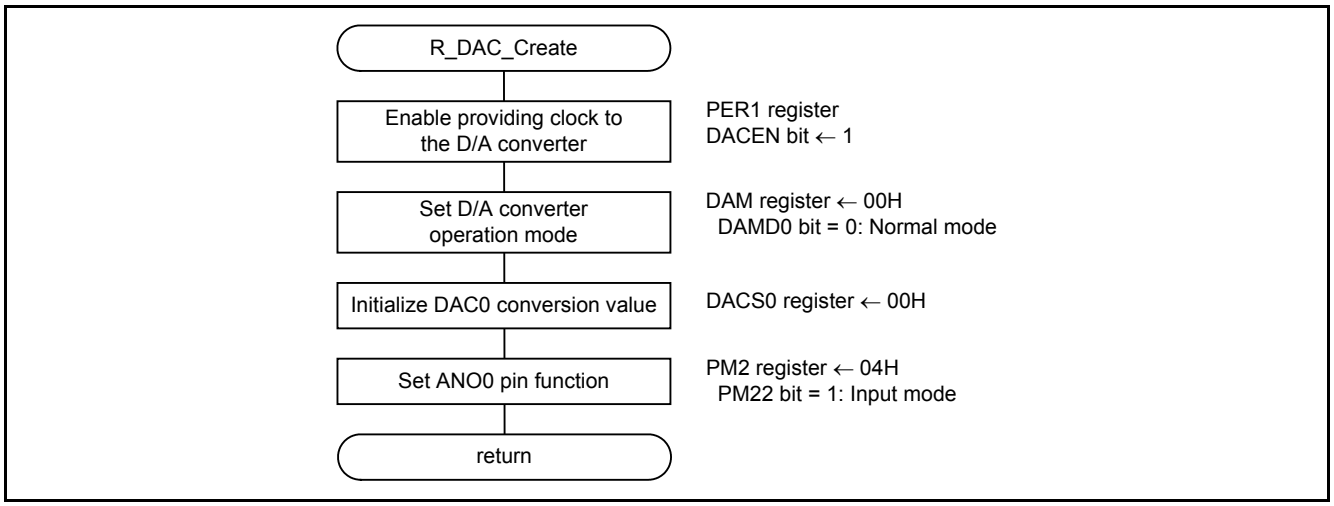


Figure 4.7 Initial Setting of the D/A Converter

Enable providing a clock to the D/A converter.

• Peripheral Enable Register 1 (PER1)

Symbol	7	6	5	4	3	2	1	0
PER1	**DACEN**	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
Setting Value	**1**	x	x	x	x	—	—	x

Bit 7

DACEN	Control of D/A converter input clock
0	Stops input clock supply. • SFR used by the D/A converter cannot be written. • The D/A converter is in the reset status.
1	**Supplies input clock.** **• SFR used by the D/A converter can be read/written.**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the D/A converter to normal mode.

• D/A Converter Mode Register (DAM)

Symbol	7	6	5	4	3	2	1	0
DAM	—	—	DACE1	DACE0	—	—	DAMD1	**DAMD0**
Setting Value	—	—	x		—	—	x	**0**

Bit 0

DAMD0	D/A converter operation mode selection
0	**Normal mode**
1	Real-time output mode

Initialize the DAC0 conversion value.

• D/A Conversion Value Setting Register 0 (DACS0)
Set 000H to the D/A conversion value.

Symbol	7	6	5	4	3	2	1	0
DACS0	**DACS07**	**DACS06**	**DACS05**	**DACS04**	**DACS03**	**DACS02**	**DACS01**	**DACS00**
Setting Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

—	Function
Bits 7 to 0	**The relation between the resolution and analog output voltage (VANO0) of the D/A converter are as follows. VANO0 = Reference voltage for D/A converter × (DACS0) / 256**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the ANO0 pin function.

• Port Mode Register 2 (PM2)

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	**PM22**	PM21	PM20
Setting Value	x	x	x	x	x	**1**	x	x

Bit 2

PM22	P22 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

4.6.7 Main Processing

Figure 4.8 shows the Main Processing.

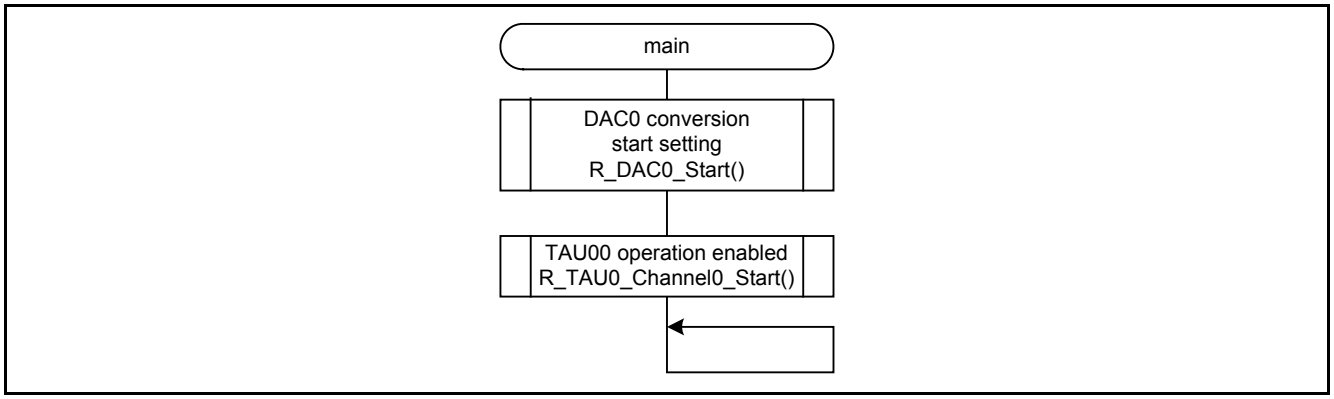


Figure 4.8 Main Processing

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.6.8 DAC0 Conversion Start Setting

Figure 4.9 shows the DAC0 Conversion Start Setting.

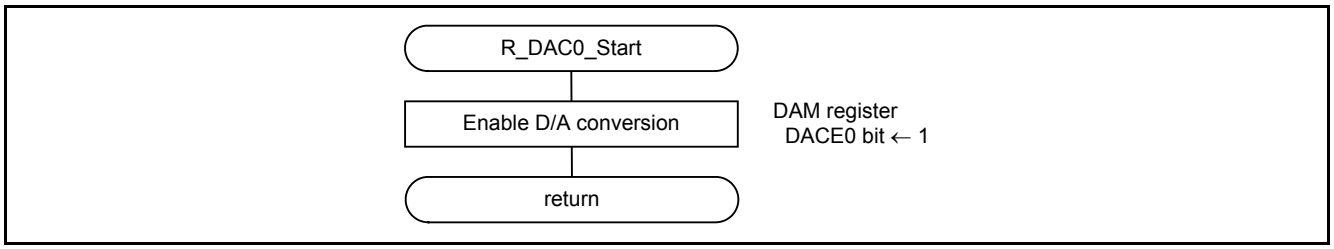


Figure 4.9 DAC0 Conversion Start Setting

Enable D/A conversion.

• D/A Converter Mode Register (DAM)

Symbol	7	6	5	4	3	2	1	0
DAM	—	—	DACE1	**DACE0**	—	—	DAMD1	DAMD0
Setting Value	—	—	x	**1**	—	—	x	

Bit 4

DACE0	D/A conversion operation control
0	Stops D/A conversion operation
1	**Enables D/A conversion operation**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.6.9 TAU00 Operation Enable Setting

Figure 4.10 shows the TAU00 Operation Enable Setting.

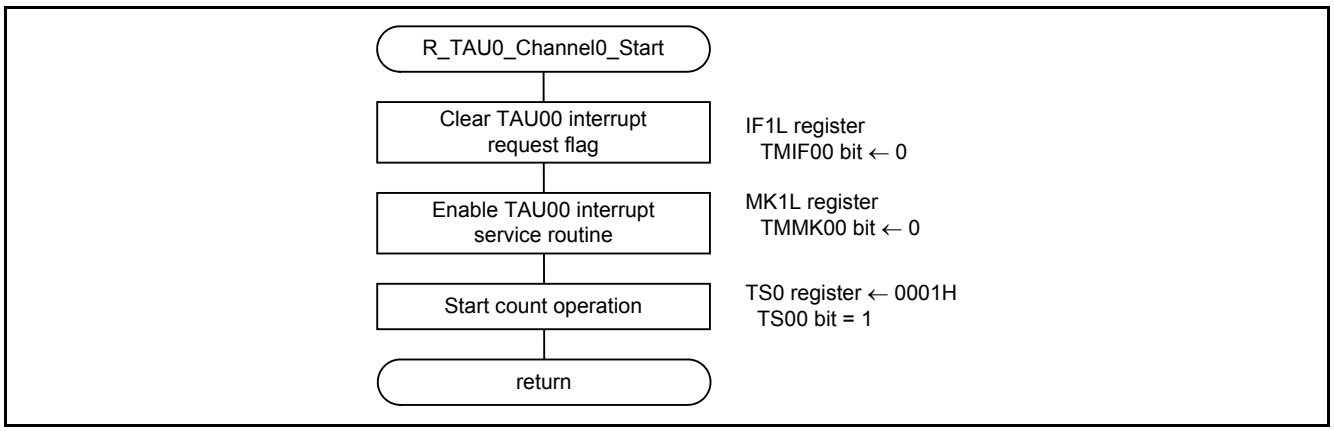


Figure 4.10 TAU00 Operation Enable Setting

Clear the TAU00 interrupt request flag.

- Interrupt Request Flag Register (IF1L)

Symbol	7	6	5	4	3	2	1	0
IF1L	TMIF03	TMIF02	TMIF01	**TMIF00**	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
Setting Value	x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Enable the TAU00 interrupt service routine.

• Interrupt Mask Flag Register (MK1L)

Symbol	7	6	5	4	3	2	1	0
MK1L	TMMK03	TMMK02	TMMK01	**TMMK00**	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
Setting Value	x	x	x	**0**	x	x	x	x

Bit 4

TMMK00	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Start count operation.

• Timer Channel Start Register (TS0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS0	0	0	0	0	TSH 03	0	TSH 01	0	0	0	0	0	TS 03	TS 02	TS 01	**TS 00**
Setting Value	—	—	—	—	×	—	×	—	—	—	—	—	×	×	×	**1**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.** **The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.6.10 TAU00 Interrupt

Figure 4.11 shows the TAU00 Interrupt.

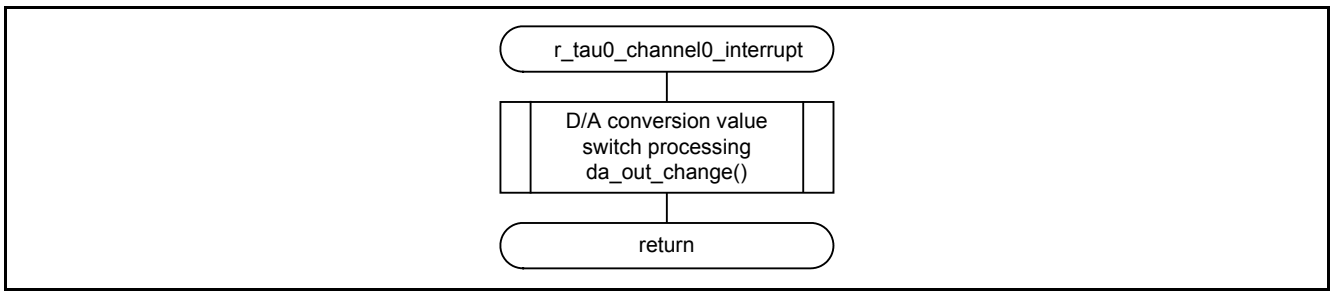


Figure 4.11 TAU00 Interrupt

4.6.11 D/A Conversion Value Switch Processing

Figure 4.12 shows the D/A Conversion Value Switch Processing.

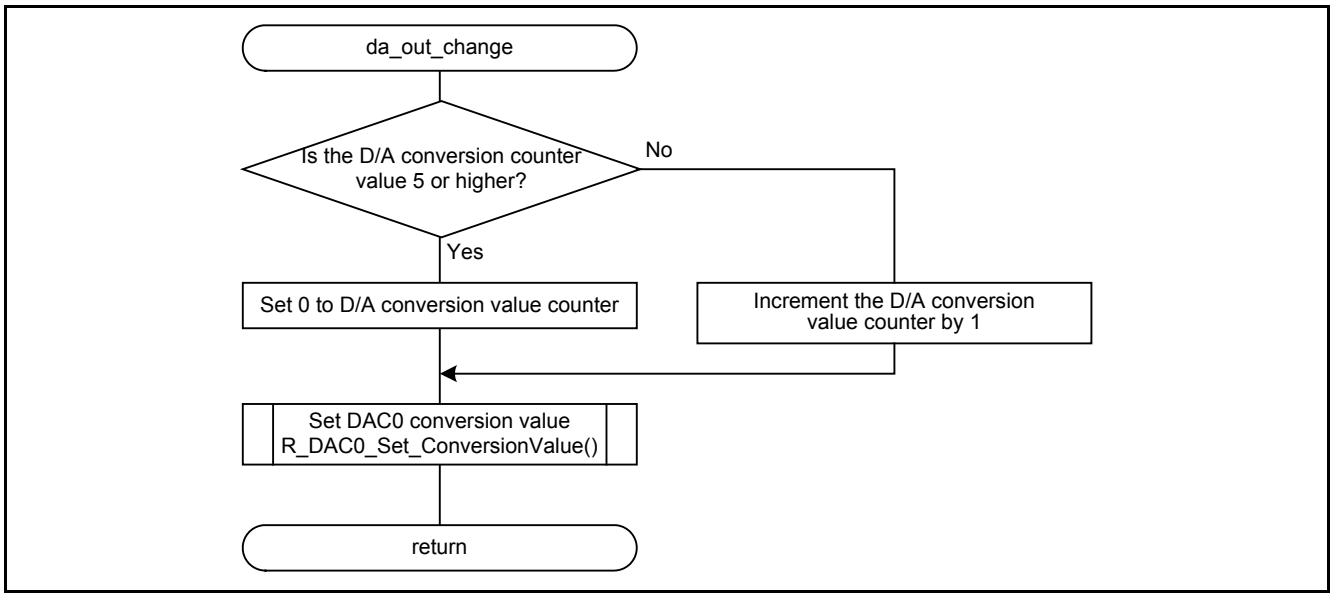


Figure 4.12 D/A Conversion Value Switch Processing

4.6.12 DAC0 Conversion Value Setting

Figure 4.13 shows the DAC0 Conversion Value Setting.

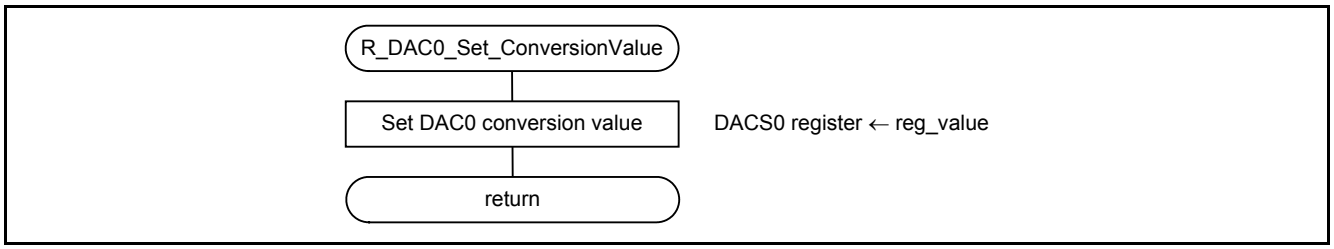


Figure 4.13 DAC0 Conversion Value Setting

Set the DAC0 conversion value.

- D/A Conversion Value Setting Register (DACS0)
  Set an analog output value output to the ANO0 pin.

Symbol	7	6	5	4	3	2	1	0
DACS0	**DACS07**	**DACS06**	**DACS05**	**DACS04**	**DACS03**	**DACS02**	**DACS01**	**DACS00**
Setting Value	**0/1**	**0/1**	**0/1**	**0/1**	**0/1**	**0/1**	**0/1**	**0/1**

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware
RL78/G14 Group User's Manual: Hardware Rev.1.00
RL78 Family User's Manual: Software Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/G14 Setting the D/A Converter's Normal Mode

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 31, 2012	—	First edition issued
1.10	June 1, 2013	4	Fixed typo in Table 2.1
		5	Fixed typo in Figure 3.1

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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