RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Timer RC to Timer Array Unit

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Introduction

This document describes how to migrate from timer RC in R8C/36M Group to the timer array unit (TAU) in RL78/G14 (This document is described in 64-pin package as an example).

Target Device

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Migration Method from R8C Family to RL78 Family

This application note explains how to achieve each mode (timer mode and PWM mode) in Timer RC of R8C/36M using RL78/G14.
Table 1.1 shows the mode in Timer RC of R8C/36M Group, and Table 1.2 shows the mode in timer array unit of RL78/G14.

In R8C/36M Group, Timer RC is a 16-bit timer with four I/O pins. Timer RC has three modes: timer mode (input capture function and output compare function), PWM mode and PWM2 mode. In timer mode (input capture function), the counter value is captured to a register, using an external signal as the trigger. In timer mode (output compare function), matches between the counter and register values are detected (pin output state changes when a match is detected). In PWM mode, pulses of a given width are output continuously. In PWM2 mode, a one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

In RL78/G14, the timer array unit has four 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more "channels" can be used to create a high-accuracy timer. A count clock is counted by the TCRmn register. Set the count value in the TDRmn register.

The same operation as that in timer mode (input capture function) of R8C/36M can be realized by using input pulse interval measurement function in TAU of RL78/G14. The count value can be captured at the TImn valid edge and the interval of the pulse input to TImn can be measured. In addition, the count value can be captured by using software operation (TSmn = 1) as a capture trigger while the TEmn bit is set to 1.

The same operation as that in timer mode (output compare function) and PWM mode of R8C/36M can be realized by using PWM output function in TAU of RL78/G14. Two channels can be used as a set to generate a pulse of any period and duty factor.

In this application note, as described in this chapter, explain the migration method for the three modes "timer mode (input capture function)", "timer mode (output compare function)" and "PWM mode".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Table 1.1 Operation Mode of Timer RC in R8C/36M

Timer RC in R8C/36M	
Mode	**Function**
Timer mode (input capture function)	The counter value is captured to a register, using an external signal as the trigger.
Timer mode (output compare function)	Matches between the counter and register values are detected. (Pin output state changes when a match is detected.)
PWM mode	Pulses of a given width are output continuously.
PWM2 mode Note	A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

Note: About PWM2 mode of R8C/36M, RL78/G14 can't realize this mode. The same operation as that in PWM2 mode of R8C/36M can be realized by using 16-bit timer KB0 of RL78/G11 or 16-bit timer KB20 of RL78/L13.

For details, please refer to the following application notes below.
- RL78/G11 IH Control using Timer KB0 CC-RL (R01AN3650)
- RL78/L13 Timer KB20 Based IH Control (100 V) CC-RL (R01AN3149)

Table 1.2 Operation Mode of TAU in RL78/G14

TAU in RL78/G14	
Mode	**Function**
Interval timer	The timer array unit can be used as a reference timer that generates INTTMmn (timer interrupt) at fixed intervals.
Square wave output	TOmn performs a toggle operation as soon as INTTMmn has been generated, and outputs a square wave with a duty factor of 50%.
External event counter	The timer array unit can be used as an external event counter that counts the number of times the valid input edge (external event) is detected in the TImn pin.
Divider	A clock input from a timer input pin (TI00) is divided and output from an output pin (TOm0).
Input pulse interval measurement	**The count value can be captured at the TImn valid edge and the interval of the pulse input to TImn can be measured.**
Measurement of high-/low-level width of input signal	By starting counting at one edge of the TImn pin input and capturing the number of counts at another edge, the signal width (high-level width/low-level width) of TImn can be measured.
Delay counter	It is possible to start counting down when the valid edge of the TImn pin input is detected (an external event), and then generate INTTMmn (a timer interrupt) after any specified interval.
One-shot pulse output	By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin.
PWM output	**Two channels can be used as a set to generate a pulse of any period and duty factor.**
Multiple PWM output	By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

2. Differences between RL78/G14 and R8C/36M Group

2.1 Differences in Function Overview

Table 2.1 lists the differences between Timer RC in R8C/36M Group and the TAU in RL78/G14.

Table 2.1 Differences

Item	R8C/36M Group Timer RC	RL78/G14 TAU
Configuration	16-bit timer	16-bit timer Note 1
Count sources	f1, fOCO40M, fOCO-F	f_{TCLK} (between f_{CLK} to $f_{CLK}/2^{15}$)
Counters	• TRC register	TCRmn register
Count value setting	• TRC register • TRCGRA register • TRCGRB register • TRCGRC register • TRCGRD register	TDRmn register
Modes	• Timer mode (input capture function) • Timer mode (output compare function) • PWM mode • PWM2 mode	• Interval timer • Square wave output • External event counter • Divider (channel 0 in unit 0 only) • Input pulse interval measurement • Measurement of high-/low-level width of input signal • Delay counter • One-shot pulse output Note 2 • PWM output Note 2 • Multiple PWM output Note 2
Count operations	Increment	• Count up Note 3 • Count down Note 3
Timer input	• TRCIOA pin • TRCIOB pin • TRCIOC pin • TRCIOD pin • TRCCLK pin • TRCTRG pin	• Channel 0 - Input from the TI00 pin - Event input signal from the ELC • Channel 1 - Input from the TI01 pin - Event input signal from the ELC - Low-speed on-chip oscillator clock (f_{IL}) - Subsystem clock (f_{SUB}) • Channel 2 - Input from the TI02 pin • Channel 3 - Input from the TI03 pin - RxD0 (Serial input pin)
I/O pin selection (output / input port)	Yes	No
Simultaneous channel operation function	No	Yes Note 2
Coordination with event link controller (ELC)	No	Yes

Notes: 1. Channels 1 and 3 can operate as 8-bit timers.
2. These modes are available by using a master channel to link with slave channels.
3. Count operations depend on modes specified.

2.2 Differences in Timer Mode (Input Capture Function)

The input pulse interval measurement in RL78/G14 corresponds to timer mode (input capture function) in R8C/36M Group.
Table 2.2 and Table 2.3 list the differences between timer mode (input capture function) in R8C/36M Group and input pulse interval measurement in RL78/G14.

Table 2.2 Differences between Timer Mode (Input Capture Function) and Input Pulse Interval Measurement (1/2)

Item	R8C/36M Group (Timer Mode (Input Capture Function))	RL78/G14 (Input Pulse Interval Measurement)
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to TRCCLK pin (rising edge)	f_{TCLK} (between f_{CLK} to $f_{CLK}/2^{15}$)
Count operations	• Increment	• Timer count register mn (TCRmn) operates as an up counter in the capture mode. • When the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, the TCRmn register counts up from 0000H in synchronization with the count clock. • When the TImn pin input valid edge is detected, the count value of the TCRmn register is transferred (captured) to timer data register mn (TDRmn) and, at the same time, the TCRmn register is cleared to 0000H.
Overflow period	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA input capture): 1/fk × (n+1) n: TRCGRA register setting value	Period of count clock × 65536
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.	1 is written to the TSmn bit in the TSm register.
Count stop conditions	0 (count stops) is written to the TSTART bit in the TRCMR register. The TRC register retains a value before count stops.	1 is written to the TTmn bit in the TTm register.
Interrupt request generation timing	• Input capture (valid edge of TRCIOj input or fOCO128 signal edge). • The TRC register overflows.	When the TImn pin input valid edge is detected, INTTMmn is output.
Counter value reset timing	Timing for setting the TRC register to 0000h: Overflow or input capture	When the TImn pin input valid edge is detected, the count value of the TCRmn register is transferred (captured) to timer data register mn (TDRmn) and, at the same time, the TCRmn register is cleared to 0000H.

Remark j = A, B, C, or D
m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Table 2.3 Differences between Timer Mode (Input Capture Function) and Input Pulse Interval Measurement (2/2)

Item	R8C/36M Group (Timer Mode (Input Capture Function))	RL78/G14 (Input Pulse Interval Measurement)
Read from timer	The count value can be read by reading TRC register.	Read the TDRmn and TCRmn registers.
Write to timer	The TRC register can be written to.	Write to the TDRmn and TCRmn registers is disabled.
Selectable functions	• Input capture input pin selection • Input capture input valid edge selection • Buffer operation • Digital filter • Timing for setting the TRC register to 0000h • Input-capture trigger selected	• Valid edge selected • Noise filter

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

2.3 Differences in Timer Mode (Output Compare Function)

Operation as PWM output in RL78/G14 corresponds to timer mode (output compare function) in R8C/36M Group. Table 2.4 and Table 2.5 list the differences between timer mode (output compare function) in R8C/36M Group and operation as PWM output in RL78/G14.

Table 2.4 Differences between Timer Mode (Output Compare Function) and Operation as PWM Output (1/2)

Item	R8C/36M Group (Timer Mode (Output Compare Function))	RL78/G14 (PWM Output)
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to TRCCLK pin (rising edge)	f_{TCLK} (between f_{CLK} to $f_{CLK}/2^{15}$)
Count operations	• Increment	Two channels can be used as a set to generate a pulse of any period and duty factor. The master channel operates in the interval timer mode. The slave channel operates in one-count mode.
PWM waveform	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA compare match): 1/fk × (n+1) n: TRCGRA register setting value	Pulse period = {Set value of TDRmn (master) + 1} × Count clock period Duty factor [%] = {Set value of TDRmp (slave)}/{Set value of TDRmn (master) + 1} × 100
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.	1 is written to the TSmn, TSHm1, or TSHm3 bit in the TSm register.
Count stop conditions	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. The output compare output pin retains output level before count stops, the TRC register retains a value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The output compare output pin retains the level after the output is changed by the compare match.	1 is written to the TTmn, TTHm1, or TTHm3 bit in the TTm register.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
p: Slave channel number (n = 0: p = 1, 2, 3; n = 2: p = 3)

Table 2.5 Differences between Timer Mode (Output Compare Function) and Operation as PWM Output (2/2)

Item	R8C/36M Group (Timer Mode (Output Compare Function))	RL78/G14 (PWM Output)
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRj match) • The TRC register overflows	Master channel: If the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, an interrupt (INTTMmn) is output. And When the counter reaches 0000H, INTTMmn is output. Slave channel: By using INTTMmn from the master channel as a start trigger, the TCRmp register loads the value of the TDRmp register and the counter counts down to 0000H. When the counter reaches 0000H, it outputs INTTMmp.
Output pin functions	Programmable I/O port or output compare output (selectable individually for each pin).	Programmable I/O port or PWM function output.
Read from timer	The count value can be read by reading the TRC register.	Read the registers TCRmn and TCRmp.
Write to timer	The TRC register can be written to.	Write to the register TDRmn and TDRmp.
Selectable functions	• Output compare output pin selection • Compare match output level selection • Initial output level selection • Timing for setting the TRC register to 0000h • Buffer operation • Pulse output forced cutoff signal input • Can be used as an internal timer by disabling timer RC output • Changing output pins for registers TRCGRC and TRCGRD • A/D trigger generation	• Whether the timer interrupt is generated when counting is started • Output pin level when pulse output is started

Remark j = A, B, C, or D
m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
p: Slave channel number (n = 0: p = 1, 2, 3; n = 2: p = 3)

2.4 Differences in PWM Mode

Operation as PWM output in RL78/G14 corresponds to PWM mode in R8C/36M Group.
Table 2.6 and Table 2.7 list the differences between PWM mode in R8C/36M Group and operation as PWM output in RL78/G14.

Table 2.6 Differences between PWM Mode and PWM Output (1/2)

Item	R8C/36M Group (PWM Mode)	RL78/G14 (PWM Output)
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to TRCCLK pin (rising edge)	f_{TCLK} (between f_{CLK} to $f_{CLK}/2^{15}$)
Count operations	• Increment	Two channels can be used as a set to generate a pulse of any period and duty factor. The master channel operates in the interval timer mode. The slave channel operates in one-count mode.
PWM waveform	PWM period: 1/fk × (m+1) Active level width: 1/fk × (m-n) Inactive width: 1/fk × (n+1) fk: Count source frequency m: TRCGRA register setting value n: TRCGRj register setting value	Pulse period = {Set value of TDRmn (master) + 1} × Count clock period Duty factor [%] = {Set value of TDRmp (slave)}/{Set value of TDRmn (master) + 1} × 100
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.	1 is written to the TSmn, TSHm1, or TSHm3 bit in the TSm register.
Count stop conditions	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. PWM output pin retains output level before count stops, TRC register retains value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The PWM output pin retains the level after the output is changed by the compare match.	1 is written to the TTmn, TTHm1, or TTHm3 bit in the TTm register.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRh match) • The TRC register overflows	Master channel: If the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, an interrupt (INTTMmn) is output. Slave channel: By using INTTMmn from the master channel as a start trigger, the TCRmp register loads the value of the TDRmp register and the counter counts down to 0000H. When the counter reaches 0000H, it outputs INTTMmp.

Remark j = B, C, or D
m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
p: Slave channel number (n = 0: p = 1, 2, 3; n = 2: p = 3)

Table 2.7 Differences between PWM Mode and PWM Output (2/2)

Item	R8C/36M Group (PWM Mode)	RL78/G14 (PWM Output)
Output pin functions	Programmable I/O port or PWM output (selectable individually for each pin).	Programmable I/O port or PWM function output.
Read from timer	The count value can be read by reading the TRC register.	Read the registers TCRmn and TCRmp.
Write to timer	The TRC register can be written to.	Write to the register TDRmn and TDRmp.
Selectable functions	• One to three pins selectable as PWM output pins • Active level selectable for each pin • Initial level selectable for each pin • Buffer operation • Pulse output forced cutoff signal input • A/D trigger generation	• Whether the timer interrupt is generated when counting is started • Output pin level when pulse output is started

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
p: Slave channel number (n = 0: p = 1, 2, 3; n = 2: p = 3)

2.5 Assigned I/O Pins

Table 2.8 lists the I/O pins assigned for use in R8C/36M Group.

Table 2.8 R8C/36M Group I/O Pins

Pin Name	Assigned Pins	I/O
TRCIOA	P0_0, P0_1, P0_2, P1_1, or P5_1	I/O
TRCIOB	P0_3, P0_4, P0_5, P1_2, P2_0, P5_2, or P6_5	I/O
TRCIOC	P0_7, P1_3, P2_1, P3_4, P5_3, or P6_6	I/O
TRCIOD	P0_6, P1_0, P2_2, P3_5, P5_4, or P6_7	I/O
TRCCLK	P1_4, P3_3, or P5_0	Input
TRCTRG	P0_0, P0_1, P0_2, P1_1, or P5_1	Input

Table 2.9 lists the I/O pins assigned for use in RL78/G14.

Table 2.9 RL78/G14 I/O Pins (64-pin products)

Unit Number	Target Channel	Pin Name	Assigned Pins	I/O
Unit 0	Channel 0	TI00	P00	Input
		TO00	P01	Output
	Channel 1	TI01	P16	Input
		TO01	P16	Output
	Channel 2	TI02	P17	Input
		TO02	P17	Output
	Channel 3	TI03	P31	Input
		TO03	P31	Output

2.6 Register Compatibility

Register compatibilities between Timer RC in R8C/36M Group and TAU in RL78/G14 are listed in Table 2.10 and Table 2.11.

Table 2.10 Register Compatibility (1/2)

Item	R8C/36M Group	RL78/G14
Count start	• TRCMR register TSTART bit	• TSm register Bits TSmn, TSHm1, TSHm3 Notes 1
Count status flag	N/A	• TEm register Bits TEmn, TEHm1, TEHm3 Notes 2
Count stop	• TRCMR register TSTART bit	• TTm register Bits TTmn, TTHm1, TTHm3 Notes 3
Pin Select	• TRCPSR0 register • TRCPSR1 register • TRBRCSR register	• PMCxx register • PMxx register • Pxx register
Operating mode select	• TRCMR register Bits PWMB, PWMC, PWMD and PWM2 • TRCIOR0 register Bits IOA2, IOB2, IOC2 and IOD2	• TMRmn register Bits MDmn1 to MDmn3
Count source select	• TRCCR1 register Bits TCK0 to TCK2	• TPSm register • TMRmn register Bits CKSmn0, CKSmn1, CCSmn
Timer	• TRC register	• Registers TCRmn, TDRmn (TCRmn: read-only, TDRmn: read/write)
Capture and compare register	• TRCGRA register • TRCGRB register • TRCGRC register • TRCGRD register	• Registers TCRmn, TDRmn (TCRmn: read-only, TDRmn: read/write)
Capture polarity select	• TRCIOR0 register Bits IOA0 and IOA1 Bits IOB0 and IOB1 • TRCIOR1 register Bits IOC0 and IOC1 Bits IOD0 and IOD1	• TMRmn register Bits CISmn0 and CISmn1
Input filter select	• TRCDF register Bits DFA, DFB, DFC and DFD	• Registers NFEN1 and NFEN2
Independent channel operation/simultaneous channel operation (slave/master) select	N/A	• TMRmn register Bits MASTERmn, SPLITmn Notes 4, 5
Count start and interrupt setting	N/A	• TMRmn register MDmn0 bit
Counter overflow status	• TRCSR register OVF bit	• TSRmn register OVF bit

Notes: 1. When channels 1 and 3 are in 8-bit timer mode, bits TSHm1 and TSHm3 are triggers to enable operation (start operation) of the higher 8-bit timer.
2. When channels 1 and 3 are in 8-bit timer mode, bits TEHm1 and TEHm3 indicate whether the higher 8-bit timer is enabled or stopped.
3. When channels 1 and 3 are in 8-bit timer mode, bits TTHm1 and TTHm3 are triggers to stop operation of the the higher 8-bit timer.
4. MASTERmn bit (n = 2)
5. SPLITmn bit (n = 1, 3)

Table 2.11 Register Compatibility (2/2)

Item	R8C/36M Group	RL78/G14
Timer input select on channels 1 and 3	N/A	• TIS0 register Bits TIS00 to TIS02 and TIS04
Timer output buffer	N/A	• TOm register TOmn bit
Timer output enable	• TRCOER register Bits EA, EB, EC and ED	• TOEm register TOEmn bit
Timer output level control	• TRCCR1 register Bit TOA, TOB, TOC and TOD • TRCIOR0 register Bits IOA0 and IOA1 Bits IOA0 and IOA1 Bits IOB0 and IOB1 • TRCIOR1 register Bits IOC0 and IOC1 Bits IOD0 and IOD1 • TRCCR2 register Bits POLB, POLC and POLD	• TOLm register TOLmn bit

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

3. How to Migrate Timer RC in this Sample Code

In this sample program, the operation of Timer RC of R8C/36M Group is realized with TAU of RL78/G14 by the method shown in Table 3.1.
For detailed contents of the sample program, please refer to "4. Example of Migration from Timer Mode (Input Capture Function)" ~ "5. Example of Migration from Timer Mode (Output Compare Function) or PWM Mode".

Table 3.1 How to migrate from R8C/36M Group to RL78/G14 in this sample program

Timer RC in R8C/36M	TAU in RL78/G14
Mode	Mode
Timer mode (input capture function)	Input pulse interval measurement
Timer mode (output compare function)	PWM output
PWM mode	

The same operation as that in timer mode (output compare function) and PWM mode of R8C/36M can be realized by using PWM output function in TAU of RL78/G14.
So in this application note, about migration from Timer mode (output compare function) and PWM mode, please refer to "5. Example of Migration from Timer Mode (Output Compare Function) or PWM Mode)".

4. Example of Migration from Timer Mode (Input Capture Function)

4.1 Specifications

When implementing timer mode (input capture function) of Timer RC in R8C/36M, RL78/G14 can use input pulse interval measurement function of TAU.
Counting is started by the valid edge of a pulse signal input to a timer input pin (TImn). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.

Table 4.1 lists the peripheral functions to be used and their uses (example of migration from Timer Mode (Input Capture Function)), and Figure 4.1 shows the operation overview (example of migration from Timer Mode (Input Capture Function)).

Table 4.1 Peripheral Functions to be Used and Their Uses

(Example of Migration from Timer Mode (Input Capture Function))

Peripheral Function	Use
Timer array unit (input pulse interval measurement)	Measure the interval of TImn input pulse

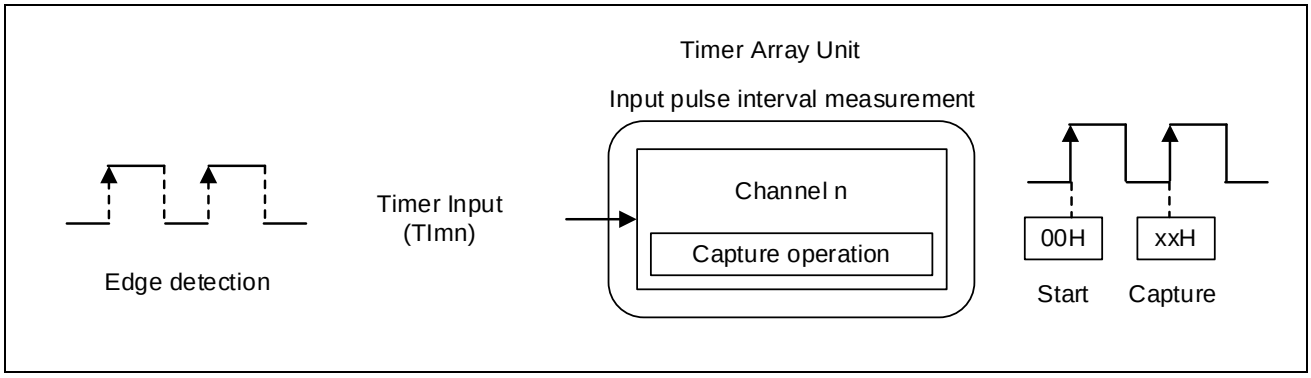

Figure 4.1 Operation Overview (Example of Migration from Timer Mode (Input Capture Function))

4.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

Table 4.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.2.0.020 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.04.00 from Renesas Electronics Corp.

4.3 Description of Hardware

4.3.1 Hardware Configuration Example

Figure 4.2 shows an example of hardware configuration that is used for this chapter.

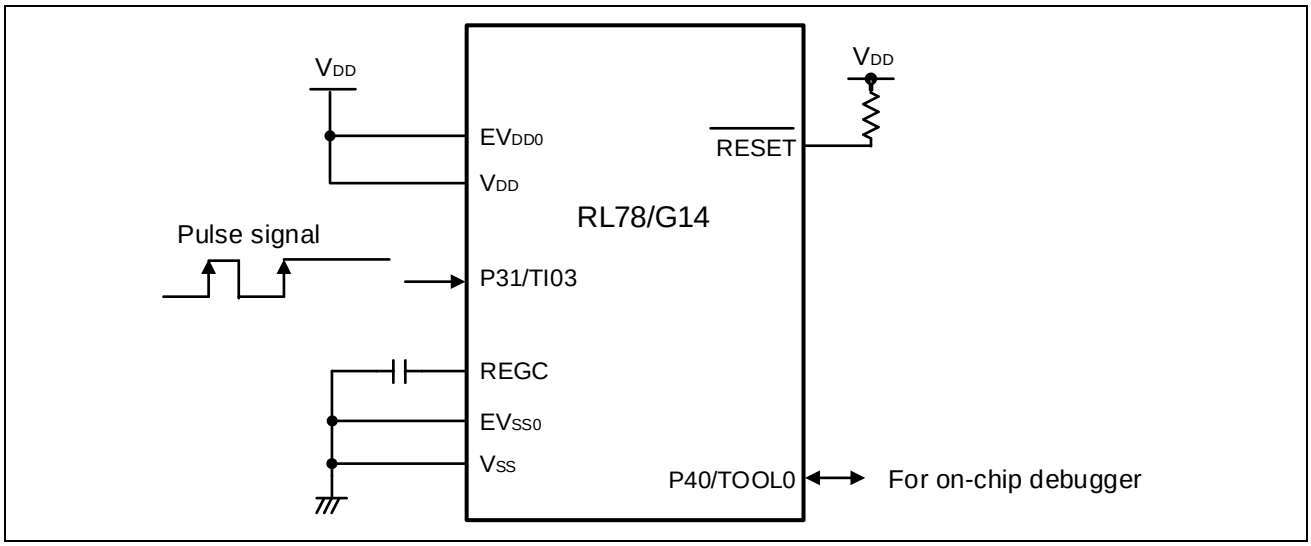

Figure 4.2 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.3.2 List of Pins to be Used

Table 4.3 lists the pins to be used and their functions.

Table 4.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P31/TI03	Input	Input pulse signals to the TAU0 channel 3.

4.4 Description of Software

4.4.1 Operation Outline

Each time a rising edge (valid edge) is detected on the timer input pin (TI03), the sample code described in this chapter captures the count value of the timer and measures the time interval between pulses which arrive at the timer input pin (TI03). When a timer interrupt (INTTM03) occurs upon completion of the capture, the sample code calculates the pulse interval and stores the calculation result in the on-chip RAM.

Table 4.4 lists the peripheral functions to be used and their uses. Figure 4.3 shows the timer and its interrupt operation.

(1) Initialize the TAU.
<Conditions for setting>
Use the P31/TI03 pin to receive pulses.
The operation clock for TAU0 channel 3 should be f_{CLK}.
Set TAU0 channel 3 to the capture mode.
Select "rising edge detection" as the input edge on the TI03 pin.
Select the TI03 pin input valid edge to trigger the capture.

(2) Set the TS03 bit of the timer channel start register 0 (TS0) to 1 to enable count operation. This clears the timer count register (TCR03) to 0000H and starts counting. The sample program executes a HALT instruction.

(3) When a valid edge is detected, the value of the timer count register (TCR03) is captured and put into the timer data register (TDR03). A timer interrupt (INTTM03) occurs upon completion of the capture. The timer count register (TCR03) is cleared to 0000H and the TAU waits for the next valid edge input.
An invalid value is captured when a timer interrupt (INTTM03) occurs upon completion of the first capture. This data is not used.

(4) In the processing of a timer interrupt (INTTM03) which occurs upon completion of the second capture, the timer data register (TDR03)'s value (pulse width) is stored in the on-chip RAM.

Table 4.4 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Timer array unit 0 channel 3	Measurement of the time interval between input pulses on the timer input pin (TI03)

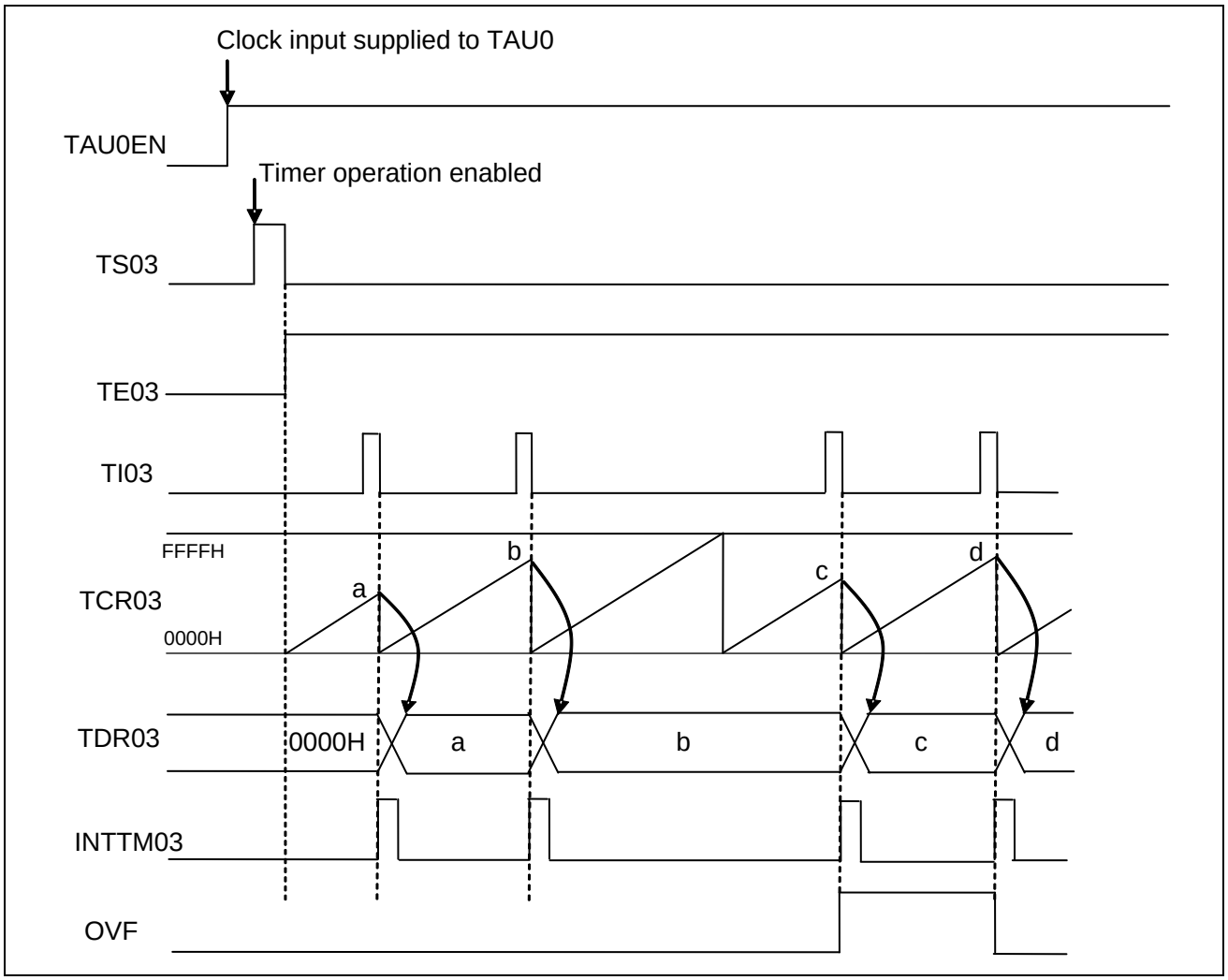

Figure 4.3 Overview of Timer Operation and Interrupts

4.4.2 List of Option Byte Setting

Table 4.5 summarizes the settings of the option bytes.

Table 4.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

4.4.3 List of Constant

Table 4.6 lists the constants that are used in this sample program.

Table 4.6 Constants for the Sample Program

Constant	Setting	Description
_0001_TAU_OVERFLOW_OCCURS	0x0001U	Detects an overflow.

4.4.4 List of Variables

Table 4.7 lists the global variables that are used in this sample program.

Table 4.7 Global Variables for the Sample Program

Type	Variable Name	Contents	Function Used
volatile uint32_t	g_tau0_ch3_width	Temporary buffer which holds the measured pulse interval	r_tau0_channel3_interrupt()

4.4.5 List of Functions

Table 4.8 lists the functions that are used in this sample program.

Table 4.8 Functions

Function Name	Outline
R_TAU0_Channel3_Start()	Starts operation of TAU0 channel 3.
r_tau0_channel3_interrupt()	Processes timer interrupts on TAU0 channel 3.

4.4.6 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TAU0_Channel3_Start()

Synopsis	TAU0 channel 3 operation start
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TAU0_Channel3_Start(void)
Explanation	This function unmasks TAU0 channel 3 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tau0_channel3_interrupt()

Synopsis	TAU0 channel 3 timer interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	static void __near r_tau0_channel3_interrupt(void)
Explanation	This function saves the interval value to RAM.
Arguments	None
Return value	None
Remarks	None

4.4.7 Flow Chart

4.4.7.1 Overall Flow

Figure 4.4 shows the overall flow of the sample program described in this chapter.

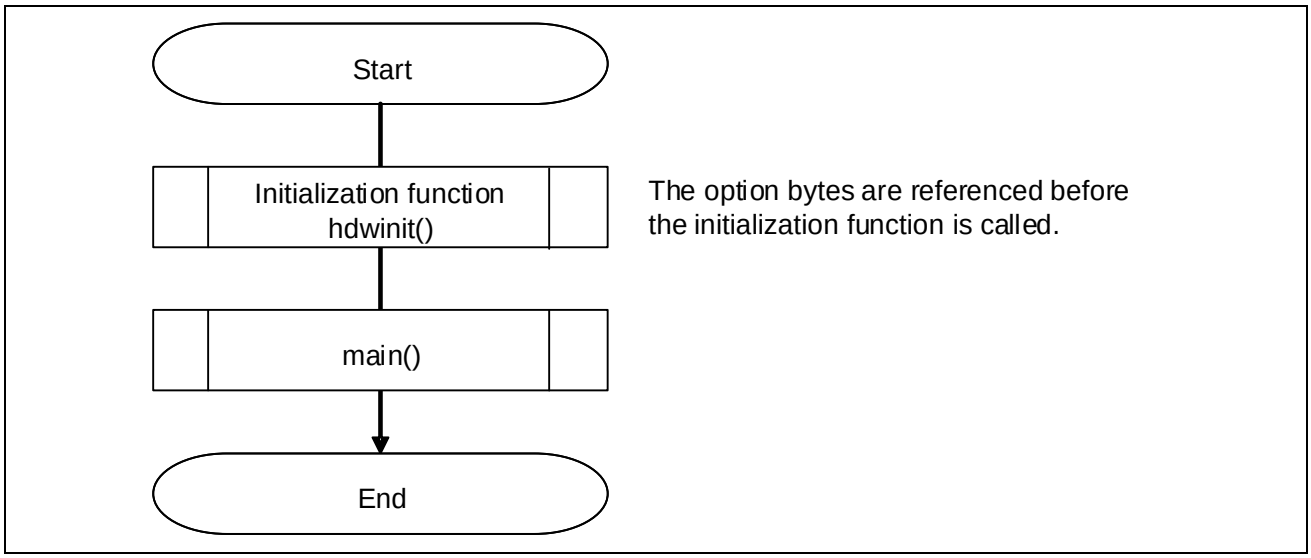

Figure 4.4 Overall Flow

4.4.7.2 Initialization Function

Figure 4.5 shows the flowchart for the initialization function.

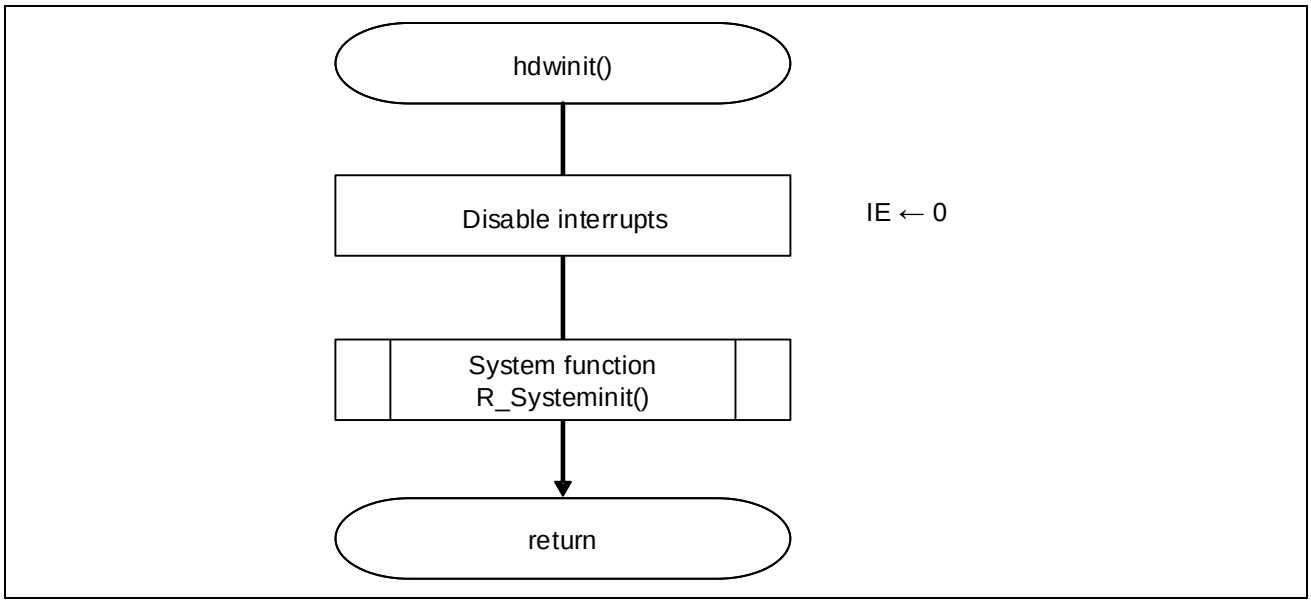

Figure 4.5 Initialization Function

4.4.7.3 System Function

Figure 4.6 shows the flowchart for the system function.

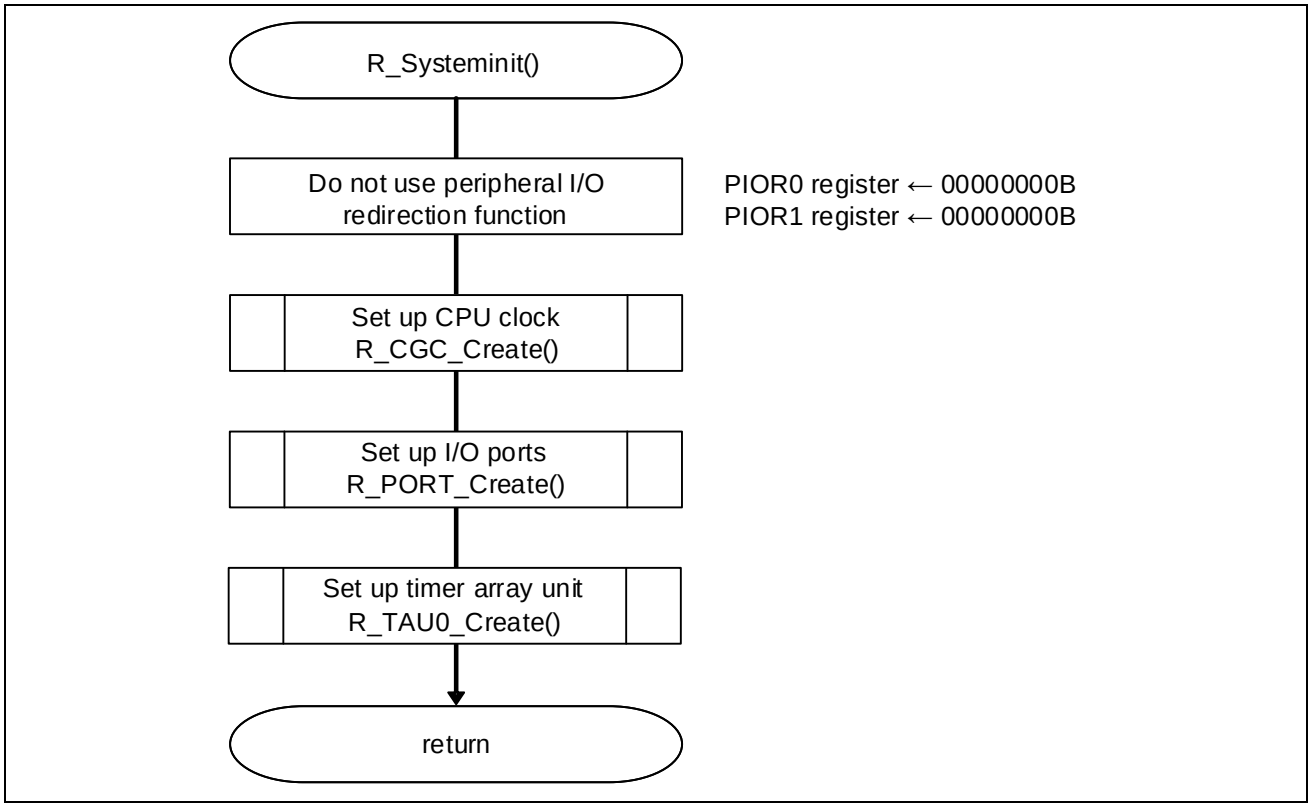

Figure 4.6 System Function

4.4.7.4 CPU Clock Setup

Figure 4.7 shows the flowchart for setting up the CPU clock.

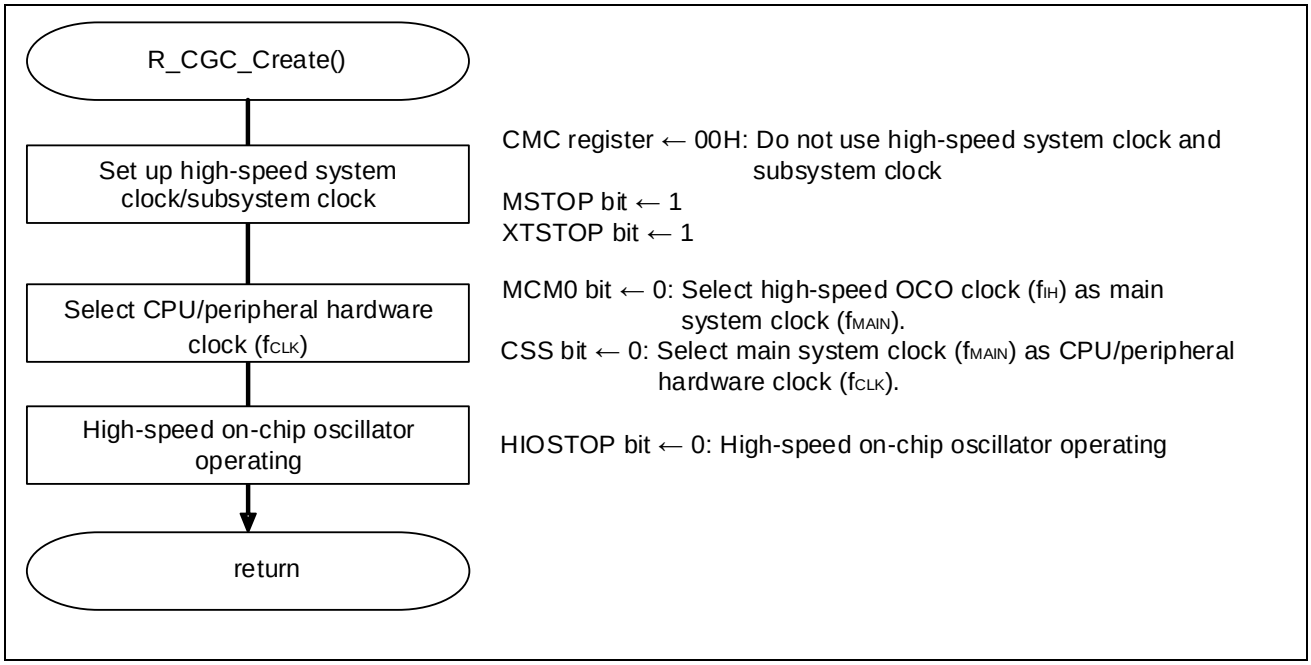

Figure 4.7 CPU Clock Setup

4.4.7.5 I/O Port Setup

Figure 4.8 shows the flowchart for setting up the I/O ports.

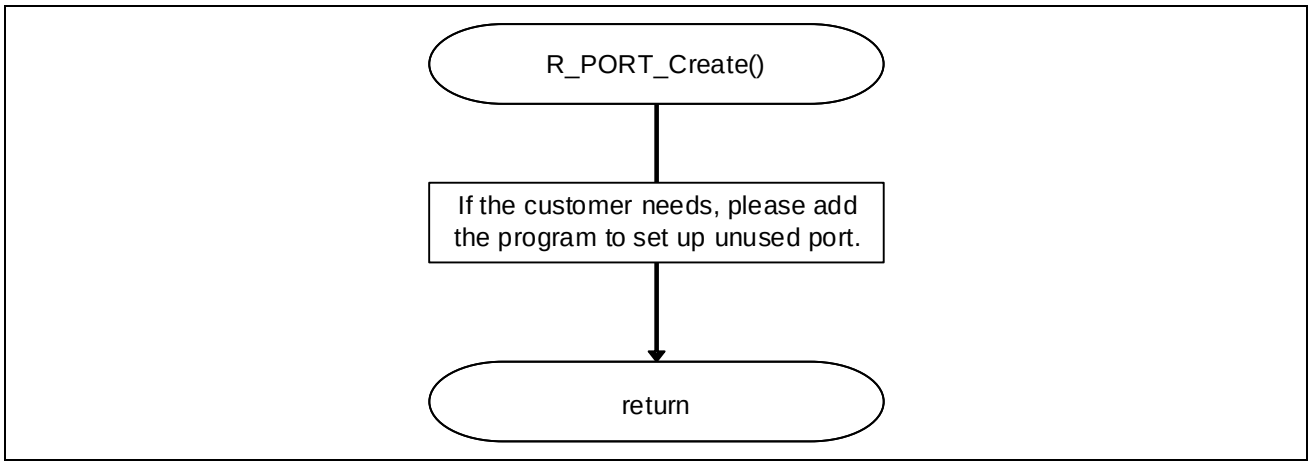

Figure 4.8 I/O Port Setup

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

4.4.7.6 Timer Array Unit Setup

Figure 4.9 shows the flowchart for setting up the timer array unit.

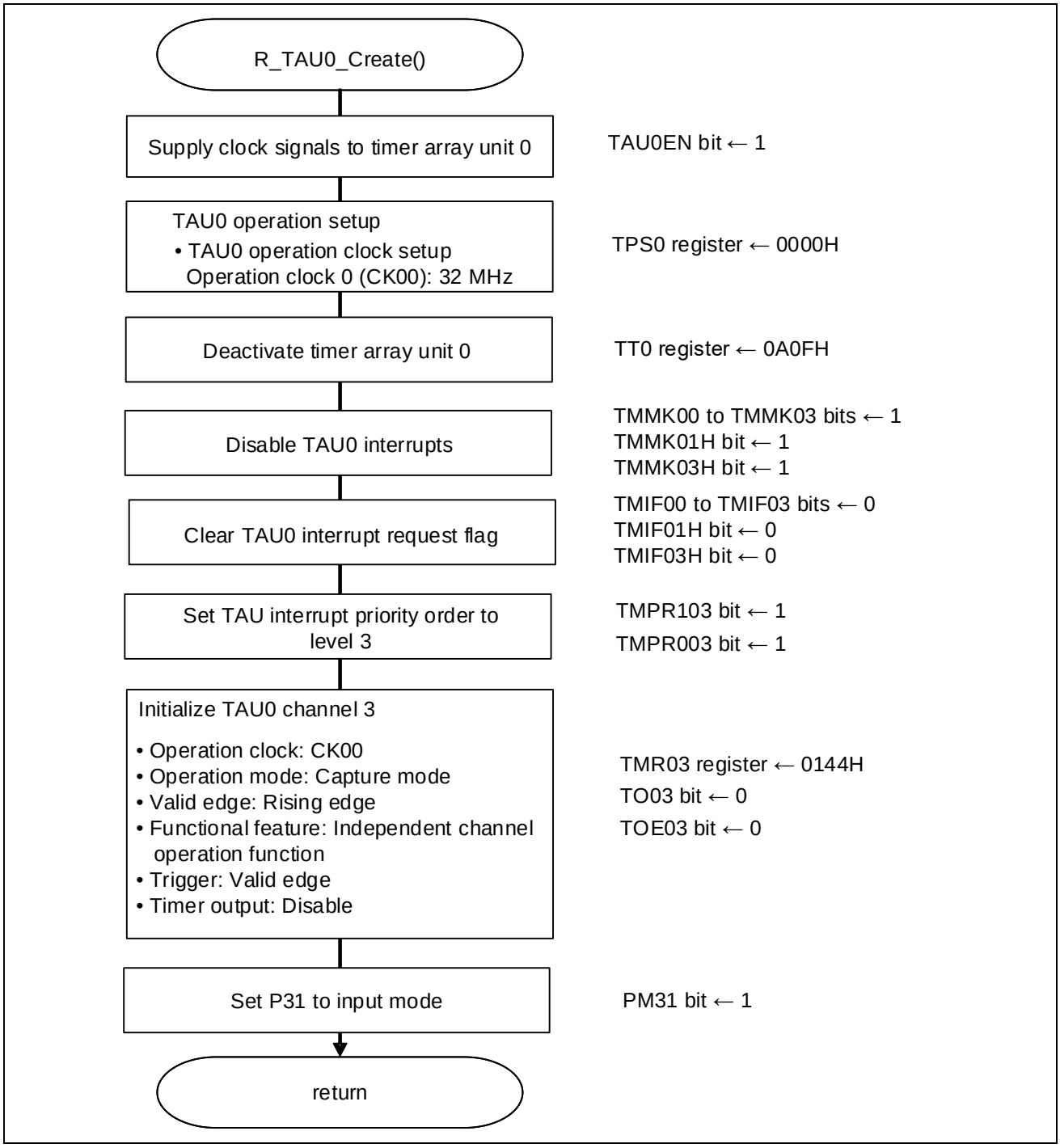

Figure 4.9 Timer Array Unit Setup

Starting clock signal supply to the timer array unit 0

• Peripheral enable register 0 (PER0)

Start supplying clock signals to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	1

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	Enables input clock supply.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Configuring the timer clock frequency

• Timer clock select register 0 (TPS0)
Select an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**PRS 031**	**PRS 030**	**0**	**0**	**PRS 021**	**PRS 020**	**PRS 013**	**PRS 012**	**PRS 011**	**PRS 010**	**PRS 003**	**PRS 002**	**PRS 001**	**PRS 000**
0	0	x	x	0	0	x	x	x	x	x	x	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
					f_{CLK}= 2 MHz	f_{CLK}= 4 MHz	f_{CLK}= 8 MHz	f_{CLK}= 20 MHz	f_{CLK}= 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	4 MHz	8 MHz	20 MHz	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2 MHz	4 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1 MHz	2 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	500 kHz	1 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	250 kHz	500 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	125 kHz	250 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	62.5 kHz	125 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	31.3 kHz	62.5 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	15.6 kHz	31.3 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	7.81 kHz	15.6 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	3.91 kHz	7.81 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	1.95 kHz	3.91 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	977 Hz	1.95 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	488 Hz	977 Hz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	244 Hz	488 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0 Hz	122 Hz	244 Hz	610 Hz	977 Hz

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting up the channel 3 operation mode

• Timer mode register 03 (TMR03)
Specify the operation mode, edge, trigger, channel and clocks.

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS031	CKS030	0	CCS03	SPLIT03	STS032	STS031	STS030	CIS031	CIS030	0	0	MD033	MD032	MD031	MD030
0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0

Bits 15 and 14

CKS031	CKS030	Selection of operation clock (f_{MCK}) of channel 3
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS03	Selection of count clock (f_{TCLK}) of channel 3
0	**Operation clock (f_{MCK}) specified by the CKS030 and CKS031 bits**
1	Valid edge of input signal input from the TI03 pin

Bit 11

SPLIT03	Selection of 8 or 16-bit timer operation for channels 1 and 3
0	**Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)**
1	Operates as 8-bit timer.

Bits 10 to 8

STS032	STS031	STS030	Setting of start trigger or capture trigger of channel 3
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	**0**	**1**	**Valid edge of the TI03 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI03 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 and 6

CIS031	CIS030	Selection of TI03 pin input valid edge
0	0	Falling edge
0	**1**	**Rising edge**
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS031	CKS030	0	CCS03	SPLIT03	STS032	STS031	STS030	CIS031	CIS030	0	0	MD033	MD032	MD031	MD030
0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0

Bits 3 to 0

MD033	MD032	MD031	MD030	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	**1**	**0**	1/**0**	**Capture mode**	**Input pulse interval measurement**	**Counting up**
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD030 bit (see table below).

Operation mode (Value set by the MD033 to MD031 bits (see table above))	MD030	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • **Capture mode (0, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation. At that time, interrupt is not generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Configuring the output value for the timer output pin
• Timer output register 0 (TO0)
Configure the output value for the timer output pin for channel 3.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**TO03**	**TO02**	**TO01**	**TO00**
0	0	0	0	0	0	0	0	0	0	0	0	**0**	x	x	x

Bit 3

TO03	Timer output of channel 3
0	**Timer output value is "0"**
1	Timer output value is "1"

Enabling the timer output
• Timer output enable register 0 (TOE0)
Enable/disable the timer output for channel 3.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**TOE03**	**TOE02**	**TOE01**	**TOE00**
0	0	0	0	0	0	0	0	0	0	0	0	**0**	x	x	x

Bit 3

TOE03	Timer output enable/disable of channel 3
0	**Timer output is disabled.** **Timer operation is not applied to the TO03 bit and the output is fixed.** **Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.**
1	Timer output is enabled. Timer operation is applied to the TO03 bit and an output waveform is generated. Writing to the TO03 bit is ignored.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

4.4.7.7 Main Processing

Figure 4.10 shows the flowchart for main processing.

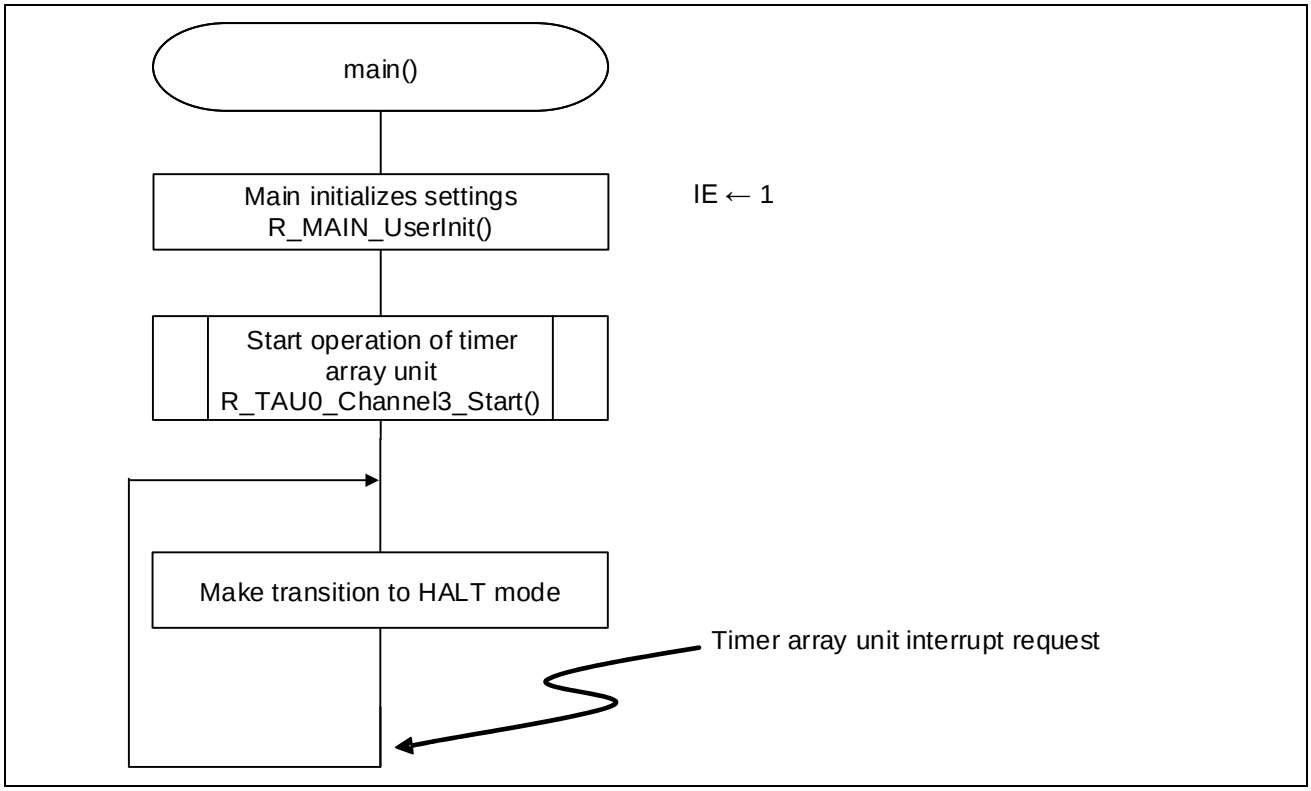

Figure 4.10 Main Processing

4.4.7.8 Timer Array Unit 0 Operation Start

Figure 4.11 shows the flowchart for starting timer array unit operation.

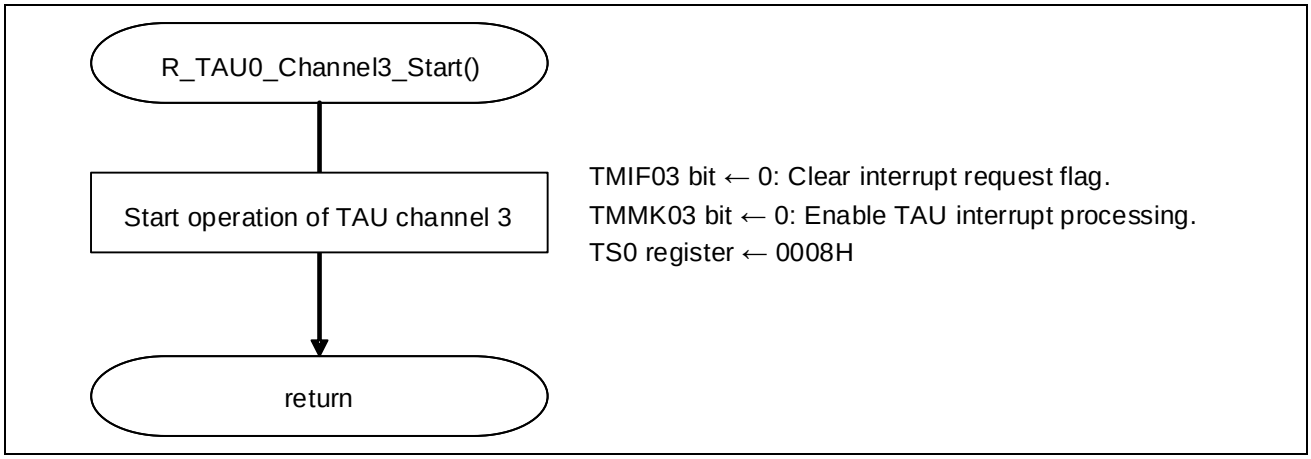

Figure 4.11 Timer Array Unit 0 Operation Start

Configuring the timer interrupt
• Interrupt request flag register (IF1L)
Clear the interrupt request flag.
• Interrupt mask flag register (MK1L)
Enable interrupt processing.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
0	x	x	x	x	x	x	x

Bit 7

TMIF03	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status.

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
0	x	x	x	x	x	x	x

Bit 7

TMMK03	Interrupt processing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Configuring the timer startup
• Timer channel start register 0 (TS0)
Enable count operation of channel 3.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH03	0	TSH01	0	0	0	0	0	TS03	TS02	TS01	TS00
0	0	0	0	x	0	x	0	0	0	0	0	1	x	x	x

Bit 3

TS03	Operation enable (start) trigger of channel 3
0	No trigger operation
1	The TE03 bit is set to 1 and the count operation becomes enabled. The TCR03 register count operation start in the count operation enabled state varies depending on each operation mode.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

4.4.7.9 INTTM03 Interrupt Processing

Figure 4.12 shows the flowchart for INTTM03 interrupt processing.

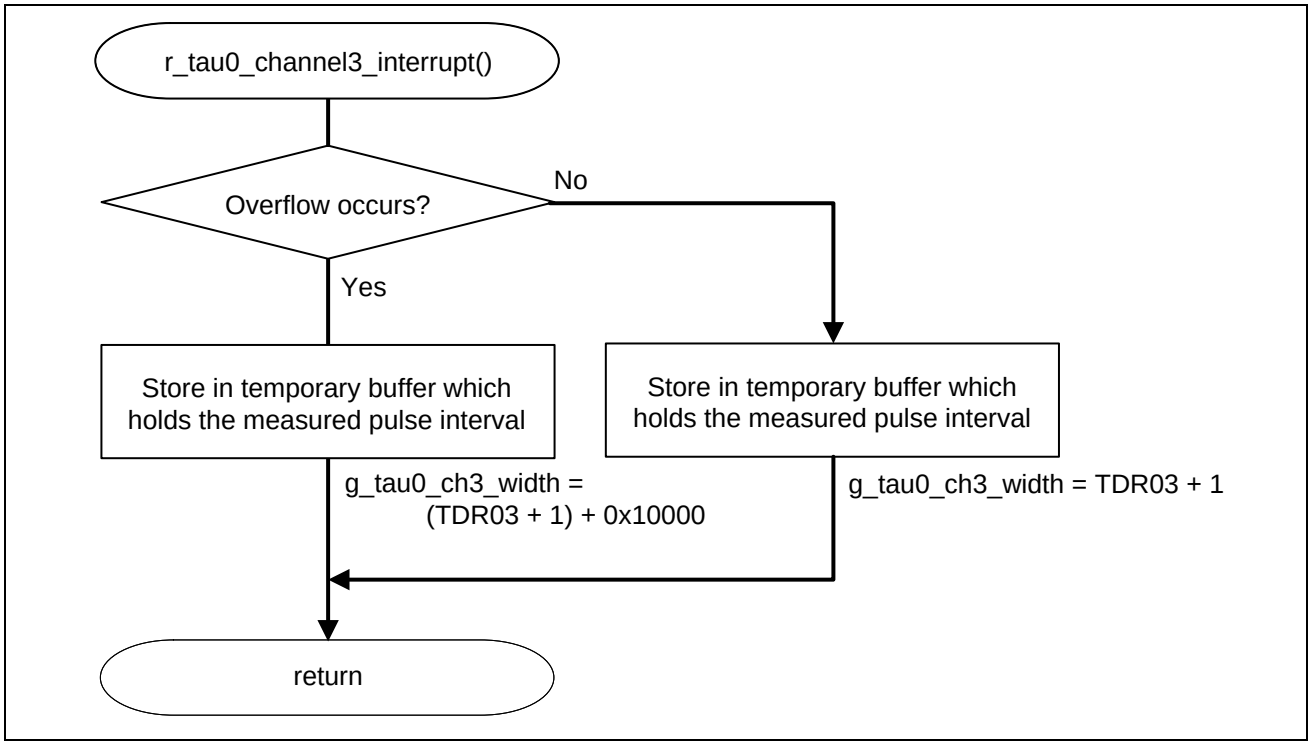

Figure 4.12 INTTM03 Interrupt Processing

5. Example of Migration from Timer Mode (Output Compare Function) or PWM Mode

5.1 Specifications

When implementing timer mode (output compare function) or PWM mode of Timer RC in R8C/36M, RL78/G14 can use PWM (Pulse Width Modulation) output of TAU.
Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.

Table 5.1 lists the peripheral functions to be used and their uses (example of migration from timer mode (output compare function) or PWM mode), and Figure 5.1 shows operation overview (example of migration from timer mode (output compare function) or PWM mode).

Table 5.1 Peripheral Functions to be Used and Their Uses (example of migration from timer mode (output compare function) or PWM mode)

Peripheral Function	Use
Timer array unit (PWM (Pulse Width Modulation) output)	Generate a pulse with a specified period and a specified duty factor

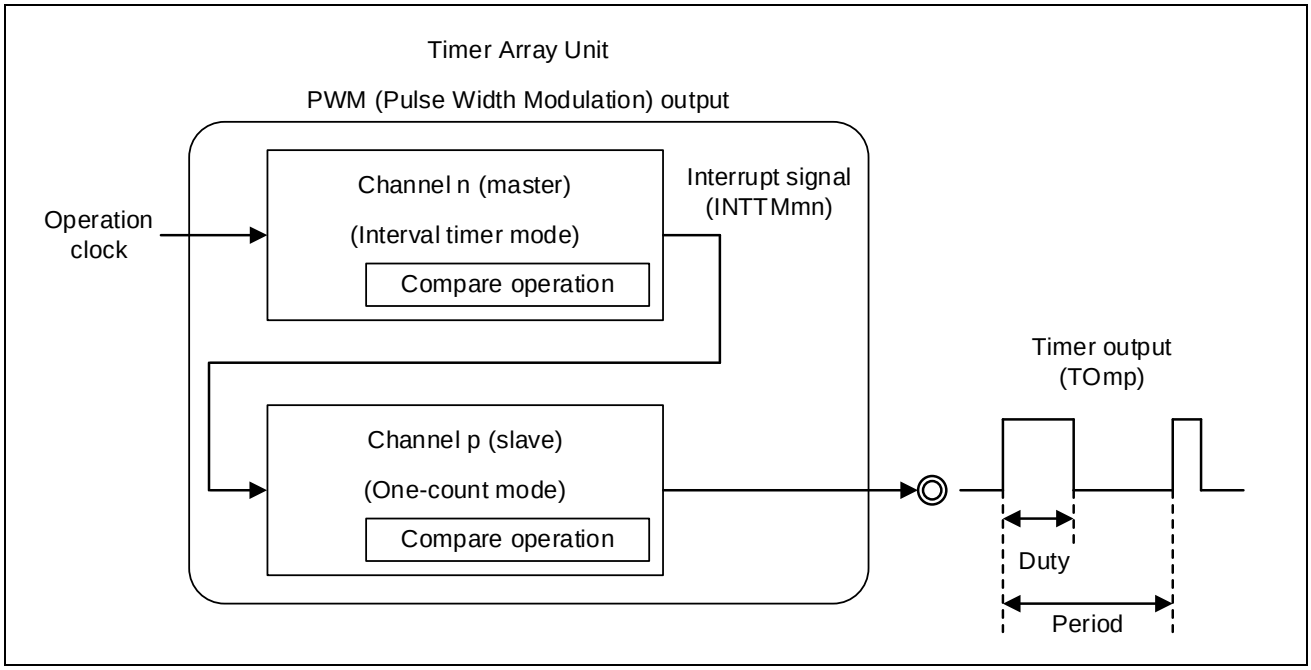

Figure 5.1 Operation Overview (example of migration from timer mode (output compare function) or PWM mode)

5.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

Table 5.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.2.0.020 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.04.00 from Renesas Electronics Corp.

5.3 Description of Hardware

5.3.1 Hardware Configuration Example

Figure 5.2 shows an example of the hardware configuration used for this chapter.

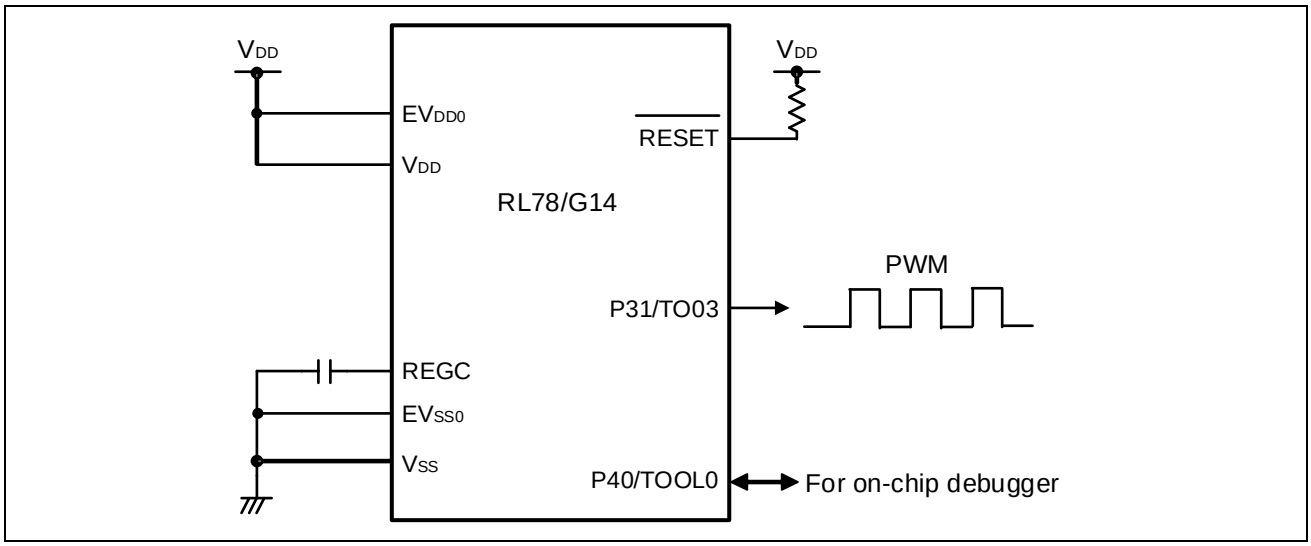

Figure 5.2 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

5.3.2 List of Pins to be Used

Table 5.3 lists the pins to be used and their functions.

Table 5.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P31/TO03	Output	PWM output port

5.4 Description of Software

5.4.1 Operation Outline

The sample program covered in this chapter implements PWM by operating channel 0 and channel 3 together, and delivers a PWM output from P31/TO03.
TO03 outputs PWM with a duty factor of 50%.

Table 5.4 lists the peripheral functions to be used and their uses. Figure 5.3 shows the timer and its interrupt operation.

(1) Initialize the TAU.
<Conditions for setting>
Set the P31/TO03 pin to a PWM output.
Set TAU0 channel 0 to 2 ms cycle interval timer mode.
Set TAU0 channel 3 to one-count mode.
Initialize the duty ratio of the PWM output to 50%.

(2) Operation starts when both the operation enable trigger bits for TAU0's channel 0 and channel 3 are set to 1 simultaneously. The sample program executes a HALT instruction.

(3) When the counter of master channel (channel 0) reaches 0000H, the value of the TDR00 register is loaded again to the TCR00 register, and the counter counts down. At the same time, PWM output (TO03) goes to the active level ("H" level).

(4) Master channel (channel 0) is used as a start trigger, the TCR03 register loads the value of the TDR03 register and the counter counts down to 0000H. When the counter of slave channel (channel 3) reaches 0000H, it waits until the next start trigger (from the master channel) is generated. At the same time, PWM output (TO03) goes to the inactive level ("L" level).

(5) The operations described in (3) and (4) above are repeated.

Table 5.4 Required Peripheral Functions and Their Uses

Peripheral Function	Use
Timer array unit 0	PWM output control for inversion of TO03 pin output

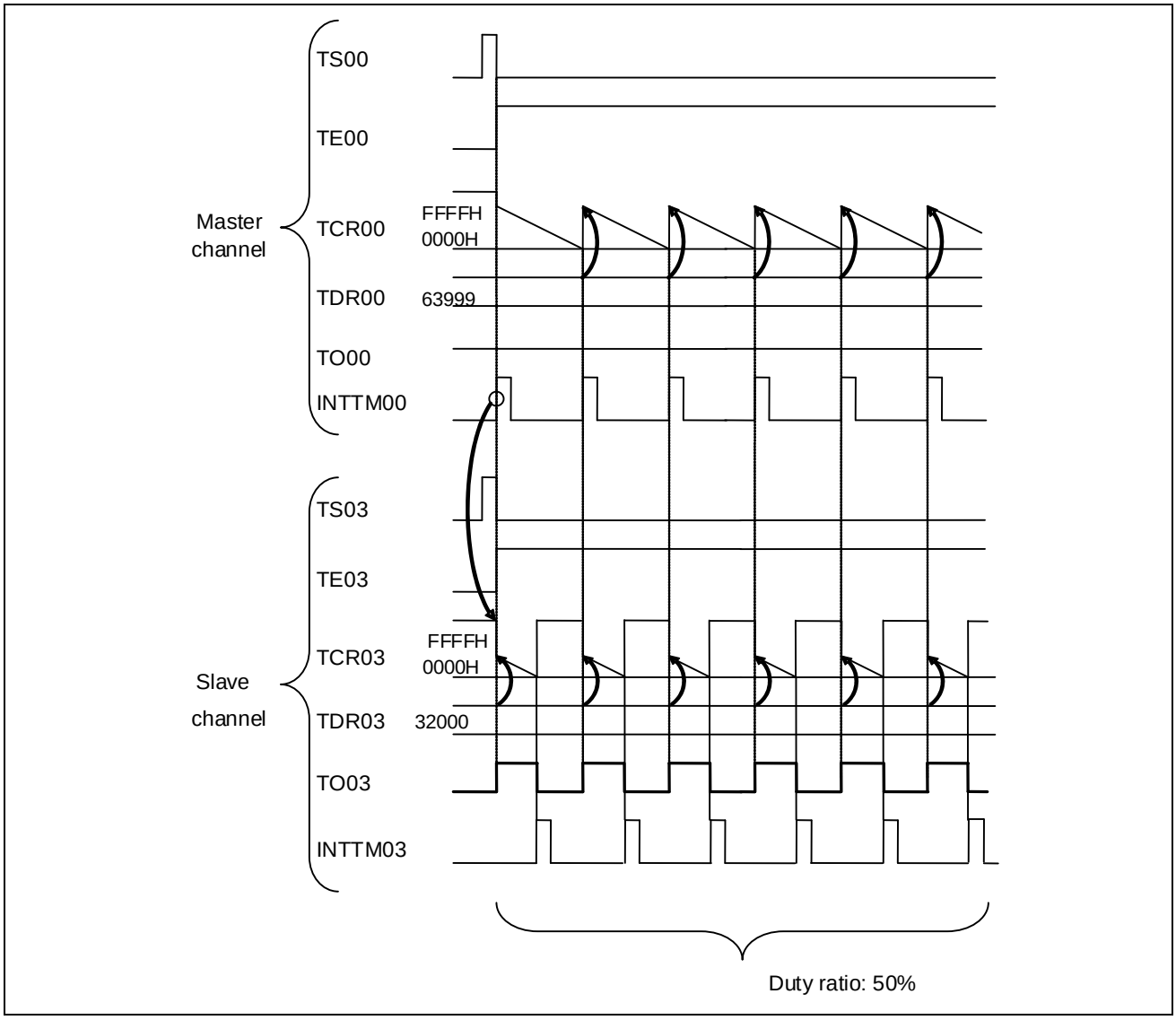

Figure 5.3 Overview of Timer Operation and Interrupts

5.4.2 List of Option Byte Setting

Table 5.5 summarizes the settings of the option bytes.

Table 5.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode, 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.4.3 List of Functions

Table 5.6 lists the functions that are used in this sample program.

Table 5.6 Functions

Function	Outline
R_TAU0_Channel0_Start	TAU0 channel 0 start processing

5.4.4 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TAU0_Channel0_Start

Synopsis	TAU0 channel 0 start processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function starts the count operation of TAU0 channel 0.
Arguments	None
Return value	None
Remarks	None

5.4.5 Flow Chart

5.4.5.1 Overall Flow

Figure 5.4 shows the overall flow of the sample program described in this chapter.

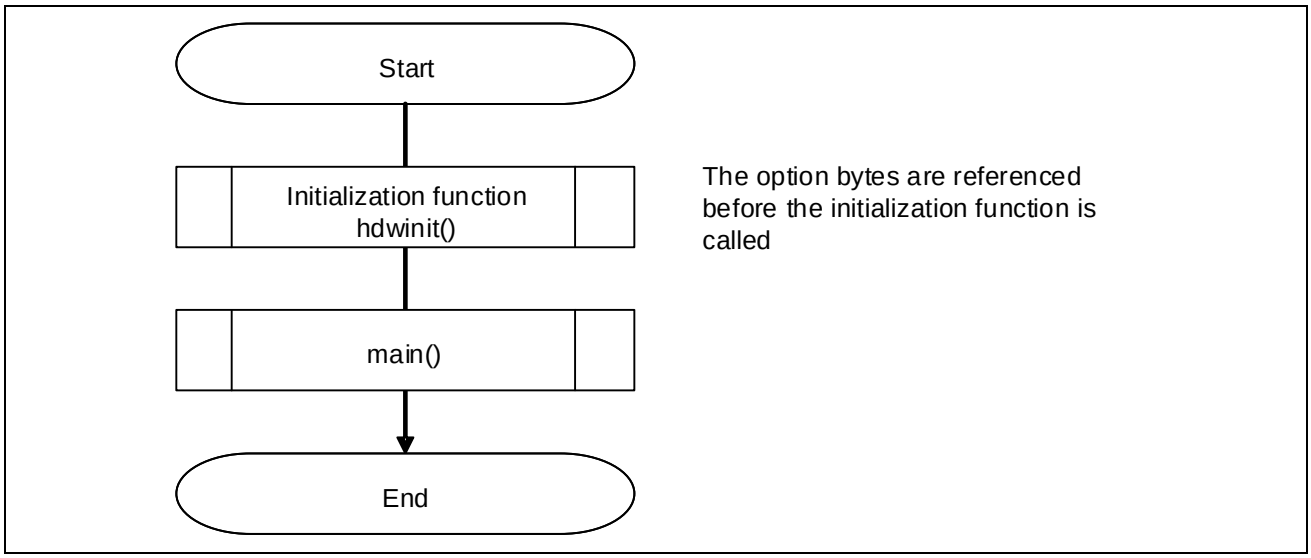

Figure 5.4 Overall Flow

5.4.5.2 Initialization Function

Figure 5.5 shows the flowchart for the initialization function.

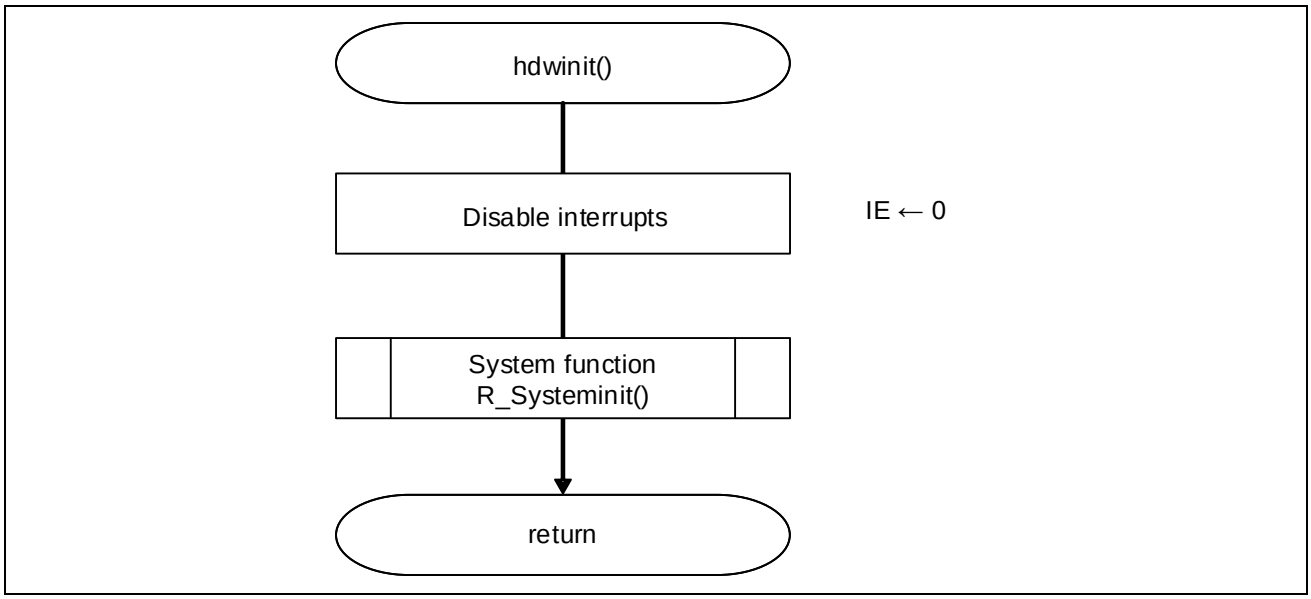

Figure 5.5 Initialization Function

5.4.5.3 System Function

Figure 5.6 shows the flowchart for the system function.

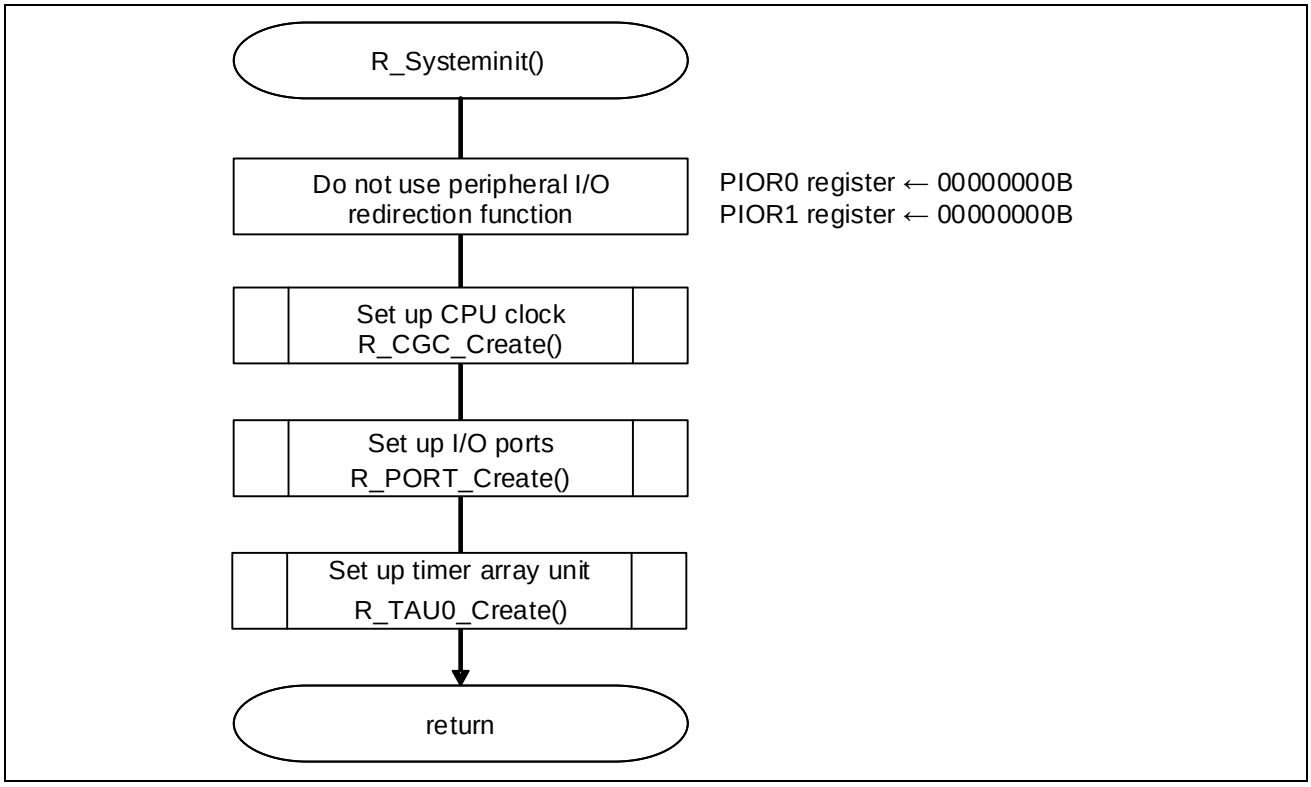

Figure 5.6 System Function

5.4.5.4 CPU Clock Setup

Figure 5.7 shows the flowchart for setting up the CPU clock.

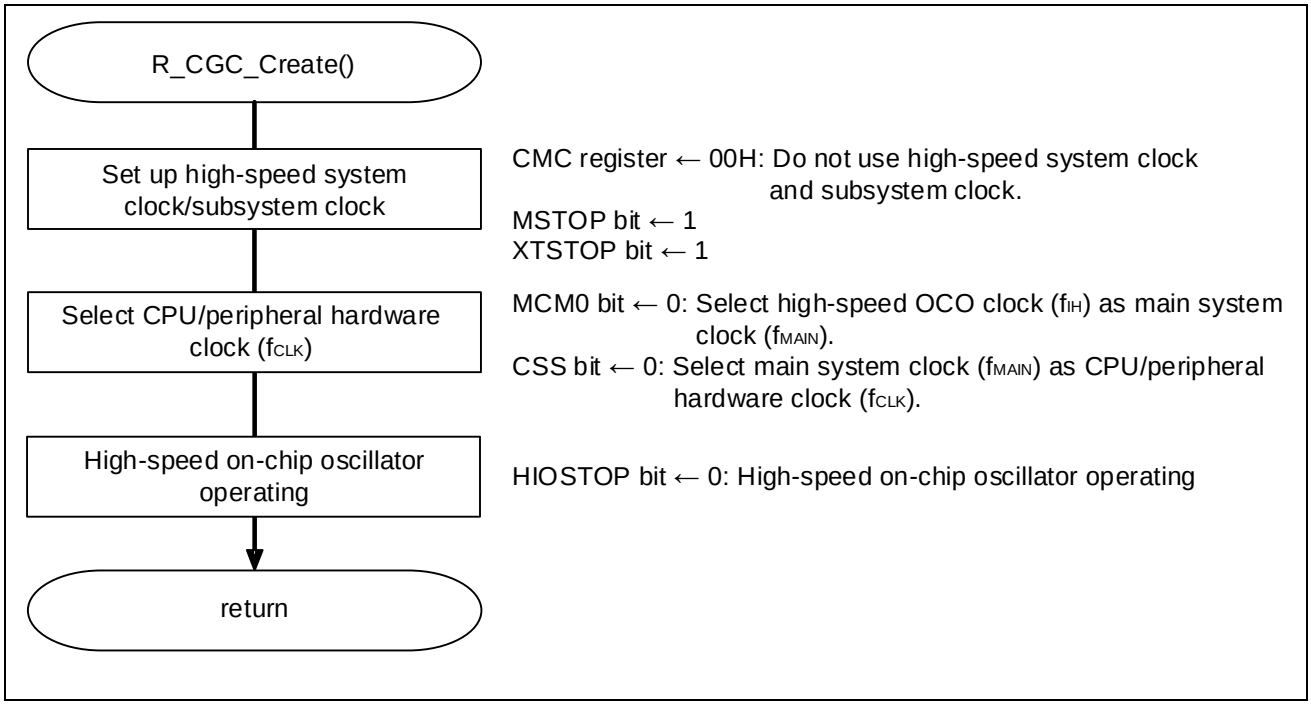

Figure 5.7 CPU Clock Setup

5.4.5.5 I/O Port Setup

Figure 5.8 shows the flowchart for setting up the I/O ports.

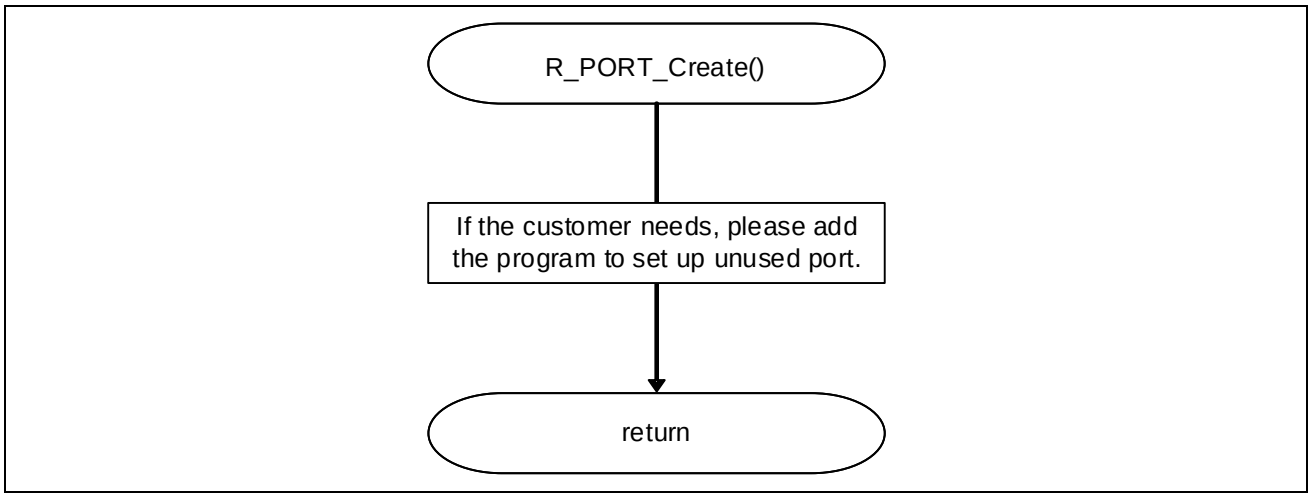

Figure 5.8 I/O Port Setup

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.4.5.6 Timer Array Unit Setup

Figures 5.9 and Figure 5.10 show the flowchart for setting up the timer array unit.

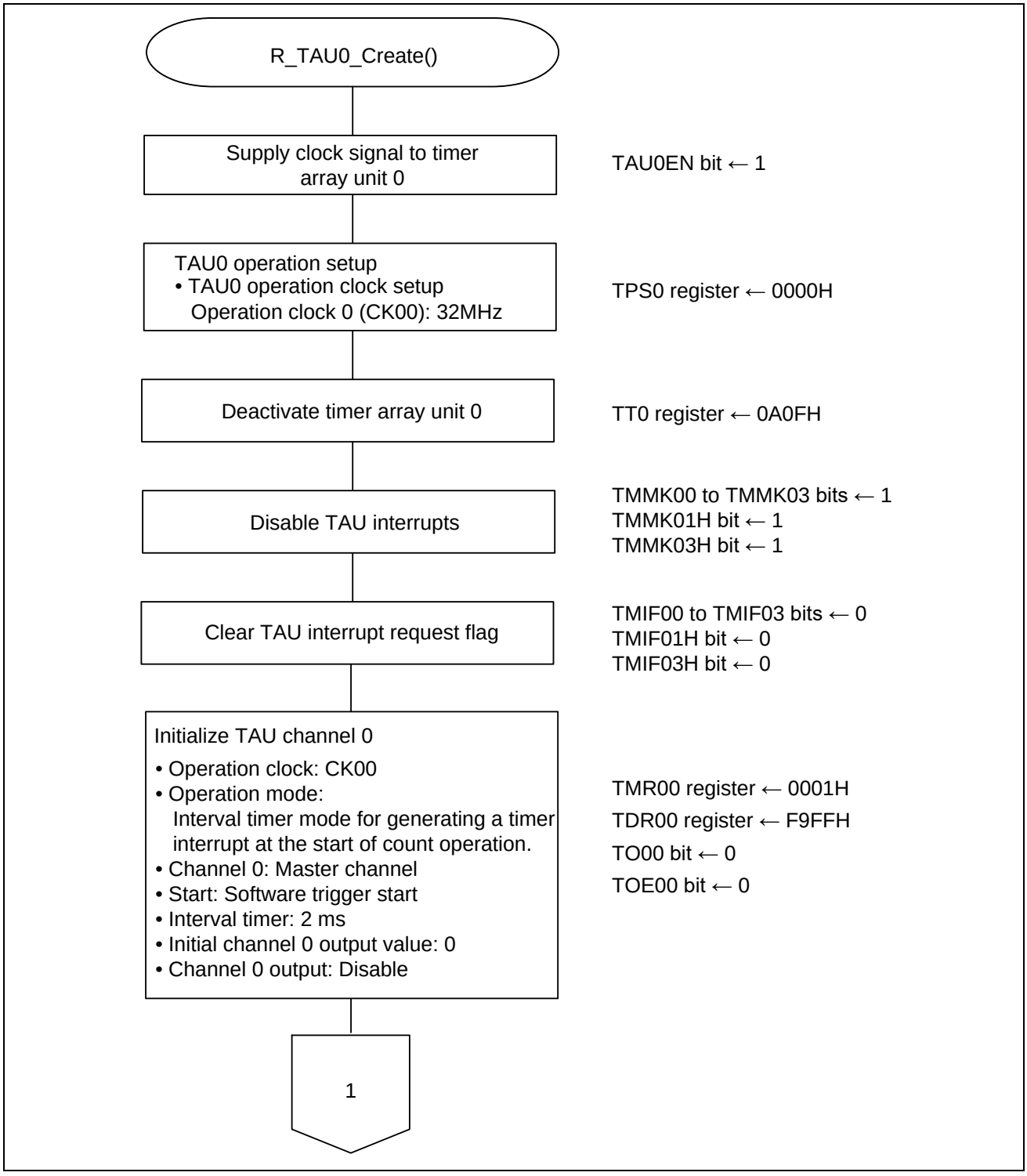

Figure 5.9 Timer Array Unit Setup (1/2)

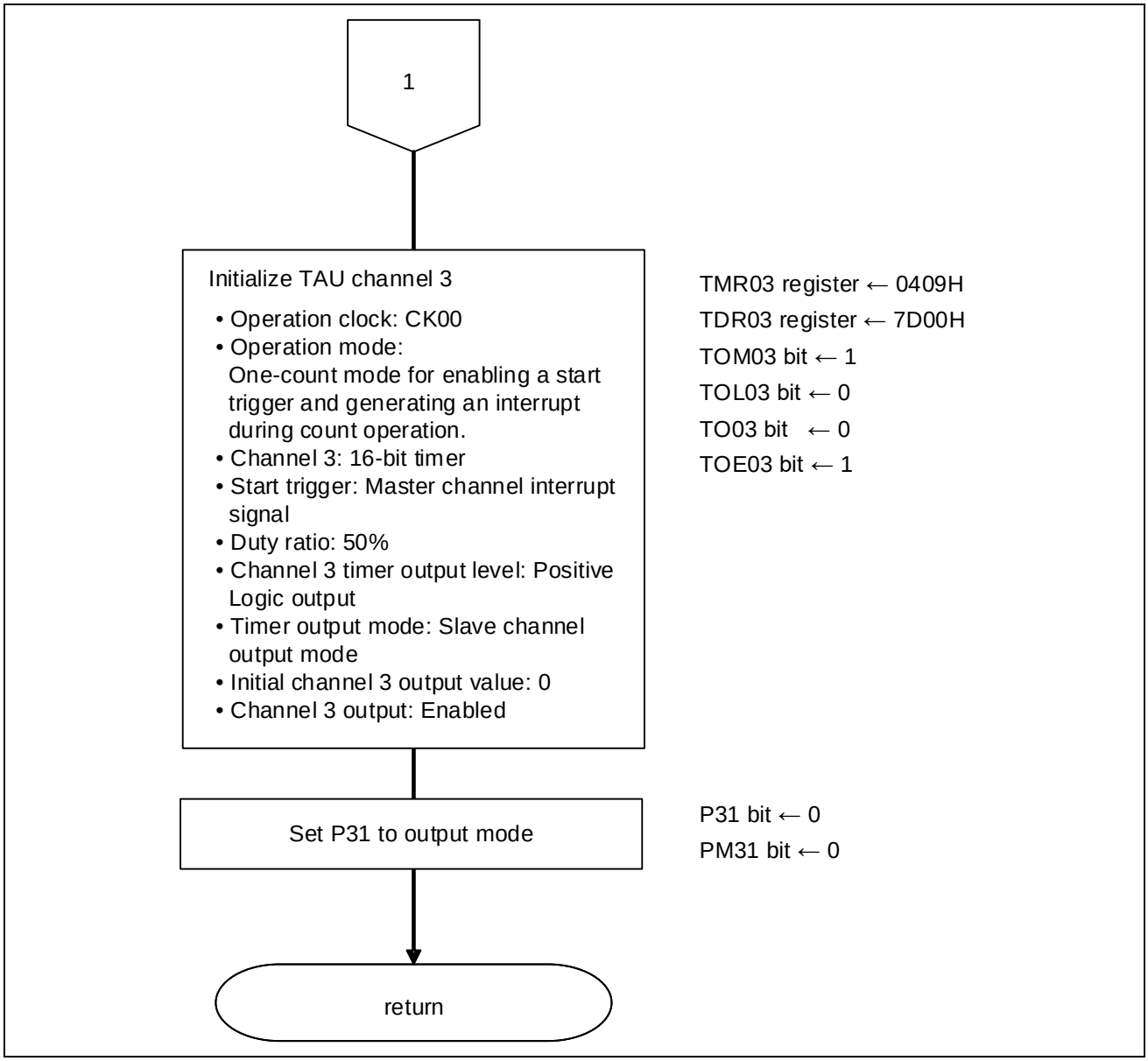

Figure 5.10 Timer Array Unit Setup (2/2)

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)

Start clock signal supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	1

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply
1	Enables input clock supply

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Configuring the timer clock frequency

- Timer clock select register 0 (TPS0)

  Select an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**PRS 031**	**PRS 030**	**0**	**0**	**PRS 021**	**PRS 020**	**PRS 013**	**PRS 012**	**PRS 011**	**PRS 010**	**PRS 003**	**PRS 002**	**PRS 001**	**PRS 000**
0	0	x	x	0	0	x	x	x	x	x	x	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
					f_{CLK}= 2 MHz	f_{CLK}= 4 MHz	f_{CLK}= 8 MHz	f_{CLK}= 20 MHz	f_{CLK}= 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	4 MHz	8 MHz	20 MHz	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2 MHz	4 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1 MHz	2 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	500 kHz	1 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	250 kHz	500 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	125 kHz	250 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	62.5 kHz	125 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	31.3 kHz	62.5 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	15.6 kHz	31.3 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	7.81 kHz	15.6 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	3.91 kHz	7.81 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	1.95 kHz	3.91 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	977 Hz	1.95 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	488 Hz	977 Hz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	244 Hz	488 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0 Hz	122 Hz	244 Hz	610 Hz	977 Hz

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00)

Select an operation clock (f_{MCK}).
Select a count clock.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	0	0	0	0	0	0	0	x	x	0	0	0	0	0	1

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits
1	Valid edge of input signal input from the TI00 pin

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	0	0	0	0	0	0	0	x	x	0	0	0	0	0	1

Bits 3 to 0

MD003	MD002	MD001	MD000	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	**0**	**0**	**1**/0	**Interval timer mode**	**Interval timer** / Square wave output / Divider function / PWM output (master)	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD000 bit (see table below).

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD000	Setting of starting counting and interrupt
• **Interval timer mode (0, 0, 0)** • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	**Timer interrupt is generated when counting is started (timer output also changes).**
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation. At that time, interrupt is not generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting up the channel 3 operation mode

- Timer mode register 03 (TMR03)

Select an operation clock (f_{MCK}).
Select a count clock.
Select the 16/8-bit timer.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS031	CKS030	0	CCS03	SPLIT03	STS032	STS031	STS030	CIS031	CIS030	0	0	MD033	MD032	MD031	MD030
0	0	0	0	0	1	0	0	x	x	0	0	1	0	0	1

Bits 15 and 14

CKS031	CKS030	Selection of operation clock (f_{MCK}) of channel 3
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS03	Selection of count clock (f_{TCLK}) of channel 3
0	**Operation clock (f_{MCK}) specified with the CKS030 and CKS031 bits**
1	Valid edge of input signal input from the TI03 pin

Bit 11

SPLIT03	Selection of 8 or 16-bit timer operation for channel 3
0	**Operates as 16-bit timer (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)**
1	Operates as 8-bit timer

Bits 10 to 8

STS032	STS031	STS030	Setting of start trigger or capture trigger of channel 3
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI03 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI03 pin input are used as a start trigger and a capture trigger.
1	**0**	**0**	**Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).**
Others than above			Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 031	CKS 030	0	CCS 03	SPLIT 03	STS 032	STS 031	STS 030	CIS 031	CIS 030	0	0	MD 033	MD 032	MD 031	MD 030
0	0	0	0	0	1	0	0	x	x	0	0	1	0	0	1

Bits 3 to 0

MD033	MD032	MD031	MD030	Operation mode of channel 3	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	**0**	**0**	**1**/0	**One-count mode**	Delay counter / One-shot pulse output / **PWM output (slave)**	**Counting down**
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD030 bit (see table below).

Operation mode (Value set by the MD033 to MD031 bits (see table above))	MD030	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	**Start trigger is valid during counting operation. At that time, interrupt is not generated.**
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Configuring the PWM output pulse cycle time
- Timer data register 00 (TDR00)
  Configure the PWM output pulse cycle time.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pulse cycle time = (TDR00 setting + 1) × Count clock cycle time
2 [ms] = (1/32[MHz]) × (TDR00 setting + 1)

⇒ TDR00 setting = 63999

Configuring the PWM output duty ratio
- Timer data register 03 (TDR03)
  Configure the PWM output duty ratio.

Symbol: TDR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Duty ratio = (TDR03 setting)/(TDR00 setting + 1) × 100
50 [%] = (TDR03 setting)/(63999 + 1) × 100

⇒ TDR03 setting = 32000

Setting up the timer output mode
- Timer output mode register 0 (TOM0)
  Set up the timer output mode for each channel.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**TOM03**	**TOM02**	**TOM01**	**0**
0	0	0	0	0	0	0	0	0	0	0	0	**1**	x	x	0

Bit 3

TOM03	Control of timer output mode of channel 3
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTM03))
1	**Slave channel output mode (output is set by the timer interrupt request signal (INTTM00) of the master channel, and reset by the timer interrupt request signal (INTTM03) of the slave channel)**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)

  Configure the output level for the timer output pin for each channel.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**TOL03**	**TOL02**	**TOL01**	**0**
0	0	0	0	0	0	0	0	0	0	0	0	**0**	x	x	0

Bit 3

TOL03	Control of timer output level of channel 3
0	**Positive logic output (active-high)**
1	Negative logic output (active-low)

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)

  Configure the output value for the timer output pin for each channel.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**TO03**	**TO02**	**TO01**	**TO00**
0	0	0	0	0	0	0	0	0	0	0	0	**0**	x	x	**0**

Bit 3

TO03	Timer output of channel 3
0	**Timer output value is "0"**
1	Timer output value is "1"

Bit 0

TO00	Timer output of channel 0
0	**Timer output value is "0"**
1	Timer output value is "1"

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Enabling the timer output

- Timer output enable register 0 (TOE0)
  Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO03 bit and an output waveform is generated.** **Writing to the TO03 bit is ignored.**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**Timer output is disabled.** **Timer operation is not applied to the TO00 bit and the output is fixed.** **Writing to the TO00 bit is enabled and the level set in the TO00 bit is output from the TO00 pin.**
1	Timer output is enabled. Timer operation is applied to the TO00 bit and an output waveform is generated. Writing to the TO00 bit is ignored.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting up the PWM output pin

- Port register (P3)
  Set the output latch.

Symbol: P3

7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**P31**	**P30**
0	0	0	0	0	0	**0**	x

Bit 1

P31	Output data control
0	**Output 0**
1	Output 1

- Port mode register (PM3)
  Select the PM31 I/O mode.

Symbol: PM3

7	6	5	4	3	2	1	0
1	**1**	**1**	**1**	**1**	**1**	**PM31**	**PM30**
1	1	1	1	1	1	**0**	x

Bit 1

PM31	P31 pin I/O mode selection
0	**Output mode (the pin functions as an output port (output buffer on))**
1	Input mode (the pin functions as an input port (output buffer off))

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.4.5.7 Main Processing

Figure 5.11 shows the flowchart for main processing.

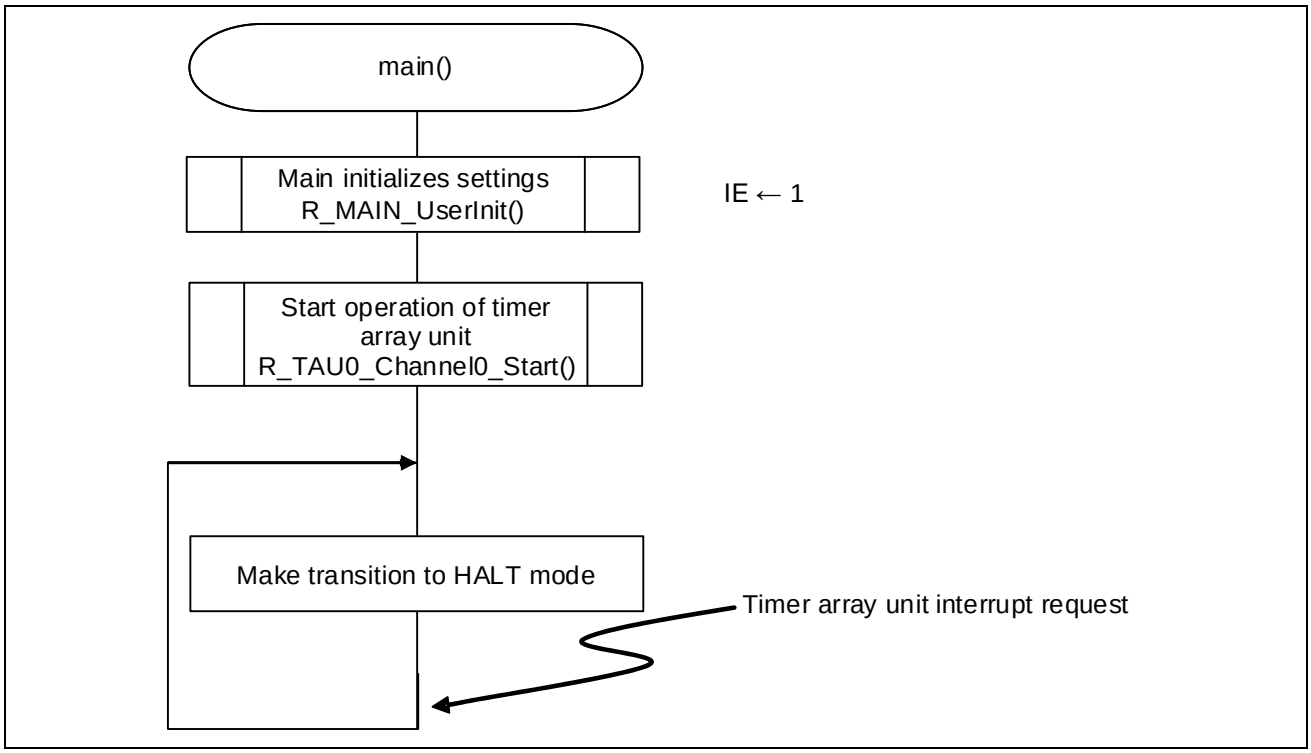

Figure 5.11 Main Processing

5.4.5.8 Timer Array Unit Operation Start

Figure 5.12 shows the flowchart for starting timer array unit operation.

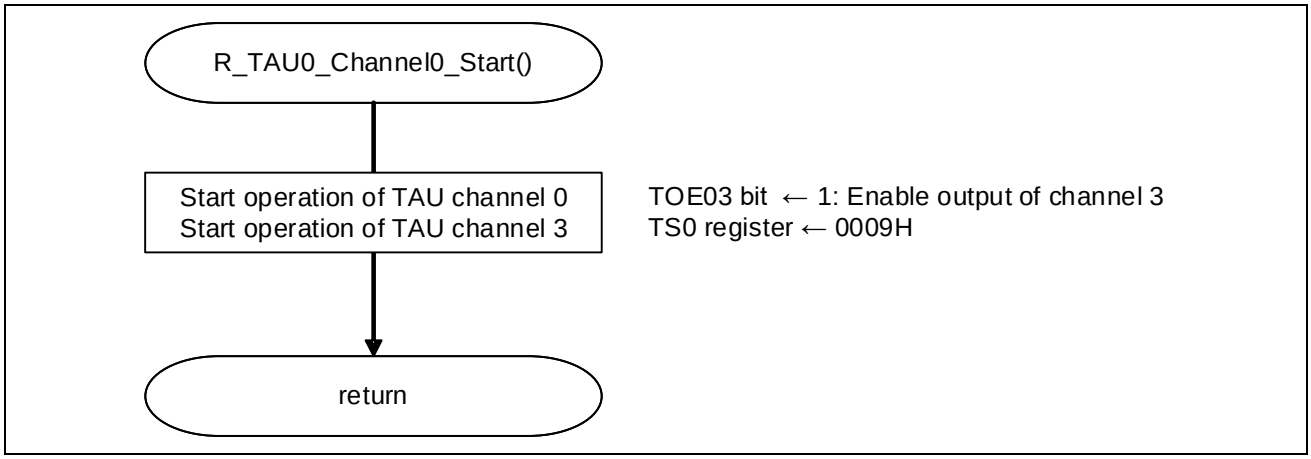

Figure 5.12 Timer Array Unit Operation Start

Enabling the timer output

- Timer output enable register 0 (TOE0)
  Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	x

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO03 bit and an output waveform is generated.** **Writing to the TO03 bit is ignored.**

Configuring the timer startup

- Timer channel start register 0 (TS0)
  Enable count operation of channel 0 and channel 3.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH03	0	TSH01	0	0	0	0	0	TS03	TS02	TS01	TS00
0	0	0	0	x	0	x	0	0	0	0	0	1	x	x	1

Bit 3

TS03	Operation enable (start) trigger of channel 3
0	No trigger operation
1	**The TE03 bit is set to 1 and the count operation becomes enabled.** **The TCR03 register count operation start in the count operation enabled state varies depending on each operation mode.**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.** **The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode.**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Application Note

RL78/G13 Timer Array Unit (Pulse Interval Measurement) CC-RL (R01AN2702)
The latest versions can be downloaded from the Renesas Electronics website.

8. Reference Documents

User's Manual: Hardware
RL78/G14 User's Manual: Hardware (R01UH0186)
R8C/36M Group User's Manual: Hardware (R01UH0259)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jan. 8, 2018	-	First edition issued

General Precautions in the Handling of MicroprocessingUnit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unitproducts from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unitproducts in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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