RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Timer RA to Timer RJ

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Introduction

This document describes how to migrate from timer RA in R8C/36M Group to timer RJ in RL78/G14 (This document is described in 64-pin package as an example).

Target Device

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Migration Method from R8C Family to RL78 Family

This application note explains how to achieve each mode (timer mode, pulse output mode, event counter mode, pulse width measurement mode and pulse period measurement mode) in timer RA of R8C/36M using RL78/G14.
Table 1.1 shows the mode in timer RA of R8C/36M Group, and Table 1.2 shows the mode in timer RJ of RL78/G14.

In R8C/36M Group, timer RA is an 8-bit timer with an 8-bit prescaler. Timer RA has five modes: timer mode, pulse output mode, event counter mode, pulse width measurement mode and pulse period measurement mode. In timer mode, the timer counts the internal count source. In pulse output mode, the timer counts the internal count source and outputs pulses which invert the polarity by underflow of the timer. In event counter mode, the timer counts external pulses. In pulse width measurement mode, the timer measures the pulse width of an external pulse. In pulse period measurement mode, the timer measures the pulse period of an external pulse.

In RL78/G14, timer RJ is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This 16-bit timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and they can be accessed by accessing the TRJ0 register. Timer RJ has five modes: timer mode, pulse output mode, event counter mode, pulse width measurement mode and pulse period measurement mode. In timer mode, the count source is counted. In pulse output mode, the count source is counted and the output is inverted at each underflow of the timer. In event counter mode, an external event is counted, and the operation is possible in STOP mode. In pulse width measurement mode, an external pulse width is measured. In pulse period measurement mode, an external pulse period is measured.

The same operation as that each mode (timer mode, pulse output mode, event counter mode, pulse width measurement mode and pulse period measurement mode) in timer RA of R8C/36M can be realized by using timer RJ of RL78/G14.

In this application note, as described in this chapter, explain the migration method for the five modes "timer mode", "pulse output mode", "event counter mode", "pulse width measurement mode" and "pulse period measurement mode".

Table 1.1 Operation Mode of Timer RA in R8C/36M

Timer RA in R8C/36M	
Mode	**Function**
Timer mode	The timer counts the internal count source.
Pulse output mode	The timer counts the internal count source and outputs pulses which invert the polarity by underflow of the timer.
Event counter mode	The timer counts external pulses.
Pulse width measurement mode	The timer measures the pulse width of an external pulse.
Pulse period measurement mode	The timer measures the pulse period of an external pulse.

Table 1.2 Corresponding Mode of Timer RJ in RL78/G14

Timer RJ in RL78/G14	
Mode	**Function**
Timer mode	The count source is counted.
Pulse output mode	The count source is counted and the output is inverted at each underflow of the timer.
Event counter mode	An external event is counted. Operation is possible in STOP mode.
Pulse width measurement mode	An external pulse width is measured.
Pulse period measurement mode	An external pulse period is measured.

2. Differences between RL78/G14 and R8C/36M Group

2.1 Differences in Function Overview

Table 2.1 lists the differences between timer RA in R8C/36M Group and timer RJ in RL78/G14.

Table 2.1 Differences

Item	R8C/36M Group Timer RA	RL78/G14 Timer RJ
Count source	• f1 • f2 • f8 • fOCO • fC32 • fC	• f_{CLK} • $f_{CLK}/2$ • $f_{CLK}/8$ • f_{IL} • f_{SUB} • Event input from the event link controller (ELC)
Configuration	8-bit timer with 8-bit prescaler (reload register included)	16-bit timer (reload register included)
External input pin	INT2	INTP4
Event counter control signals	• Event input always enabled • Event input enabled at INT2 level • Event input enabled for low signal period of TRCIOD	• Event is always counted • Event is counted during polarity period specified for INTP4 • Event is counted during polarity period specified for timer output signals (TRDIOD1, TRDIOC1, TO02, and TO03)
Input edge polarity and output polarity selection in event counter mode	• Starts counting at rising edge of the TRAIO input and TRAO starts output at “L”. • Starts counting at falling edge of the TRAIO input and TRAO starts output at “H”.	Input edge polarity and output polarity selection is independent. • TRJIO0 input edge polarity can switch between "count at rising edge" and "count at falling edge". • TRJO0 output polarity can select "output is started at low (Initialization level: Low)" or "output is started at high (Initialization level: High)".
Coordination with event link controller (ELC)	No	Yes

2.2 Differences in Timer mode

The operation of timer mode in timer RA of R8C/36M Group corresponds to timer mode in timer RJ of RL78/G14. Table 2.2 lists the differences between timer mode in timer RA of R8C/36M Group and timer mode in timer RJ of RL78/G14.

Table 2.2 Differences between Timer RA (Timer Mode) and Timer RJ (Timer Mode)

Item	R8C/36M Group (Timer RA (Timer Mode))	RL78/G14 (Timer RJ (Timer Mode))
Count sources	f1, f2, f8, fOCO, fC32, fC	f_{CLK}, $f_{CLK}/2$, $f_{CLK}/8$, f_{IL}, f_{SUB}, or event input from the event link controller (ELC) selectable
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.	1 (count starts) is written to the TSTART bit in the TRJCR0 register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.	• 0 (count stops) is written to the TSTART bit in the TRJCR0 register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJCR0 register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].	When the counter underflows.
Pin function	TRAIO pin: programmable I/O port TRAO pin: programmable I/O port	TRJIO0 pin: not used (programmable I/O port) TRJO0 pin: TRJO0 pin output
Read from timer	The count value can be read by reading registers TRA and TRAPRE.	The read value is read from the counter TRJ0 register.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter.	The write value is written to the reload register.
Selectable functions	N/A	• Coordination with the event link controller (ELC). Event input from the ELC is selectable as a count source.

2.3 Differences in Pulse Output Mode

The operation of pulse output mode in timer RA of R8C/36M Group corresponds to pulse output mode in timer RJ of RL78/G14.
Table 2.3 lists the differences between pulse output mode in timer RA of R8C/36M Group and operation as pulse output mode in timer RJ of RL78/G14.

Table 2.3 Differences between Timer RA (Pulse Output Mode) and Timer RJ (Pulse Output Mode)

Item	R8C/36M Group (Timer RA (Pulse Output Mode))	RL78/G14 (Timer RJ (Pulse Output Mode))
Count sources	f1, f2, f8, fOCO, fC32, fC	f_{CLK}, $f_{CLK}/2$, $f_{CLK}/8$, f_{IL}, f_{SUB}, or event input from the event link controller (ELC) selectable
Count operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register	1/(n+1) n: Value set in TRJ0 register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.	1 (count starts) is written to the TSTART bit in the TRJCR0 register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.	• 0 (count stops) is written to the TSTART bit in the TRJCR0 register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJCR0 register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].	When the counter underflows.
Pin functions	TRAIO pin: pulse output, programmable output port TRAO pin: programmable I/O port or inverted output of TRAIO	TRJIO0 pin: pulse output TRJO0 pin: programmable I/O port or TRJO0 pin output
Read from timer	The count value can be read by reading registers TRA and TRAPRE.	The read value is read from the counter TRJ0 register.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter.	The write value is written to the reload register.
Selectable functions	• TRAIO signal polarity switch function • TRAO output function • Pulse output stop function • TRAIO pin select function • TRAO pin select function	• TRJIO0 signal polarity switch function • TRJO0 output function • Pulse output stop function • TRJIO0 pin select function • TRJO0 pin select function • Coordination with the event link controller (ELC).

2.4 Differences in Event Counter Mode

The operation of event counter mode in timer RA of R8C/36M Group corresponds to event counter mode in timer RJ of RL78/G14.
Table 2.4 lists the differences between event counter mode in timer RA of R8C/36M Group and operation as event counter mode in timer RJ of RL78/G14.

Table 2.4 Differences between Timer RA (Event Counter Mode) and Timer RJ (Event Counter Mode)

Item	R8C/36M Group (Timer RA (Event Counter Mode))	RL78/G14 (Timer RJ (Event Counter Mode))
Count source	External signal which is input to TRAIO pin (active edge selectable by a program)	External event signal (count source) input to the TRJIO0 pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: setting value of TRAPRE register, m: setting value of TRA register	1/(n+1) n: Value set in TRJ0 register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.	1 (count starts) is written to the TSTART bit in the TRJCR0 register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.	• 0 (count stops) is written to the TSTART bit in the TRJCR0 register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJCR0 register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].	When the counter underflows.
Pin functions	TRAIO pin: count source input TRAO pin: programmable I/O port or pulse output	TRJIO0 pin: event input pin TRJO0 pin: programmable I/O port or toggle output
Read from timer	The count value can be read by reading registers TRA and TRAPRE.	The read value is read from the counter TRJ0 register.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter.	The write value is written to the reload register.
Selectable functions	• TRAIO input polarity switch function • Count source input pin select function • Pulse output function • TRAO pin select function • Digital filter function • Event input control function	• TRJIO0 input polarity switch function • Count source input pin select function • Pulse output function • TRJO0 pin select function • Digital filter function • Event input control function • Coordination with the event link controller (ELC).

2.5 Differences in Pulse Width Measurement Mode

The operation of pulse width measurement mode in timer RA of R8C/36M Group corresponds to pulse width measurement mode in timer RJ of RL78/G14.
Table 2.5 lists the differences between pulse width measurement mode in timer RA of R8C/36M Group and operation as pulse width measurement mode in timer RJ of RL78/G14.

Table 2.5 Differences between Timer RA (Pulse Width Measurement Mode) and Timer RJ (Pulse Width Measurement Mode)

Item	R8C/36M Group (Timer RA (Pulse Width Measurement Mode))	RL78/G14 (Timer RJ (Pulse Width Measurement Mode))
Count sources	f1, f2, f8, fOCO, fC32, fC	f_{CLK}, $f_{CLK}/2$, $f_{CLK}/8$, f_{IL}, f_{SUB}, or event input from the event link controller (ELC) selectable
Count operations	• Decrement • Continuously counts the selected signal only when measurement pulse is “H” level, or conversely only “L” level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.	• Decrement • When the level specified by the TEDGSEL bit in the TRJIOC0 register is input to the TRJIO0 pin, the decrement is started with the selected count source. When the specified level on the TRJIO0 pin ends, the counter is stopped, the TEDGF bit in the TRJCR0 register is set to 1 (active edge received).
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.	1 (count starts) is written to the TSTART bit in the TRJCR0 register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.	• 0 (count stops) is written to the TSTART bit in the TRJCR0 register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJCR0 register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]	• When the counter underflows. • When the measurement of the active width of the external input (TRJIO0) is completed.
Pin functions	TRAIO pin: measured pulse input TRAO pin: programmable I/O port	TRJIO0 pin: external signal input TRJO0 pin: programmable I/O port or TRJO0 pin output
Read from timer	The count value can be read by reading registers TRA and TRAPRE.	The read value is read from the counter TRJ0 register.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter.	The write value is written to the reload register.
Selectable functions	• Measurement level setting • Measured pulse input pin select function • Digital filter function	• Measurement level setting • Measured pulse input pin select function • Digital filter function • Coordination with the event link controller (ELC).

2.6 Differences in Pulse Period Measurement Mode

The operation of pulse period measurement mode in timer RA of R8C/36M Group corresponds to pulse period measurement mode in timer RJ of RL78/G14.
Table 2.6 lists the differences between pulse period measurement mode in timer RA of R8C/36M Group and operation as pulse period measurement mode in timer RJ of RL78/G14.

Table 2.6 Differences between Timer RA (Pulse Period Measurement Mode) and Timer RJ (Pulse Period Measurement Mode)

Item	R8C/36M Group (Timer RA (Pulse Period Measurement Mode))	RL78/G14 (Timer RJ (Pulse Period Measurement Mode))
Count sources	f1, f2, f8, fOCO, fC32, fC	f_{CLK}, $f_{CLK}/2$, $f_{CLK}/8$, f_{IL}, f_{SUB}, or event input from the event link controller (ELC) selectable
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents in the reload register at the second underflow of timer RA prescaler and continues counting.	• Decrement • When a pulse with the period specified by the TEDGSEL bit in the TRJIOC0 register is input to the TRJIO0 pin, the count value is transferred to the read-out buffer at the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.	1 (count starts) is written to the TSTART bit in the TRJCR0 register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.	• 0 (count stops) is written to the TSTART bit in the TRJCR0 register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRJCR0 register.
Interrupt request generation timing	• When timer RA underflows or reloads. • Rising or falling of the TRAIO input (end of measurement period).	• When the counter underflows. • When the set edge of the external input (TRJIO0) is input.
Pin functions	TRAIO pin: measured pulse input TRAO pin: programmable I/O port	TRJIO0 pin: external signal input TRJO0 pin: programmable I/O port or TRJO0 pin output
Read from timer	The count value can be read by reading registers TRA and TRAPRE.	The read value is read from the counter TRJ0 register.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter.	The write value is written to the reload register.
Selectable functions	• Measurement period selection • Measured pulse input pin select function • Digital filter function	• Measurement period selection • Measured pulse input pin select function • Digital filter function • Coordination with the event link controller (ELC).

2.7 Assigned I/O Pins

Table 2.7 lists the I/O pins assigned for use in R8C/36M Group.

Table 2.7 R8C/36M Group I/O Pins

Pin Name	Assigned Pins	I/O
INT2	P6_6 or P3_2	Input
TRAIO	P1_5, P1_7 or P3_2	I/O
TRAO	P3_0, P3_7 or P5_6	Output

Table 2.8 lists the I/O pins assigned for use in RL78/G14.

Table 2.8 RL78/G14 I/O Pins

Pin Name	Assigned Pins	I/O
INTP4	P31, P55 Note 1, or P146 Note 2	Input
TRJIO0	P01, P31, P41 Note 3 or P06 Note 4	I/O
TRJO0	P00, P30 or P50	Output

Notes: 1. This pin is only available on 64-pin and 80-pin packages.
2. This pin is only available on 100-pin package.
3. This pin is only available on 44-pin, 48-pin, 52-pin, 64-pin, 80-pin, and 100-pin packages.
4. This pin is only available on 64-pin, 80-pin, and 100-pin packages.

2.8 Register Compatibility

Register compatibilities between timer RA in R8C/36M Group and timer RJ in RL78/G14 are listed in Table 2.9.

Table 2.9 Register Compatibility

Item	R8C/36M Group	RL78/G14
Count start	• TRACR register TSTART bit	• TRJCR0 register TSTART bit
Count status flag	• TRACR register TCSTF bit	• TRJCR0 register TCSTF bit
Count forcible stop	• TRACR register TSTOP bit	• TRJCR0 register TSTOP bit Note 1
Active edge judgment flag	• TRACR register TEDGF bit	• TRJCR0 register TEDGF bit
Underflow flag	• TRACR register TUNDF bit	• TRJCR0 register TUNDF bit
Polarity switch	• TRAIOC register TEDGSEL bit	• TRJIOC0 register TEDGSEL bit
I/O pin output control	• TRAIOC register TOPCR bit	• Port mode register • Port register
Output pin output enable	• TRAIOC register TOENA bit	• TRJIOC0 register TOENA bit
Hardware LIN function select	• TRAIOC register TIOSEL bit	N/A
I/O pin input filter select	• TRAIOC register Bits TIPF0 and TIPF1	• TRJIOC0 register Bits TIPF0 and TIPF1
Event input control	• TRAIOC register Bits TIOGT0 and TIOGT1 Note 2	• TRJIOC0 register Bits TIOGT0 and TIOGT1 • TRJMR0 register TEDGPL bit • TRJISR0 register Note 3
Operating mode select	• TRAMR register Bits TMOD0 to TMOD2	• TRJMR0 register Bits TMOD0 to TMOD2
Count source select	• TRAMR register Bits TCK0 to TCK2	• TRJMR0 register Bits TCK0 to TCK2 • OSMC register
Count source cutoff	• TRAMR register TCKCUT bit	N/A
Input clock control	N/A	• PER1 register TRJ0EN bit
Counter	• TRAPRE register • TRA register	• TRJ0 register
Pin select	• TRASR register	• PIOR1 register

Notes: 1. Only writing is enabled; this bit cannot be read.
2. When using event input enabled at INT2 level, also set registers related to INT2.
3. This register can be used only in event counter mode.

2.8.1 Differences between I/O Control Registers

When using the R8C/36M Group MCU in pulse output mode, the TOPCR bit in the TRAIOC register controls output of the TRAIO pin. In contrast, the PMxx register in the RL78/G14 MCU controls port output (xx = 0 to 8, 10 to 12, 14, and 15). As RL78/G14 supports the hardware LIN using channel 3 in timer array unit 0 and UART0 in the serial array unit, it does not include the TIOSEL bit in the TRAIOC register.

TRAIOC (R8C/36M Group)

b7	b6	b5	b4	b3	b2	b1	b0
TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL

TRJIOC0 (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
TIOGT1	TIOGT0	TIPF1	TIPF0	–	TOENA	–	TEDGSEL

2.8.2 Differences between Mode Registers

The R8C/36M Group MCU controls to provide or cut off the count source by the TCKCUT bit in the TRAMR register, however, RL78/G14 does not include the TCKCUT bit. In addition, RL78/G14 has options to select event input from the ELC by bits TCK0 to TCK2 in the TRJMR0 register and to set the TEDGPL bit to specify the TRJIO0 edge polarity (one edge or both edges) in event counter mode.

TRAMR (R8C/36M Group)

b7	b6	b5	b4	b3	b2	b1	b0
TCKCUT	TCK2	TCK1	TCK0	–	TMOD2	TMOD1	TMOD0

TRJMR0 (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
–	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0

2.8.3 Differences between Timer RA and Timer RJ Counter Registers

While an 8-bit prescaler and a timer counts events in the R8C/36M Group MCU, a 16-bit down counter counts events in RL78/G14.

TRA (R8C/36M Group)

b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	–	–	–

TRAPRE (R8C/36M Group)

b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	–	–	–

TRJ0 (RL78/G14)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

2.8.4 Differences between the Timer RA Pin Select Register and Timer RJ Event Pin Select Register

In the R8C/36M Group MCU, the TRASR register is used to assign pins. The PIOR1 register assigns pins in RL78/G14. In addition, the TRJISR0 register is used to specify the timer output signal, INTP4 polarity, and timer output signals in RL78/G14.

TRASR (R8C/36M Group)

b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	TRAO SEL1	TRAO SEL0	–	TRAIO SEL1	TRAIO SEL0

PIOR1 (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	PIOR13	PIOR12	PIOR11	PIOR10

TRJISR0 (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	RCCP SEL2	RCCP SEL1	RCCP SEL0

3. Major Differences between Notes on Timers

3.1 Controlling Timer Count Start and Stop

After writing 1 to the TSTART bit while the timer stops counting, the TCSTF bit is set to 0 for the period listed in Table 3.1.

Table 3.1 Period to Start Counting

R8C/36M Group	RL78/G14	
	Event count mode is set or the count source is set to the ELC	Other than "event count mode is set or the count source is set to the ELC"
0 to 1 cycles of the count source	2 cycles of the CPU clock	3 cycles of the count source

After writing 0 to the TSTART bit when the timer is counting, the TCSTF bit is set to 1 for the period listed in Table 3.2.

Table 3.2 Period to Stop Counting

R8C/36M Group	RL78/G14	
	Event count mode is set or the count source is set to the ELC	Other than "event count mode is set or the count source is set to the ELC"
0 to 1 cycles of the count source	2 cycles of the CPU clock	3 cycles of the count source

3.2 Setting When Not Using Timer RJ

When not using timer RJ is not used in the RL78/G14, set bits TMOD2 to TMOD0 in the TRJMR0 register to 000B (set to timer mode), and the TOENA bit in the TRJIOC0 register to 0 (set to disable the TRJO0 output).

3.3 Notes When Using the Digital Filter

When using the digital filter in the RL78/G14, set bits TIPF0 and TIPF1 in the TRJIOC0 register, and wait for 5 cycles of the digital filter clock before starting the timer. When the TEDGSEL bit in the TRJIOC0 register is changed while the digital filter is used, wait for 5 cycles of the digital filter clock before starting the timer as well.

3.4 Notes On Specifying f_{IL} as the Count Source

When f_{IL} is specified as the count source for the RL78/G14, set the WUTMMCK0 bit in the OSMC register to 1. Note that f_{IL} cannot be specified as the count source of timer RJ if f_{SUB} is specified as the count source of the real-time clock or 12-bit interval timer.

4. How to Migrate Timer RA in this Sample Code

In this sample program, the operation of timer RA of R8C/36M group is realized with RL78/G14 by the method shown in Table 4.1.
For detailed contents of the sample program, please refer to "5. Example of Migration from Timer Mode" ~ "9. Example of Migration from Pulse Period Measurement Mode ".

Table 4.1 How to migrate from R8C/36M Group to RL78/G14 in this sample program

Timer RA in R8C/36M	Timer RJ in RL78/G14
Mode	Mode
Timer mode	Timer mode
Pulse output mode	Pulse output mode
Event counter mode	Event counter mode
Pulse width measurement mode	Pulse width measurement mode
Pulse period measurement mode	Pulse period measurement mode

5. Example of Migration from Timer Mode

5.1 Specifications

The same operation as that in timer mode in timer RA of R8C/36M can be realized by using timer RJ of RL78/G14. In timer mode, the count value is decremented by 1 each time the count source is input. When the count value reaches 0000H and the next count source is input, an underflow occurs and an interrupt request is generated.

Table 5.1 lists the peripheral functions to be used and their uses (example of migration from timer mode), and Figure 5.1 shows the operation overview (example of migration from timer mode).

Table 5.1 Peripheral Functions to be Used and Their Uses

(Example of Migration from Timer Mode)

Peripheral Function	Use
Timer RJ (timer mode)	The count source is counted.

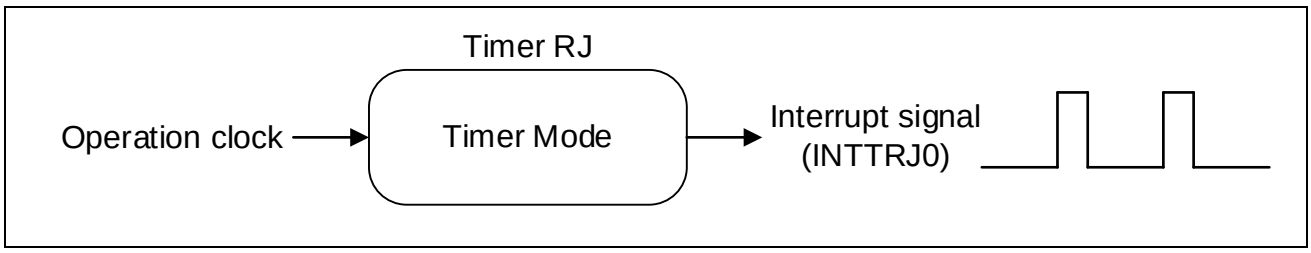

Figure 5.1 Operation Overview (Example of Migration from Timer Mode)

5.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

Table 5.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V6.0.0 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

5.3 Description of Hardware

5.3.1 Hardware Configuration Example

Figure 5.2 shows an example of hardware configuration that is used for this chapter.

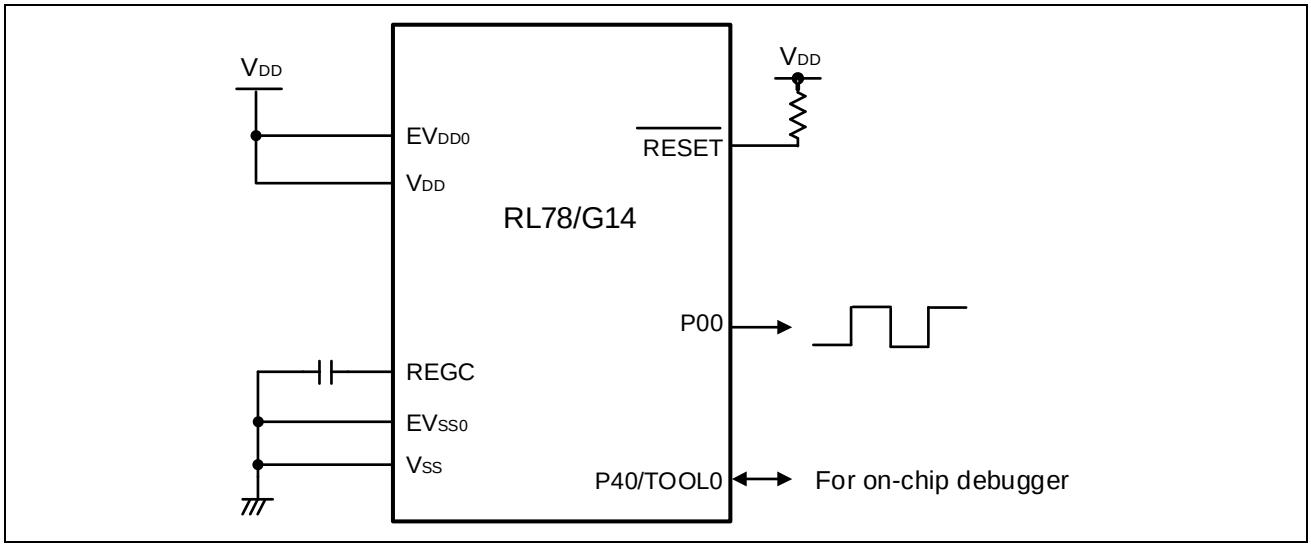

Figure 5.2 Hardware Configuration (Timer Mode)

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

5.3.2 List of Pins to be Used

Table 5.3 lists the pins to be used and their functions.

Table 5.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P00	Output	Toggle the output level when timer RJ interrupt occurs.

5.4 Description of Software

5.4.1 Operation Outline

This chapter describes how to set up the timer mode of timer RJ.
This setup is followed by operation for counting the number of timer interrupts (INTTRJ0) generated by the interval timer. Each time the count reaches 1 ms, the output level of P00 is inverted.

Table 5.4 lists the peripheral functions to be used and their uses. Figure 5.3 shows the timer mode and its interrupt operation.

(1) Initialize the timer RJ.
<Conditions for setting>
Use the timer mode as the timer RJ operation mode.
Select f_{CLK} as the count source of timer RJ.
Initialize timer RJ counter register 0 (TRJ0), and set the timer interval to 1 ms.
Use timer interrupts (INTTRJ0) from timer RJ.

(2) Sets "1" (starts counter operation) to TSTART bit of TRJCR0 register to start the count of timer RJ.

(3) Execute a HALT instruction to wait for timer interrupts (INTTRJ0).

(4) When the interrupt request is generated at 1 ms interval, toggles the output level of P00 pin.

(5) The sample code returns to step (3) to executes HALT instruction and waits for the next timer interrupt (INTTRJ0) from timer RJ.

Table 5.4 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Timer RJ	Control for inversion of the P00 pin output.

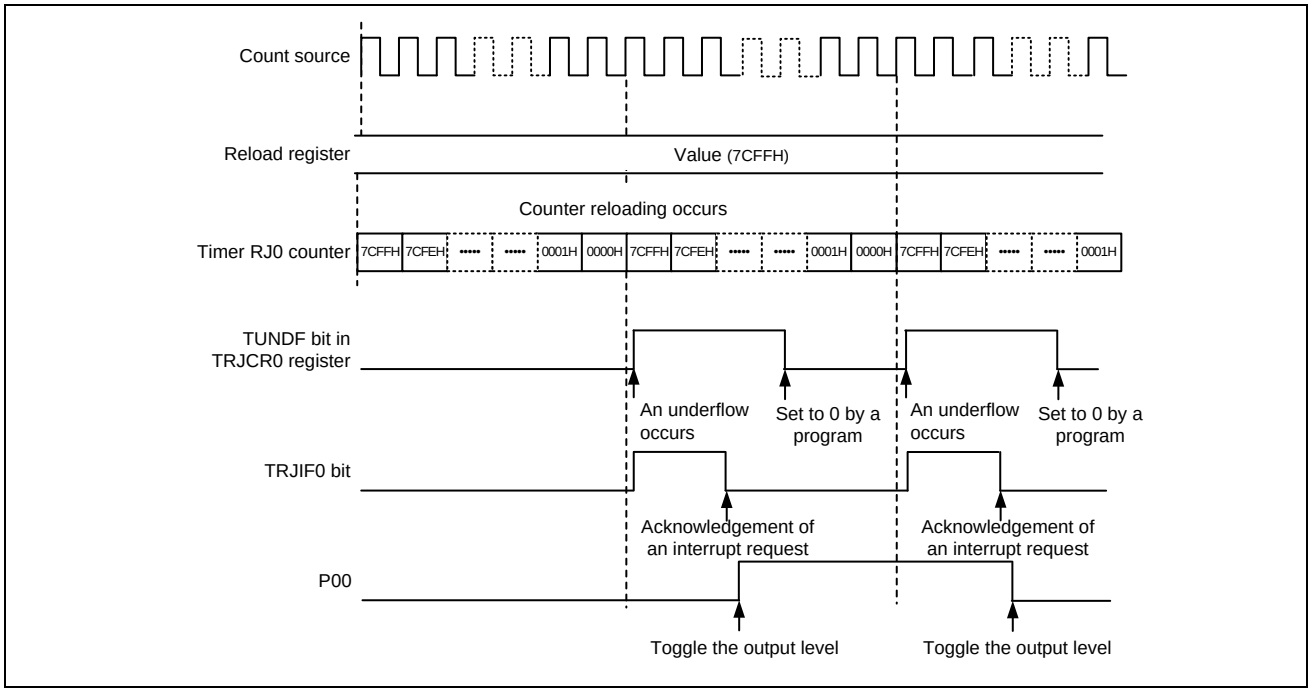

Figure 5.3 Overview of Timer RJ Operation and Interrupts (Timer Mode)

5.4.2 List of Option Byte Setting

Table 5.5 summarizes the settings of the option bytes.

Table 5.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.4.3 List of Functions

Table 5.6 lists the functions that are used in this sample program.

Table 5.6 Functions

Function Name	Outline
R_TMR_RJ0_Create()	Initializes timer RJ.
R_TMR_RJ0_Start()	Starts timer RJ operation.
r_tmr_rj0_interrupt()	Processes timer interrupts on timer RJ.

5.4.4 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TMR_RJ0_Create()

Synopsis	Initializes timer RJ
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Create(void)
Explanation	This function initializes timer RJ.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TMR_RJ0_Start()

Synopsis	Starts timer RJ operation
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Start(void)
Explanation	This function enables timer RJ interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tmr_rj0_interrupt ()

Synopsis	Timer RJ interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	static void __near r_tmr_rj0_interrupt(void)
Explanation	This function toggles the output level of P00.
Arguments	None
Return value	None
Remarks	None

5.4.5 Flow Chart

5.4.5.1 Overall Flow

Figure 5.4 shows the overall flow of the sample program described in this chapter.

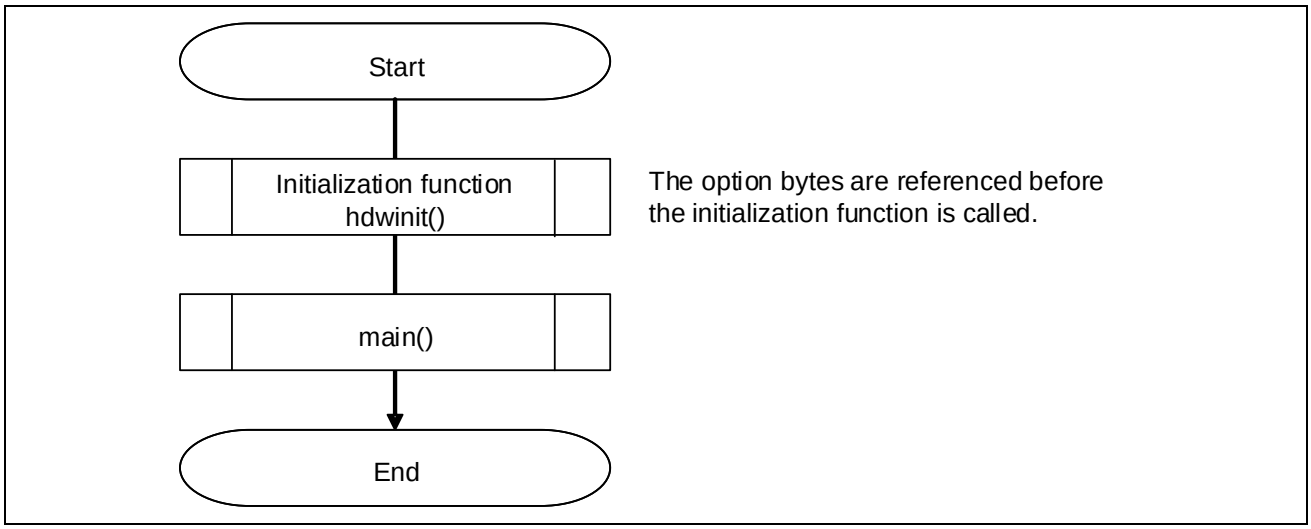

Figure 5.4 Overall Flow

5.4.5.2 Initialization Function

Figure 5.5 shows the flowchart for the initialization function.

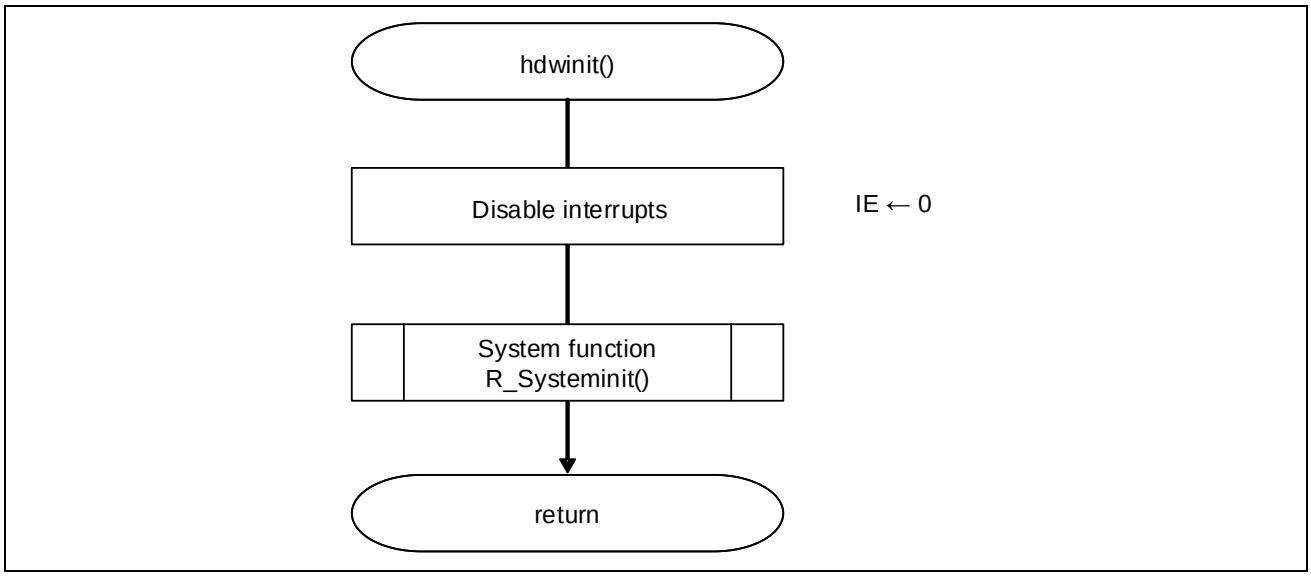

Figure 5.5 Initialization Function

5.4.5.3 System Function

Figure 5.6 shows the flowchart for the system function.

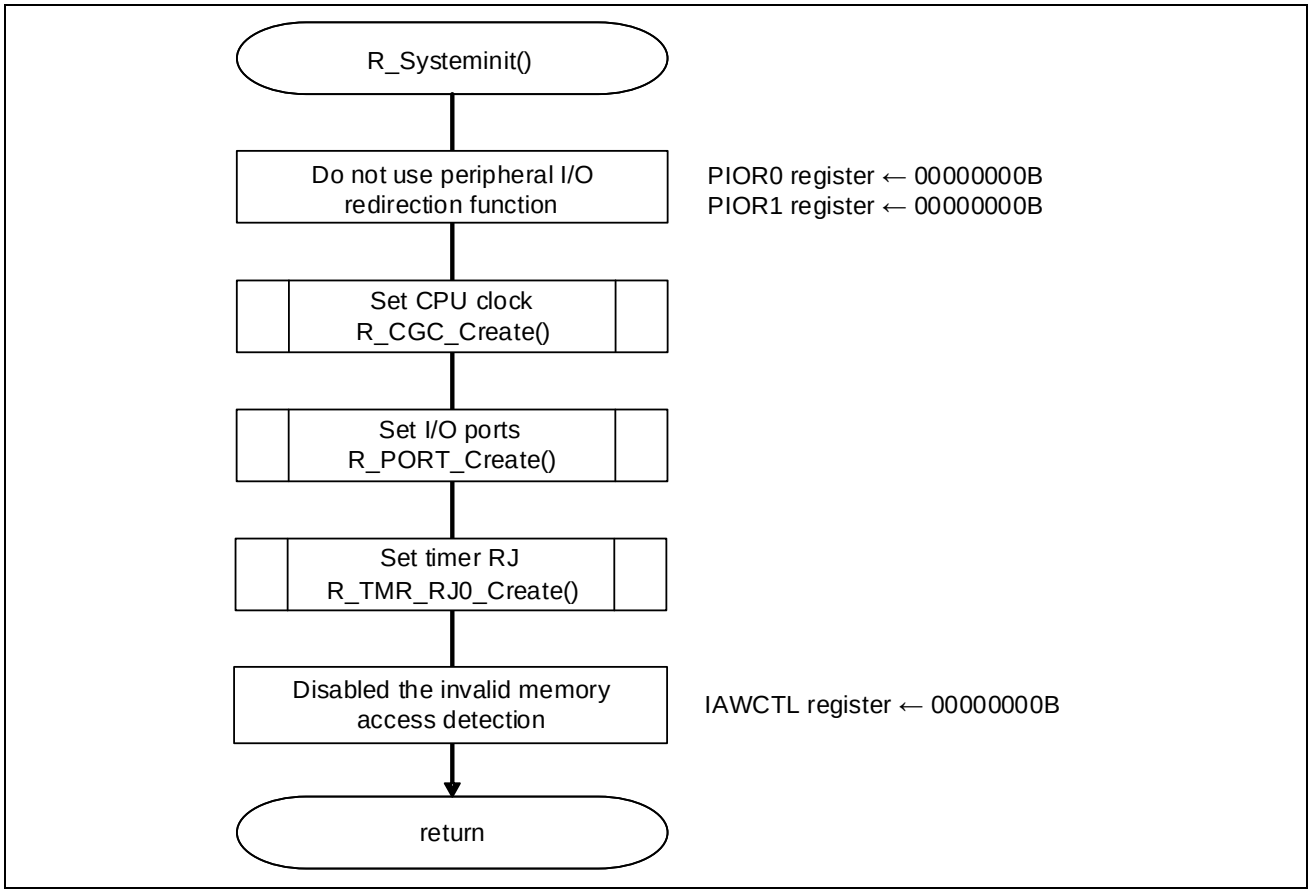

Figure 5.6 System Function

5.4.5.4 CPU Clock Setting

Figure 5.7 shows the flowchart for setting the CPU clock.

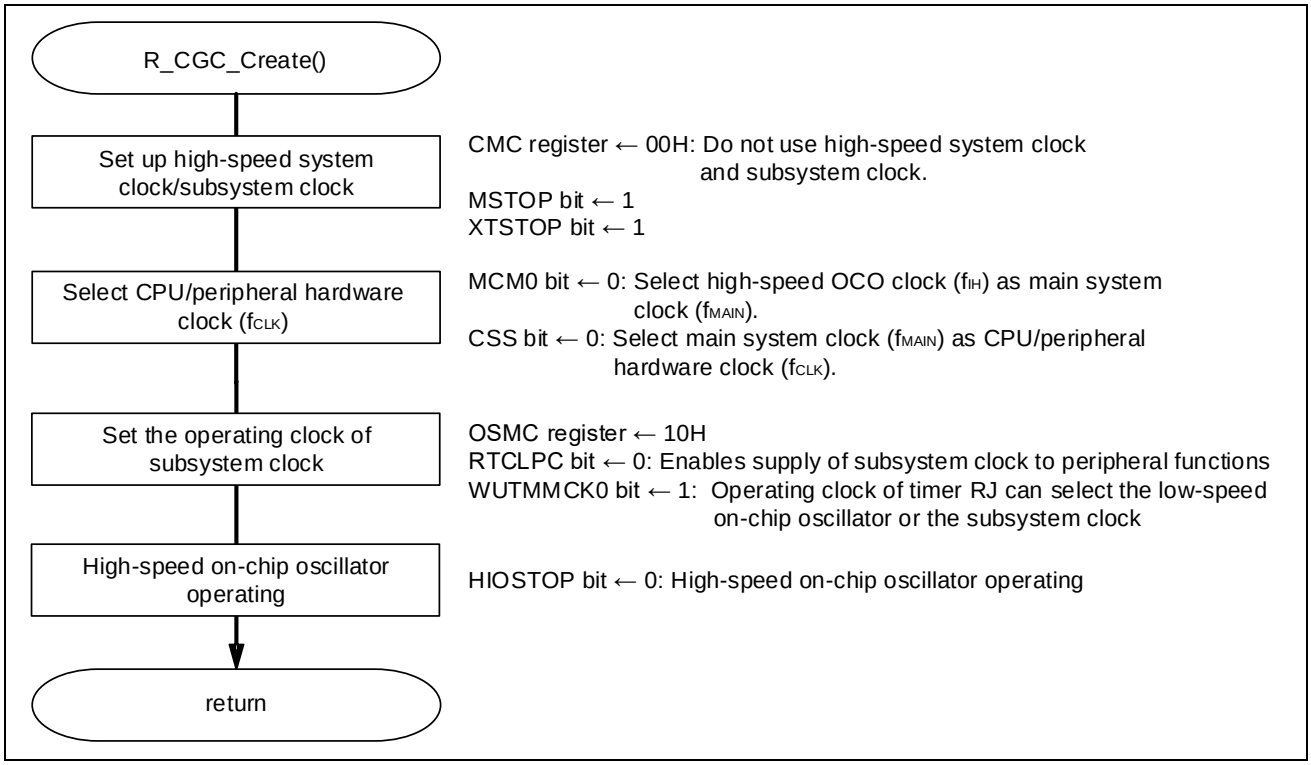

Figure 5.7 CPU Clock Setting

5.4.5.5 I/O Port Setting

Figure 5.8 shows the flowchart for setting the I/O ports.

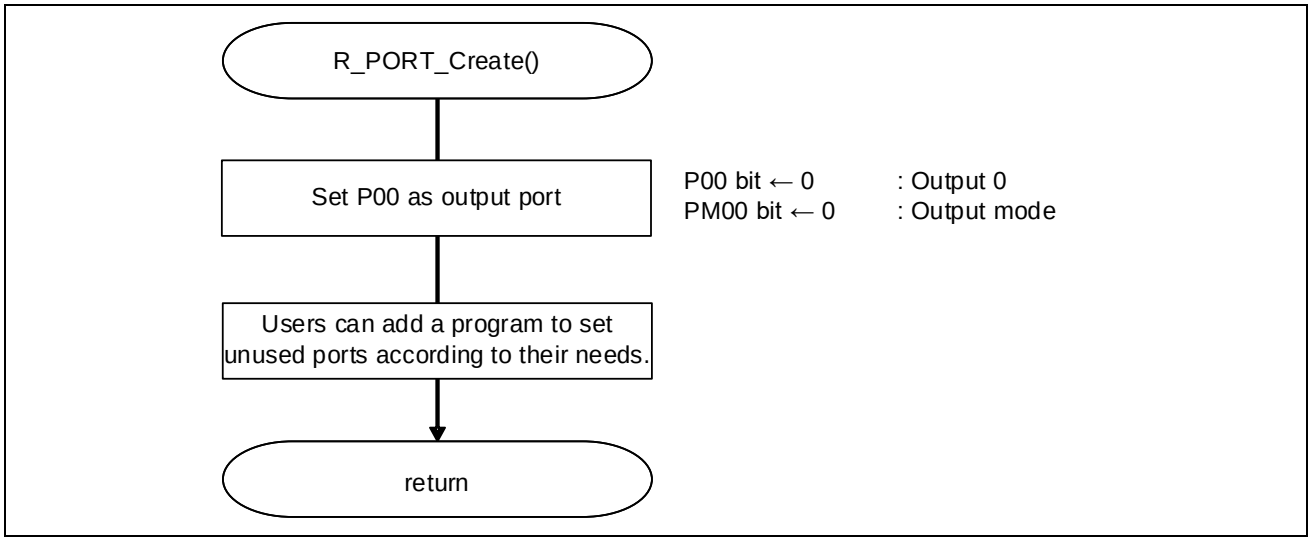

Figure 5.8 I/O Port Setting

Caution: Please provide proper pin treatment and make sure that the electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.4.5.6 Timer RJ Setting

Figure 5.9 shows the flowchart for setting timer RJ.

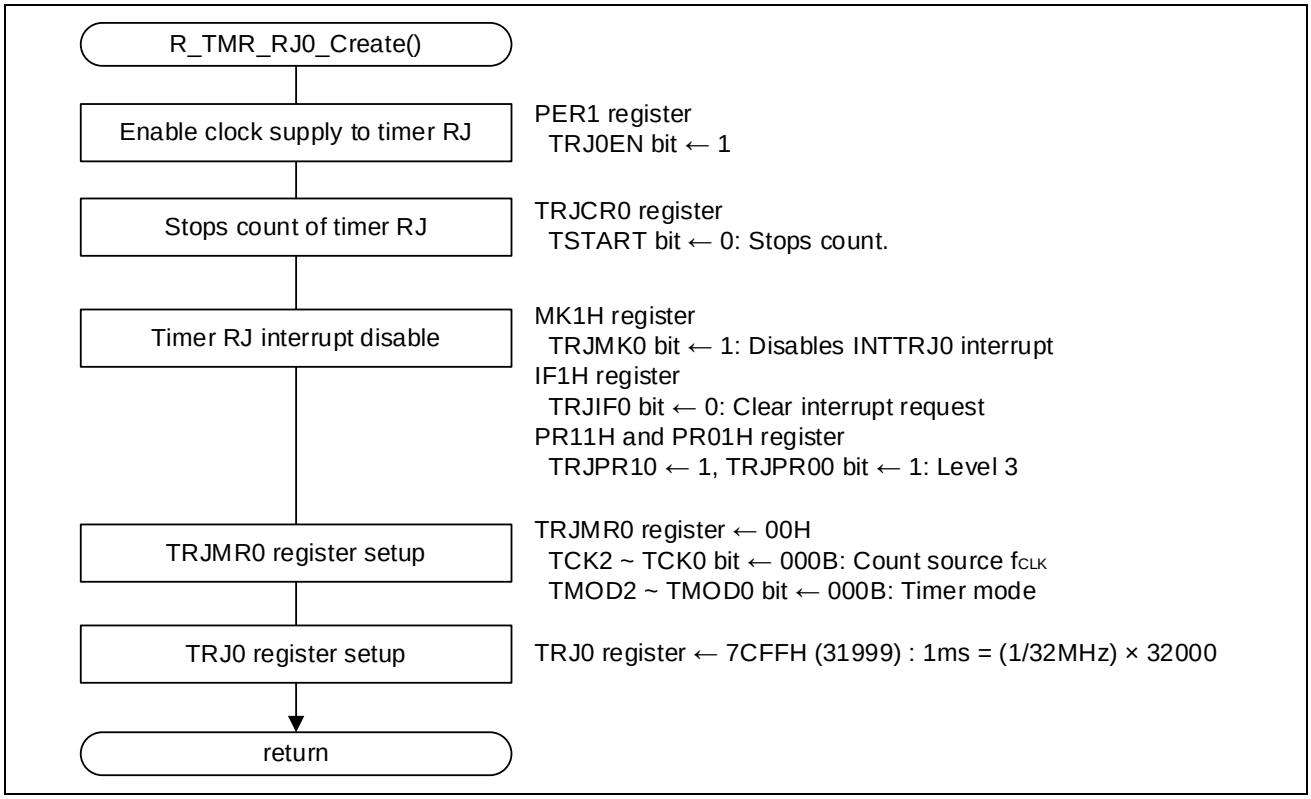

Figure 5.9 Timer RJ Setting

Start supplying clock to Timer RJ
• Peripheral enable register 1 (PER1)
Starts to supply clock to timer RJ.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
x	x	x	x	x	0	0	**1**

Bit 0

TRJ0EN	Control of timer RJ0 input clock supply
0	Stops input clock supply. • SFR used by timer RJ0 cannot be written. • Timer RJ0 is in the reset status.
1	**Enables input clock supply.** **• SFR used by timer RJ0 can be read/written.**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setup of timer RJ operation and interrupt level

• Timer RJ control register 0 (TRJCR0)
Stops Timer RJ counter operation.
Sets the interrupt cycle.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	**0**	**TUNDF**	**TEDGF**	**0**	**TSTOP**	**TCSTF**	**TSTART**
0	0	x	x	0	x	x	**0**

Bit 0

TSTART	Timer RJ count start
0	**Count stops**
1	Count starts

Disabling timer RJ interrupt
• Interrupt mask flag register (MK1H)
Disables interrupt processing.
• Interrupt request flag register (IF1H)
Clears the interrupt request flag.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	**TRJMK0**	**SRMK3 CSIMK31 IICMK31**	**STMK3 CSIMK30 IICMK30**	**KRMK**	**ITMK**	**RTCMK**	**ADMK**
x	**1**	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	**TRJIF0**	**SRIF3 CSIIF31 IICIF31**	**STIF3 CSIIF30 IICIF30**	**KRIF**	**ITIF**	**RTCIF**	**ADIF**
x	**0**	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting timer RJ interrupt priority level
• Priority Specification Flag Register (PR11H, PR01H)
Specifies level 3 (low priority level).

Symbol: PR11H

7	6	5	4	3	2	1	0
TMPR110	TRJPR10	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
x	**1**	x	x	x	x	x	x

Symbol: PR01H

7	6	5	4	3	2	1	0
TMPR010	TRJPR00	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
x	**1**	x	x	x	x	x	x

Bit 6

TRJPR10	TRJPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the timer RJ operation
• Timer RJ mode register 0 (TRJMR0)
Count source selection and operation mode selection.

Symbol: TRJMR0

7	6	5	4	3	2	1	0
0	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
0	0	0	0	x	0	0	0

Bit 6 to 4

TCK2	TCK1	TCK0	Timer RJ count source select
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/8$
0	1	1	$f_{CLK}/2$
1	0	0	f_{IL}
1	0	1	Event input from ELC
1	1	0	f_{SUB}
Other than above			Setting prohibited

Bit 2 to 0

TMOD2	TMOD1	TMOD0	Timer RJ operating mode select
0	0	0	Timer mode
0	0	1	Pulse output mode
0	1	0	Event counter mode
0	1	1	Pulse width measurement mode
1	0	0	Pulse period measurement mode
Other than above			Setting prohibited

Setting TRJ0 register
• Timer RJ counter register 0 (TRJ0)
Setup of Timer RJ interrupt cycles.

Symbol: TRJ0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1

Generation of Timer RJ interrupt (INTTRJ0) = (Setup value of TRJ0 + 1) × Count clock period
1 ms = (31999 + 1) x (1/32000000)

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.4.5.7 Main Processing

Figure 5.10 shows the flowchart for main processing.

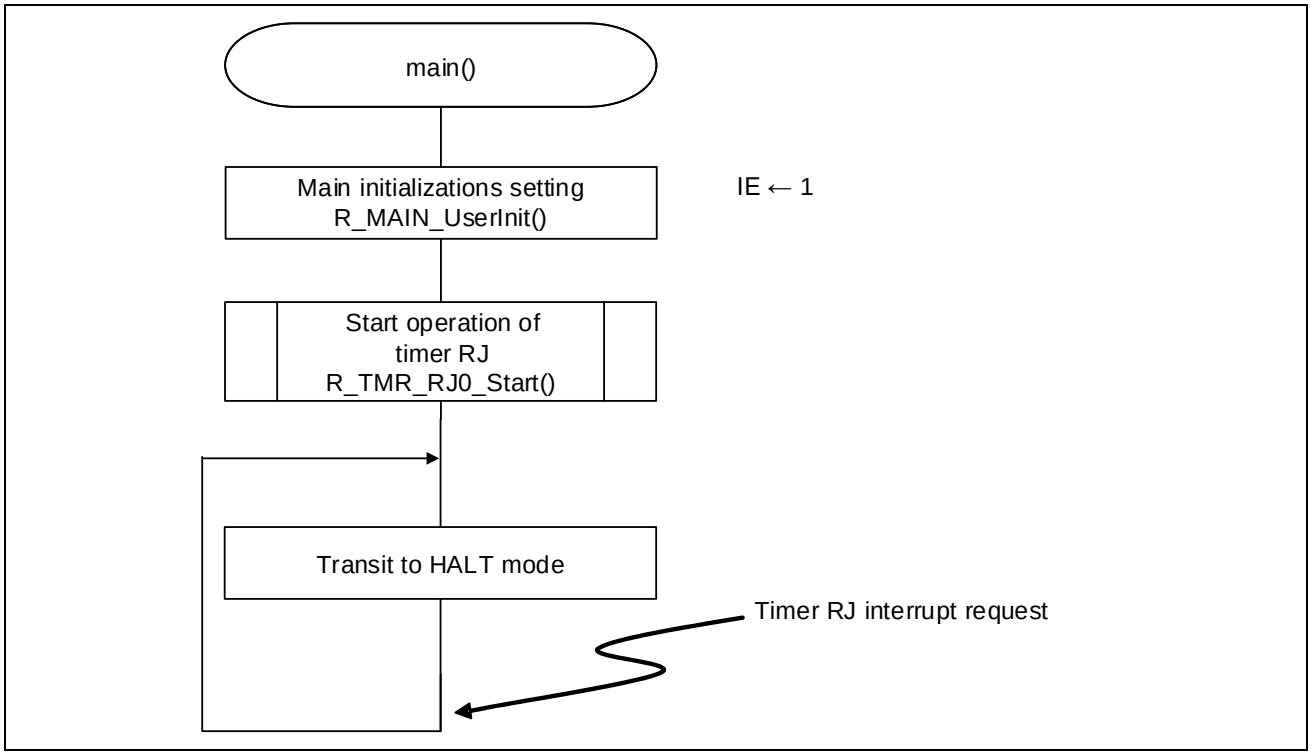

Figure 5.10 Main Processing

5.4.5.8 Timer RJ Operation Start

Figure 5.11 shows the flowchart for starting timer RJ operation.

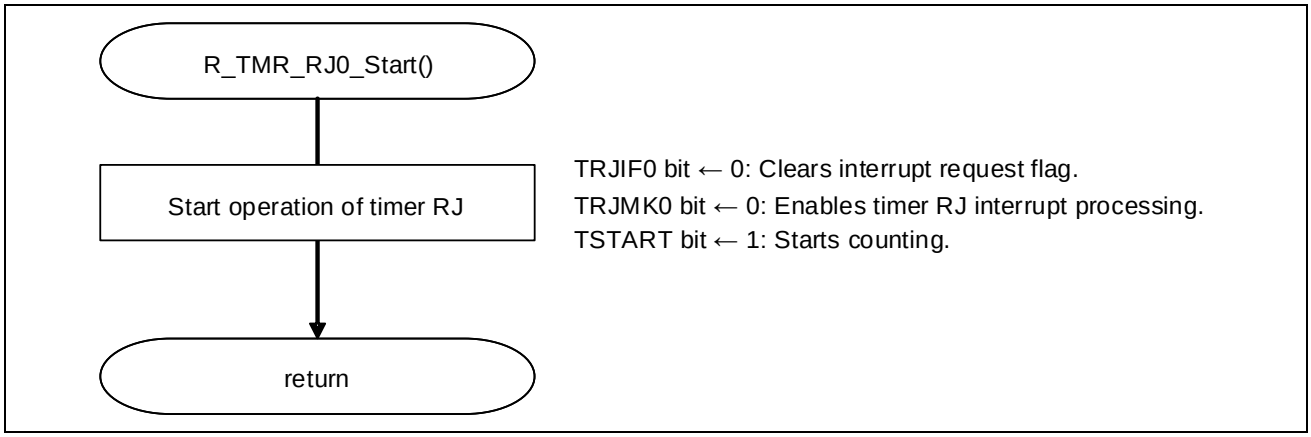

Figure 5.11 Timer RJ Operation Start

Configuring the timer interrupt
• Interrupt request flag register (IF1H)
Clears the interrupt request flag.
• Interrupt mask flag register (MK1H)
Enables interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	0	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	0	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Starting timer RJ counter operation
• Timer RJ control register 0 (TRJCR0)
Starts timer RJ counter operation.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSTF	TSTART
0	0	x	x	0	x	x	1

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	Count starts

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.4.5.9 INTTRJ0 Interrupt Processing

Figure 5.12 shows the flowchart for INTTRJ0 interrupt processing.

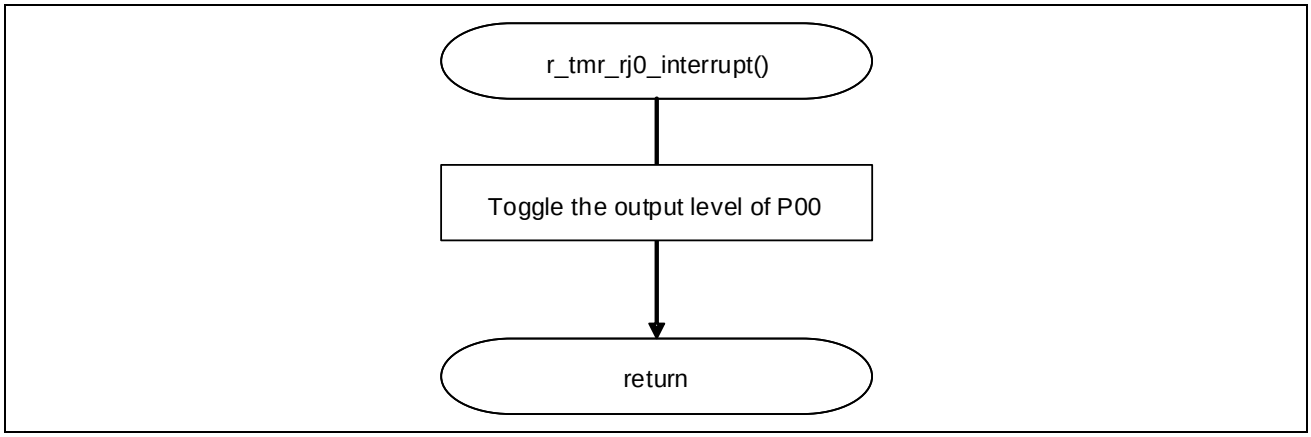

Figure 5.12 INTTRJ0 Interrupt Processing

6. Example of Migration from Pulse Output Mode

6.1 Specifications

The same operation as that in pulse output mode in timer RA of R8C/36M can be realized by using timer RJ of RL78/G14.
In pulse output mode, the count value is decremented by 1 each time the count source is input. When the count value reaches 0000H and the next count source is input, an underflow occurs and an interrupt request is generated.
In addition, a pulse can be output from pins TRJIO0 and TRJO0. The output level is inverted each time an underflow occurs. The pulse output from the TRJO0 pin can be stopped by the TOENA bit in the TRJIOC0 register.

Table 6.1 lists the peripheral functions to be used and their uses (example of migration from pulse output mode), and Figure 6.1 shows the operation overview (example of migration from pulse output mode).

Table 6.1 Peripheral Functions to be Used and Their Uses

(Example of Migration from Pulse Output Mode)

Peripheral Function	Use
Timer RJ (pulse output mode)	The count source is counted and the output is inverted at each underflow of the timer.

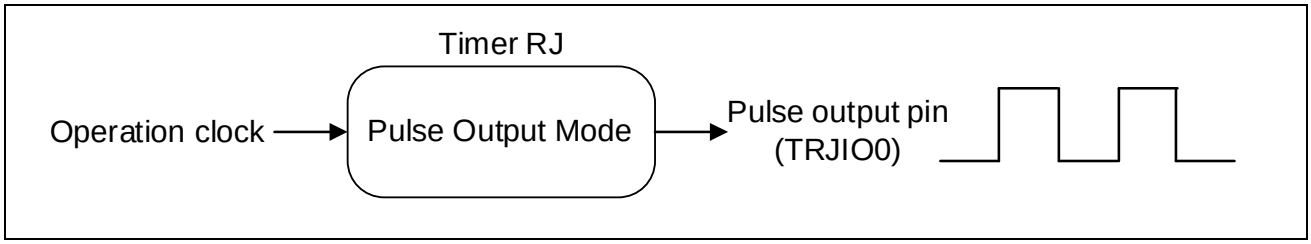

Figure 6.1 Operation Overview (Example of Migration from Pulse Output Mode)

6.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

Table 6.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (VLVD): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V6.0.0 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

6.3 Description of Hardware

6.3.1 Hardware Configuration Example

Figure 6.2 shows an example of hardware configuration that is used for this chapter.

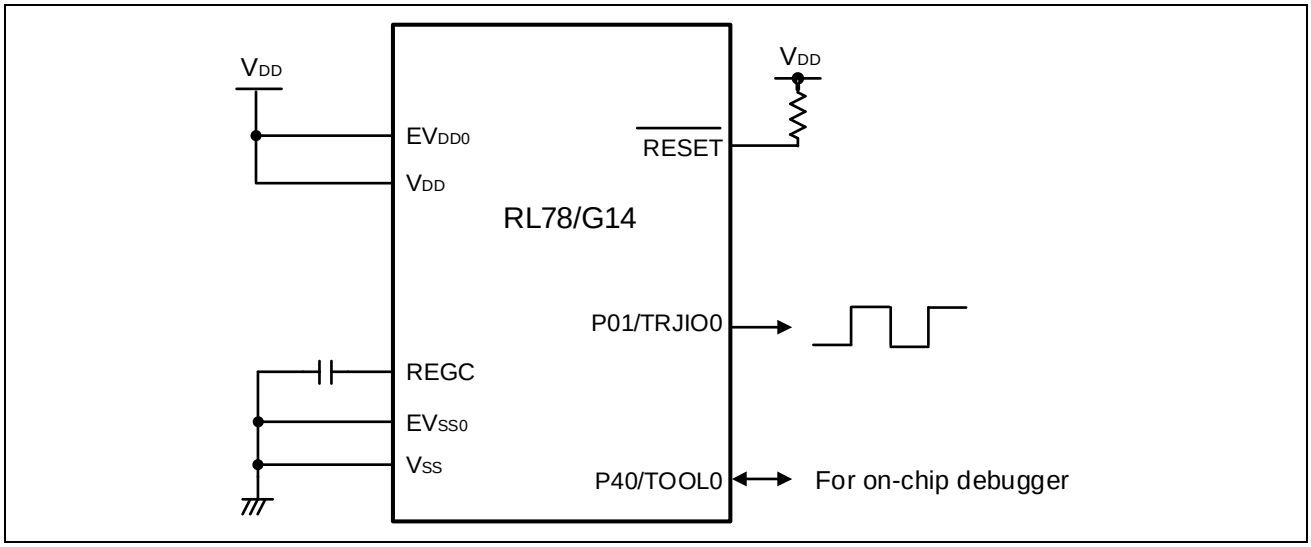

Figure 6.2 Hardware Configuration (Pulse Output Mode)

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

6.3.2 List of Pins to be Used

Table 6.3 lists the pins to be used and their functions.

Table 6.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P01/TRJIO0	Output	Output pulse.

6.4 Description of Software

6.4.1 Operation Outline

This chapter describes how to set up the pulse output mode of timer RJ.
In this mode, the counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR0 register, and the output level of TRJIO0 pin is inverted each time an underflow occurs.

Table 6.4 lists the peripheral functions to be used and their uses. Figure 6.3 shows the pulse output mode and its interrupt operation.

(1) Initialize the timer RJ.
<Conditions for setting>
Use the pulse output mode as the timer RJ operation mode.
Select f_{CLK} as the count source of timer RJ.
Initialize timer RJ counter register 0 (TRJ0), and set the timer interval to 1 ms.

(2) Sets "1" (starts counter operation) to TSTART bit of TRJCR0 register to start the count of timer RJ.

(3) Execute a HALT instruction to wait for timer interrupts (INTTRJ0).

(4) When the underflow occurs, output of TRJIO0 pin is inverted.

Table 6.4 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Timer RJ	P01/TRJIO0 output pulse (timer interval is 1ms).

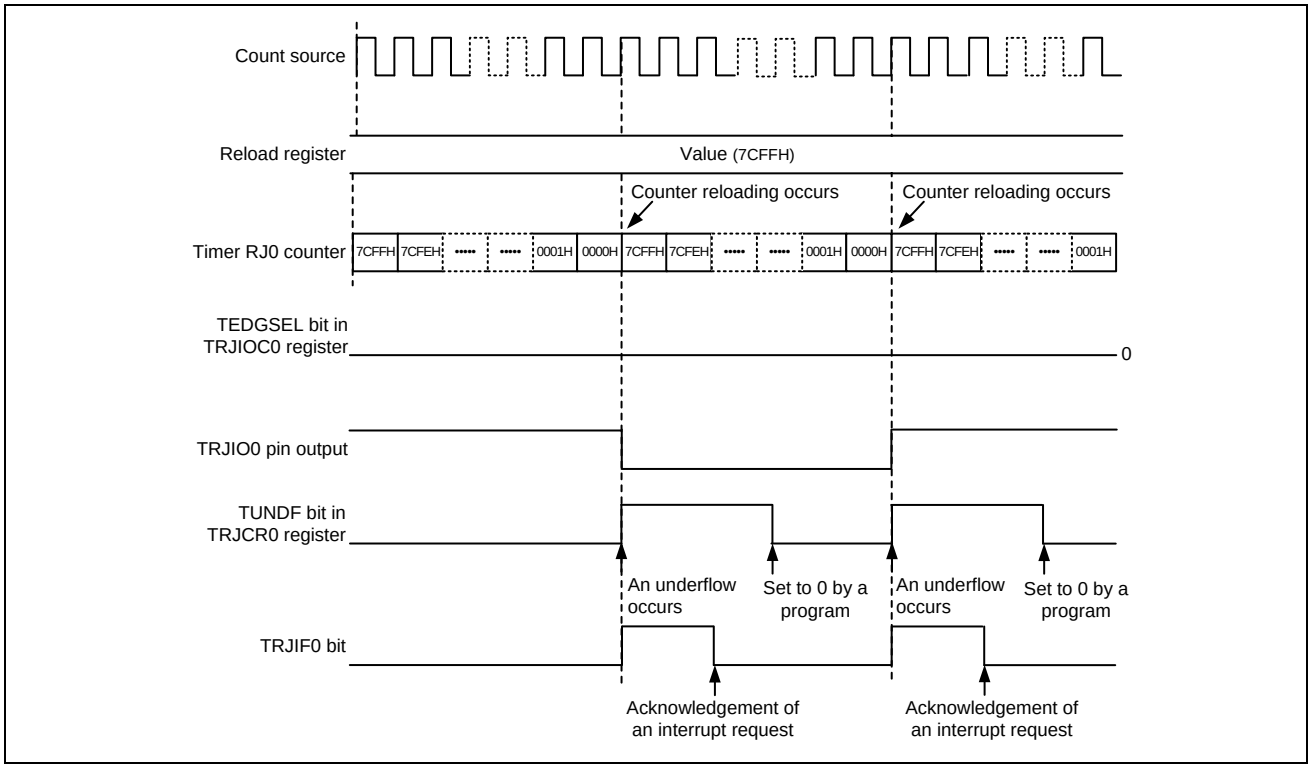

Figure 6.3 Overview of Timer RJ Operation and Interrupts (Pulse Output Mode)

6.4.2 List of Option Byte Setting

Table 6.5 summarizes the settings of the option bytes.

Table 6.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

6.4.3 List of Functions

Table 6.6 lists the functions that are used in this sample program.

Table 6.6 Functions

Function Name	Outline
R_TMR_RJ0_Create()	Initializes timer RJ.
R_TMR_RJ0_Start()	Starts timer RJ operation.

6.4.4 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TMR_RJ0_Create()

Synopsis	Initializes timer RJ
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Create(void)
Explanation	This function initializes timer RJ.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TMR_RJ0_Start()

Synopsis	Starts timer RJ operation
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Start(void)
Explanation	This function starts count operation.
Arguments	None
Return value	None
Remarks	None

6.4.5 Flow Chart

6.4.5.1 Overall Flow

Figure 6.4 shows the overall flow of the sample program described in this chapter.

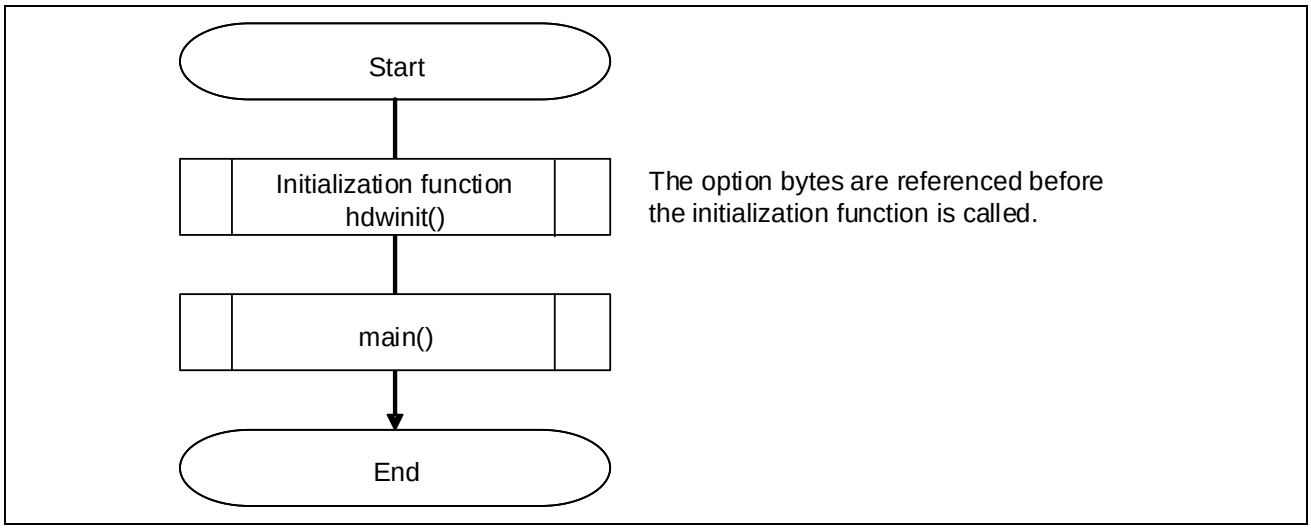

Figure 6.4 Overall Flow

6.4.5.2 Initialization Function

Figure 6.5 shows the flowchart for the initialization function.

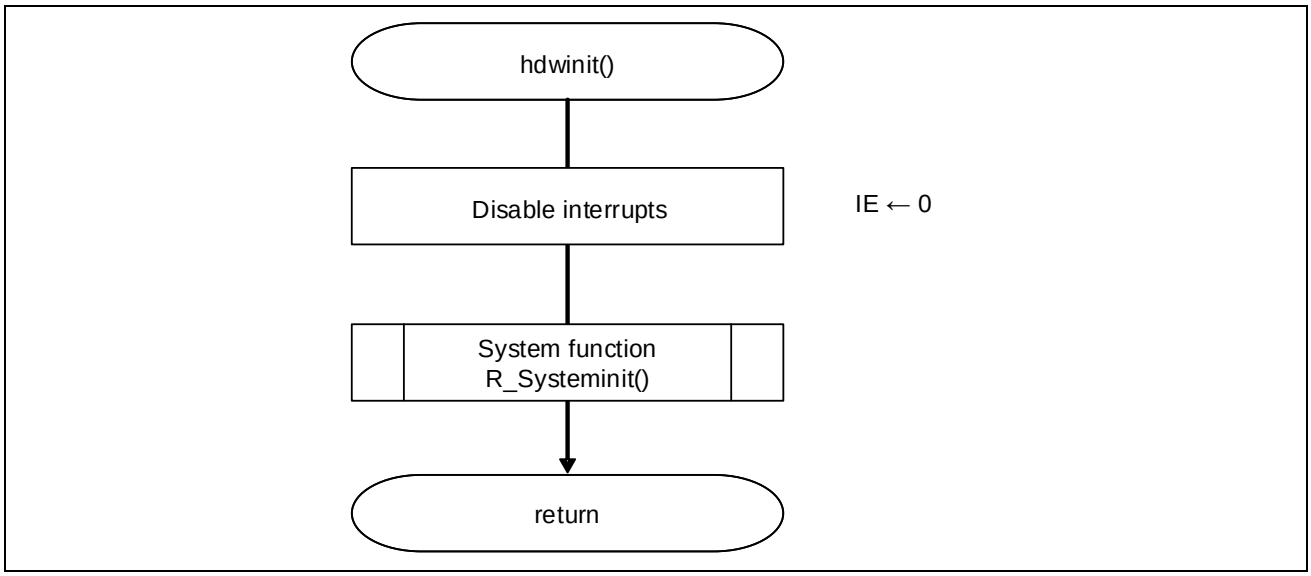

Figure 6.5 Initialization Function

6.4.5.3 System Function

Figure 6.6 shows the flowchart for the system function.

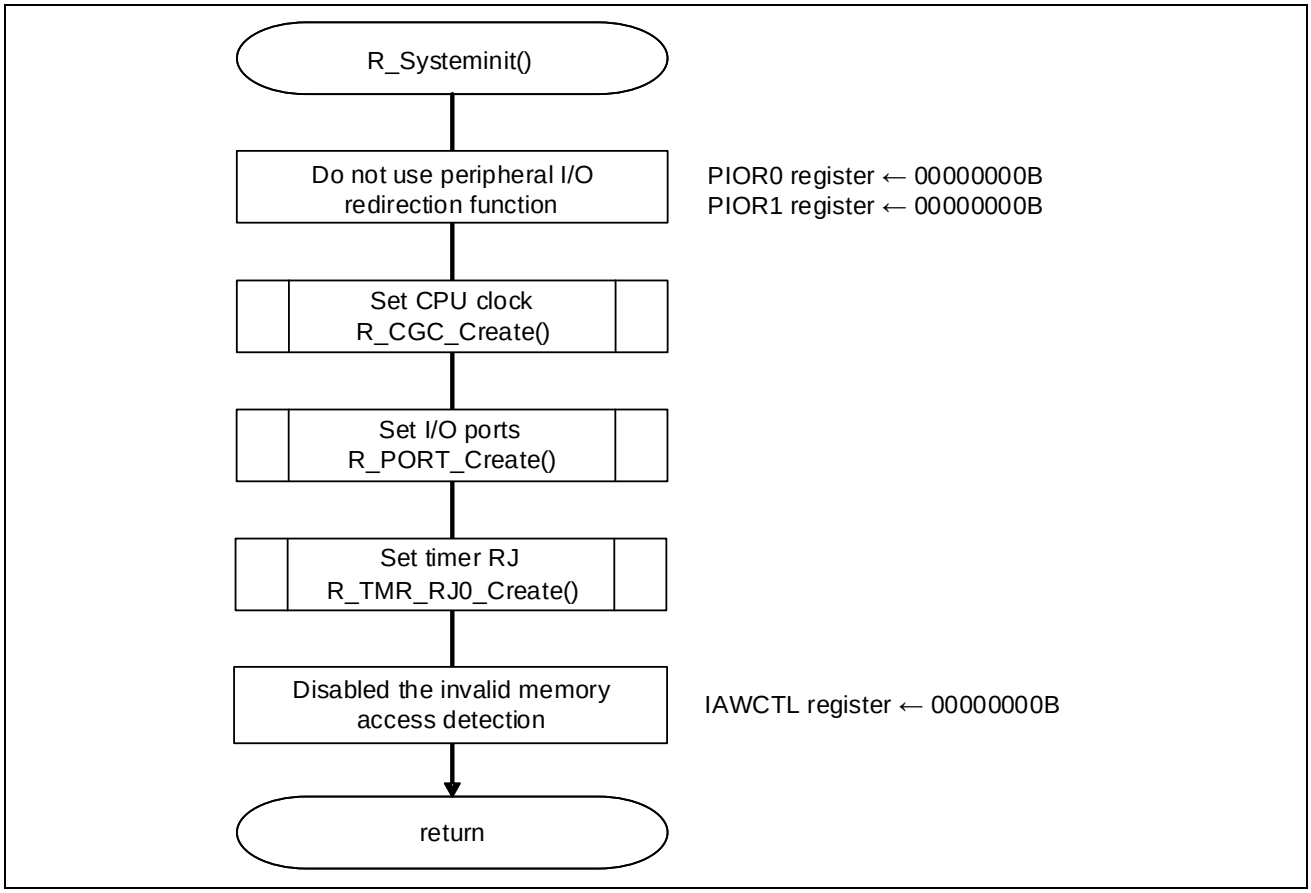

Figure 6.6 System Function

6.4.5.4 CPU Clock Setting

Figure 6.7 shows the flowchart for setting the CPU clock.

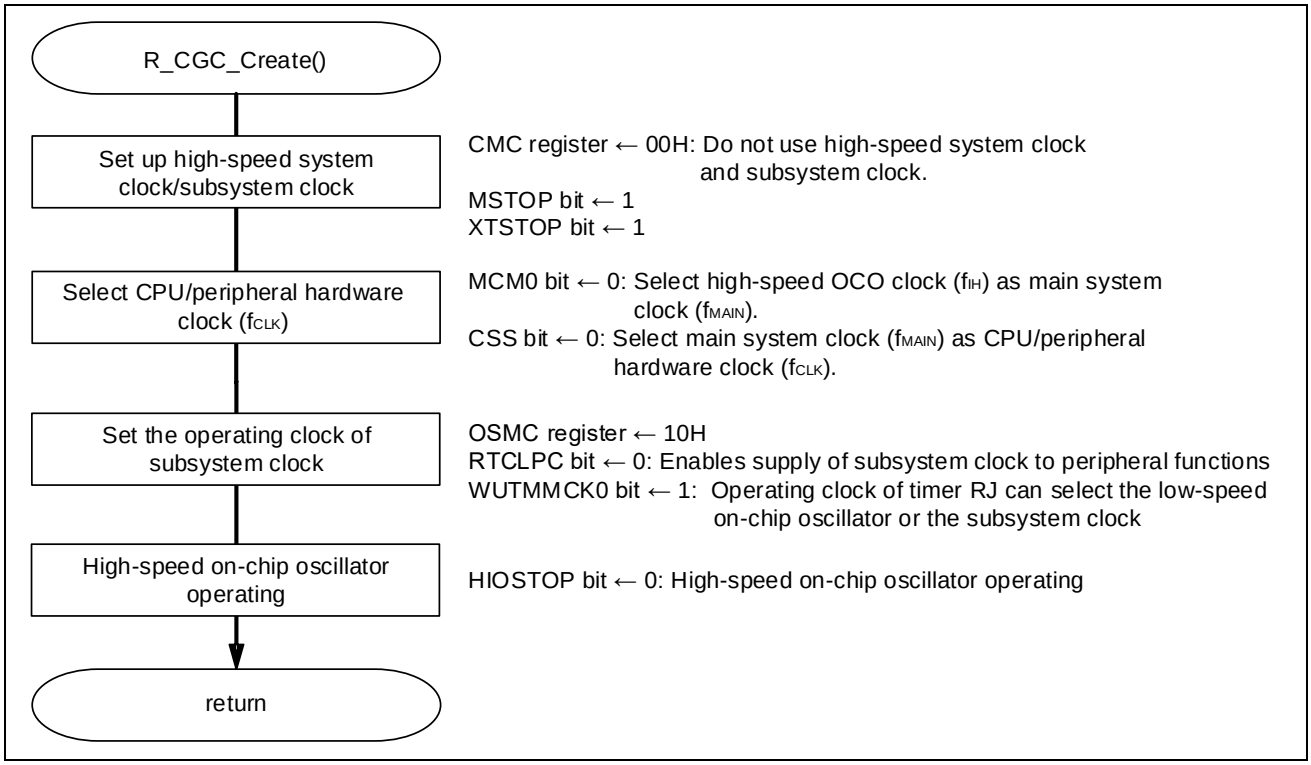

Figure 6.7 CPU Clock Setting

6.4.5.5 I/O Port Setting

Figure 6.8 shows the flowchart for setting the I/O ports.

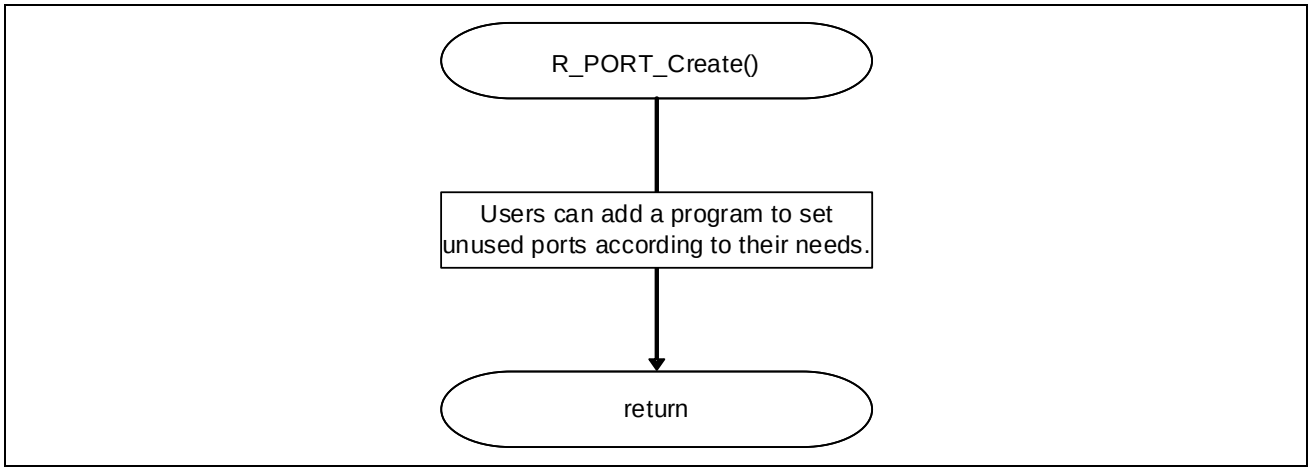

Figure 6.8 I/O Port Setting

Caution: Please provide proper pin treatment and make sure that the electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

6.4.5.6 Timer RJ Setting

Figure 6.9 shows the flowchart for setting timer RJ.

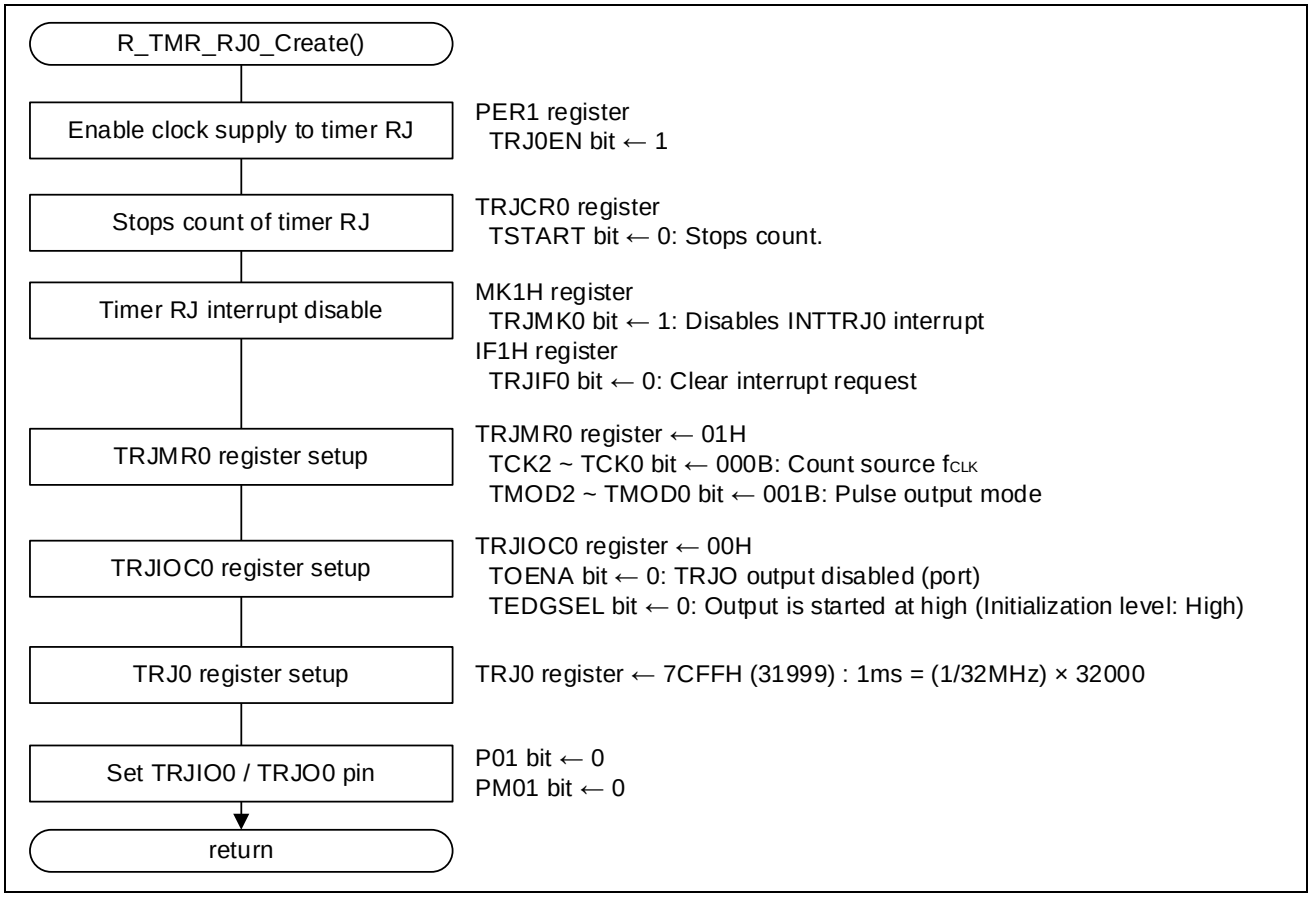

Figure 6.9 Timer RJ Setting

Start supplying clock to Timer RJ
• Peripheral enable register 1 (PER1)
Starts to supply clock to timer RJ.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
x	x	x	x	x	0	0	**1**

Bit 0

TRJ0EN	Control of timer RJ0 input clock supply
0	Stops input clock supply. • SFR used by timer RJ0 cannot be written. • Timer RJ0 is in the reset status.
1	**Enables input clock supply.** **• SFR used by timer RJ0 can be read/written.**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setup of timer RJ operation and interrupt level

• Timer RJ control register 0 (TRJCR0)
Stops Timer RJ counter operation.
Sets the interrupt cycle.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSTF	TSTART
0	0	x	x	0	x	x	0

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	Count starts

Disabling timer RJ interrupt
• Interrupt mask flag register (MK1H)
Disables interrupt processing.
• Interrupt request flag register (IF1H)
Clears the interrupt request flag.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	1	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	0	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the timer RJ operation

• Timer RJ mode register 0 (TRJMR0)
Count source selection and operation mode selection.

Symbol: TRJMR0

7	6	5	4	3	2	1	0
0	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
0	0	0	0	x	0	0	1

Bit 6 to 4

TCK2	TCK1	TCK0	Timer RJ count source select
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/8$
0	1	1	$f_{CLK}/2$
1	0	0	f_{IL}
1	0	1	Event input from ELC
1	1	0	f_{SUB}
Other than above			Setting prohibited

Bit 2 to 0

TMOD2	TMOD1	TMOD0	Timer RJ operating mode select
0	0	0	Timer mode
0	0	1	Pulse output mode
0	1	0	Event counter mode
0	1	1	Pulse width measurement mode
1	0	0	Pulse period measurement mode
Other than above			Setting prohibited

• Timer RJ I/O control register 0 (TRJIOC0)
The input/output of timer RJ setting.

Symbol: TRJIOC0

7	6	5	4	3	2	1	0
TIOGT1	TIOGT0	TIPF1	TIPF0	0	TOENA	0	TEDGSEL
x	x	x	x	0	0	0	0

Bit 2

TOENA	TRJO output enable
0	TRJO output disabled (port)
1	TRJO output enabled

- Pulse output mode

Bit 0

TEDGSEL	TRJIO I/O polarity switch
0	Output is started at high (Initialization level: High)
1	Output is started at low (Initialization level: Low)

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting TRJ0 register
• Timer RJ counter register 0 (TRJ0)
Setup of Timer RJ interrupt cycles.

Symbol: TRJ0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1

Generation of Timer RJ interrupt (INTTRJ0) = (Setup value of TRJ0 + 1) × Count clock period
1 ms = (31999 + 1) × (1/32000000)

Setting TRJIO0 pin
• Port register 0 (P0)
• Port mode register (PM0)
Set TRJIO0 pin as output mode.

Symbol: P0

7	6	5	4	3	2	1	0
0	P06	P05	P04	P03	P02	P01	P00
0	x	x	x	x	x	0	x

Bit 1

P01	Output data control (in output mode)
0	Output 0
1	Output 1

Symbol: PM0

7	6	5	4	3	2	1	0
1	PM06	PM05	PM04	PM03	PM02	PM01	PM00
1	x	x	x	x	x	0	x

Bit 1

PM01	P01 pin I/O mode selection
0	Output mode (the pin functions as an output port (output buffer on))
1	Input mode (the pin functions as an input port (output buffer off))

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

6.4.5.7 Main Processing

Figure 6.10 shows the flowchart for main processing.

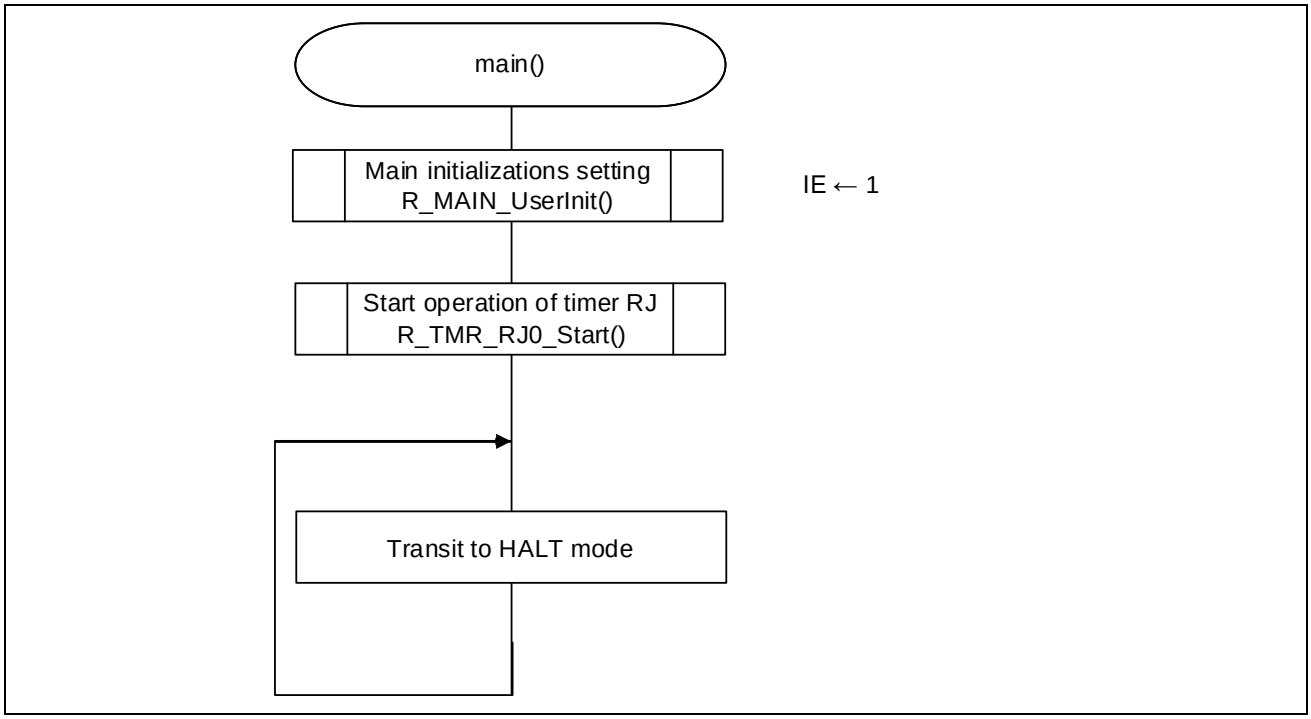

Figure 6.10 Main Processing

6.4.5.8 Timer RJ Operation Start

Figure 6.11 shows the flowchart for starting timer RJ operation.

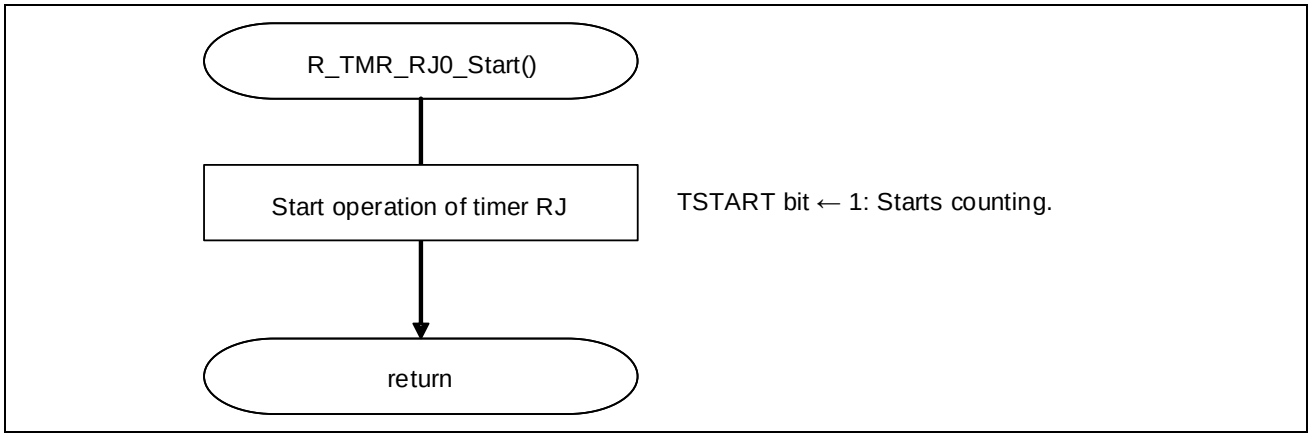

Figure 6.11 Timer RJ Operation Start

Starting timer RJ counter operation

• Timer RJ control register 0 (TRJCR0)
Starts timer RJ counter operation.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	**0**	**TUNDF**	**TEDGF**	**0**	**TSTOP**	**TCSTF**	**TSTART**
0	0	x	x	0	x	x	**1**

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	**Count starts**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

7. Example of Migration from Event Counter Mode

7.1 Specifications

The same operation as that in event counter mode in timer RA of R8C/36M can be realized by using timer RJ of RL78/G14.
In event counter mode, the counter is decremented by an external event signal (count source) input to the TRJIO0 pin. Various periods for counting events can be set by bits TIOGT0 and TIOGT1 in the TRJIOC0 register and the TRJISR0 register. In addition, the filter function for the TRJIO0 input can be specified by bits TIPF0 and TIPF1 in the TRJIOC0 register.
Also, the output from the TRJO0 pin can be toggled even in event counter mode.

Table 7.1 lists the peripheral functions to be used and their uses (example of migration from event counter mode), and Figure 7.1 shows the operation overview (example of migration from event counter mode).

Table 7.1 Peripheral Functions to be Used and Their Uses

(Example of Migration from Event Counter Mode)

Peripheral Function	Use
Timer RJ (event counter mode)	The external event is counted.

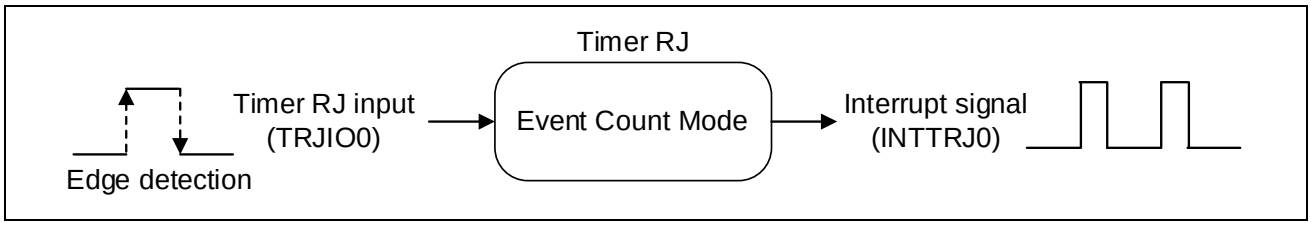

Figure 7.1 Operation Overview (Example of Migration from Event Counter Mode)

7.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

Table 7.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (VLVD): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V6.0.0 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

7.3 Description of Hardware

7.3.1 Hardware Configuration Example

Figure 7.2 shows an example of hardware configuration that is used for this chapter.

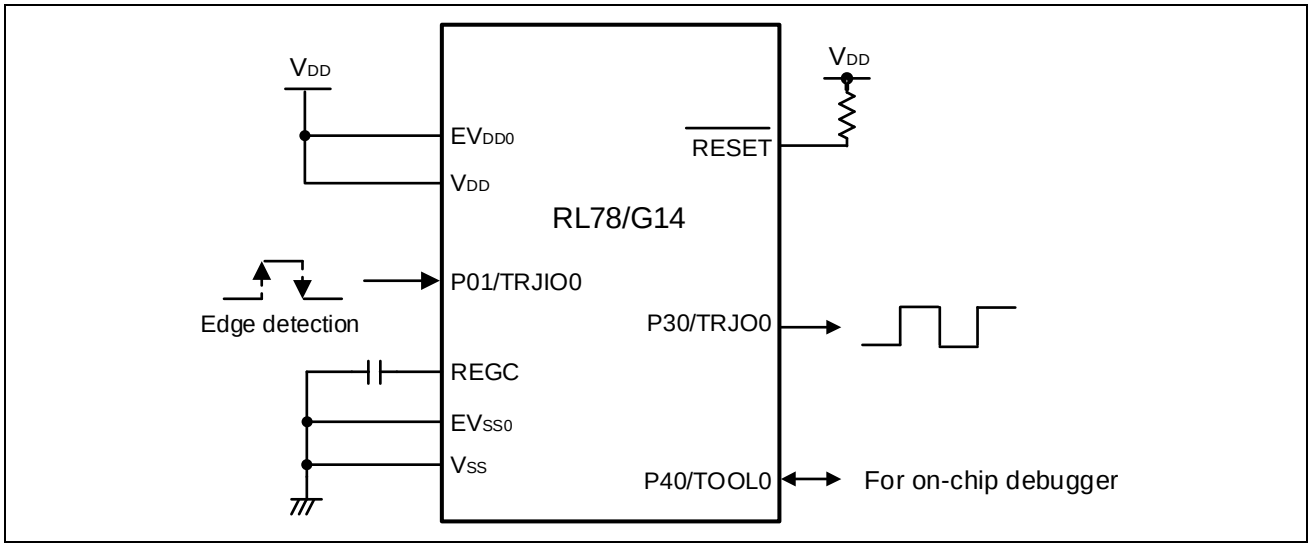

Figure 7.2 Hardware Configuration (Event Counter Mode)

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

7.3.2 List of Pins to be Used

Table 7.3 lists the pins to be used and their functions.

Table 7.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P01/TRJIO0	Input	An external event signal (count source) is inputted.
P30/TRJO0	Output	The output level is inverted each time an underflow occurs.

7.4 Description of Software

7.4.1 Operation Outline

This chapter describes how to set up the event count mode of timer RJ.
This setup is followed by operation for an external event signal (count source) input to the TRJIO0 pin. And the output from the TRJO0 pin can be toggled.

Table 7.4 lists the peripheral functions to be used and their uses. Figure 7.3 shows the event counter mode and its interrupt operation.

(1) Initialize the timer RJ.
<Conditions for setting>
Use the event counter mode as the timer RJ operation mode.
TRJIO0 edge polarity select rising edge, and event is always counted.
TRJIO0 input filter select: filter sampled at f_{CLK}.
Use TRJO0 output the toggle level.

(2) Sets "1" (starts counter operation) to TSTART bit of TRJCR0 register to start the count of timer RJ.

(3) Execute a HALT instruction to wait for the external event signal.

(4) The external event signal input to TRJIO0 pin is counted, inverts the output level from TRJO0 pin each time an underflow occurs.

Table 7.4 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Timer RJ	The external event signal input to TRJIO0 pin is counted, inverts the output level from TRJO0 pin each time an underflow occurs.

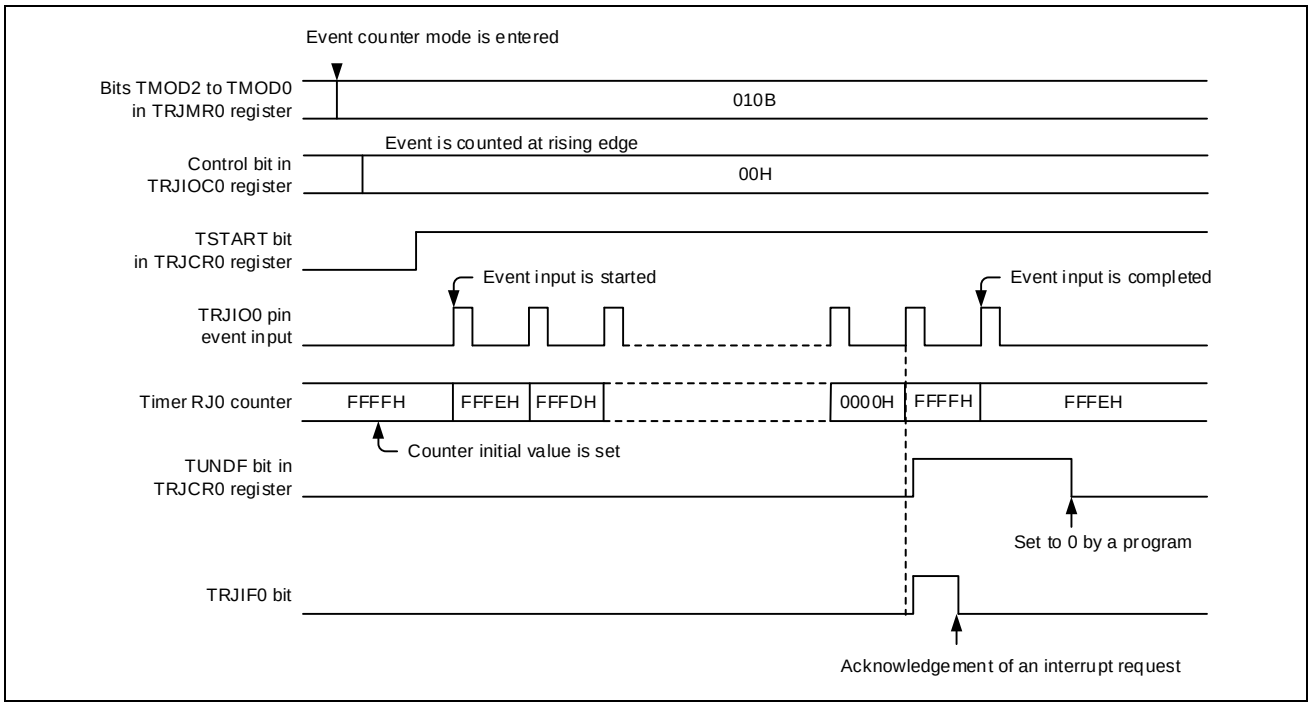

Figure 7.3 Overview of Timer RJ Operation and Interrupts (Event Counter Mode)

7.4.2 List of Option Byte Setting

Table 7.5 summarizes the settings of the option bytes.

Table 7.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

7.4.3 List of Functions

Table 7.6 lists the functions that are used in this sample program.

Table 7.6 Functions

Function Name	Outline
R_TMR_RJ0_Create()	Initializes timer RJ.
R_TMR_RJ0_Start()	Starts timer RJ operation.

7.4.4 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TMR_RJ0_Create()

Synopsis	Initializes timer RJ
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Create(void)
Explanation	This function initializes timer RJ.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TMR_RJ0_Start()

Synopsis	Starts timer RJ operation
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Start(void)
Explanation	This function starts count operation of timer RJ.
Arguments	None
Return value	None
Remarks	None

7.4.5 Flow Chart

7.4.5.1 Overall Flow

Figure 7.4 shows the overall flow of the sample program described in this chapter.

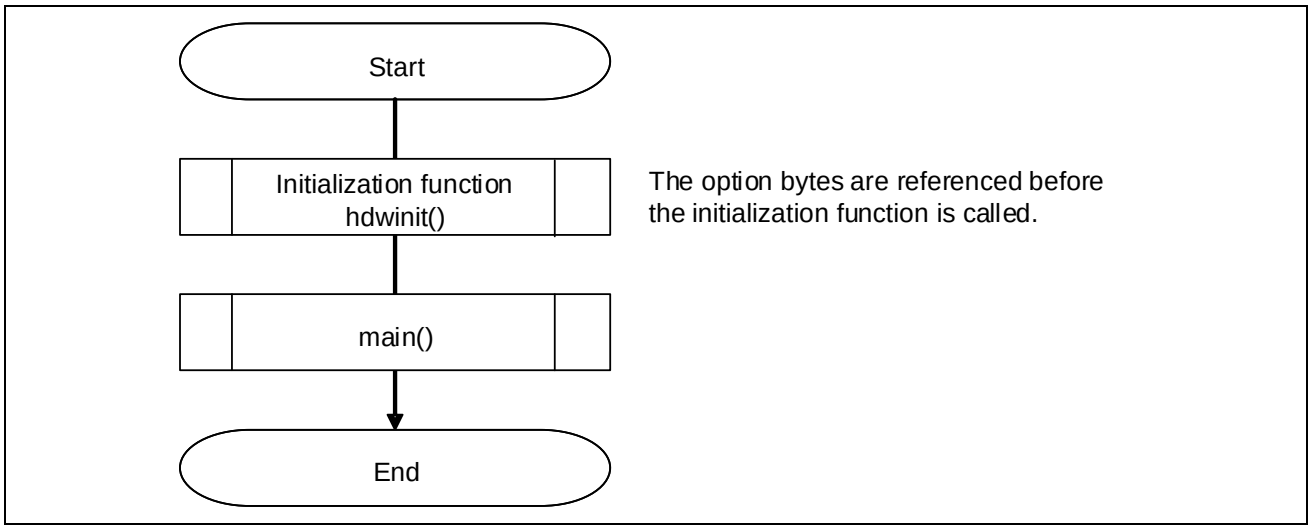

Figure 7.4 Overall Flow

7.4.5.2 Initialization Function

Figure 7.5 shows the flowchart for the initialization function.

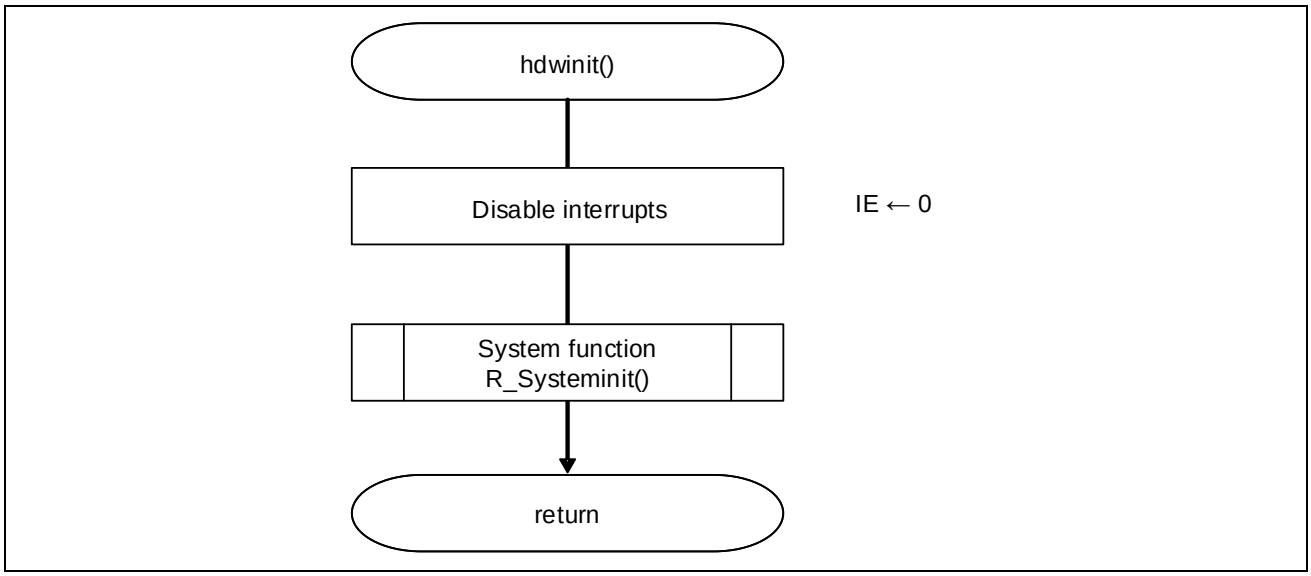

Figure 7.5 Initialization Function

7.4.5.3 System Function

Figure 7.6 shows the flowchart for the system function.

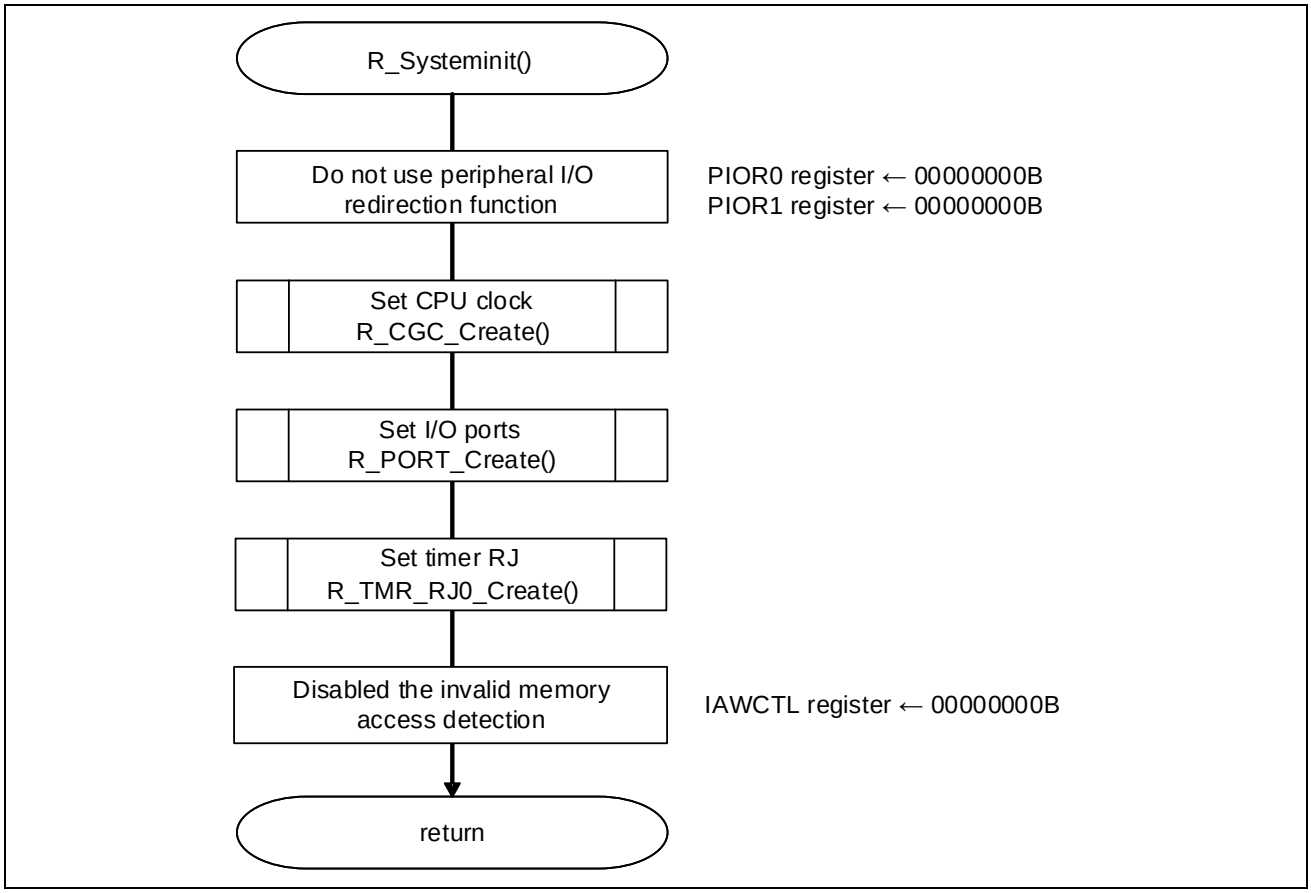

Figure 7.6 System Function

7.4.5.4 CPU Clock Setting

Figure 7.7 shows the flowchart for setting the CPU clock.

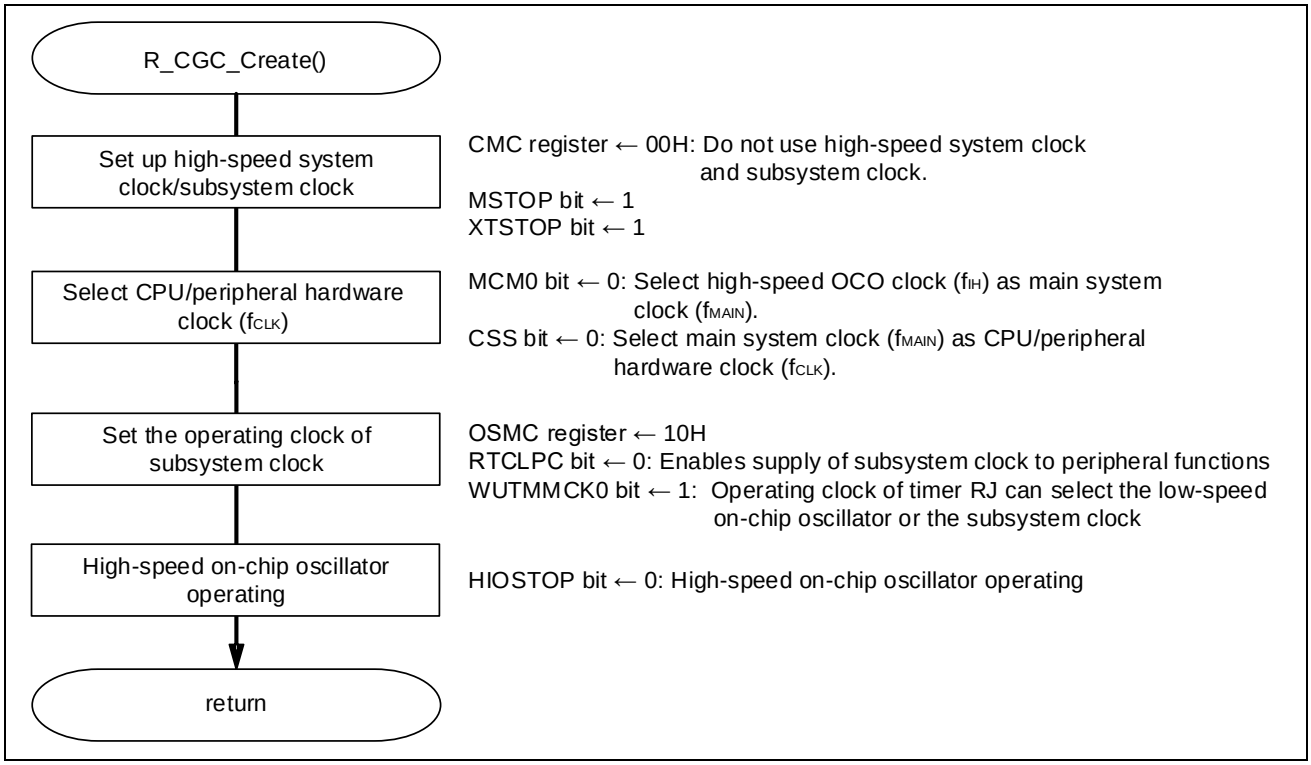

Figure 7.7 CPU Clock Setting

7.4.5.5 I/O Port Setting

Figure 7.8 shows the flowchart for setting the I/O ports.

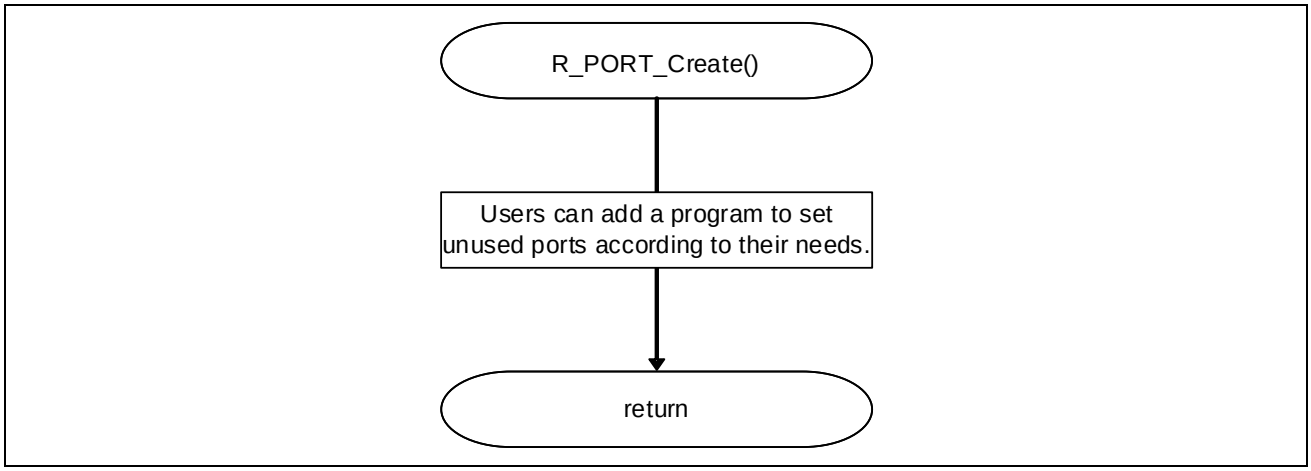

Figure 7.8 I/O Port Setting

Caution: Please provide proper pin treatment and make sure that the electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

7.4.5.6 Timer RJ Setting

Figure 7.9 shows the flowchart for setting timer RJ.

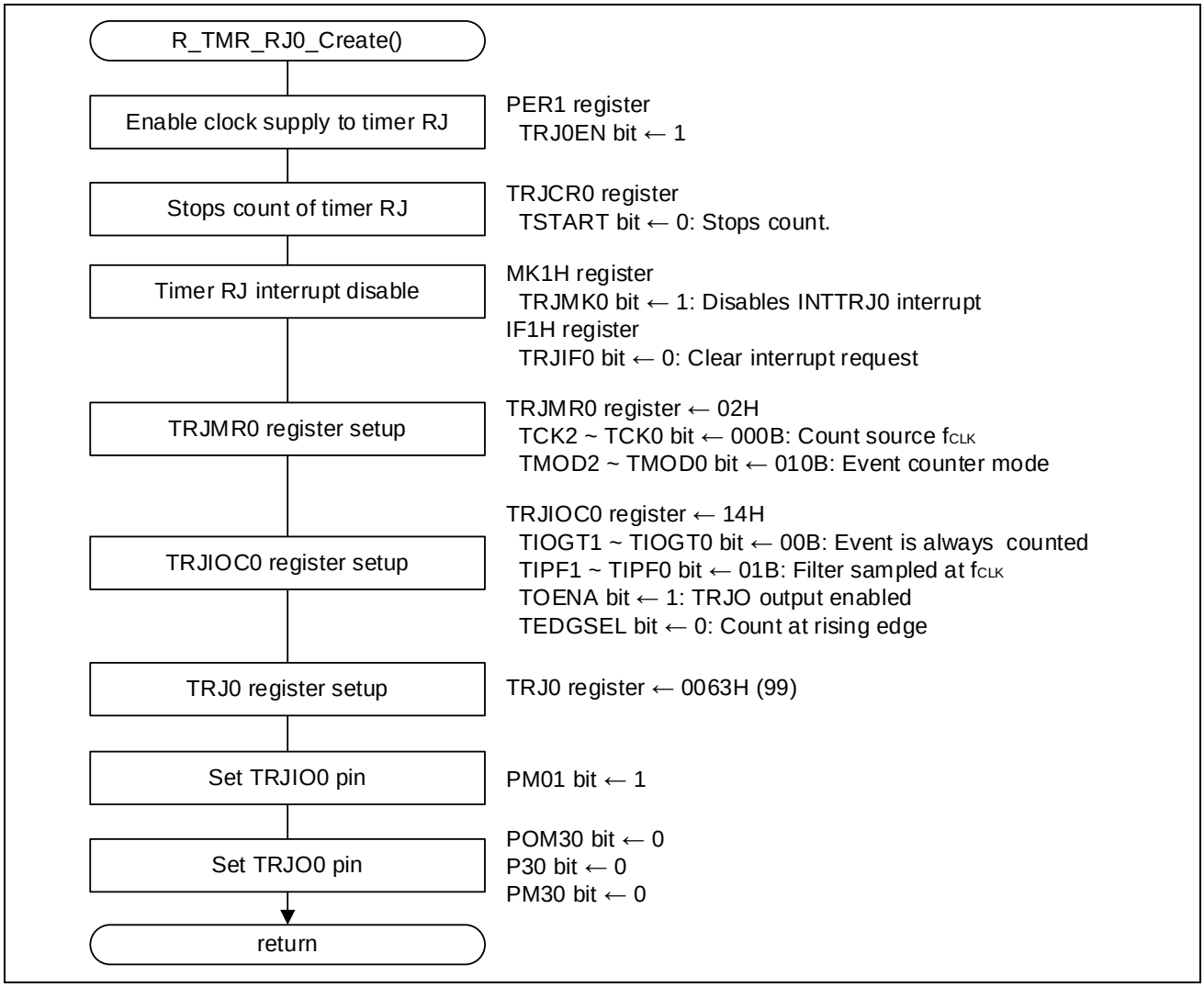

Figure 7.9 Timer RJ Setting

Start supplying clock to Timer RJ
• Peripheral enable register 1 (PER1)
Starts to supply clock to timer RJ.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
x	x	x	x	x	0	0	**1**

Bit 0

TRJ0EN	Control of timer RJ0 input clock supply
0	Stops input clock supply. • SFR used by timer RJ0 cannot be written. • Timer RJ0 is in the reset status.
1	**Enables input clock supply.** **• SFR used by timer RJ0 can be read/written.**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setup of timer RJ operation and interrupt level

• Timer RJ control register 0 (TRJCR0)
Stops Timer RJ counter operation.
Sets the interrupt cycle.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSTF	TSTART
0	0	x	x	0	x	x	0

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	Count starts

Disabling timer RJ interrupt
• Interrupt mask flag register (MK1H)
Disables interrupt processing.
• Interrupt request flag register (IF1H)
Clears the interrupt request flag.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	1	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	0	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the timer RJ operation

• Timer RJ mode register 0 (TRJMR0)
Count source selection and operation mode selection.

Symbol: TRJMR0

7	6	5	4	3	2	1	0
0	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
0	0	0	0	x	0	1	0

Bit 6 to 4

TCK2	TCK1	TCK0	Timer RJ count source select
0	**0**	**0**	**f_{CLK}**
0	0	1	$f_{CLK}/8$
0	1	1	$f_{CLK}/2$
1	0	0	f_{IL}
1	0	1	Event input from ELC
1	1	0	f_{SUB}
Other than above			Setting prohibited

Bit 2 to 0

TMOD2	TMOD1	TMOD0	Timer RJ operating mode select
0	0	0	Timer mode
0	0	1	Pulse output mode
0	**1**	**0**	**Event counter mode**
0	1	1	Pulse width measurement mode
1	0	0	Pulse period measurement mode
Other than above			Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

• Timer RJ I/O control register 0 (TRJIOC0)
The input/output of timer RJ setting.

Symbol: TRJIOC0

7	6	5	4	3	2	1	0
TIOGT1	TIOGT0	TIPF1	TIPF0	0	TOENA	0	TEDGSEL
0	0	0	1	0	1	0	0

Bit 7 to 6

TIOGT1	TIOGT0	TRJIO count control
0	**0**	**Event is always counted**
0	1	Event is counted during polarity period specified for INTP4
1	0	Event is counted during polarity period specified for timer output signal
Other than above		Setting prohibited

Bit 5 to 4

TIPF1	TIPF0	TRJIO input filter select
0	0	No filter
0	**1**	**Filter sampled at f_{CLK}**
1	0	Filter sampled at $f_{CLK}/8$
1	1	Filter sampled at $f_{CLK}/32$

Bit 2

TOENA	TRJO output enable
0	TRJO output disabled (port)
1	**TRJO output enabled**

- Event counter mode

Bit 0

TEDGSEL	TRJIO I/O polarity switch
0	**Count at rising edge**
1	Count at falling edge

Setting TRJ0 register

• Timer RJ counter register 0 (TRJ0)
Setup the initial value of TRJ0 register.

Symbol: TRJ0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting TRJIO0 pin
• Port mode register (PM0)
Set TRJIO0 pin as input mode.

Symbol: PM0

7	6	5	4	3	2	1	0
1	**PM06**	**PM05**	**PM04**	**PM03**	**PM02**	**PM01**	**PM00**
1	x	x	x	x	x	**1**	x

Bit 1

PM01	P01 pin I/O mode selection
0	Output mode (the pin functions as an output port (output buffer on))
1	**Input mode (the pin functions as an input port (output buffer off))**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting TRJO0 pin
- Port output mode register 3 (POM3)
- Port register 3 (P3)
- Port mode register (PM3)

Set TRJO0 pin as output mode.

Symbol: POM3

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	POM30
0	0	0	0	0	0	0	0

Bit 0

POM30	P30 pin output mode selection
0	Normal output mode
1	N-ch open-drain output (EV_{DD} tolerance) mode

Symbol: P3

7	6	5	4	3	2	1	0
0	0	0	0	0	0	P31	P30
0	0	0	0	0	0	x	0

Bit 0

P30	Output data control (in output mode)
0	Output 0
1	Output 1

Symbol: PM3

7	6	5	4	3	2	1	0
1	1	1	1	1	1	PM31	PM30
1	1	1	1	1	1	x	0

Bit 0

PM30	P30 pin I/O mode selection
0	Output mode (the pin functions as an output port (output buffer on))
1	Input mode (the pin functions as an input port (output buffer off))

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

7.4.5.7 Main Processing

Figure 7.10 shows the flowchart for main processing.

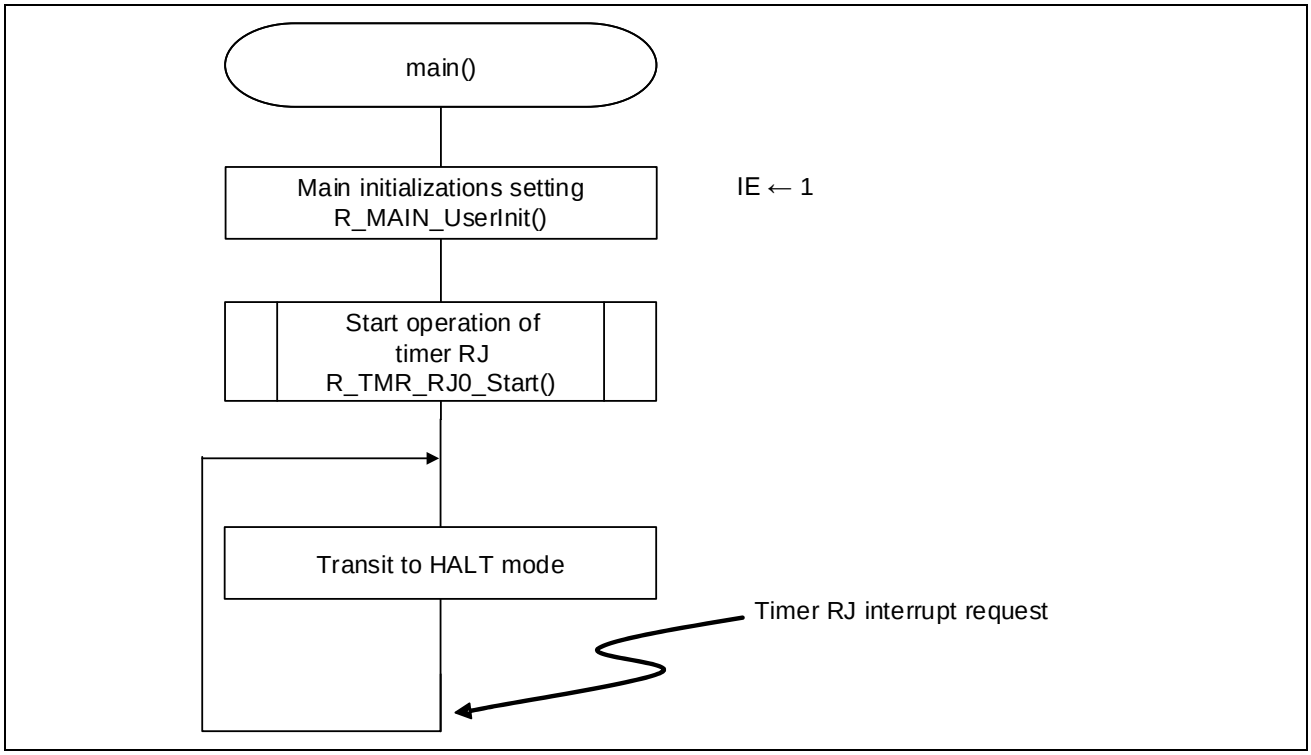

Figure 7.10 Main Processing

7.4.5.8 Timer RJ Operation Start

Figure 7.11 shows the flowchart for starting timer RJ operation.

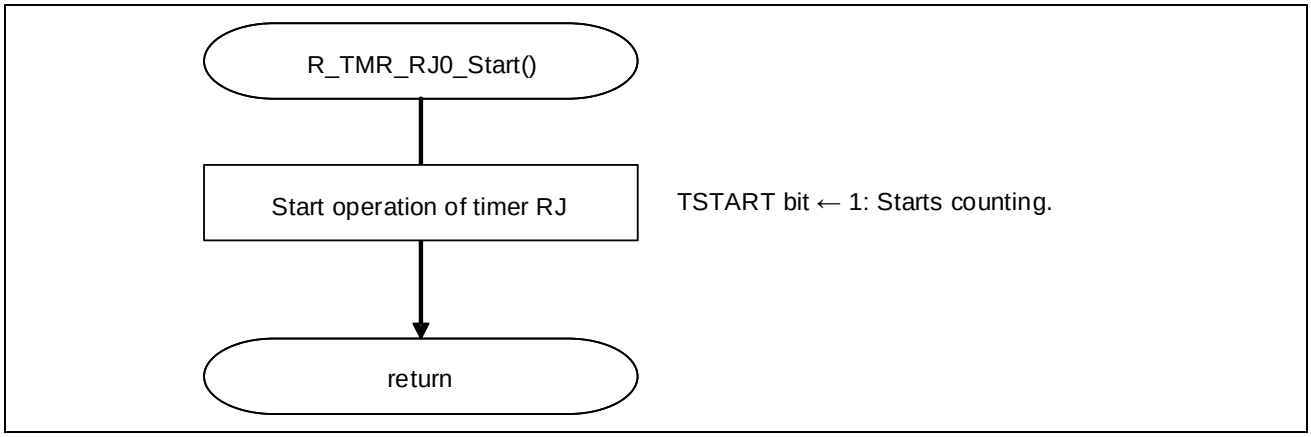

Figure 7.11 Timer RJ Operation Start

Starting timer RJ counter operation

• Timer RJ control register 0 (TRJCR0)
Starts timer RJ counter operation.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	**0**	**TUNDF**	**TEDGF**	**0**	**TSTOP**	**TCSTF**	**TSTART**
0	0	x	x	0	x	x	**1**

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	**Count starts**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

8. Example of Migration from Pulse Width Measurement Mode

8.1 Specifications

The same operation as that in pulse width measurement mode in timer RA of R8C/36M can be realized by using timer RJ of RL78/G14.
In pulse width measurement mode, the pulse width of an external signal input to the TRJIO0 pin is measured.
When the level specified by the TEDGSEL bit in the TRJIOC0 register is input to the TRJIO0 pin, the decrement is started with the selected count source. When the specified level on the TRJIO0 pin ends, the counter is stopped, the TEDGF bit in the TRJCR0 register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDF bit in the TRJCR0 register is set to 1 (underflow) and an interrupt request is generated.

Table 8.1 lists the peripheral functions to be used and their uses (example of migration from pulse width measurement mode), and Figure 8.1 shows the operation overview (example of migration from pulse width measurement mode).

Table 8.1 Peripheral Functions to be Used and Their Uses

(Example of Migration from Pulse Width Measurement Mode)

Peripheral Function	Use
Timer RJ (pulse width measurement mode)	Measure the pulse width of an external signal.

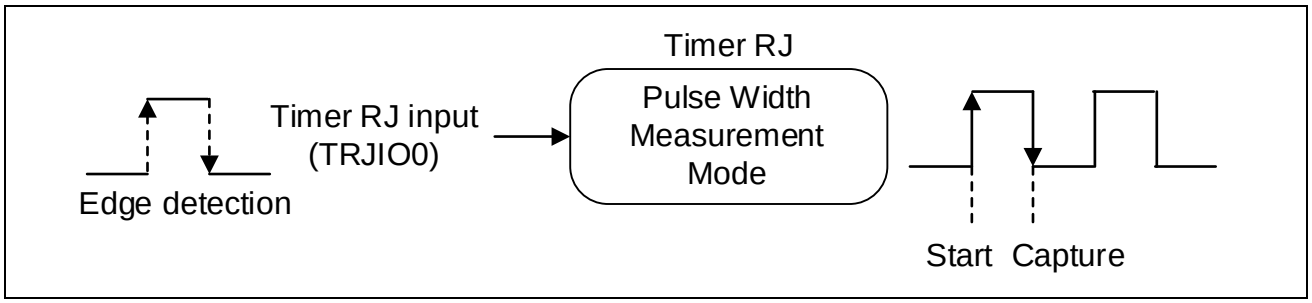

Figure 8.1 Operation Overview (Example of Migration from Pulse Width Measurement Mode)

8.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

Table 8.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (VLVD): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V6.0.0 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

8.3 Description of Hardware

8.3.1 Hardware Configuration Example

Figure 8.2 shows an example of hardware configuration that is used for this chapter.

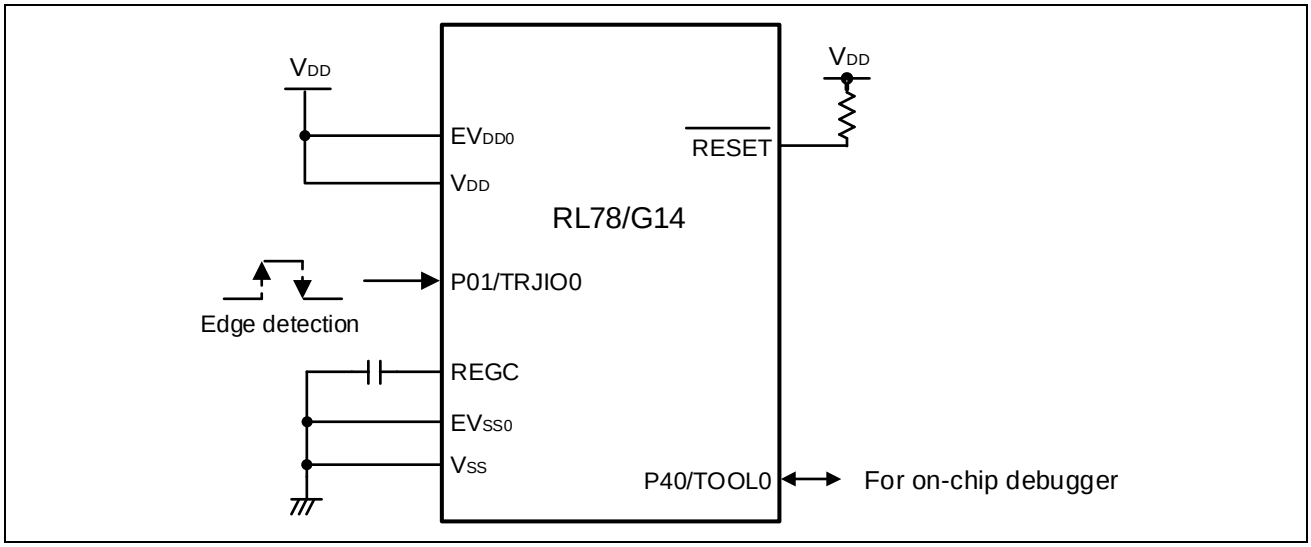

Figure 8.2 Hardware Configuration (Pulse Width Measurement Mode)

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

8.3.2 List of Pins to be Used

Table 8.3 lists the pins to be used and their functions.

Table 8.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P01/TRJIO0	Input	Measure the pulse width.

8.4 Description of Software

8.4.1 Operation Outline

This chapter describes how to set up the pulse width measurement mode of timer RJ.
Each time a valid edge (high-level input ends) is detected on the timer RJ input pin (TRJIO0), the sample code described in this chapter captures the count value of the timer and measures the high-level width of the pulse which arrives at the timer RJ input pin (TRJIO0). When a timer interrupt (INTTRJ0) occurs upon completion of the capture, the sample code calculates the pulse width and stores the calculation result in the on-chip RAM.

Table 8.4 lists the peripheral functions to be used and their uses. Figure 8.3 shows the pulse width measurement mode and its interrupt operation.

(1) Initialize the timer RJ.
<Conditions for setting>
Use the pulse width measurement mode as the timer RJ operation mode.
Select f_{CLK} as the count source of timer RJ.
Initialize timer RJ counter register 0 (TRJ0), and measure "H" width of the pulse input to TRJIO0 pin.
Use timer interrupts (INTTRJ0) from timer RJ.

(2) Sets "1" (starts counter operation) to TSTART bit of TRJCR0 register to start the count of timer RJ.

(3) Execute a HALT instruction to wait for timer interrupts (INTTRJ0).

(4) When the interrupt request is generated, calculates the pulse width and stores the calculation result in the on-chip RAM.

(5) The sample code returns to step (3) to execute HALT instruction and waits for the next timer interrupt (INTTRJ0) from timer RJ.

Table 8.4 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Timer RJ	Measure the pulse width of TRJIO0 pin.

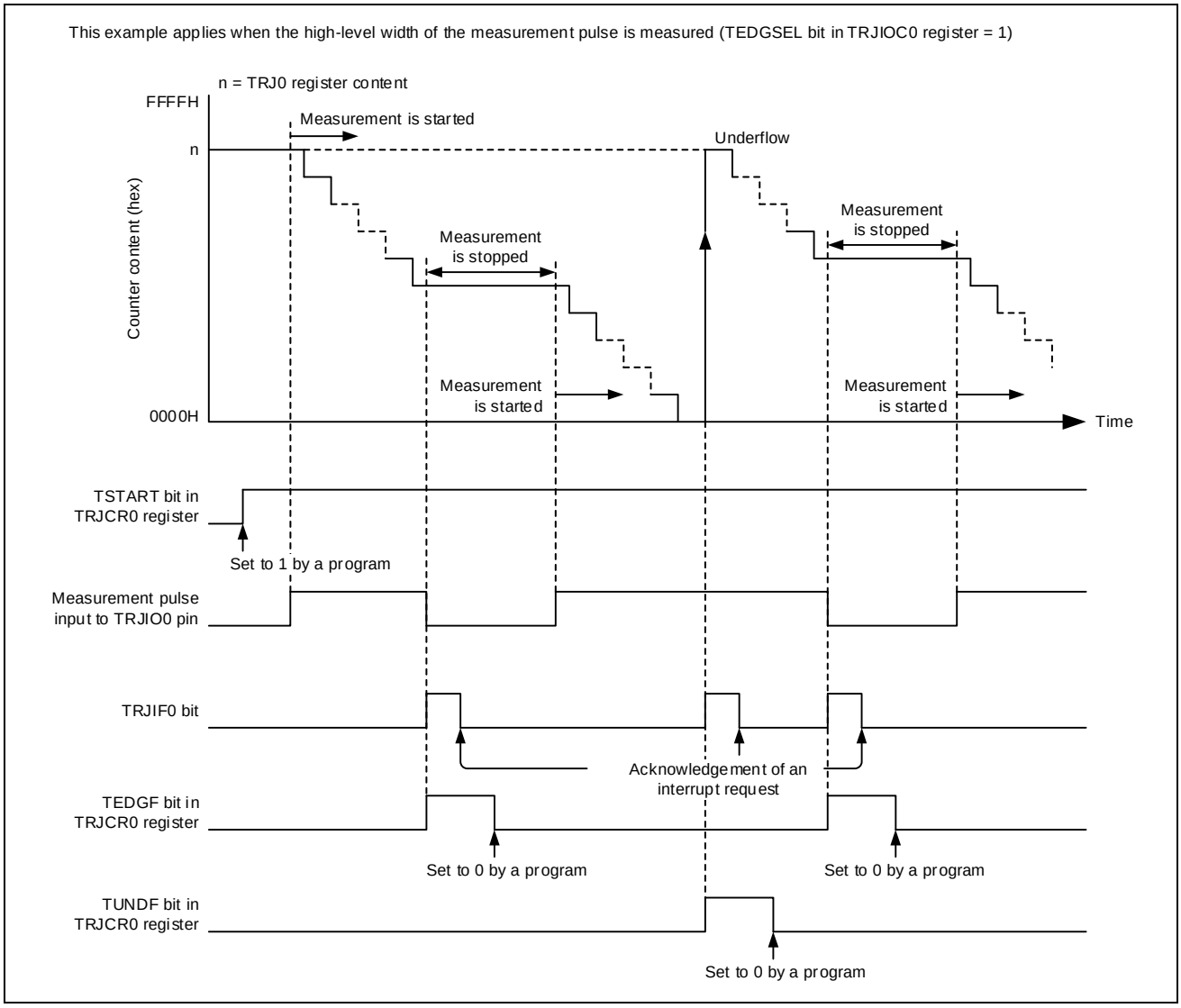

Figure 8.3 Overview of Timer RJ Operation and Interrupts (Pulse Width Measurement Mode)

8.4.2 List of Option Byte Setting

Table 8.5 summarizes the settings of the option bytes.

Table 8.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

8.4.3 List of Functions

Table 8.6 lists the functions that are used in this sample program.

Table 8.6 Functions

Function Name	Outline
R_TMR_RJ0_Create()	Initializes timer RJ.
R_TMR_RJ0_Start()	Starts timer RJ operation.
r_tmr_rj0_interrupt()	Processes timer interrupts on timer RJ.

8.4.4 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TMR_RJ0_Create()

Synopsis	Initializes timer RJ
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Create(void)
Explanation	This function initializes timer RJ.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TMR_RJ0_Start()

Synopsis	Starts timer RJ operation
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Start(void)
Explanation	This function enables timer RJ interrupts and prepares to measure the pulse width.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tmr_rj0_interrupt()

Synopsis	Timer RJ interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	static void __near r_tmr_rj0_interrupt(void)
Explanation	This function calculates the pulse width and stores the calculation result in the on-chip RAM.
Arguments	None
Return value	None
Remarks	None

8.4.5 Flow Chart

8.4.5.1 Overall Flow

Figure 8.4 shows the overall flow of the sample program described in this chapter.

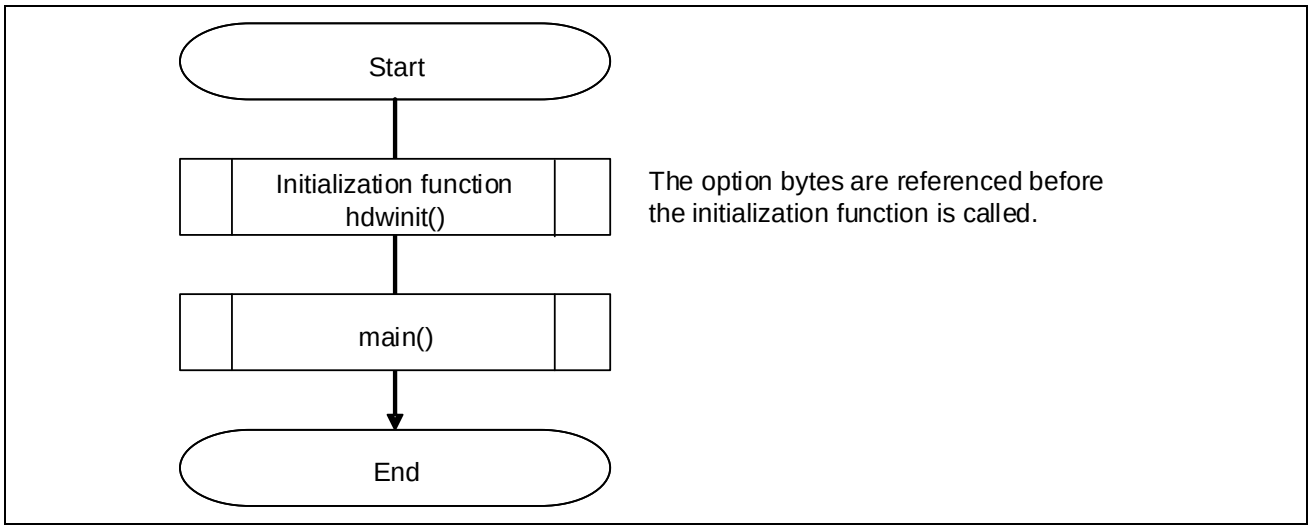

Figure 8.4 Overall Flow

8.4.5.2 Initialization Function

Figure 8.5 shows the flowchart for the initialization function.

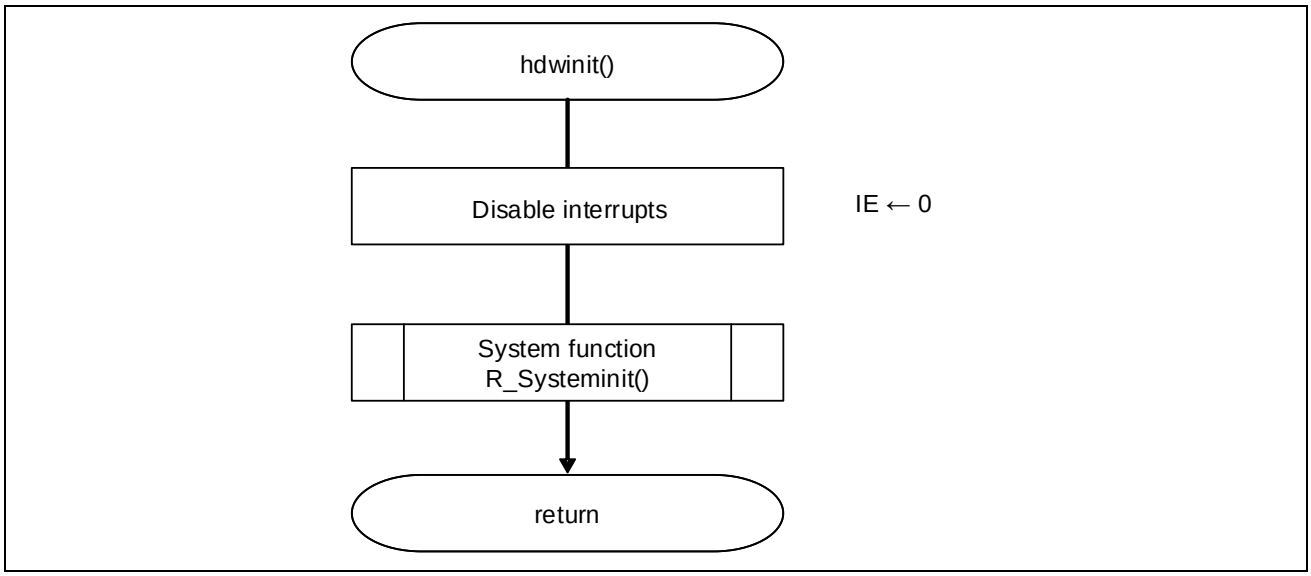

Figure 8.5 Initialization Function

8.4.5.3 System Function

Figure 8.6 shows the flowchart for the system function.

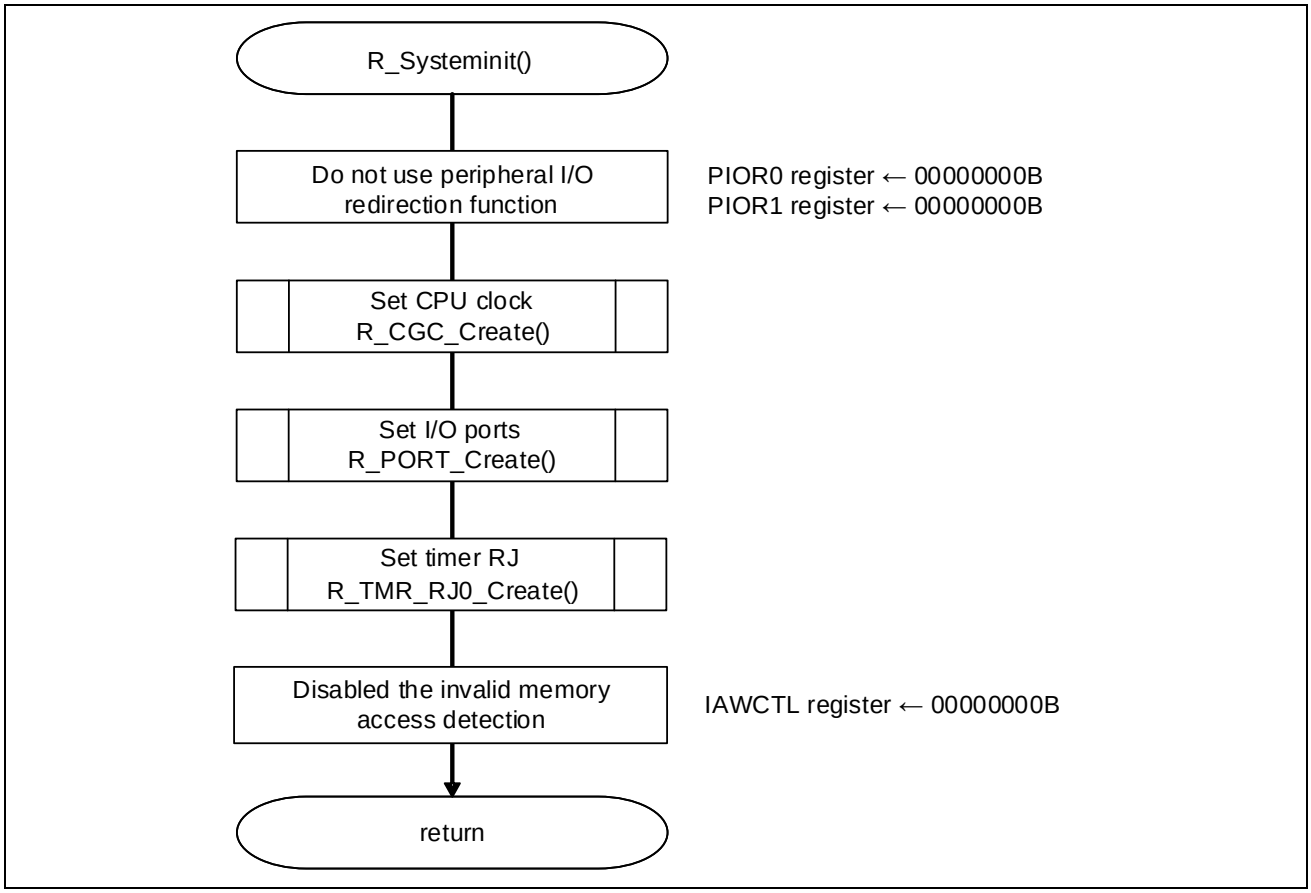

Figure 8.6 System Function

8.4.5.4 CPU Clock Setting

Figure 8.7 shows the flowchart for setting the CPU clock.

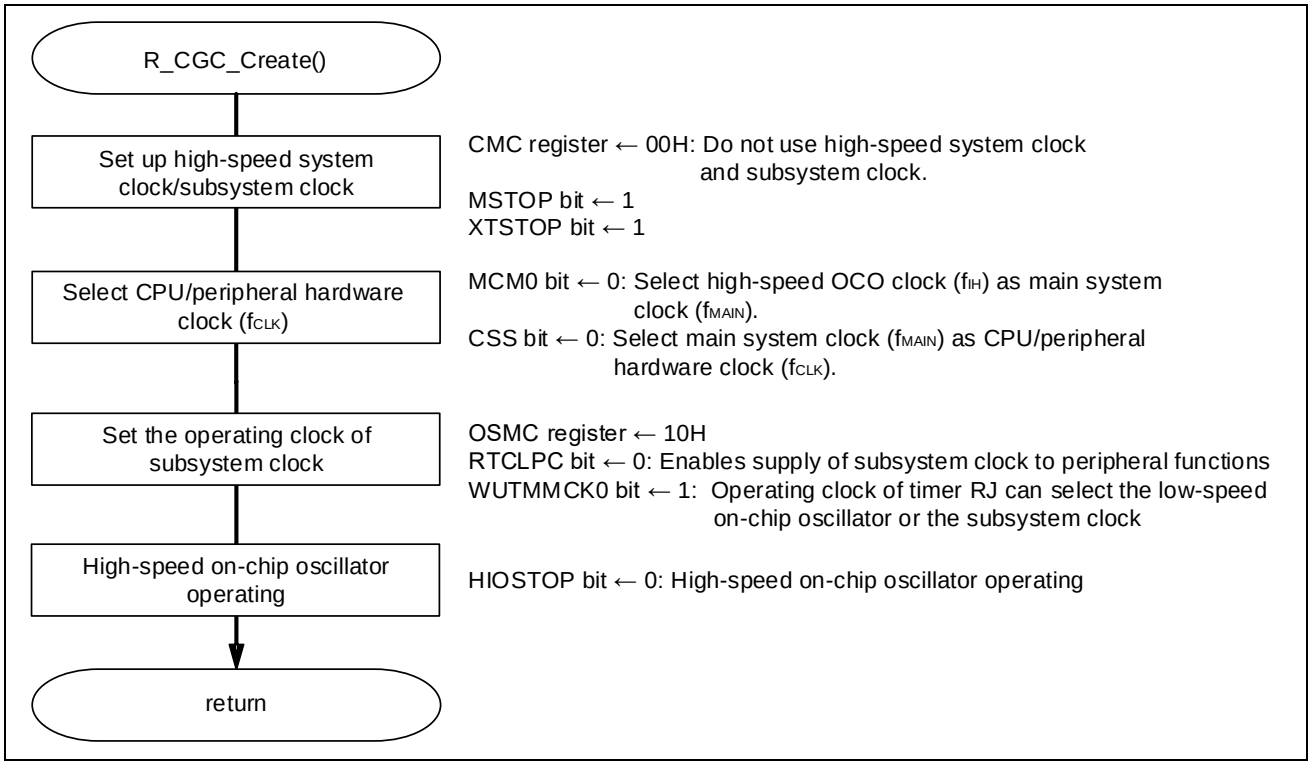

Figure 8.7 CPU Clock Setting

8.4.5.5 I/O Port Setting

Figure 8.8 shows the flowchart for setting the I/O ports.

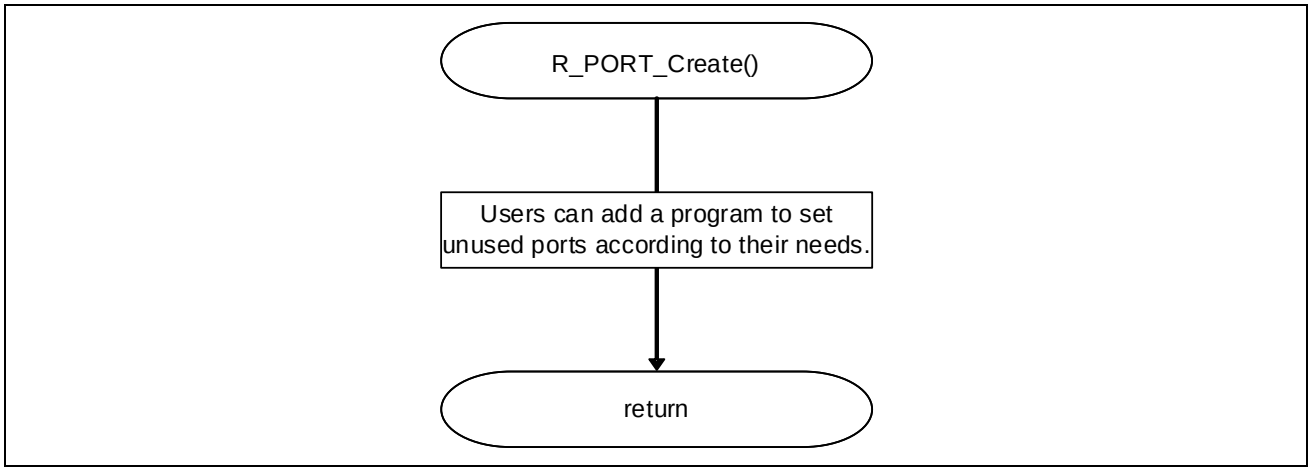

Figure 8.8 I/O Port Setting

Caution: Please provide proper pin treatment and make sure that the electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

8.4.5.6 Timer RJ Setting

Figure 8.9 shows the flowchart for setting timer RJ.

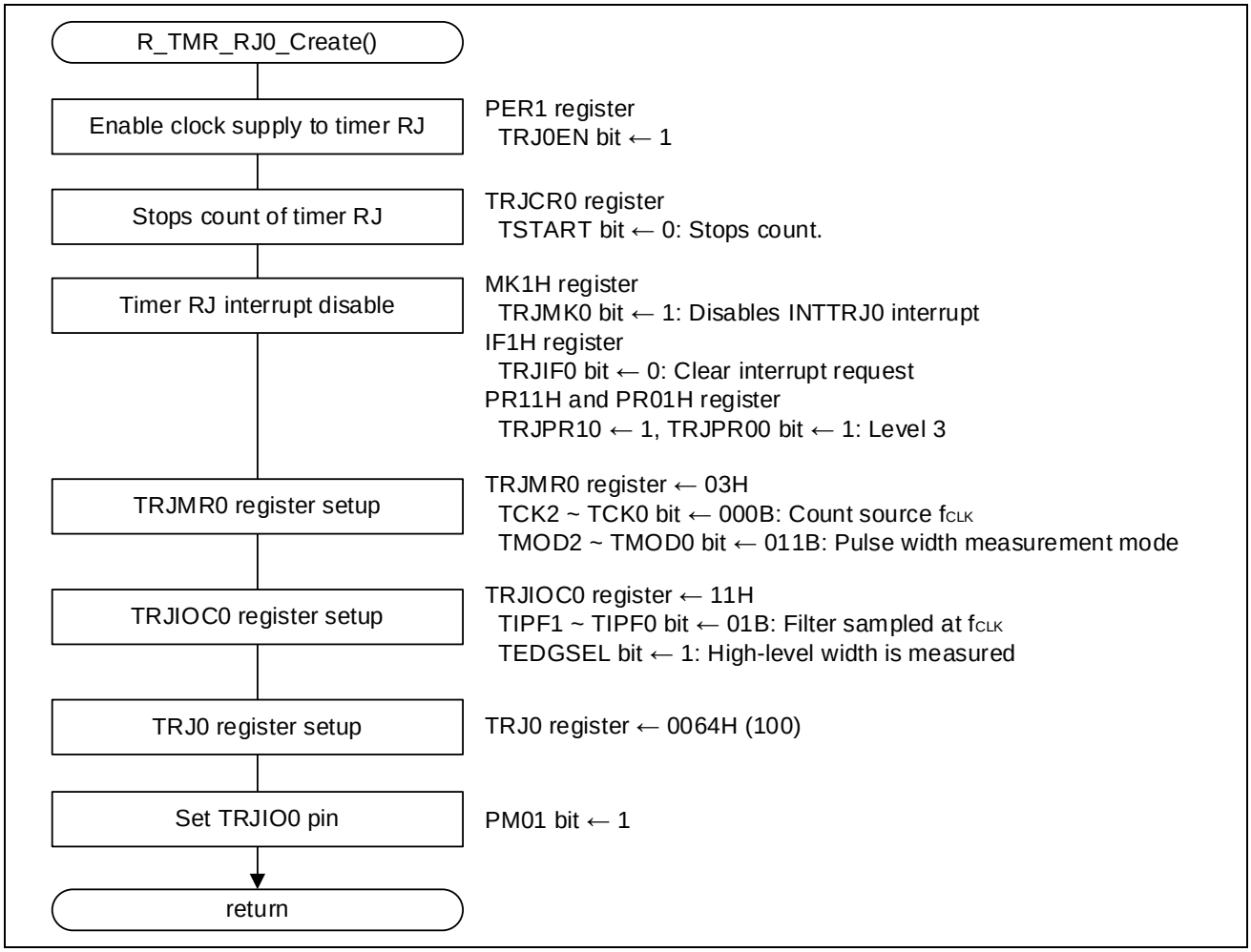

Figure 8.9 Timer RJ Setting

Start supplying clock to Timer RJ
• Peripheral enable register 1 (PER1)
Starts to supply clock to timer RJ.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
x	x	x	x	x	0	0	**1**

Bit 0

TRJ0EN	Control of timer RJ0 input clock supply
0	Stops input clock supply. • SFR used by timer RJ0 cannot be written. • Timer RJ0 is in the reset status.
1	**Enables input clock supply.** **• SFR used by timer RJ0 can be read/written.**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setup of timer RJ operation and interrupt level

• Timer RJ control register 0 (TRJCR0)
Stops Timer RJ counter operation.
Sets the interrupt cycle.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	**0**	**TUNDF**	**TEDGF**	**0**	**TSTOP**	**TCSTF**	**TSTART**
0	0	x	x	0	x	x	**0**

Bit 0

TSTART	Timer RJ count start
0	**Count stops**
1	Count starts

Disabling timer RJ interrupt
• Interrupt mask flag register (MK1H)
Disables interrupt processing.
• Interrupt request flag register (IF1H)
Clears the interrupt request flag.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	**TRJMK0**	**SRMK3 CSIMK31 IICMK31**	**STMK3 CSIMK30 IICMK30**	**KRMK**	**ITMK**	**RTCMK**	**ADMK**
x	**1**	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	**TRJIF0**	**SRIF3 CSIIF31 IICIF31**	**STIF3 CSIIF30 IICIF30**	**KRIF**	**ITIF**	**RTCIF**	**ADIF**
x	**0**	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting timer RJ interrupt priority level
• Priority Specification Flag Register (PR11H, PR01H)
Specifies level 3 (low priority level).

Symbol: PR11H

7	6	5	4	3	2	1	0
TMPR110	TRJPR10	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
x	**1**	x	x	x	x	x	x

Symbol: PR01H

7	6	5	4	3	2	1	0
TMPR010	TRJPR00	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
x	**1**	x	x	x	x	x	x

Bit 6

TRJPR10	TRJPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the timer RJ operation

• Timer RJ mode register 0 (TRJMR0)
Count source selection and operation mode selection.

Symbol: TRJMR0

7	6	5	4	3	2	1	0
0	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
0	0	0	0	x	0	1	1

Bit 6 to 4

TCK2	TCK1	TCK0	Timer RJ count source select
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/8$
0	1	1	$f_{CLK}/2$
1	0	0	f_{IL}
1	0	1	Event input from ELC
1	1	0	f_{SUB}
Other than above			Setting prohibited

Bit 2 to 0

TMOD2	TMOD1	TMOD0	Timer RJ operating mode select
0	0	0	Timer mode
0	0	1	Pulse output mode
0	1	0	Event counter mode
0	1	1	Pulse width measurement mode
1	0	0	Pulse period measurement mode
Other than above			Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

• Timer RJ I/O control register 0 (TRJIOC0)
The input/output of timer RJ setting.

Symbol: TRJIOC0

7	6	5	4	3	2	1	0
TIOGT1	TIOGT0	TIPF1	TIPF0	0	TOENA	0	TEDGSEL
x	x	0	1	0	0	0	1

Bit 5 to 4

TIPF1	TIPF0	TRJIO input filter select
0	0	No filter
0	1	Filter sampled at f_{CLK}
1	0	Filter sampled at $f_{CLK}/8$
1	1	Filter sampled at $f_{CLK}/32$

Bit 2

TOENA	TRJO output enable
0	TRJO output disabled (port)
1	TRJO output enabled

- Pulse width measurement mode
Bit 0

TEDGSEL	TRJIO I/O edge and polarity switching
0	Low-level width is measured
1	High-level width is measured

Setting TRJ0 register
• Timer RJ counter register 0 (TRJ0)
Setup the initial value of TRJ0 register.

Symbol: TRJ0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Setting TRJIO0 pin
• Port mode register (PM0)
Set TRJIO0 pin as input mode.

Symbol: PM0

7	6	5	4	3	2	1	0
1	PM06	PM05	PM04	PM03	PM02	PM01	PM00
1	x	x	x	x	x	1	x

Bit 1

PM01	P01 pin I/O mode selection
0	Output mode (the pin functions as an output port (output buffer on))
1	Input mode (the pin functions as an input port (output buffer off))

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

8.4.5.7 Main Processing

Figure 8.10 shows the flowchart for main processing.

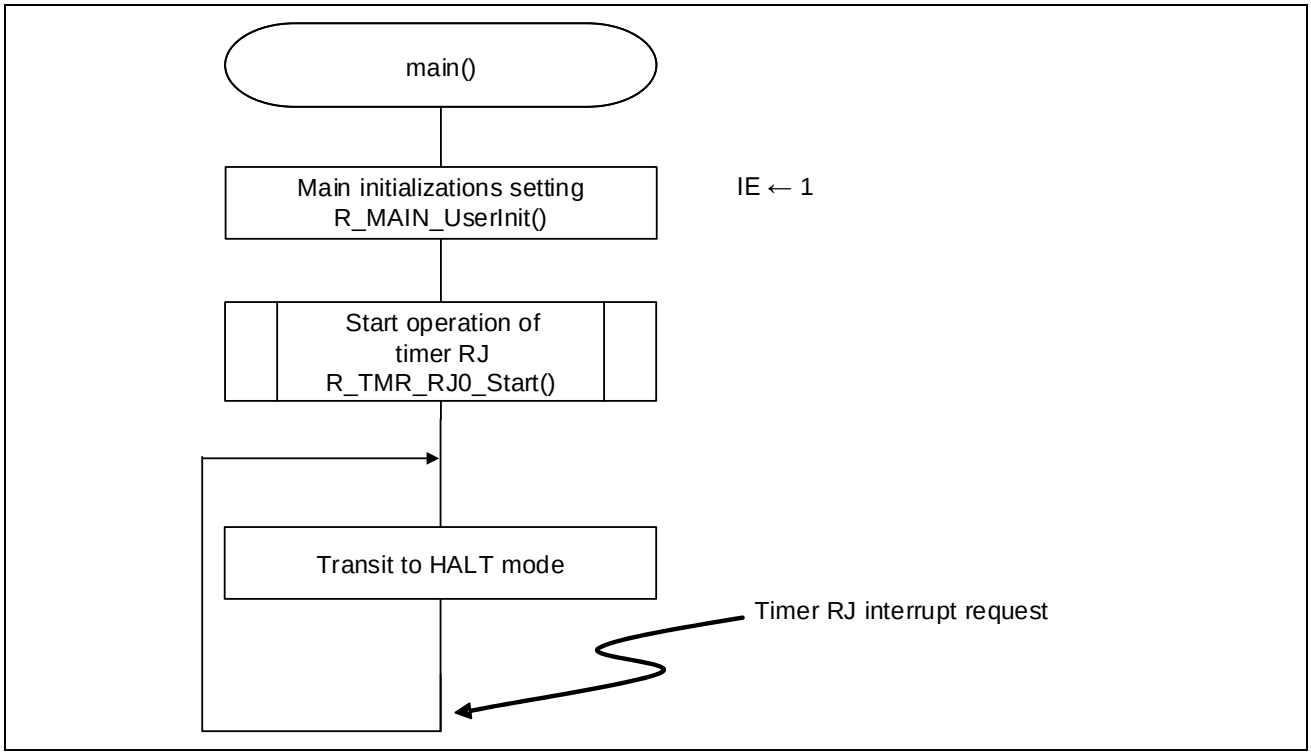

Figure 8.10 Main Processing

8.4.5.8 Timer RJ Operation Start

Figure 8.11 shows the flowchart for starting timer RJ operation.

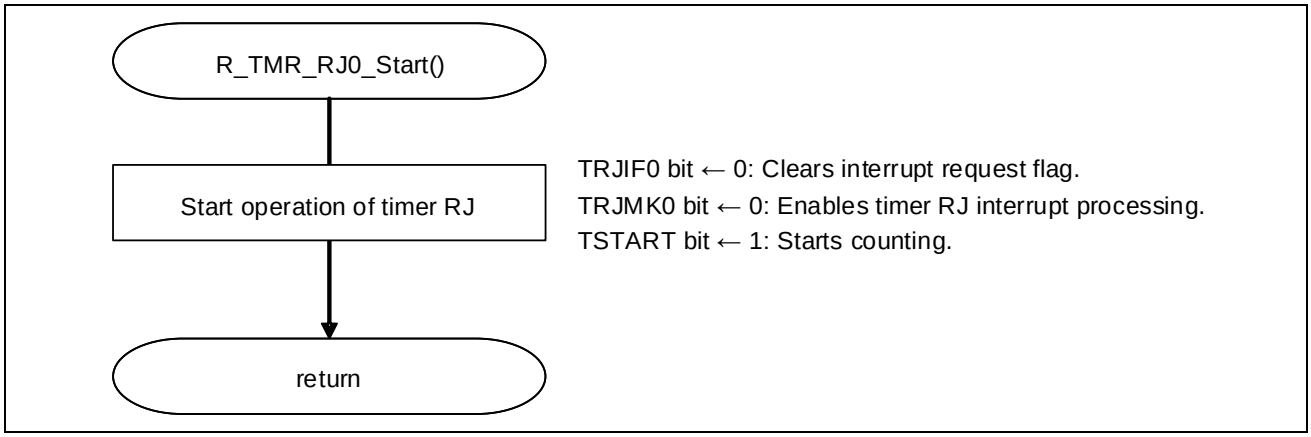

Figure 8.11 Timer RJ Operation Start

Configuring the timer interrupt
• Interrupt request flag register (IF1H)
Clears the interrupt request flag.
• Interrupt mask flag register (MK1H)
Enables interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	0	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	0	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Starting timer RJ counter operation
• Timer RJ control register 0 (TRJCR0)
Starts timer RJ counter operation.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSTF	TSTART
0	0	x	x	0	x	x	1

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	Count starts

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

8.4.5.9 INTTRJ0 Interrupt Processing

Figure 8.12 shows the flowchart for INTTRJ0 interrupt processing.

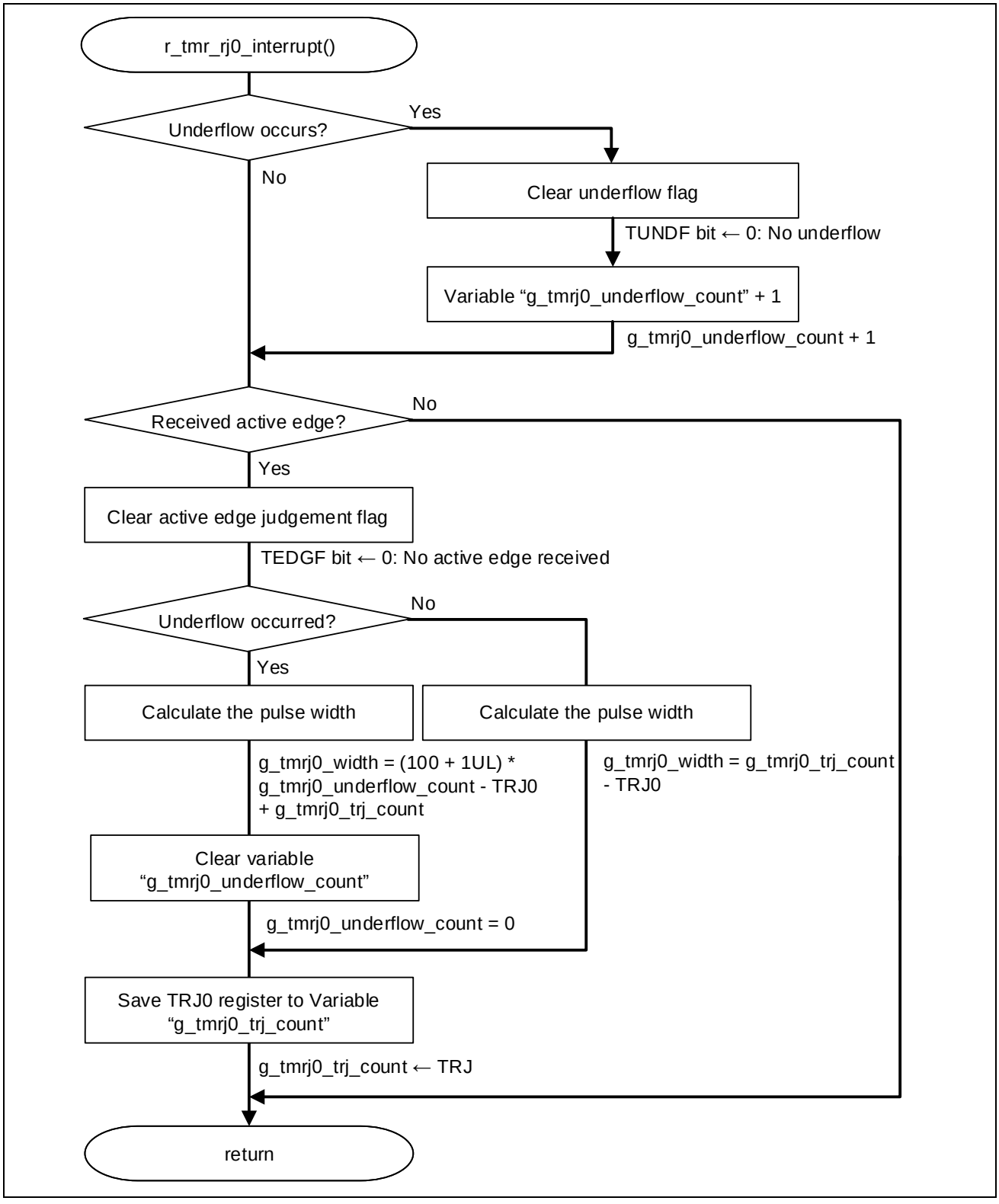

Figure 8.12 INTTRJ0 Interrupt Processing

9. Example of Migration from Pulse Period Measurement Mode

9.1 Specifications

The same operation as that in pulse period measurement mode in timer RA of R8C/36M can be realized by using timer RJ of RL78/G14.
In pulse period measurement mode, the pulse period of an external signal input to the TRJIO0 pin is measured. The counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR0 register. When a pulse with the period specified by the TEDGSEL bit in the TRJIOC0 register is input to the TRJIO0 pin, the count value is transferred to the read-out buffer at the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGF bit in the TRJCR0 register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (TRJ0 register) is read at this time and the difference from the reload value is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF bit in the TRJCR0 register is set to 1 (underflow) and an interrupt request is generated.

Table 9.1 lists the peripheral functions to be used and their uses (example of migration from pulse period measurement mode), and Figure 9.1 shows the operation overview (example of migration from pulse period measurement mode).

Table 9.1 Peripheral Functions to be Used and Their Uses

(Example of Migration from Pulse Period Measurement Mode)

Peripheral Function	Use
Timer RJ (pulse period measurement mode)	Measure the pulse period of an external signal.

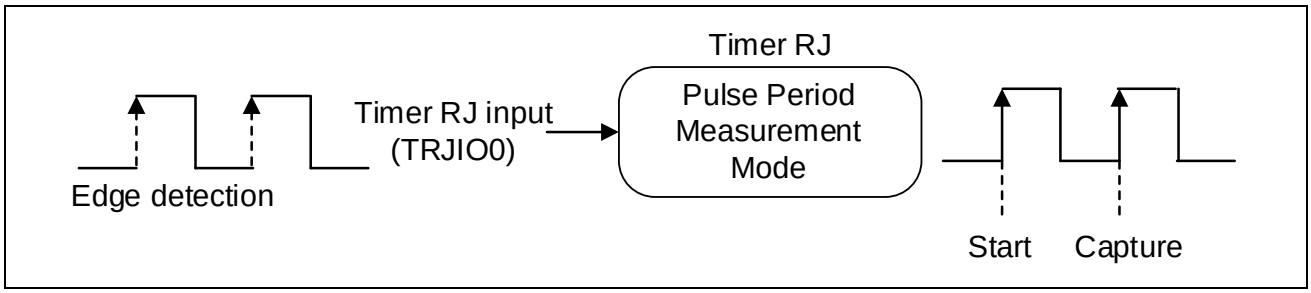

Figure 9.1 Operation Overview (Example of Migration from Pulse Period Measurement Mode)

This example applies when the TEDGSEL bit in the TRJIOC0 register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

9.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

Table 9.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (VLVD): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V6.0.0 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

9.3 Description of Hardware

9.3.1 Hardware Configuration Example

Figure 9.2 shows an example of hardware configuration that is used for this chapter.

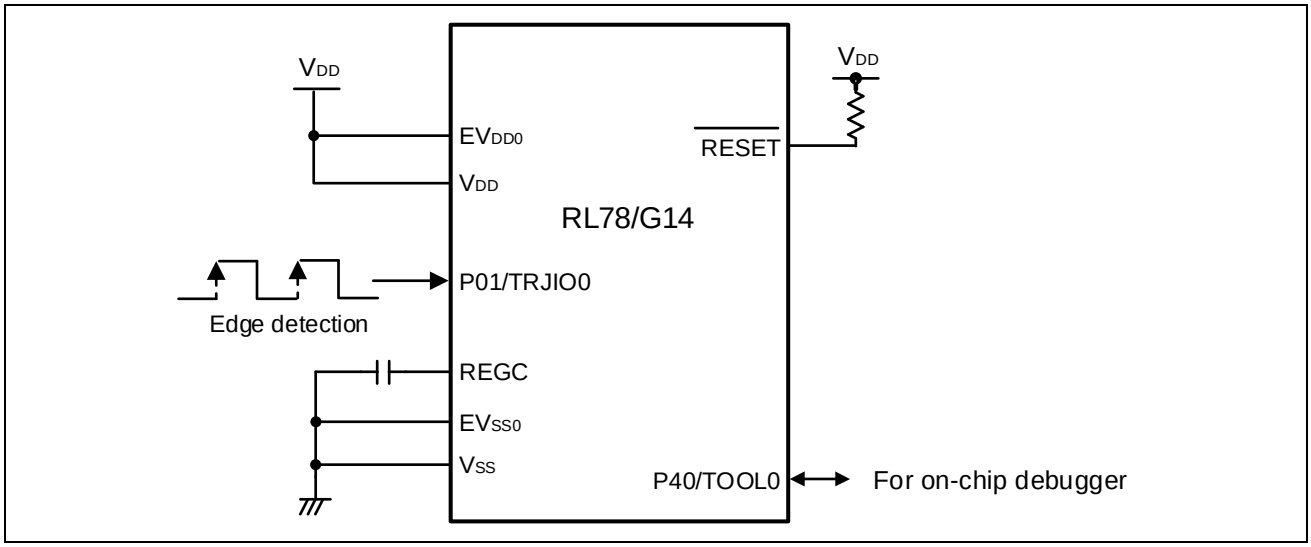

Figure 9.2 Hardware Configuration (Pulse Period Measurement Mode)

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

9.3.2 List of Pins to be Used

Table 9.3 lists the pins to be used and their functions.

Table 9.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P01/TRJIO0	Input	Measure the pulse period.

9.4 Description of Software

9.4.1 Operation Outline

This chapter describes how to set up the pulse period measurement mode of timer RJ.
Each time a valid edge (rising edge of the measurement pulse) is detected on the timer RJ input pin (TRJIO0), the sample code described in this chapter captures the count value of the timer and measures the period of the pulse which arrives at the timer RJ input pin (TRJIO0). When a timer interrupt (INTTRJ0) occurs upon completion of the capture, the sample code calculates the pulse period and stores the calculation result in the on-chip RAM.

Table 9.4 lists the peripheral functions to be used and their uses. Figure 9.3 shows the pulse period measurement mode and its interrupt operation.

(1) Initialize the timer RJ.
<Conditions for setting>
Use the pulse period measurement mode as the timer RJ operation mode.
Select f_{CLK} as the count source of timer RJ.
Initialize timer RJ counter register 0 (TRJ0), and measure from one rising edge to the next rising edge of the pulse input to TRJIO0 pin.
Use timer interrupts (INTTRJ0) from timer RJ.

(2) Sets "1" (starts counter operation) to TSTART bit of TRJCR0 register to start the count of timer RJ.

(3) Execute a HALT instruction to wait for timer interrupts (INTTRJ0).

(4) When the interrupt request is generated, calculates the pulse period and stores the calculation result in the on-chip RAM.

(5) The sample code returns to step (3) to execute HALT instruction and waits for the next timer interrupt (INTTRJ0) from timer RJ.

Table 9.4 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Timer RJ	Measure the pulse period of TRJIO0 pin.

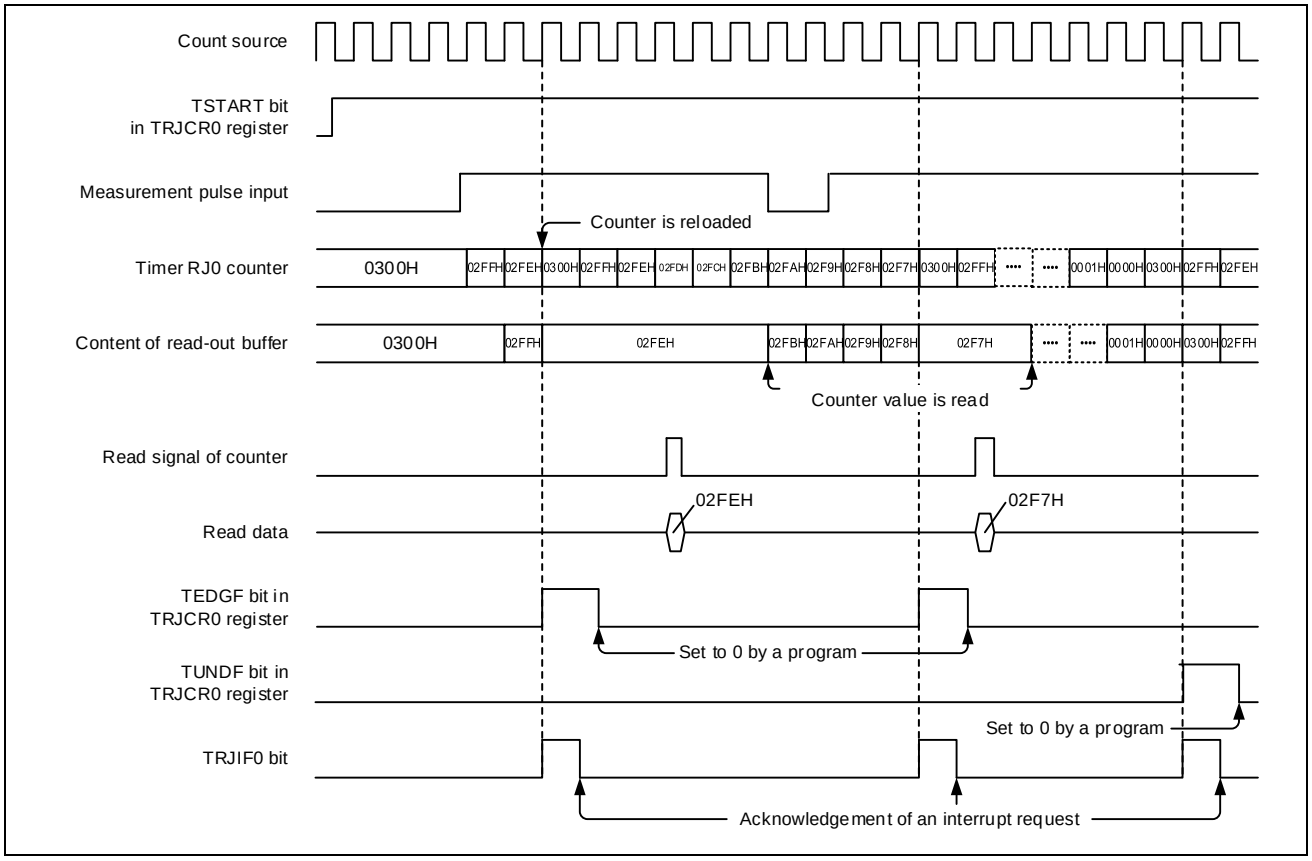

Figure 9.3 Overview of Timer RJ Operation and Interrupts (Pulse Period Measurement Mode)

9.4.2 List of Option Byte Setting

Table 9.5 summarizes the settings of the option bytes.

Table 9.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

9.4.3 List of Functions

Table 9.6 lists the functions that are used in this sample program.

Table 9.6 Functions

Function Name	Outline
R_TMR_RJ0_Create()	Initializes timer RJ.
R_TMR_RJ0_Start()	Starts timer RJ operation.
r_tmr_rj0_interrupt()	Processes timer interrupts on timer RJ.

9.4.4 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TMR_RJ0_Create()

Synopsis	Initializes timer RJ
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Create(void)
Explanation	This function initializes timer RJ.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TMR_RJ0_Start()

Synopsis	Starts timer RJ operation
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RJ0_Start(void)
Explanation	This function enables timer RJ interrupts and prepares to measure the pulse period.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tmr_rj0_interrupt()

Synopsis	Timer RJ interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	static void __near r_tmr_rj0_interrupt(void)
Explanation	This function calculates the pulse period and stores the calculation result in the on-chip RAM.
Arguments	None
Return value	None
Remarks	None

9.4.5 Flow Chart

9.4.5.1 Overall Flow

Figure 9.4 shows the overall flow of the sample program described in this chapter.

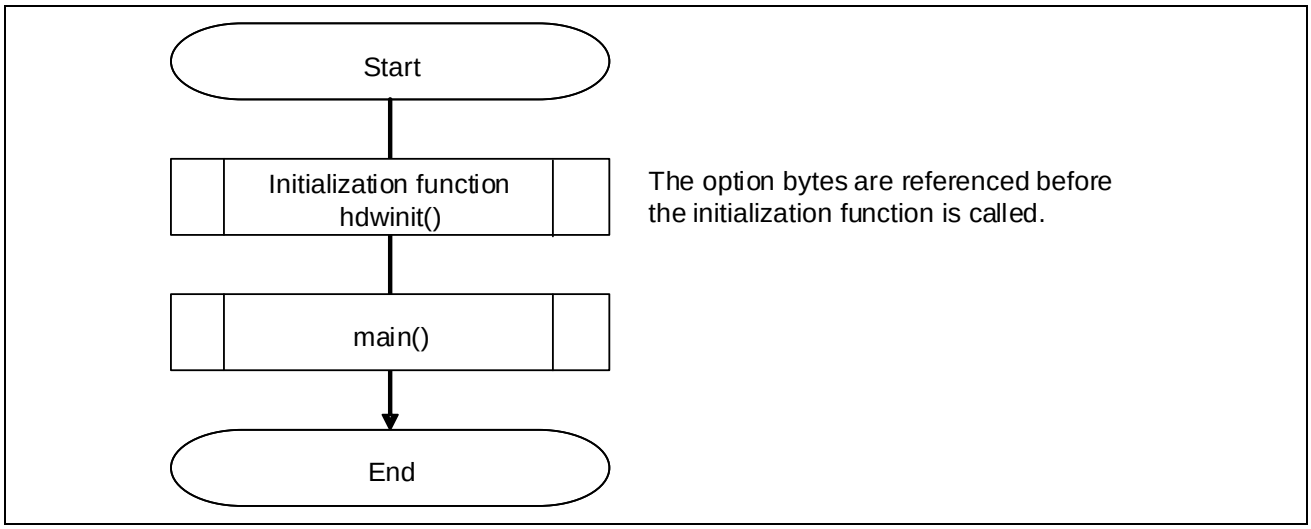

Figure 9.4 Overall Flow

9.4.5.2 Initialization Function

Figure 9.5 shows the flowchart for the initialization function.

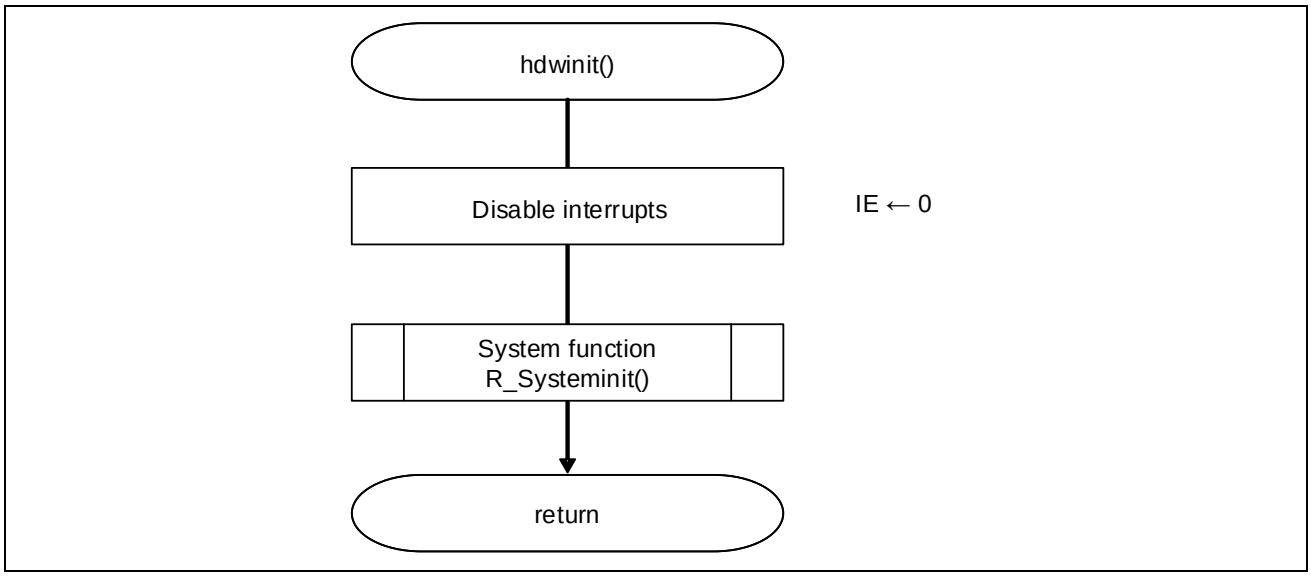

Figure 9.5 Initialization Function

9.4.5.3 System Function

Figure 9.6 shows the flowchart for the system function.

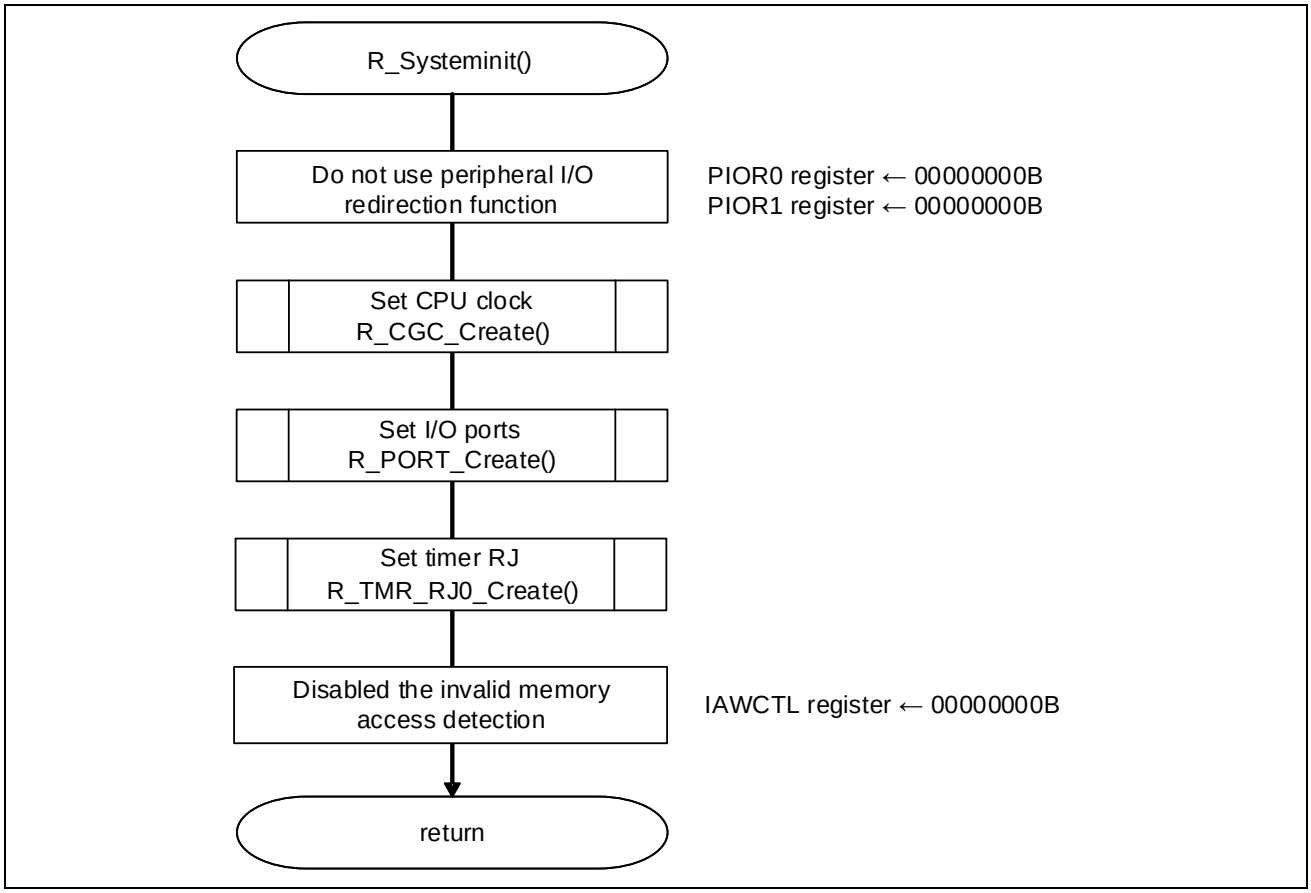

Figure 9.6 System Function

9.4.5.4 CPU Clock Setting

Figure 9.7 shows the flowchart for setting the CPU clock.

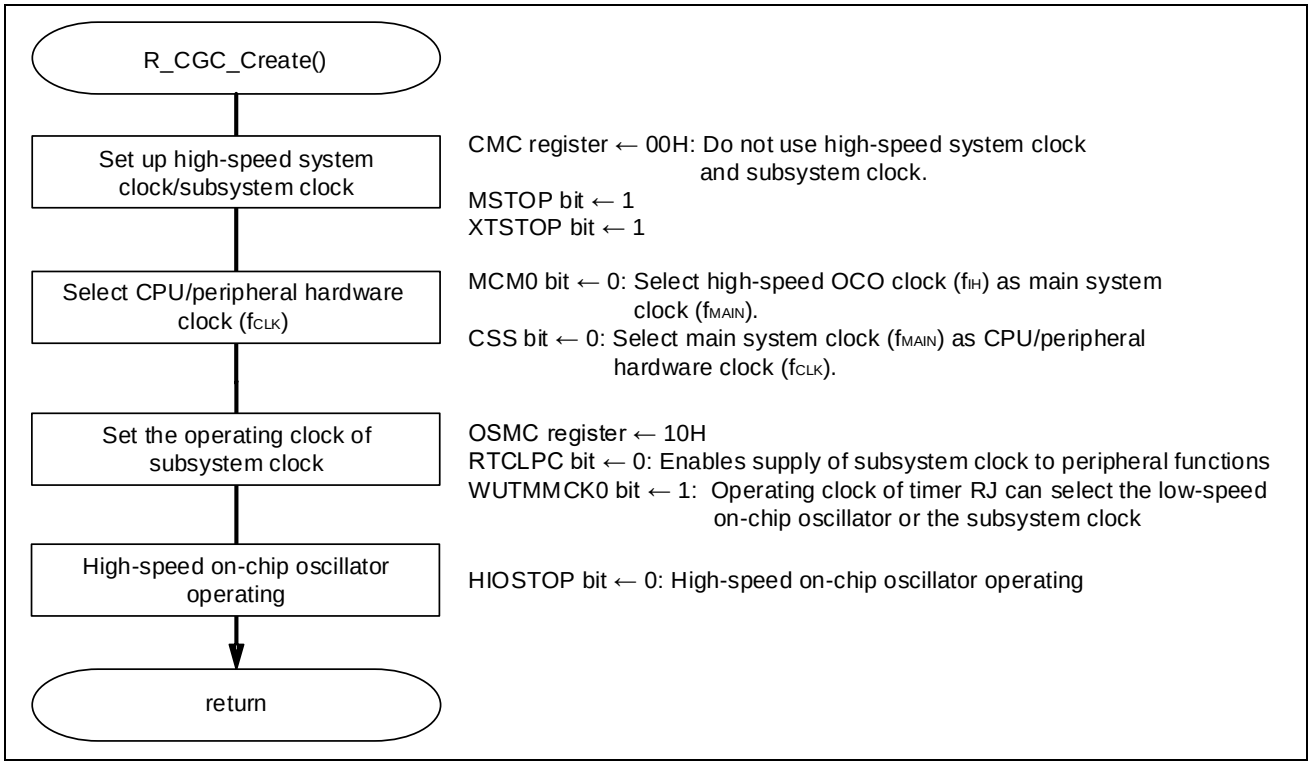

Figure 9.7 CPU Clock Setting

9.4.5.5 I/O Port Setting

Figure 9.8 shows the flowchart for setting the I/O ports.

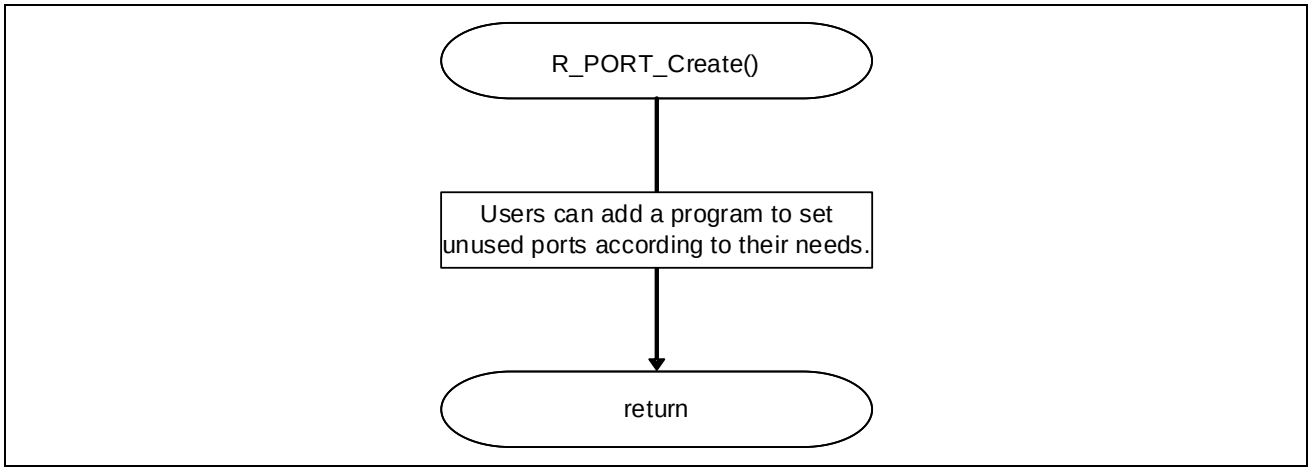

Figure 9.8 I/O Port Setting

Caution: Please provide proper pin treatment and make sure that the electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

9.4.5.6 Timer RJ Setting

Figure 9.9 shows the flowchart for setting timer RJ.

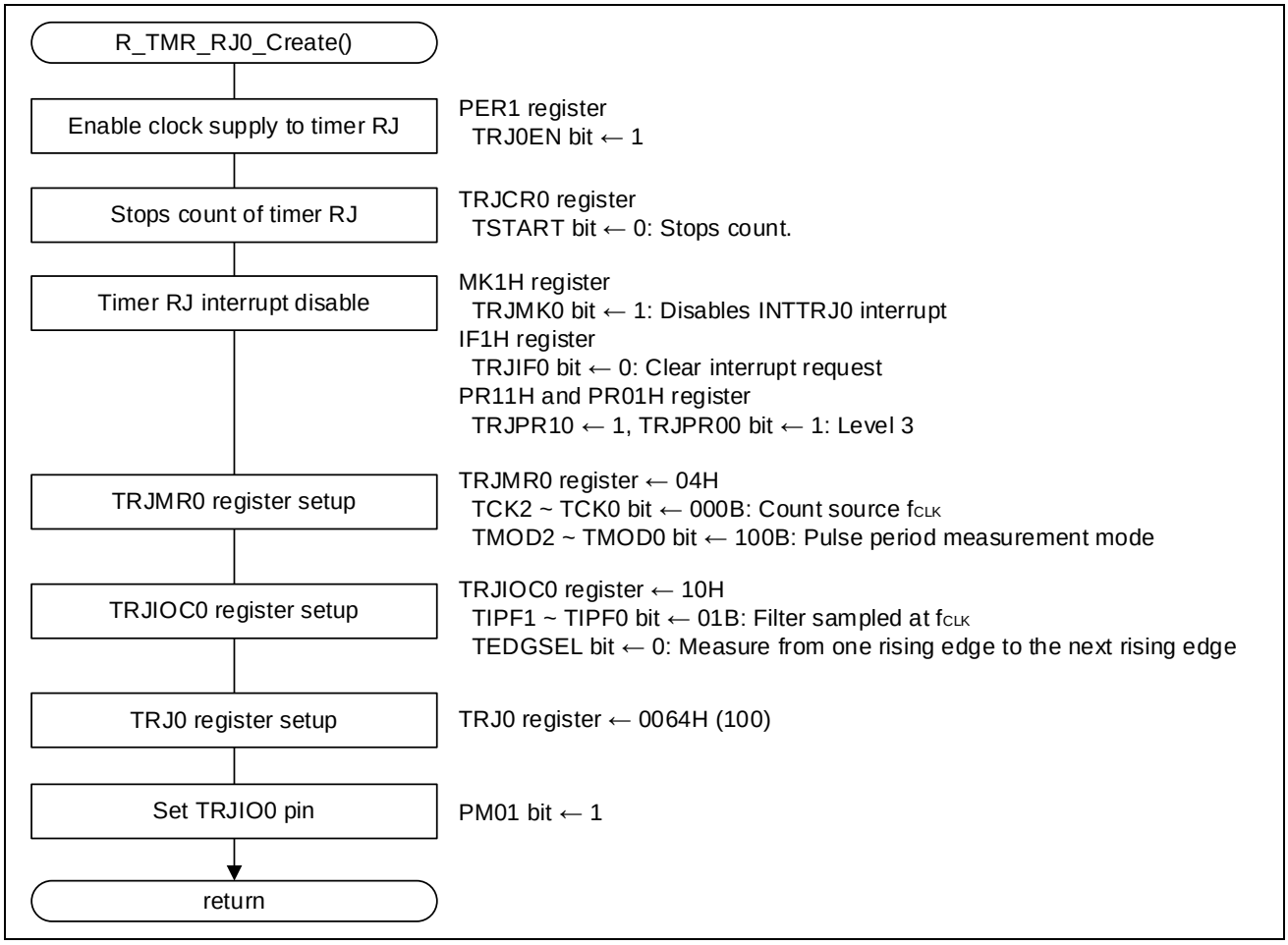

Figure 9.9 Timer RJ Setting

Start supplying clock to Timer RJ
• Peripheral enable register 1 (PER1)
Starts to supply clock to timer RJ.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
x	x	x	x	x	0	0	1

Bit 0

TRJ0EN	Control of timer RJ0 input clock supply
0	Stops input clock supply. • SFR used by timer RJ0 cannot be written. • Timer RJ0 is in the reset status.
1	**Enables input clock supply.** **• SFR used by timer RJ0 can be read/written.**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setup of timer RJ operation and interrupt level

• Timer RJ control register 0 (TRJCR0)
Stops Timer RJ counter operation.
Sets the interrupt cycle.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	**0**	**TUNDF**	**TEDGF**	**0**	**TSTOP**	**TCSTF**	**TSTART**
0	0	x	x	0	x	x	**0**

Bit 0

TSTART	Timer RJ count start
0	**Count stops**
1	Count starts

Disabling timer RJ interrupt
• Interrupt mask flag register (MK1H)
Disables interrupt processing.
• Interrupt request flag register (IF1H)
Clears the interrupt request flag.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	**TRJMK0**	**SRMK3 CSIMK31 IICMK31**	**STMK3 CSIMK30 IICMK30**	**KRMK**	**ITMK**	**RTCMK**	**ADMK**
x	**1**	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	**TRJIF0**	**SRIF3 CSIIF31 IICIF31**	**STIF3 CSIIF30 IICIF30**	**KRIF**	**ITIF**	**RTCIF**	**ADIF**
x	**0**	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting timer RJ interrupt priority level
• Priority Specification Flag Register (PR11H, PR01H)
Specifies level 3 (low priority level).

Symbol: PR11H

7	6	5	4	3	2	1	0
TMPR110	TRJPR10	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
x	**1**	x	x	x	x	x	x

Symbol: PR01H

7	6	5	4	3	2	1	0
TMPR010	TRJPR00	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
x	**1**	x	x	x	x	x	x

Bit 6

TRJPR10	TRJPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the timer RJ operation

• Timer RJ mode register 0 (TRJMR0)
Count source selection and operation mode selection.

Symbol: TRJMR0

7	6	5	4	3	2	1	0
0	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
0	0	0	0	x	1	0	0

Bit 6 to 4

TCK2	TCK1	TCK0	Timer RJ count source select
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/8$
0	1	1	$f_{CLK}/2$
1	0	0	f_{IL}
1	0	1	Event input from ELC
1	1	0	f_{SUB}
Other than above			Setting prohibited

Bit 2 to 0

TMOD2	TMOD1	TMOD0	Timer RJ operating mode select
0	0	0	Timer mode
0	0	1	Pulse output mode
0	1	0	Event counter mode
0	1	1	Pulse width measurement mode
1	0	0	Pulse period measurement mode
Other than above			Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

• Timer RJ I/O control register 0 (TRJIOC0)
The input/output of timer RJ setting.

Symbol: TRJIOC0

7	6	5	4	3	2	1	0
TIOGT1	TIOGT0	TIPF1	TIPF0	0	TOENA	0	TEDGSEL
x	x	0	1	0	0	0	0

Bit 5 to 4

TIPF1	TIPF0	TRJIO input filter select
0	0	No filter
0	1	Filter sampled at f_{CLK}
1	0	Filter sampled at $f_{CLK}/8$
1	1	Filter sampled at $f_{CLK}/32$

Bit 2

TOENA	TRJO output enable
0	TRJO output disabled (port)
1	TRJO output enabled

- Pulse period measurement mode
Bit 0

TEDGSEL	TRJIO I/O edge and polarity switch
0	Measure from one rising edge to the next rising edge
1	Measure from one falling edge to the next falling edge

Setting TRJ0 register
• Timer RJ counter register 0 (TRJ0)
Setup the initial value of TRJ0 register.

Symbol: TRJ0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Setting TRJIO0 pin
• Port mode register (PM0)
Set TRJIO0 pin as input mode.

Symbol: PM0

7	6	5	4	3	2	1	0
1	PM06	PM05	PM04	PM03	PM02	PM01	PM00
1	x	x	x	x	x	1	x

Bit 1

PM01	P01 pin I/O mode selection
0	Output mode (the pin functions as an output port (output buffer on))
1	Input mode (the pin functions as an input port (output buffer off))

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

9.4.5.7 Main Processing

Figure 9.10 shows the flowchart for main processing.

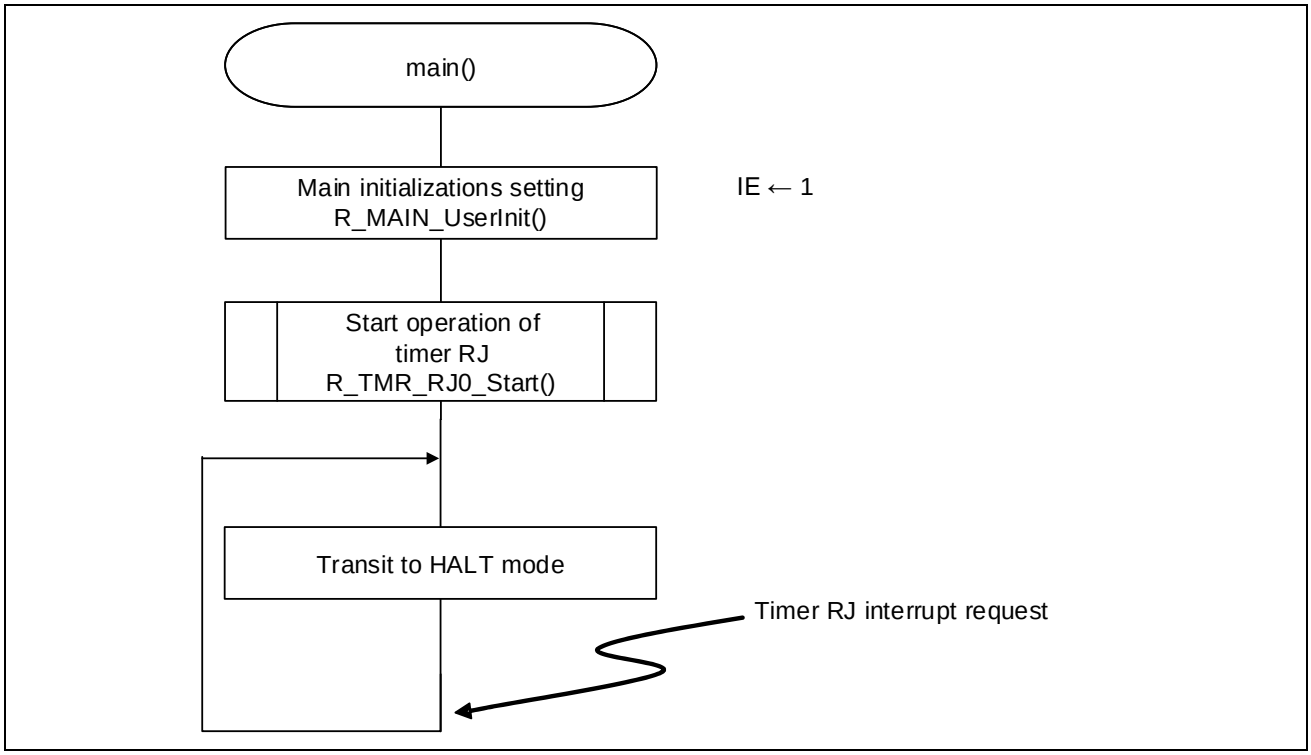

Figure 9.10 Main Processing

9.4.5.8 Timer RJ Operation Start

Figure 9.11 shows the flowchart for starting timer RJ operation.

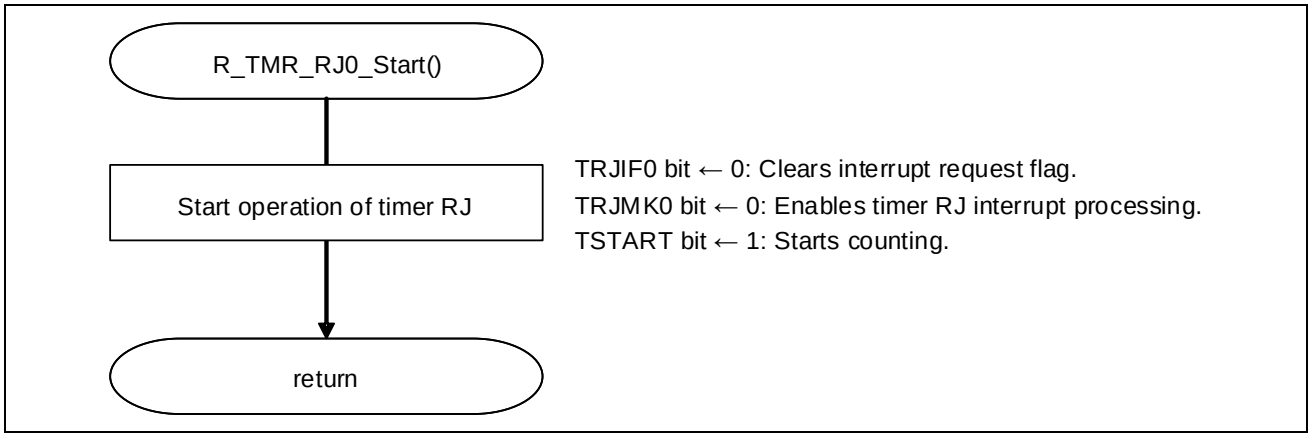

Figure 9.11 Timer RJ Operation Start

Configuring the timer interrupt
• Interrupt request flag register (IF1H)
Clears the interrupt request flag.
• Interrupt mask flag register (MK1H)
Enables interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	0	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	0	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Starting timer RJ counter operation
• Timer RJ control register 0 (TRJCR0)
Starts timer RJ counter operation.

Symbol: TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSTF	TSTART
0	0	x	x	0	x	x	1

Bit 0

TSTART	Timer RJ count start
0	Count stops
1	Count starts

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

9.4.5.9 INTTRJ0 Interrupt Processing

Figure 9.12 shows the flowchart for INTTRJ0 interrupt processing.

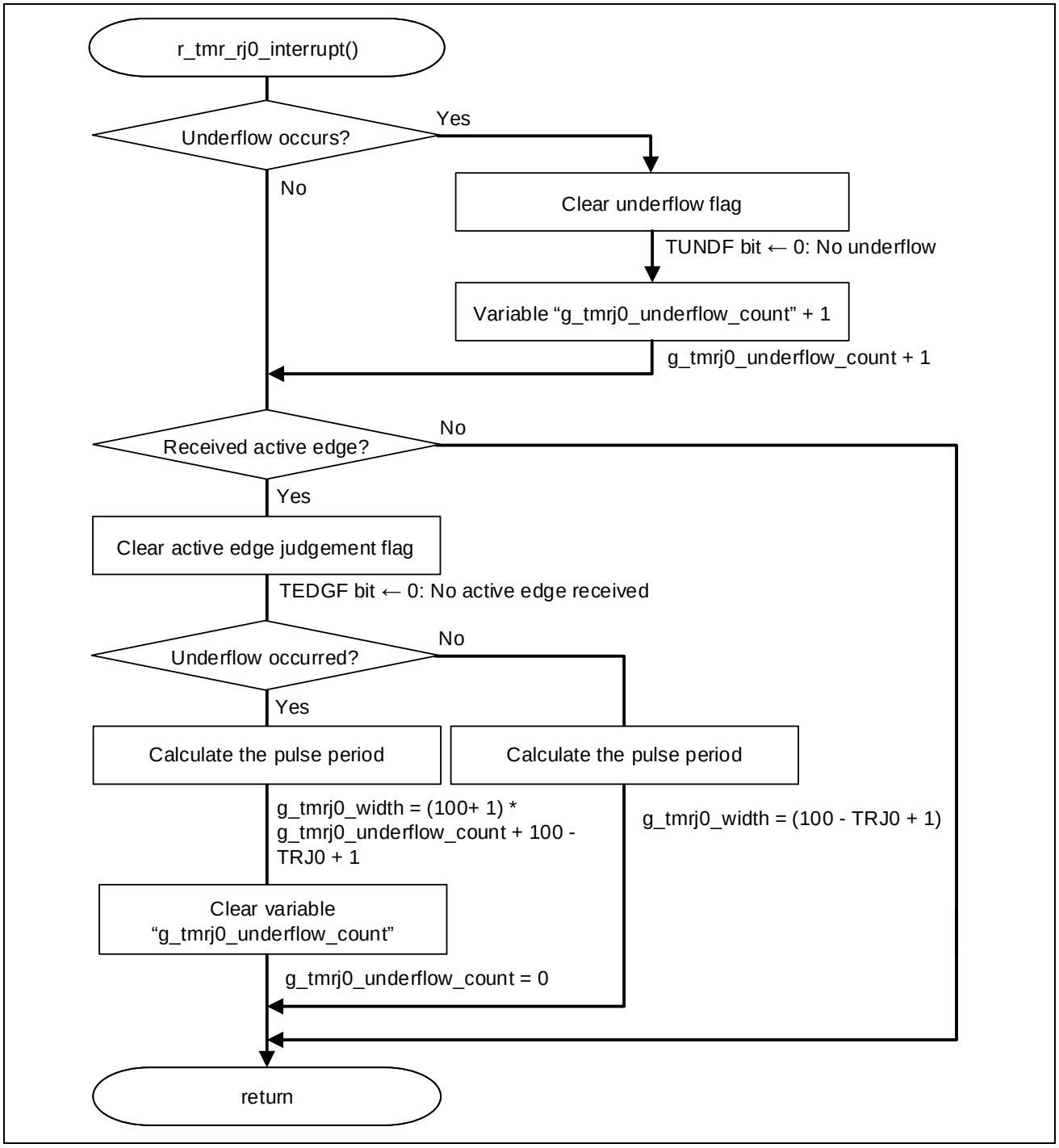

Figure 9.12 INTTRJ0 Interrupt Processing

10. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

11. Reference Documents

User's Manual: Hardware
RL78/G14 User's Manual: Hardware (R01UH0186)
R8C/36M Group User's Manual: Hardware (R01UH0259)
The latest versions can be downloaded from the Renesas Electronics website.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Apr. 12, 2018	-	First edition issued
1.01	Oct. 22, 2018	6	Modification of description in Table 2.1
		11	Modification of description in Table 2.6
		16	Modification of description in Table 3.1
		16	Modification of description in Table 3.2
		56	Modification of error in Table 7.3
		56	Modification of error in 7.4.1 Operation Outline
		57	Modification of error in Table 7.4
		75	Modification of description in 8.4.1 Operation Outline
		95	Addition of description in 9.4.1 Operation Outline
		113	Deletion of old 11. Reference Application Note

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Colophon 7.2