RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Reset Function

Introduction

This document describes how to migrate the reset function of the R8C/36M Group to the reset function of the RL78/G14 (a 64-pin product is taken as an example in this document).

Target Device

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1.   Migration Method from R8C Family to RL78 Family

The following sections describe how to implement the reset function of the R8C/36M by using the reset function of the RL78/G14.

Table 1.1 shows the reset function of the R8C/36M group, and Table 1.2 shows the reset function of the RL78/G14.

Table 1.1 Reset Function in R8C/36M

Reset Function in R8C/36M	
Reset Name	**Source**
Hardware reset	**Input voltage of RESET pin is held low**
Power-on reset	**VCC rises**
Voltage monitor 0 reset	**VCC falls (monitor voltage: Vdet0)**
Watchdog timer reset	**Underflow of watchdog timer**
Software reset	**Write 1 to PM03 bit in PM0 register**

Table 1.2 Reset Function in RL78/G14

Reset Function in RL78/G14
External reset input via RESET pin (input a low level)
Internal reset by watchdog timer program loop detection
Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit
Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage
Internal reset by execution of illegal instruction (instruction code FFH)
Internal reset by RAM parity error
Internal reset by illegal-memory access

The R8C/36M group has five types of reset functions and the RL78/G14 has seven types of reset functions.

Table 1.3 shows the correspondence between the R8C/36M group reset functions and RL78/G14 reset functions.

Table 1.3 Correspondence between Reset Functions

R8C/36M Group	RL78/G14
Hardware reset	External reset input via RESET pin (Input a low level to the RESET pin)
Power-on reset	Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit
Voltage monitor 0 reset	Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage
Watchdog timer reset	Internal reset by watchdog timer program loop detection
Software reset	— (Note that an equivalent reset can be generated by execution of an illegal instruction (instruction code FFH). (Note 1))

Note 1: Reset is not generated by execution of an illegal instruction during emulation with the in-circuit emulator or on-chip debug emulator.

2. Differences between RL78/G14 and R8C/36M Group

2.1 Differences in Reset Function

Table 2.1 shows the differences between the R8C/36M group reset functions and RL78/G14 reset functions.

Refer to the relevant user's manual of the product for the differences between each MCU's reset function specifications, SFR (special function register) state after reset, and electric characteristics.

Table 2.1 Differences between Reset Functions (Summary)

Item	R8C/36M Group	RL78/G14
CPU clock after reset release	Low-speed on-chip oscillator (undivided clock)	High-speed on-chip oscillator (clock selected with the option bytes)
Program counter (PC) value after reset release	Reset vector Value at (addresses 0FFFEh to 0FFFCh)	Reset vector table Value at (addresses 00000H and 00001H)
RAM value after reset release	Undefined	Undefined
Protect state after reset release (Note 1)	Protection of the important registers by using the PRCR register: Enabled	SFR guard function: Disabled (protection canceled)
Clock supply to peripheral hardware after reset release (Note 2)	Enabled	Disabled

Note 1. The logic (setting values) for the bits to enable/disable the protect functions of the R8C/36M is reverse to that of the RL78/G14. Be sure to set the appropriate values; otherwise, the registers are not protected correctly.

Note 2. The logic (setting values) for the bits to enable/disable the clock supply to the peripheral hardware of the R8C/36M is reverse to that of the RL78/G14. Be sure to set the appropriate values; otherwise, the peripheral hardware will not operate.

2.1.1   Migration from Hardware reset

To provide the RL78/G14 with the equivalent operation to the hardware reset of the R8C/36M, execute "external reset input via the RESET pin (input a low level to the RESET pin)."

Table 2.2 shows the reset via the RESET pin of the R8C/36M group and RL78/G14.

Table 2.2 Reset via RESET Pin of R8C/36M Group and RL78/G14

Item	R8C/36M Group	RL78/G14
Condition for enabling a reset when power supply is stable	(1) Input a low level to the RESET pin. (2) Wait for $10\,\mu$ s. (3) Input a high level to the RESET pin.	(1) Input a low level to the RESET pin. (2) Wait for $10\,\mu$ s or more. (3) Input a high level to the RESET pin.
Condition for enabling a reset at power on	(1) Input a low level to the RESET pin. (2) Increase the supply voltage until it meets the recommended operating conditions. (Note 1) (3) Wait for the time for internal power supply stabilization during power-on (td(P-R)) or more to allow the internal power supply to stabilize. (Note 2) (4) Wait for $10\,\mu$ s. (5) Input a high level to the RESET pin.	(1) Input a low level to the RESET pin. (2) Turn power on and continue to input a low level for $10\,\mu$ s or more within the operating voltage range shown in the AC Characteristics section. (Note 3) (3) Input a high level to the RESET pin.

Note 1. For the recommended operating conditions, refer to the Electrical Characteristics chapter of the R8C/36M Group User's Manual.

Note 2. For the time for internal power supply stabilization during power-on (td(P-R)), refer to the Power Supply Circuit Timing Characteristics table in the R8C/36M Group User's Manual.

Note 3. For the operating voltage range, refer to the Electrical Specifications chapter of the RL78/G14 User's Manual.

2.1.2   Migration from Power-on reset

To provide the RL78/G14 with the equivalent operation to the power-on reset of the R8C/36M, execute "internal reset by comparison of supply voltage and detection voltage of the power-on-reset (POR) circuit." When using POR, the voltage detection circuit (LVD) (voltage monitor 0 circuit of the R8C/36M group) needs to be used together. For LVD operation mode setting, set the LVIMDS1 and LVIMDS0 bits to 11b (reset mode) at addresses 000C1H/010C1H in the option bytes.

For details, refer to the following application note.

- APPLICATION NOTE RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: Power-on Reset and Voltage Detector (R01AN1352)

Note   The voltage detection level for "internal reset by comparison of supply voltage and detection voltage of the power-on-reset (POR) circuit" of the RL78/G14 is different from that of the power-on reset function of the R8C/36M. For the RL78/G14, the voltage detection level same as the detection level for the R8C/36M cannot be set; therefore, set the appropriate LVD voltage detection level for the system used, and fully evaluate the operation.

2.1.3   Migration from Voltage monitor 0 reset

For details on how to provide the RL78/G14 with the equivalent operation to the voltage monitor 0 reset of the R8C/36M, refer to the shown chapter of the following application note.

- APPLICATION NOTE RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: Power-on Reset and Voltage Detector (R01AN1352)
  Reset Mode section

2.1.4   Migration from Watchdog timer reset

For details on how to provide the RL78/G14 with the equivalent operation to the watchdog timer reset of the R8C/36M, refer to the following application note.

- APPLICATION NOTE RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: Watchdog Timer CC-RL (R01AN3060)

2.1.5   Migration from Software reset

The RL78/G14 is not provided with the function equivalent to the software reset (PM03 bit in the PM0 register) of the R8C/36M group. The following methods can be used to reset the RL78/G14 at a desired timing.

An internal reset is generated by execution of an illegal instruction (instruction code FFH). (Notes 1 and 2)

When the watchdog timer is used, an internal reset is generated by executing the refresh process at the value other than the refresh code (by writing data other than ACH to the WDTE register).

Note 1.   Reset is not generated by execution of an illegal instruction during emulation with the in-circuit emulator or on-chip debug emulator.

Note 2.   The reset control flag register (RESF) can indicate the reset source (an internal reset by execution of an illegal instruction). However, it is impossible to distinguish the intentionally generated internal reset from the internal reset caused by an abnormality. Be sure to confirm that this does not have an adverse effect on the system.

2.2   Register Compatibility

Table 2.3 compares the registers for the reset functions of the R8C/36M group to the corresponding registers of the RL78/G14.

Table 2.3 Register Compatibility

Item	R8C/36M Group	RL78/G14
Software reset application	• PM0 register PM03 bit	—
Reset process determination at power on/when a reset occurs during operation	• RSTFR register CWR bit	—
Hardware reset detect flag	• RSTFR register HWR bit	—
Software reset detect flag	• RSTFR register SWR bit	—

Watchdog timer reset detect flag	• RSTFR register
	
	  WDR bit
		• RESF register
		
		  WDTRF bit

Determination flag for internal reset by execution of an illegal instruction	—	• RESF register TRAP bit
Determination flag for internal reset by a RAM parity error	—	• RESF register RPERF bit
Determination flag for internal reset by illegal memory access	—	• RESF register IAWRF bit
Determination flag for internal reset by the voltage detector (LVD)	—	• RESF register LVIRF bit

— : There is no corresponding register.

3.   Reference Application Note

RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Power-on Reset and Voltage Detector (R01AN1352)
RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Watchdog Timer CC-RL (R01AN3060)
The latest versions can be downloaded from the Renesas Electronics website.

4.   Reference Documents

User's Manual: Hardware

RL78/G14 User's Manual: Hardware (R01UH0186)
R8C/36M Group User's Manual: Hardware (R01UH0259)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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Revision History

Rev.	Date	Description	
		Page	**Summary**
1.00	June 27, 2018	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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