RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: I/O Ports

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Abstract

This document describes how to migrate the R8C/36M Group I/O ports to the port functions in the RL78/G14 100-pin package.

Products

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences between the R8C/36M Group and RL78/G14

Table 1.1 lists the differences between I/O ports in the R8C/36M Group and the port functions in RL78/G14.

Table 1.1 Differences

Item	R8C/36M Group	RL78/G14
Number of ports	60	• 30-pin package: 26 • 32-pin package: 28 • 36-pin package: 32 • 40-pin package: 36 • 44-pin package: 40 • 48-pin package: 44 • 52-pin package: 48 • 64-pin package: 58 • 80-pin package: 74 • 100-pin package: 92
I/O buffer power supply	VCC	• V_{DD} (1) • EV_{DD0} (2) • EV_{DD1} (2)
Ground for port pins	VSS	• V_{SS} (1) • EV_{SS0} (2) • EV_{SS1} (2)
Drive capacity control	Yes	No
Through-current protection to input buffers	No	Yes
Controlling the input threshold value	Three voltage levels can be specified using registers VLT0, VLT1, and VLT2	Two input threshold values can be specified by setting EV_{DD0} (2) to comply with the power supply of the device connected to the MCU, or setting the PIMxx register

PIMxx: xx = 0, 1, 3 to 5, 8, and 14

Notes: 1. Applies to port pins P20 to P27, P121 to P124, P137 P150 to P156, and pins other than port pins.
2. Applies to port pins other than P20 to P27, P121 to P124, P137, and P150 to P156.

2. Register Compatibility

Register compatibility between I/O ports in the R8C/36M Group and RL78/G14 is listed in Table 2.1 and Table 2.2.

Table 2.1 Register Compatibility (1/2)

Item	R8C/36M Group	RL78/G14
Port level control	• Pi register	• Pxx register
Port direction select	• PDi register	• PMxx register
Pin assign control	• TRASR register • TRBRCSR register • TRCPSR0 register • TRCPSR1 register • TRDPSR0 register • TRDPSR1 register • TIMSR register • TRFOUT register • U0SR register • U1SR register • U2SR0 register • U2SR1 register • SSUIICSR register • INTSR register	• PIOR0 register • PIOR1 register
XIN/XOUT pin connect	• CM0 register CM05 bit • CM1 register CM13 bit	• CMC register Bits OSCSEL, EXCLK
XCIN/XCOUT pin connect	• PINSR register XCSEL bit • CM0 register CM04 bit	• CMC register Bits OSCSELS, EXCLKS
I/O port input function select	• PINSR register IOINSEL bit	• PMS register
Pull-up control	• PUR0 register • PUR1 register • PUR2 register	• PUxx register
Drive capacity control	• P1DRR register • P2DRR register • DRR0 register • DRR1 register • DRR2 register	N/A
Input threshold control	• VLT0 register • VLT1 register • VLT2 register	• PIMxx register

i = 0 to 6, 8
PMxx: xx = 0 to 8, 10 to 12, 14, 15
Pxx: xx = 0 to 8, 10 to 15
PUxx: xx = 0, 1, 3 to 8, 10 to 12, 14
PIMxx: xx = 0, 1, 3 to 5, 8, 14

Table 2.2 Register Compatibility (2/2)

Item	R8C/36M Group	RL78/G14
Port output mode select	N/A	• POMxx register
Digital I/O or analog I/O select	N/A	• PMCxx register • ADPC register
Through-current protection	N/A	• GDIDIS register

POMxx: xx = 0, 1, 3 to 5, 7, 8, 14
PMCxx: xx = 0, 1, 10, 12, 14

3. Comparison of I/O Ports and Port Functions

3.1 Selecting the Port Direction

3.1.1 R8C/36M Group

In the R8C/36M Group, the PDi register is used to set the input or output mode of ports (i = 0 to 6, 8). Table 3.1 lists the functions of the PDi register.

Table 3.1 PDi Register Function

PDi_j Bit	Function
0	Input mode (functions as an input port)
1	Output mode (functions as an output port)

j: 0 to 7

3.1.2 RL78/G14

In RL78/G14, set the PMm register to specify input or output of ports (m = 0 to 8, 10 to 12, 14, 15). Table 3.2 lists the functions of the PMm register.

Table 3.2 PMm Register Function

PMmn Bit	Function
0	Output mode (output buffer on)
1	Input mode (output buffer off)

n = 0 to 7

3.2 Controlling the Input Threshold

3.2.1 R8C/36M Group

In the R8C/36M Group, the input threshold value can be selected among three voltage levels. The input threshold for all ports can be controlled. Table 3.3 lists the electrical characteristics of the high level input voltage. Table 3.4 lists the electrical characteristics of the low level input voltage.

Table 3.3 High Level Input Voltage Electrical Characteristics

Input Level Selection	Condition	Minimum	Maximum
0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	Vcc
	2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	Vcc
	1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	Vcc
0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	Vcc
	2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	Vcc
	1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	Vcc
0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	Vcc
	2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	Vcc
	1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	Vcc

Table 3.4 Low Level Input Voltage Electrical Characteristics

Input Level Selection	Condition	Minimum	Maximum
0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	0.2 Vcc
	2.7 V ≤ Vcc < 4.0 V	0	0.2 Vcc
	1.8 V ≤ Vcc < 2.7 V	0	0.2 Vcc
0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	0.4 Vcc
	2.7 V ≤ Vcc < 4.0 V	0	0.3 Vcc
	1.8 V ≤ Vcc < 2.7 V	0	0.2 Vcc
0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	0.55 Vcc
	2.7 V ≤ Vcc < 4.0 V	0	0.45 Vcc
	1.8 V ≤ Vcc < 2.7 V	0	0.35 Vcc

3.2.2 RL78/G14

In RL78/G14, the input threshold value can be modified by setting the EV_{DD0} to comply with the power supply of the device connected to the MCU, or setting the PIMm register (m = 0, 1, 3 to 5, 8, 14). The input threshold values of the following ports can be controlled: P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, and P143.

Table 3.5 lists the electrical characteristics of the high level input voltage. Table 3.6 lists the electrical characteristics of the low level input voltage.

Table 3.5 High Level Input Voltage Electrical Characteristics

Condition		Minimum	Maximum
Normal input buffer	1.6 V ≤ EV_{DD0} ≤ 5.5 V	0.8 EV_{DD0}	EV_{DD0}
TTL input buffer	4.0 V ≤ EV_{DD0} ≤ 5.5 V	2.2	EV_{DD0}
	3.3 V ≤ EV_{DD0} < 4.0 V	2.0	EV_{DD0}
	1.6 V ≤ EV_{DD0} < 3.3 V	1.50	EV_{DD0}

Note: $EV_{DD0} = EV_{DD1}$

Table 3.6 Low Level Input Voltage Electrical Characteristics

Condition		Minimum	Maximum
Normal input buffer	1.6 V ≤ EV_{DD0} ≤ 5.5 V	0	0.2 EV_{DD0}
TTL input buffer	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0	0.8
	2.7 V ≤ EV_{DD0} < 4.0 V	0	0.5
	1.6 V ≤ EV_{DD0} < 2.7 V	0	0.32

Note: $EV_{DD0} = EV_{DD1}$

3.3 Multiplexed Pins with Peripheral Functions

3.3.1 Switching between Digital I/O and Analog I/O (RL78/G14 Only)

In RL78/G14, the ADPC register is used to switch between the A/D converter analog input and the digital I/O of ports, and between the D/A converter analog input and the digital I/O of ports.

The following ports are used to switch between the A/D converter analog input and the digital I/O of ports: P20/ANI0, P21/ANI1, P22/ANI2/ANO0, P23/ANI3/ANO1, P24/ANI4 to P27/ANI7, and ANI8/P150 to ANI14/P156.

The following ports are used to switch between the D/A converter analog output and the digital I/O of ports: P22/ANI2/ANO0, and P23/ANI3/ANO1.

As the ADPC register switches pins ANI0 to ANIxx to analog input, careful consideration should be given to which analog I/O pins are used in the user system before setting them (xx: 1 to 14).

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Switch between Analog I/O (A) and Digital I/O (D)													
				ANI14/P156	ANI13/P155	ANI12/P154	ANI11/P153	ANI10/P152	ANI9/P151	ANI8/P150	ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/ANO1/P23	ANI2/ANO0/P22	ANI1/P21	ANI0/P20
0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	1	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A
0	0	1	1	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A
0	1	0	0	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A
0	1	0	1	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A
0	1	1	0	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A
0	1	1	1	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A
1	0	0	0	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A
1	0	0	1	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A
1	0	1	0	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A
1	0	1	1	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A
1	1	0	0	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A
1	1	0	1	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	0	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	1	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Other than above				Do not set.														

3.3.2 Other Peripheral Functions

For details on the differences in multiplexed pins between the R8C/36M Group and RL78/G14, refer to the R8C/36M Group User's Manual: Hardware and RL78/G14 User's Manual: Hardware.

4. Handling Unassigned Pins

4.1 R8C/36M Group

Table 4.1 lists the unassigned pin handling of the R8C/36M Group.

Table 4.1 R8C/36M Group Unassigned Pin Handling

Pin Name	Connection
Ports P0, P1, P2, P3, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6, P8_0 to P8_6	• After setting to input mode, connect each pin to VSS via a pull-down resistor or connect each pin to VCC via a pull-up resistor. • After setting to output mode, leave these pins open.
Port P4_2/VREF	Connect to VCC
$\overline{\text{RESET}}$	Connect to VCC via a pull-up resistor

4.2 RL78/G14

Table 4.2 lists the unassigned pin handling of RL78/G14.

Table 4.2 RL78/G14 Unassigned Pin Handling

Pin Name	Connection
P00 to P06, P10 to P17, P30, P31, P41 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	• Input: Connect these pins independently to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor • Output: Leave open
P20 to P27, P150 to P156	• Input: Connect these pins independently to V_{DD} or V_{SS} • Output: Leave open
P40	• Input: Connect this pin independently to V_{DD} or leave open • Output: Leave open
P130	Leave open
P121 to P124, P137	Connect these pins independently to V_{DD} or V_{SS}
$\overline{\text{RESET}}$	Connect this pin to V_{DD} directly or via a resistor
REGC	Connect this pin to V_{SS} via a capacitor (0.47 to 1µF)

5. Notes

5.1 Notes on Pin Setting in RL78/G14 (Except 100-pin Package)

The P15 pin in RL78/G14 (except 100-pin package) may be multiplexed with other output functions. For details on the multiplexed functions and pin handling, refer to the RL78/G14 User's Manual: Hardware.

6. Reference Documents

User's Manual: Hardware

RL78/G14 User's Manual: Hardware Rev.1.00

R8C/36M Group User's Manual: Hardware Rev.1.00

The latest versions can be downloaded from the Renesas Electronics website.

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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