RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: I2C bus Interface

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Introduction

This application note describes how to provide the serial interface (IICA) of the RL78/G14 with the communication modes equivalent to I^2C bus interface mode of the I^2C bus interface incorporated in the clock synchronous serial interface of the R8C/36M group.

Note that this application note does not cover clock synchronous serial mode of the I^2C bus interface incorporated in the I^2C bus interface of the R8C/36M group. If you are considering migration from clock synchronous serial mode, use 3-wire serial I/O (CSI) mode of the SAU incorporated in the RL78/G14.

Target Device

RL78/G14, R8C/36M Group

When applying the sample program covered in this application note to another microcontroller, modify the program according to the specifications for the target microcontroller and conduct an extensive evaluation of the modified program. For the specifications and electrical characteristics, refer to the relevant hardware manuals and technical updates.

Contents

1. Migration Method from R8C Family to RL78 Family

The following sections describe how to implement I²C bus interface mode of the I²C bus interface of the R8C/36M group by using the serial interface IICA of the RL78/G14.

Table 1.1 shows the operation modes of the I²C bus interface of the R8C/36M group.

Table 1.2 shows the operation modes of the serial interface IICA of the RL78/G14.

Table 1.1 Operation Modes of I²C bus Interface in R8C/36M Group (Summary)

I²C bus Interface in R8C/36M Group	
Operation Mode	Function
I²C bus interface mode	**This mode performs communication based on the I²C bus format.**
Clock synchronous serial mode	This mode performs clocked serial communication.

Table 1.2 Operation Modes of Serial Interface IICA in RL78/G14 (Summary)

Serial Interface IICA in RL78/G14	
Operation Mode	Function
Operation stop mode	This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.
I2C bus mode (multimaster supported)	**This mode performs communication based on the I²C bus format.**
Wakeup mode	The STOP mode can be released by generating an interrupt request signal (INTIICAn) when an extension code from the master device or a local address has been received while in STOP mode.

The I²C bus interface of the R8C/36M group supports I²C bus interface mode and clock synchronous serial mode.

The serial interface IICA of the RL78/G14 has three operation modes: operation stop mode, I²C bus mode (multimaster supported), and wakeup mode.

I²C bus interface mode of the R8C/36M group and I²C bus mode of the RL78/G14 can perform communication based on the I²C bus format. For the specific differences of the communication using the I²C bus interface between RL78/G14 and R8C/36M group, refer to chapter 2. Differences between RL78/G14 and the R8C/36M Group.

The major difference is the method of setting the transfer clock for I²C communication.

With the R8C/36M group, the transfer clock (Hz) is the internal clock selected by the CKS0 to CKS3 bits in the ICCR1 register and IICTCTWI and IICTCHALF bits in the PINSR register, and is output from the SCL pin. For the transfer clock setting for the R8C/36M group, refer to the relevant text in the following hardware manual.

- R8C/36M Group Hardware Manual
  Chapter: I²C Bus Interface
  Section: Common Items for Multiple Modes
  Subsection: Transfer Clock

With the RL78/G14, the transfer clock (bps) is determined by setting the values for controlling the low and high levels of the SCLAn pin signal to the IICWLn and IICWHn registers, respectively.

For the method of calculating the optimal values to be set to the IICWLn and IICWHn registers for the transfer clock (bps) used for communication, refer to the relevant text in the following hardware manual.

- RL78/G14 Hardware Manual
  Chapter: Serial Interface IICA
  - Section: Registers for Controlling Serial Interface IICA
    Subsection: IICA low-level width setting register n (IICWLn) and
    IICA high-level width setting register n (IICWHn)

  - Section: I²C Bus Mode Functions
    Subsection: Setting transfer clock by using IICWLn and IICWHn registers

Program creation for the system using I²C communication depends on the method of controlling the devices connected to the RL78/G14; refer to the following documents to create the suitable program for your system.

- Related application notes
  Refer to chapter 3. Related Application Note

- RL78/G14 User's Manual: Hardware
  Chapter: Serial Interface IICA
  Section: I²C Bus Definitions and Control Methods
  Subsection: Communication operations

2. Differences between RL78/G14 and the R8C/36M Group

This chapter describes the differences of the communication using the I²C bus interface (I²C communication) between the RL78/G14 and R8C/36M group.

2.1 Differences between I²C bus Interface and serial Interface IICA

Table 2.1 shows the differences between I²C bus interface mode of the R8C/36M group and I²C bus mode of the RL78/G14.

Table 2.1 Differences between I²C bus interface mode of R8C/36M group and I²C bus mode of RL78/G14

Item	R8C/36M Group I²C bus Interface I²C bus interface mode	RL78/G14 serial Interface IICA I²C bus mode
Communication formats	I²C bus format	I²C bus format
I/O pins	SCL(I/O) Serial clock I/O pin SDA(I/O) Serial data I/O pin	SCLA0, SCLA1 Serial clock I/O pins of serial interface IICA0, IICA1 - SDAA0, SDAA1 Serial data I/O pins of serial interface IICA0, IICA1 (Note1)
Transfer clock	Internal clock (Master mode) / External clock (Slave mode)	Internal clock (Master mode) / External clock (Slave mode)
Interrupt generation timing	Upon 'transmit data empty' (including when slave address matches)	- Falling edge of eighth or ninth clock of the serial clock (set by the WTIMn bit) (Note2) - Interrupt request generated when a stop condition is detected (set by the SPIEn bit)
	Upon 'end of transmission' Upon 'receive data full' (including when slave address matches)	
	Upon arbitration lost detection	
	Upon NACK detection	
	Upon stop condition detection	
ACK/NACK detection	Enabled	Enabled
Arbitration lost detection	Enabled	Enabled
Selection of output level for the acknowledge signal during reception	Enabled	Enabled
Selection of digital delay value for the SDA pin	Enabled	—
Noise cancel function	Noise canceller is provided.	Use of digital filter function can be selected.

—: There is no corresponding function.

Note1. 80, 100-pin products only. SCLA1 and SDAA1 are provided for 80- and 100-pin products only.

Note2. When slave operation, the received address does not match the contents of the slave address register and extension code is not received, neither interrupt nor a wait occurs.

2.2 Comparison between Registers

Table 2.2, Table 2.3, and Table 2.4 compare the registers for the I²C bus interface of the R8C/36M group to the corresponding registers for the IICA of the RL78/G14.

Table 2.2 Comparison between Registers (1)

Setting Items	R8C/36M Group I²C bus Interface I²C bus interface mode	RL78/G14 serial Interface IICA I²C bus mode
Enabling clock supply to the peripheral hardware	- MSTCR register MSTIIC bit	- PER0 register IICA0EN bit, IICA1EN bit (Note1)
Communication mode (Selection of I²C bus interface mode)	- SSUIICSR register IICSEL bit - SAR register FS bit	—
Operation stop mode	- ICCR1 register ICE bit (When ICE = 0 (stopped), SCL and SDA pins function as ports.)	- IICCTLn0 register IICEn bit (When IICEn = 0 (stopped), SCLA0 and SDAA0 pins output low level (fixed). (Note2)
Wakeup mode	—	- IICCTLn1 register WUPn bit
Operation mode switching (transfer rate switching)	—	- IICCTLn1 register SMCn bit
Bit rate	Internal clock setting in master mode - ICCR1 register CKS3 to CKS0 bits - PINSR register IICTCTWI and IICTCHALF bits	- IICWLn register - IICWHn register
Transmit buffer	- ICDRT register	- IICAn register
Receive buffer	- ICDRR register	
IIC bus shift register	- ICDRS register	
Slave address register	- SAR register	- SVAn register Upper 7 bits (bit 0 is fixed to 0)
Count source selection	f1 only	- CKC register CSS, MCM0 bit - IICCTLn1 register PRSn bit
Selection of wait insertion in master mode	- ICMR register WAIT bit (Selects whether or not to insert waits.)	— (Waits automatically generated according to the WTIMn bit setting in the IICCTLn0 register.)

—: There is no corresponding register.
IICA1 is provided for 80- and 100-pin products only.
n = 0 or 1 (n = 1 is available for 80- and 100-pin products only.)
Note 1. For 80- and 100-pin products only.
Note 2. Set PM60, PM61, P60, and P61 to 0 to use the serial interface IICA.

Table 2.3 Comparison between Registers (2)

Setting Items	R8C/36M Group	RL78/G14
Selection of digital delay value for SDA pin	- PINSR register SDADLY1 bit, SDADLY0 bit	—
Selection of MSB or LSB first (data transfer direction)	- ICMR register MLS bit	— (Fixed to MSB first)
Selection of master or slave mode	- ICCR1 register MST bit	— (Master communication state is entered when a start condition (ST) is detected after ST is generated. Slave state is entered when a match of the slave address is detected.)
Selection of transmit or receive mode	- ICCR1 register TRS bit	—
Enabling transmit interrupt (Transmit data empty interrupt)	- ICIER register TIE bit	—
Transmit data empty flag	- ICSR register TDRE bit	—
Enabling transmit end interrupt	- ICIER register TEIE bit	- MK1L register IICAMK0 bit - MK2H register IICAMK1 bit (Note[1]) - IICCTLn0 register WTIMn bit (Sets INTIICAn generation timing)
Transmit end flag	- ICSR register TEND bit	—
Enabling receive interrupt	- ICIER register RIE bit	- MK1L register IICAMK0 bit - MK2H register IICAMK1 bit (Note[1]) - IICCTLn0 register WTIMn bit (Sets INTIICAn generation timing)
Receive data register full flag	- ICSR register RDRF bit	—
Selection of receive operation continuation after 1-byte data reception	- ICCR1 register RCVD bit	—
Selection of acknowledge output level in receive mode	- ICIER register ACKBT bit	- IICCTLn0 register ACKEn bit
Selection of operation on detection of acknowledge bit	- ICIER register ACKE bit	—
ACK/NACK detection	- ICIER register ACKBR bit	- IICSn register ACKDn bit

—: There is no corresponding register.
IICA1 is provided for 80- and 100-pin products only.
n = 0 or 1(n = 1 is available for 80- and 100-pin products only.)
Note 1. For 80- and 100-pin products only.

Table 2.4 Comparison between Registers (3)

Setting Items	R8C/36M Group	RL78/G14
Start condition generation	- ICCR2 register SCP bit, BBSY bit	- IICCTLn0 register STTn bit
Stop condition generation	- ICCR2 register SCP bit, BBSY bit	- IICCTLn0 register SPTn bit
Bus status (released/occupied) check	- ICCR2 register BBSY bit	- IICFn register IICBSYn bit
Enabling stop condition detection interrupt	- ICIER register STIE bit	- MK1L register IICAMK0 bit - MK2H register IICAMK1 bit (Note1) - IICCTLn0 register SPIEn bit
Stop condition detection flag	- ICSR register STOP bit	- IICSn register SPDn bit
Pin selection	- SSUIICSR register IICSEL bit - SAR register FS bit - ICCR1 register ICE bit	- IICCTLn0 register IICEn bit - PM6 register PM60, PM61 bit - P6 register P60, P61 bit (Note2)
SCL pin status (L/H) check	- ICCR2 register SCLO bit	- IICCTLn1 register CLDn bit
SDA pin status (L/H) check	- ICCR2 register SDAO bit	- IICCTLn1 register DADn bit
SDA pin output value control	- ICCR2 register SDAOP bit, SDAO bit	—
I^2C bus control block reset	- ICCR2 register IICRST bit (Port and register settings are not reset.)	- PER0 register IICAnEN bit (The serial interface IICA control registers are reset to the initial values.)
Enabling NACK receive interrupt	- ICIER register NAKIE bit	—
No acknowledge detection flag	- ICSR register NACKF bit	—
Arbitration lost flag	- ICSR register AL bit	- IICSn register ALDn bit
Slave address recognition flag	- ICSR register AAS bit	- IICSn register COIn bit
General call address recognition flag	- ICSR register ADZ bit	- IICSn register EXCn bit

—: There is no corresponding register.

IICA1 is provided for 80- and 100-pin products only.

n = 0 or 1 (n = 1 is available for 80- and 100-pin products only.)

Note 1. For 80- and 100-pin products only.

Note 2. Set PM60, PM61 (I/O mode), P60, and P61 (output latch) to 0 to use the serial interface IICA. Before switching to output mode (PM60 and PM61 = 0), set the IICEn bit to 1.

3. Related Application Note

- RL78/G12 Serial Interface IICA (for Master Transmission/Reception) CC-RL (R01AN2987E)
- RL78/G12 Serial Interface IICA (for Slave Transmission/Reception) CC-RL (R01AN2988E)
- RL78/G13 Serial Interface IICA (for Master Transmission/Reception) CC-RL (R01AN2759E)
- RL78/G13 Serial Interface IICA (for Slave Transmission/Reception) CC-RL (R01AN2760E)

4. Documents for Reference

User's Manual:

- RL78/G14 User's Manual: Hardware (R01UH0186)
- R8C/36M Group User's Manual: Hardware (R01UH0259)

The latest versions can be downloaded from the Renesas Electronics website.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 8, 2018	-	First edition issued
1.10	Jun. 9, 2020		Fixed the interrupt generation timing on RL78/G14

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1. Handling of Unused Pins

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   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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