RL78/G14, H8/36109

Migration Guide from H8 to RL78: Watchdog Timer

Introduction

This application note describes how to migrate the Watchdog Timer of the H8/36109 to the Watchdog Timer of the RL78/G14.

Target Device

RL78/G14, H8/36109

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Summary of Differences between Functions

Table 1.1 summarizes the differences between Watchdog Timer of the H8/36109 and the RL78/G14.

Table 1.1 Differences

Item	H8/36109	RL78/G14
Overflow Time	Depends on the setting value of TCWD register.	$2^6/f_{IL}$, $2^7/f_{IL}$, $2^8/f_{IL}$, $2^9/f_{IL}$, $2^{11}/f_{IL}$, $2^{13}/f_{IL}$, $2^{14}/f_{IL}$, $2^{16}/f_{IL}$
Count clock	φ/64 - φ/8192, WDT dedicated internal oscillator (Note1)	f_{IL} (Note2)
Count mode	Count up	Count up
Operation after release from reset	Operable	Can choose to operate or stop.
Window Open Period	None	Yes

Note1. H8/36109: Internal oscillator overflow time: t_{OVF} = 0.2s (Min) - 0.4s (Typ)

Note2. RL78/G14: f_{IL} = TYP. 15kHz (15kHz±15%)

The watchdog timer in the H8/36109 is provided with an 8-bit counter. After the reset state is released, TCWD starts counting up. When the TCWD count value overflows H'FF, an internal reset signal is generated. The internal reset signal is output for a period of 256 φRC clock cycles. As TCWD is a writable counter, it starts counting from the value set in TCWD. An overflow period in the range of 1 to 256 input clock cycles can therefore be set, according to the TCWD set value. When the watchdog timer is not used, stop TCWD counting by writing 0 to B2WI and WDON simultaneously while the TCSRWE bit in TCSRWD is set to 1.

The counting operation of the watchdog timer in the RL78/G14 is set by the option byte (000C0H). The watchdog timer operates with the low-speed on-chip oscillator clock (f_{IL}) to detect an inadvertent program loop. It generates an internal reset signal upon detecting an inadvertent program loop. A window open period can be specified in the watchdog timer. During the window open period, writing "ACH" to the WDTE register causes the watchdog timer to clear the counter and restart counting. During the window close period, writing "ACH" to the WDTE register is detected as an abnormality. In addition, an interval interrupt can be generated when 75% of the overflow time + 1/2 f_{IL} is reached.

Figure 1.1 shows the case where the window open period for the watchdog timer is set to 75% of the overflow time.

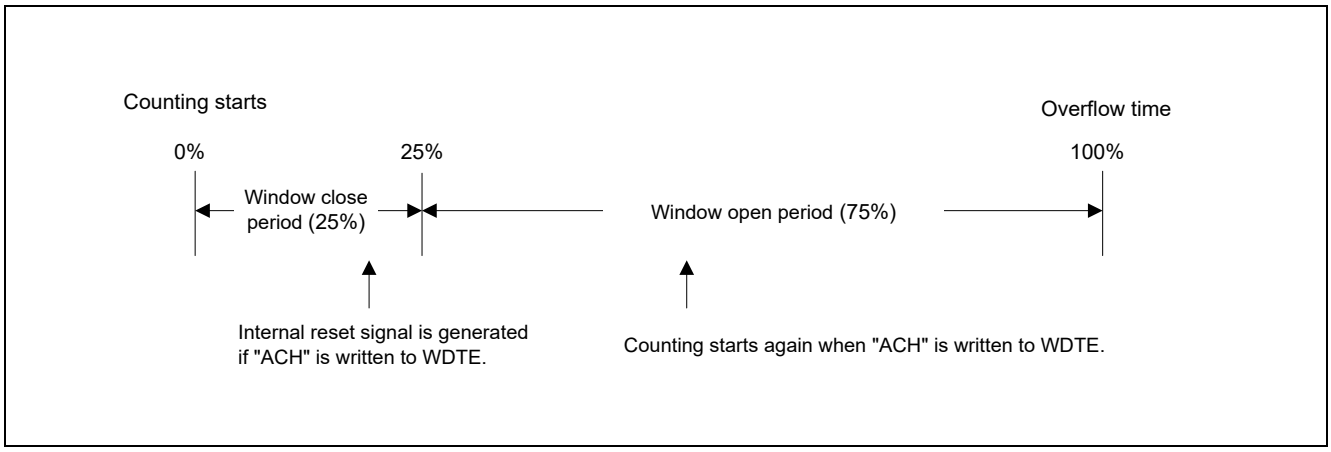

Figure 1.1 If the window open period of watchdog timer is 75%

2. Comparison between Registers

Table 2.1 compare the registers for the H8/36109 Watchdog Timer and the registers for the RL78/G14 Watchdog Timer.

Table 2.1 Comparison between Registers

Item	H8/36109 Watchdog Timer	RL78/G14 Watchdog Timer
Control of Watchdog Timer input clock supply	MSTCR1 register MSTWD bit	None
Timer Control/Status Register	TCSRWD register	None
Bit 6 Write Inhibit	TCSRWD register B6WI bit	None
Timer Counter WD Write Enable	TCSRWD register TCWE bit	None
Bit 4 Write Inhibit	TCSRWD register B4WI bit	None
Timer Control/Status Register WD Write Enable	TCSRWD register TCSRWE bit	None
Bit 2 Write Inhibit	TCSRWD register B2WI bit	None
Watchdog Timer On	TCSRWD register WDON bit	None
Bit 0 Write Inhibit	TCSRWD register B0WI bit	None
Watchdog Timer Reset	TCSRWD register WRST bit	None
Timer Counter	TCWD register	None
Timer Mode Register	TMWD register	None
Clock Select	TMWD register CKS3 - CKS0 bit	None
Watchdog timer enable register	None	WDTE register
Option Byte	None	Option Byte (Address: 000C0H)
Watchdog timer interval interrupt	None	Option Byte (Address: 000C0H) bit7 (WDTINT)
Window open period	None	Option Byte (Address: 000C0H) bit 6, 5 (WINDOW1, WINDOW0)
Controlling counter operation of watchdog timer	None	Option Byte (Address: 000C0H) bit 4 (WDTON)
Overflow time of watchdog timer	None	Option Byte (Address: 000C0H) bit 3-1 (WDCS2- WDCS0)
Controlling counter operation of watchdog timer (in HALT/STOP mode)	None	Option Byte (Address: 000C0H) bit 0 (WDSTBYON)

3. Documents for Reference

User's Manual:

- RL78/G14 User's Manual: Hardware (R01UH0186)
- H8/36109 Group User's Manual: Hardware (R01UH0294)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.25, 2020	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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