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RL78/G14

A/D conversion using DTC realizes the low-power consumption of the system CC-RL

Abstract

This document describes low-power consumption of the system using DTC, Timer RJ, 12-bit interval timer, A/D converter (SNOOZE mode).

Products

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This document describes low-power consumption of the system using DTC, Timer RJ, 12-bit interval timer (12-bit IT), A/D converter (SNOOZE mode).

DTC performs ON/OFF control of a sensor power source, and stores the A/D conversion result. Timer RJ generates the on/off control timing of the sensor power supply. 12-bit IT generates the start timing of the A/D conversion. Furthermore, the low-power consumption of the system realizes by using the SNOOZE mode function of the A/D converter.

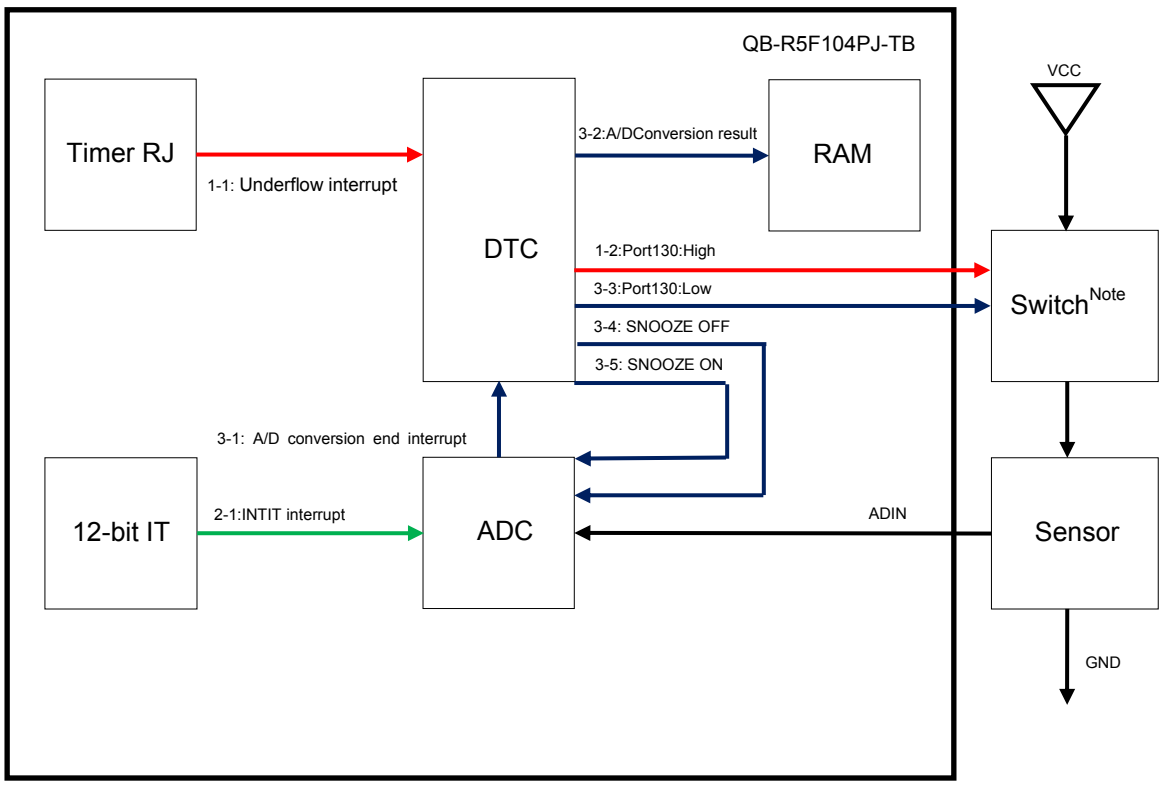
In this application note, a sensor power supply is turned on at intervals of 100 ms. The A/D conversion is performed 4 times at the ON period of a sensor power supply. When the fourth A/D conversion is completed, turn off a sensor power supply. After that, this processing is repeated.

- The Timer RJ generates timer interrupt every 100 ms, and activates DTC.
- DTC makes a sensor power supply turn on by making P130 High level.
- 12-bit IT measures the sensor stable waiting time (10 ms) after a sensor power supply injection only the first time. After the second, according to the control cycle of a sensor power supply (100 ms), the interrupt (INTIT) is generated, and it makes the A/D conversion start.
- When A/D conversion end interrupt occurs, DTC makes a sensor power supply turn off by making P130 Low level. In addition, DTC transfers A/D conversionresult to RAM and performs the reset of the SNOOZE mode.

Table 1.1 lists the Peripheral Functions and Their Applications, and Figure 1.1 shows the Operation Overview.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Timer RJ	Period count of the power supply to a sensor (100 ms)
DTC	The following is carried out by interrupt of the Timer RJ. ・P130 to a high-level output (power supply start to a sensor) The following is carried out by A/D conversion end interrupt. ・A/D conversion result is transferred to RAM ・P130 to a low-level output (power supply stop to a sensor) ・Clear AWC（Stop SNOOZE） ・Set AWC（Switch into SNOOZE mode）
P130	Sensor power supply control (ON/OFF)
12-bit IT	Count of the stable waiting time of the sensor(only as for the first time 10ms) Count of the period of the A/D conversion (100ms)
ADC	Convert the analog signal input level of the P22/ANI2 pin



Note The switches in the figure mentioned above will be OFF by low-level input (power supply stop to a sensor), and will be ON by high-level input (power supply start to a sensor).

Figure1.1 Outline of operation

1-1：DTC is started by underflow interruption of the Timer RJ.

1-2：P130 is set as a high level output by DTC.

2-1：A/D conversion is started by interruption of 12 bit-IT.

3-1：DTC is started by A/D conversion end interrupt.

3-2：A/D conversion result is transferred to RAM by DTC.

3-3：P130 is set as a Low output by DTC.

3-4：You set up for "Do not use SNOOZE mode function" by DTC.

3-5：You set up for "Use SNOOZE mode function" by DTC.

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 **Operation Confirmation Conditions**

Item	Contents
MCU used	RL78/G14 (R5F104PJAFB)
Operating frequencies	● High-speed on-chip oscillator (HOCO) clock : 8MHz ● CPU/peripheral hardware clock : 8MHz ● 12bit-IT operation clock (f_{sub}):32.768kHz(standard)
Operating voltage	5.0V (operation enabled from 2.9 to 5.5 V) LVD operation (V_{LVD}): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment (CS+)	Renesas Electronics Corporation CS+ V3.01.00
C compiler (CS+)	Renesas Electronics Corporation CC-RL V1.01.00
Integrated development environment (e^2 studio)	Renesas Electronics Corporation e^2 studio V4.0.0.26
C compiler (e^2 studio)	Renesas Electronics Corporation CC-RL V1.0.0.26
Board used	RL78/G14 CPU Board (QB-R5F104PJ-TB)

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

RL78/G13 Initialization（R01AN2575E）

RL78/G13 A/D Converter（R01AN2581E）

RL78/G14 How to Use the DTC for the RL78/G14 (R01AN0861E）

RL78/G14 Transferring A/D Conversion Result Using the DTC (R01AN2574E）

4. Hardware

4.1 Hardware Configuration

Figure 4.1 shows the Hardware Configuration used in this document.

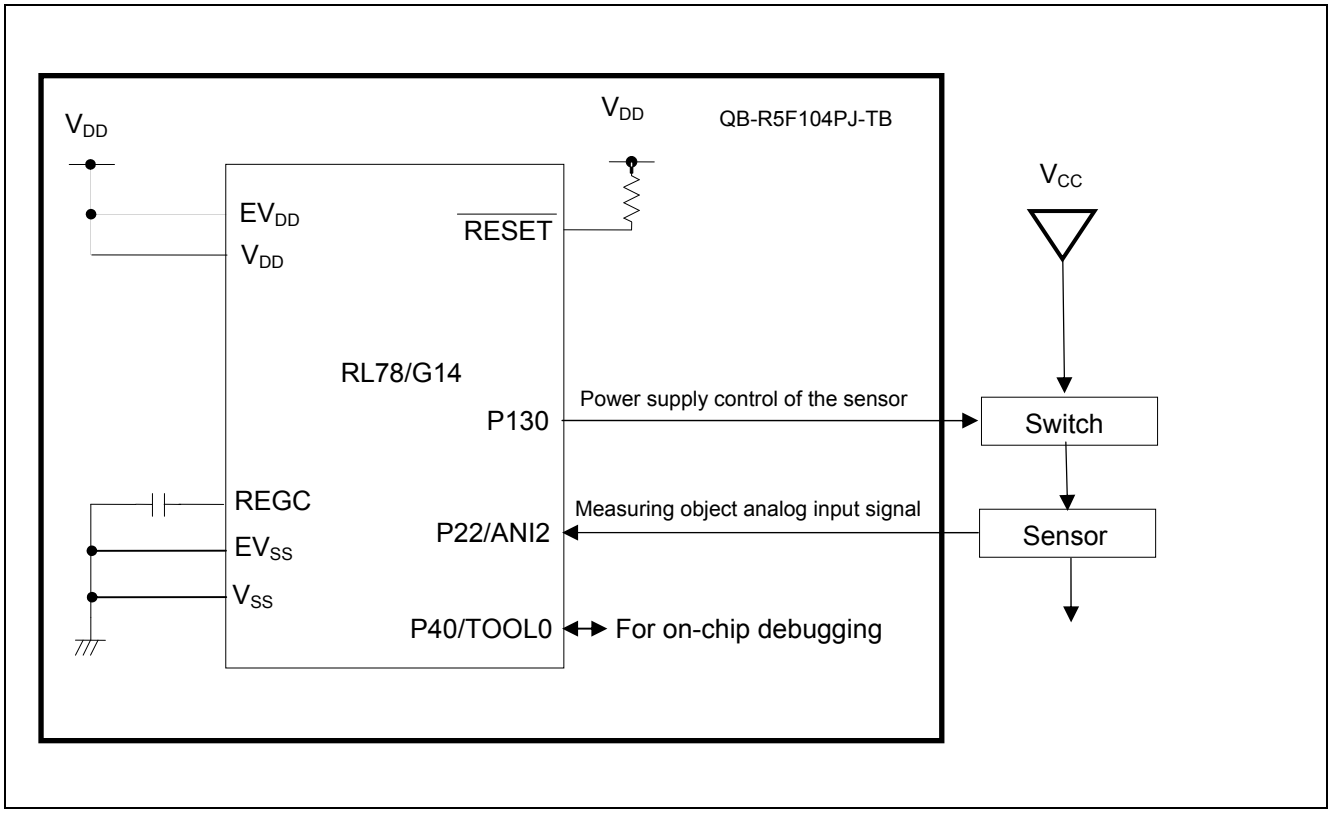


Figure 4.1 Hardware Configuration

Notes:

1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics. Connect input-only ports independently to V_{DD} or V_{SS} via resistors.
2. Connect pins with names that begin with EV_{SS} to V_{SS}, and pins with names that begin with EV_{DD} to V_{DD}.
3. Make sure to set V_{DD} greater than the detection voltage (V_{LVD}) specified by the LVD.

4.2 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P22/ANI2	Input	A/D converter input
P130	Output	Power supply control of the sensor High : Power ON Low : Power OFF

5. Software

5.1 Operation Overview

This document describes low-power consumption of the system using DTC, Timer RJ, 12-bit IT, A/D converter (SNOOZE mode).

DTC performs ON/OFF control of a sensor power source, and stores the A/D conversion result.
Timer RJ generates the on/off control timing of the sensor power supply. 12-bit IT generates the start timing of the A/D conversion. Furthermore, the low-power consumption of the system realizes by using the SNOOZE mode function of the A/D converter.

In this application note, a sensor power supply is turned on at intervals of 100 ms. The A/D conversion is performed 4 times at the ON period of a sensor power supply. When the fourth A/D conversion is completed, turn off a sensor power supply. After that, this processing is repeated.

- The Timer RJ generates timer interrupt every 100 ms, and activates DTC.
- DTC makes a sensor power supply turn on by making P130 High level.
- 12-bit IT measures the sensor stable waiting time (10 ms) after a sensor power supply injection only the first time. After the second, according to the control cycle of a sensor power supply (100 ms), the interrupt (INTIT) is generated, and it makes the A/D conversion start.
- When A/D conversion end interrupt occurs, DTC makes a sensor power supply turn off by making P130 Low level. In addition, DTC transfers A/D conversionresult to RAM and performs the reset of the SNOOZE mode.

It indicates to following (1)～(21) for details.

(1) Set the I/O ports.

<Setup conditions>

- Set P75 and P76 to a high-level output and turn off LED1, LED2.
- Set P130 to a low-level output and switch off the sensor.

(2) Initialize the A/D converter.

< Setup conditions >

- Pin P22/ANI2 is used for the analog input.
- A/D conversion channel selection mode is set to select mode.
- A/D conversion operation mode is set to one-shot conversion mode.
- A/D conversion is started using the hardware trigger wait mode.
- Set interrupt signal of the 12-bit IT (INTIT) to a hardware trigger signal.

(3) Initialize the 12-bit IT.

< Setup conditions >

- Set 100ms for the interval time.

(4) Initialize the Timer RJ.

< Setup conditions >

- Use timer mode for the operation mode of Timer RJ.
- Set 100ms for the timer value.

(5) Initialize the DTC.

< Setup conditions >

- DTC0(transfer data of 0xFE900 to P13 register)
  - Transfer source address: 0xE900
  - Transfer destination address: 0xFF0D
  - Set the data length to 8 bits
  - Chain transfer disabled
  - DTC Activation Sources: Timer RJ underflow
  - Number of data transfers: 1
  - Set repeat mode
  - Set repeat mode interrupts disabled.
- DTC1(transfer data of 0xEA00 - 0EA07 from ADCR register)
  - Transfer source address: 0xEA00
  - Transfer destination address: 0xEA00 - 0EA07
  - Set the data length to 16 bits
  - Chain transfer enabled
  - DTC Activation Sources: A/D conversion end
  - Number of data transfers: 4
  - Set repeat mode
  - Set repeat mode interrupts enabled
- DTC2 (transfer data of 0xFE901 to P13 register)
  - Transfer source address: 0xE901
  - Transfer destination address: 0xFF0D
  - Set the data length to 8 bits
  - Chain transfer enabled
  - DTC Activation Sources: A/D conversion end
  - Number of data transfers: 4
  - Set normal mode

- DTC3 (transfer data of 0xFE901 to ADM2 register)
  - Transfer source address: 0xE901
  - Transfer destination address: 0x0010
  - Set the data length to 8 bits
  - Chain transfer enabled
  - DTC Activation Sources: A/D conversion end
  - Number of data transfers: 4
  - Set normal mode

- DTC4 (transfer data of 0xFE902 to ADM2 register)
  - Transfer source address: 0xE902
  - Transfer destination address: 0x0010
  - Set the data length to 8 bits
  - Chain transfer disabled
  - DTC Activation Sources: A/D conversion end
  - Number of data transfers: 4
  - Set normal mode

(6) Initialize main processing.

< Setup conditions >

- Initialize variables
  - Set "0x0000" in variable (result_buffer[0-3])
  - Set "0x01" (P130 = High) in variable (g_p130_high)
  - Set "0x00" (P130 = Low) in variable (g_p130_low)
  - Set "0x04" (use SNOOZE mode function) in variable (snooze_on)

(7) Start DTCD0.

- Set "1" (activation enable) in DTCEN42 bits of DTCEN4 resister

(8) Start count of Timer RJ.

- Set "1"(start count) in the TSTART bit of the TRJCR0 register
  - An underflow interrupt of Timer RJ occurs every 100ms and DTC starts and transfers data (1byte) of the 0xFE900 to 0xFFF0D (P13 register).

(9) Start the count of 12bit-IT.

- Set "0"(interrupt enable) in the ITMK bit of the MK1H register
- Set "1"(start count) in the RINTE bit of the ITMC register, and set "147H" (interval time(10ms)) in the ITCMP 11 - ITCMP 0 bits

(10) Switch into HALT mode.

(11) An interrupt of 12-bit IT occurs and it returns from HALT mode.

(12) Stop the count of 12 bit-IT.

< Setup conditions >

- Set "1" (interrupt enable) in ITMK bits of MK1H resister
- Set "0"(stop count) in the RINTE bit of the ITMC register, and set "000H" in the ITCMP 11 - ITCMP 0 bits
- Set "0" (clear an interrupt request flag) in ITIF bits of IF1H resister

(13) Start DTCD1.

- Set "1" (activation enable) in DTCEN15bits of DTCEN1 resister

(14) Make an A/D converter into SNOOZE mode.

< Setup conditions >

- Set "1" (use SNOOZE mode) in the AWC bit of the ADM2 register
- Set "0" (unmask interrupt) ADMK bit of the MK1H register
- Set "0" (clear an interrupt request flag) in ADIF bits of IF1H resister

(15) Start the count of 12bit-IT again (Period count of the A/D conversion).

< Setup conditions >

- Set "1"(start count) in the RINTE bit of the ITMC register, and set "CCCH" (interval time(100ms)) in the ITCMP 11 - ITCMP 0 bits

(16) Switch into STOP mode.

(17) An interrupt of the 12-bit IT is generated and starts A/D conversion with SNOOZE mode.

(18) A/D conversion end interrupt is generated and DTC starts and starts the transfer of data. DTC performs one time of following a series of transfer here.

- The data (2 bytes) of a 0xFFF1E address (ADCR register) is transferred to RAM. The transfer destination address changes with the number of times of the A/D conversion

  The destination address of an A/D conversion result.

  The 1st time (After DTC initial setting): 0xEA00 (variable: get_adcr[0])

  The 2nd time (After DTC initial setting): 0xEA02 (variable: get_adcr[1])

  The 3rd time (After DTC initial setting): 0xEA04 (variable: get_adcr[2])

  The 4th time (After DTC initial setting): 0xEA06 (variable: get_adcr[3])
- Transfer data (1byte) of the 0xFE901 to 0xFFF0D (P13 register)
- Transfer data (1byte) of the 0xFE901 to 0xF0010 (ADM2 register)
- Transfer data (1byte) of the 0xFE902 to 0xF0010 (ADM2 register)

(19) After transfer completion of DTC, it returns to STOP mode from SNOOZE mode. And after that, repeat (16) - (18) 3 times.

(20) After transfer of the A/D conversion result by 4th DTC is completed, perform the following processing.

- Clear a Timer RJ underflow flag.
  - Set "0"(no underflow) in the TUNDF bit of the TRJCR0 register
- A/D conversion result reading
  - Shift the variable (get_adcr[0-3]) that transferred to RAM in DTC to the 6 bits right.
- Clear an interrupt request flag of A/D converter
  - Set "0"(clear an interrupt request flag) in the ADIF bit of the IF1H register
- Reboot of DTC (After the completion of DTC starting, it will be in startup halt state and the number of start is set as 0)
  - Set "1" (activation enable) in DTCEN15 bits of DTCEN1 resister
  - Set "4" (the number of start) in DTCCT2- DTCCT4 resister

(21) After that repeat (16) - (20)

Figure 5.1 shows the Time chart.

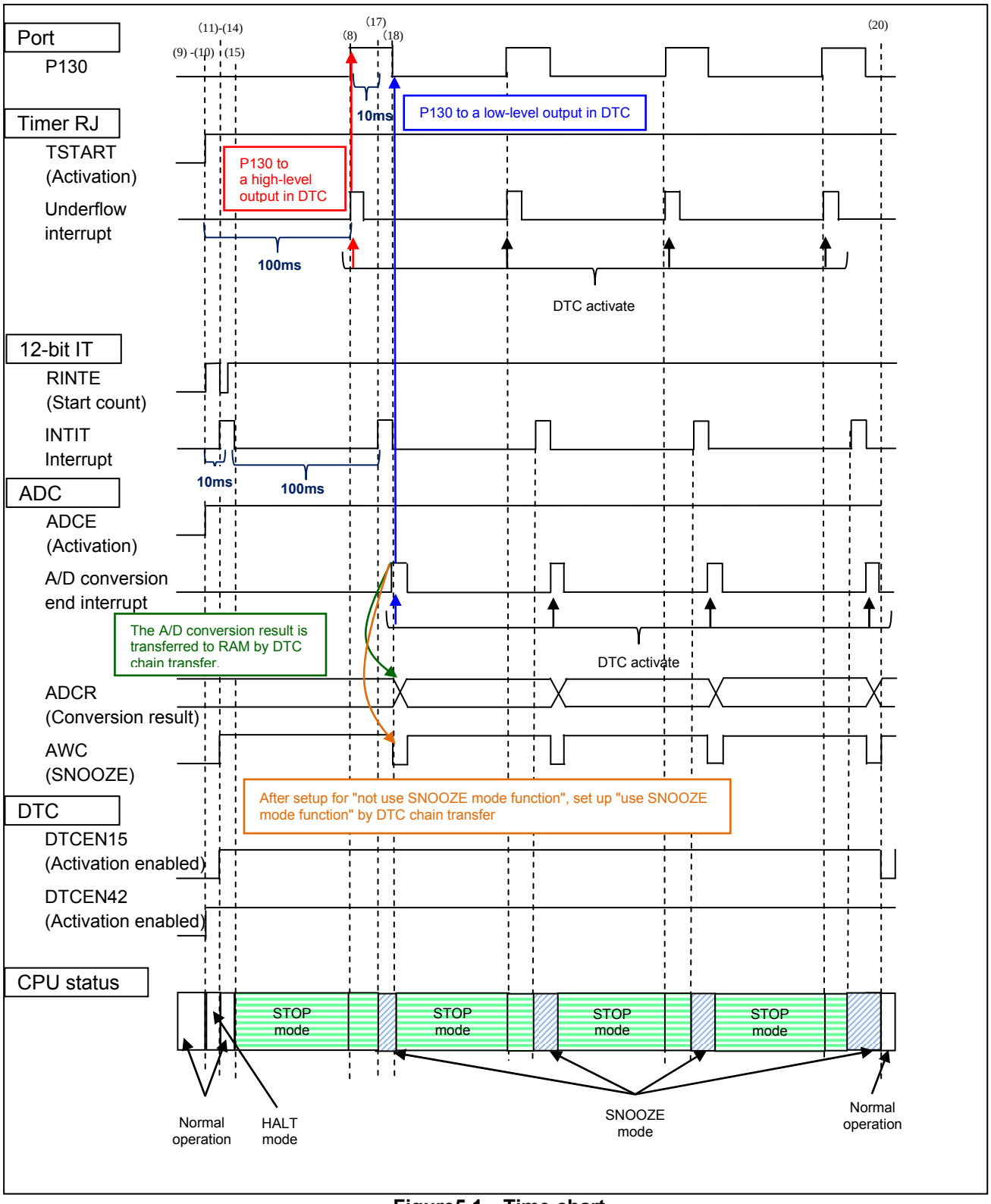


Figure5.1 Time chart

5.2 Option Byte Settings

Table 5.1 lists the Option Byte Settings.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	10101010B	LS mode, HOCO: 8 MHz
000C3H/010C3H	10000100B	On-chip debug enabled Erases data of flash memory in case of failures in authenticating on-chip debug security ID.

5.3 List of Constants

Table 5.2 lists the constant that is used in this sample program

Table 5.2 Constants for the Sample Program

Constant	Value	Description
MAX_BUFFER	4	Buffer size for A/D conversion result storage

5.4 List of Variables

Table 5.3 lists the global variables that are used by this sample program.

Table 5.3 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	p130_high	Set value of P130(High)	R_MAIN_UserInit ()
uint8_t	p130_low	Set value of P130(Low)	R_MAIN_UserInit ()
uint8_t	snooze_on	Set value of AWC (use SNOOZE mode function)	R_MAIN_UserInit ()
uint16_t	get_adcr[]	A/D conversion result value	main () R_MAIN_UserInit ()
uint16_t	result_buffer[]	The value carried out 6 bit shifts of the A/D conversion result	main () R_MAIN_UserInit ()
uint8_t	buffer_count	Buffer number to use	main () R_MAIN_UserInit ()

5.5 Functions

Table 5.4 lists the Functions

Table 5.4 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	CPU initial setting
R_PORT_Create	Initial setting of I/O ports
R_ADC_Create	Initial setting of A/D converter
R_IT_Create	Initial setting of 12-bit IT
R_TMR_RJ0_Create	Initial setting of Timer RJ
R_DTC_Create	Initial setting of DTC
main	Main processing
R_MAIN_UserInit	Initial setting of main
R_DTCD0_Start	DTC0 activation
R_DTCD1_Start	DTC1 activation
R_ADC_Set_SnoozeOn	Permission to use SNOOZE mode function of A/D conversion
R_ADC_Start	Start A/D conversion
R_DTCD_Set_Count	Set count number of times of DTC

5.6 Function Specifications

The following tables list the sample code function specifications.

[Function Name] hdwinit

Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_Systeminit

Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_CGC_Create

Outline	CPU initial setting
Header	r_cg_cgc.h
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_PORT_Create

Outline	Initial setting of I/O ports
Header	r_cg_port.h
Declaration	void R_PORT_Create(void)
Description	Perform the initial setting to use the I/O ports.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_ADC_Create

Outline	Initial setting of A/D converter
Header	r_cg_adc.h
Declaration	void R_ADC_Create(void)
Description	Perform the initial setting to use the A/D converter in hardware trigger wait mode (select mode and one-shot conversion mode) .
Argument	None
Return Value	None
Remarks	None

[Function Name] R_IT_Create

Outline	Initial setting of 12-bit IT
Header	r_cg_it.h
Declaration	void R_IT_Create(void)
Description	Perform the initial setting to use the 12-bit IT.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_TMR_RJ0_Create

Outline	Initial setting of Timer RJ
Header	r_cg_timer.h
Declaration	void R_TMR_RJ0_Create(void)
Description	Perform the initial setting to use the Timer RJ in timer mode.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_DTC_Create

Outline	Initial setting of DTC
Header	r_cg_dtc.h
Declaration	void R_DTC_Create(void)
Description	Perform the initial setting to use the DTC.
Argument	None
Return Value	None
Remarks	None

[Function Name] main

Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_MAIN_UserInit

Outline	Initial setting of Main
Header	None
Declaration	void R_MAIN_UserInit(void)
Description	Perform the initial setting main.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_DTCD0_Start

Outline	DTC0 activation
Header	r_cg_dtc.h
Declaration	void R_DTCD0_Start(void)
Description	Enable DTC0 activation.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_DTCD1_Start

Outline	DTC1 activation
Header	r_cg_dtc.h
Declaration	void R_DTCD1_Start(void)
Description	Enable DTC1 activation.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_ADC_Set_SnoozeOn

Outline	Start the SNOOZE mode function of A/D conversion
Header	r_cg_adc.h
Declaration	void R_ADC_Set_SnoozeOn(void)
Description	Start the SNOOZE mode function of A/D conversion.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_ADC_Start

Outline	Start A/D conversion
Header	r_cg_adc.h
Declaration	void R_ADC_Start(void)
Description	Perform A/D conversion.
Argument	None
Return Value	None
Remarks	None

[Function Name] R_DTCD_Set_Count

Outline	Set count number of times of DTC
Header	r_cg_dtc.h
Declaration	void R_DTCD_Set_Count(void)
Description	Set count number of times of DTC.
Argument	None
Return Value	None
Remarks	None

5.7 Flowcharts

Figure 5.2 shows the overall flowchart of the sample program described in this application note.

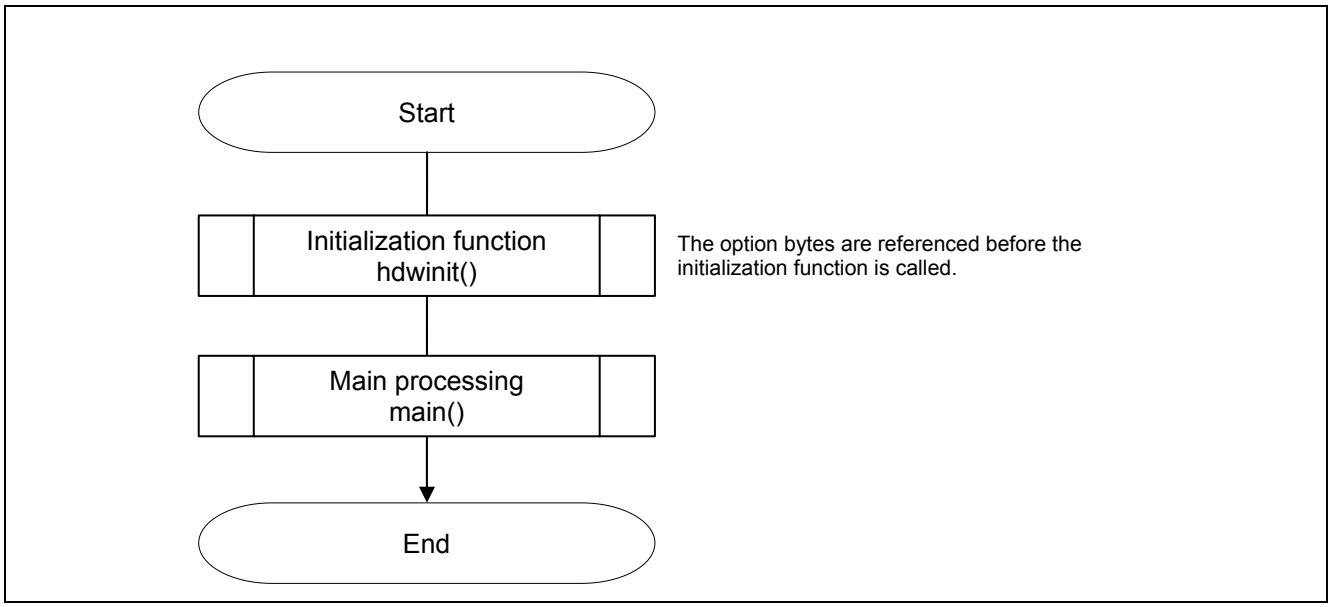


Figure 5.2 Overall Flowchart

5.7.1 Initial Setting

Figure 5.3 shows the initialization function.

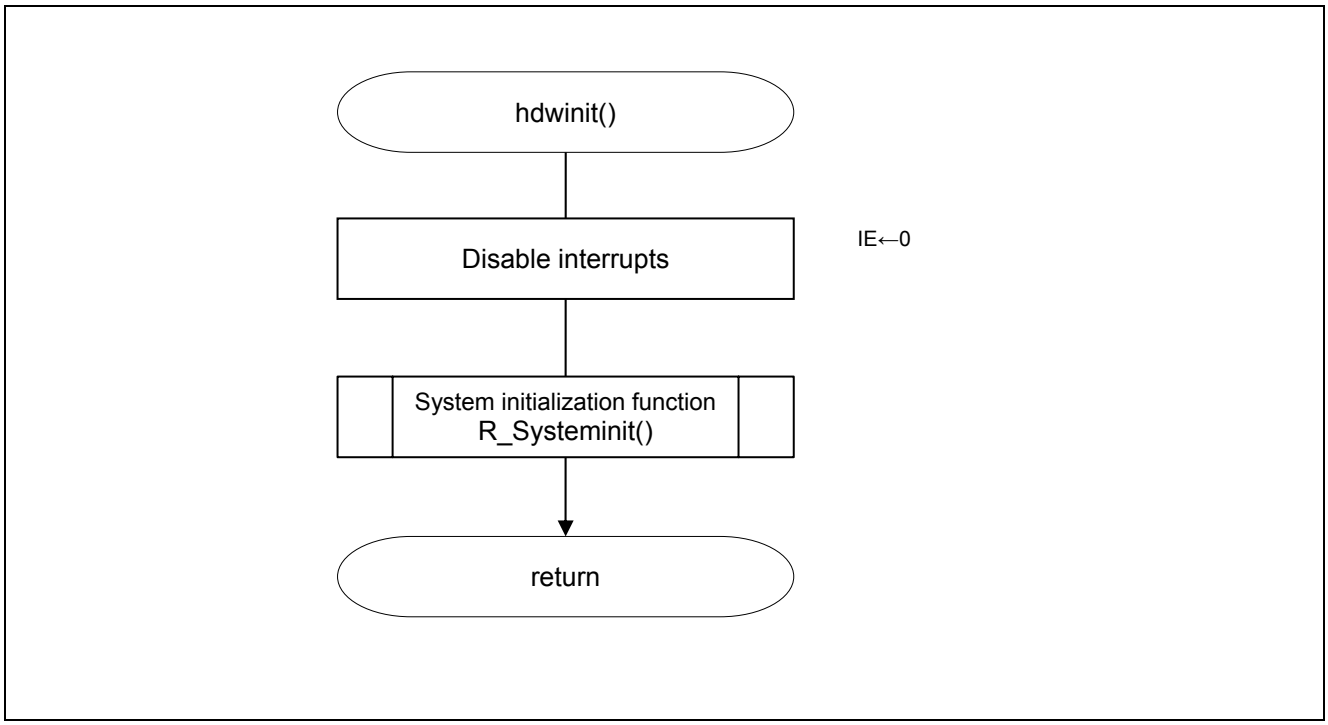


Figure 5.3 Initialization Function

5.7.2 Initial Setting of Peripheral Functions

Figure 5.4 shows the Initial Setting of Peripheral Functions

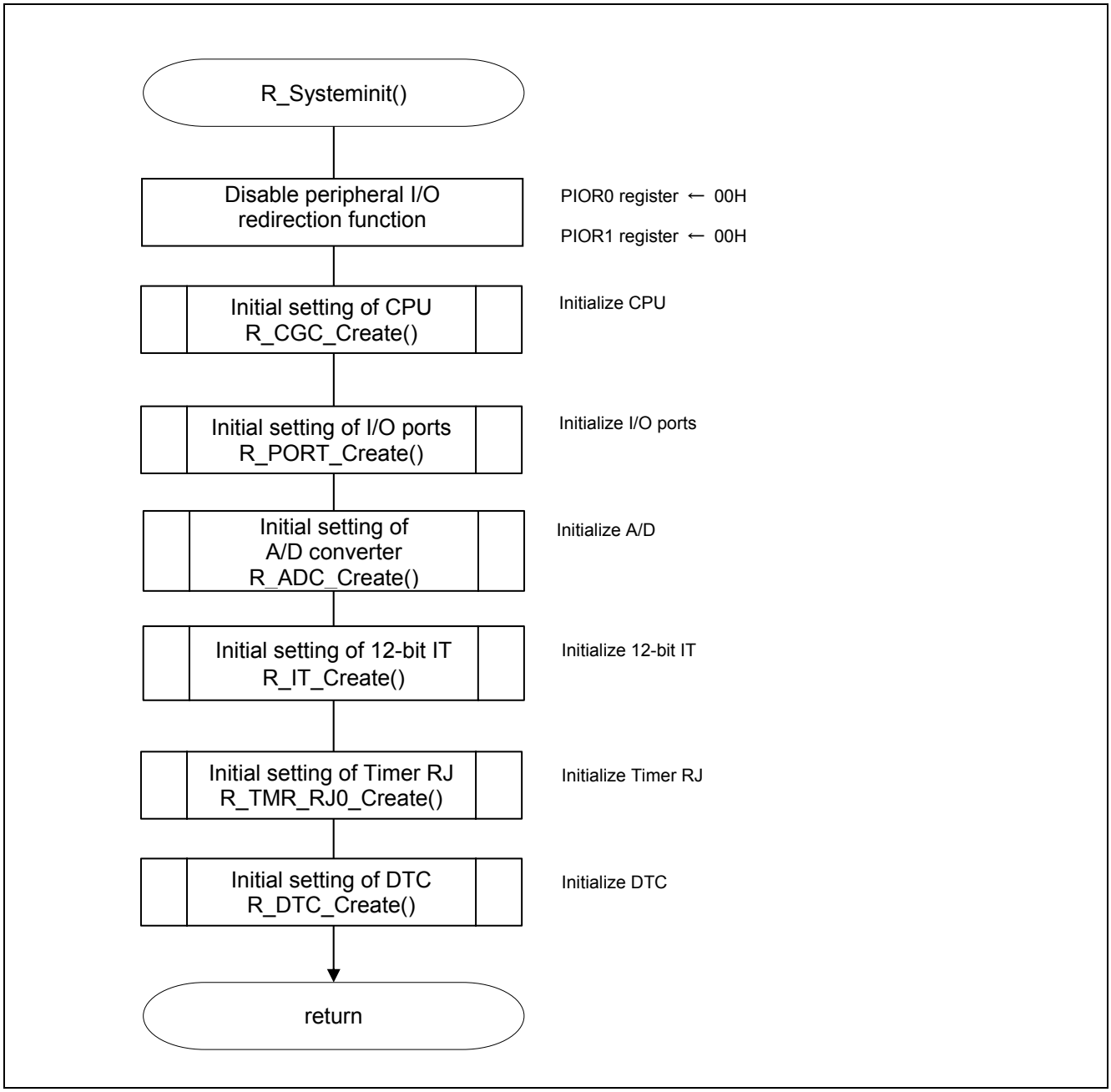


Figure 5.4 Initial Setting of Peripheral Functions

5.7.3 Initial Setting of CPU

Figure 5.5 shows the Initial Setting of the CPU.

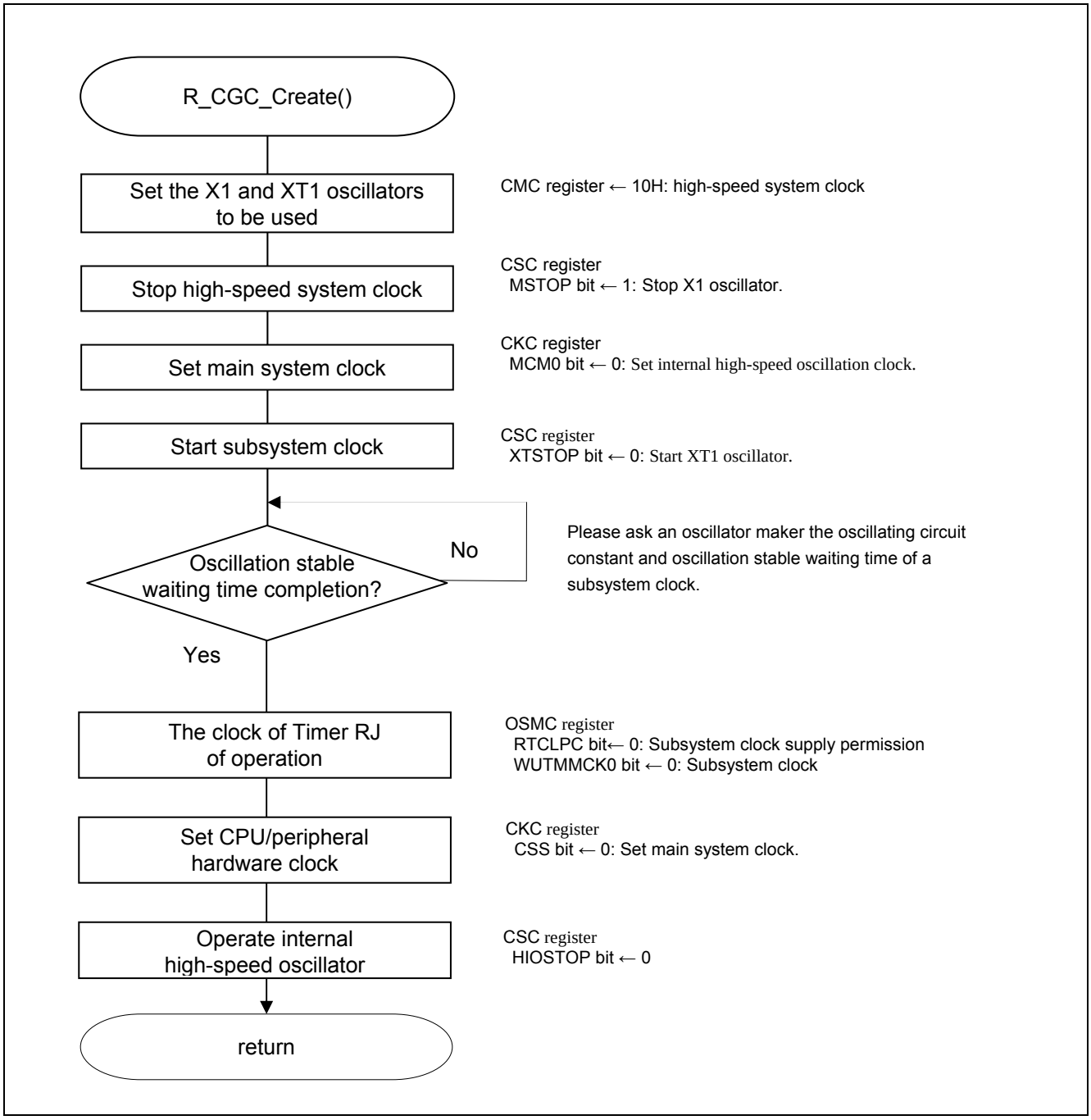


Figure 5.5 Initial Setting of the CPU

5.7.4 Setting up the I/O Ports

Figure 5.6 shows the setting up the I/O ports.

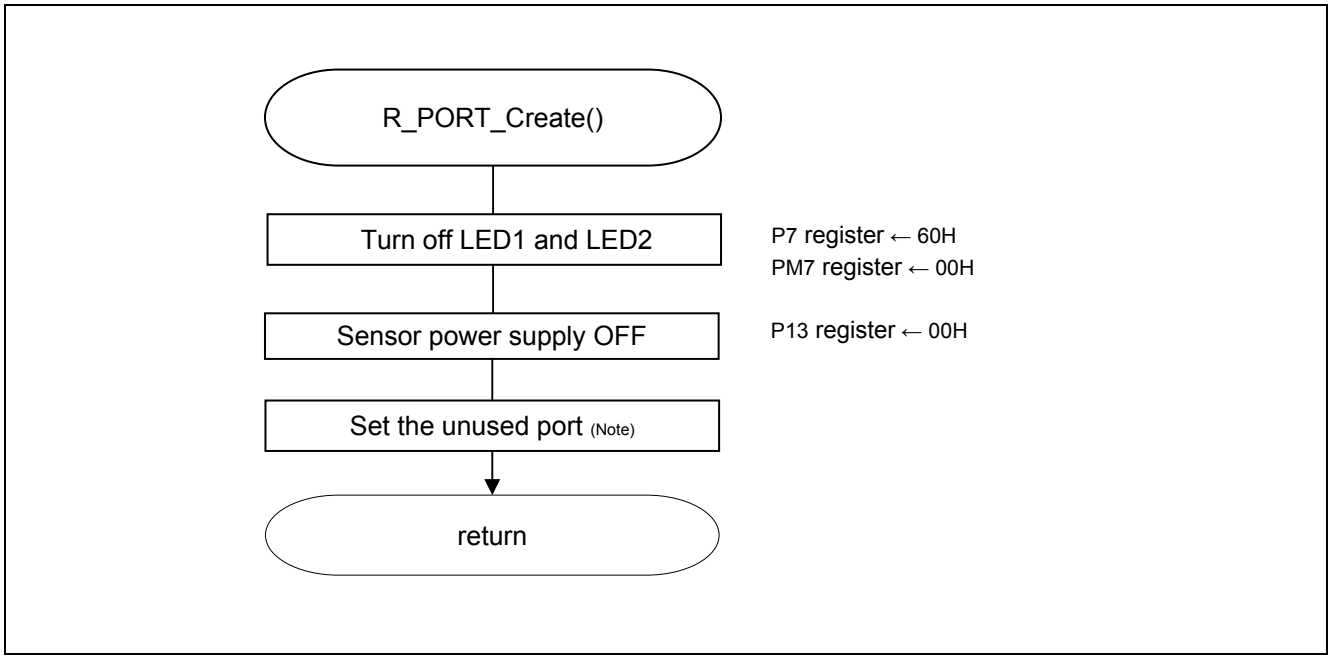


Figure 5.6 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.7.5 Initial Setting of the A/D Converter

Figure 5.7 shows the Initial Setting of the A/D Converter.

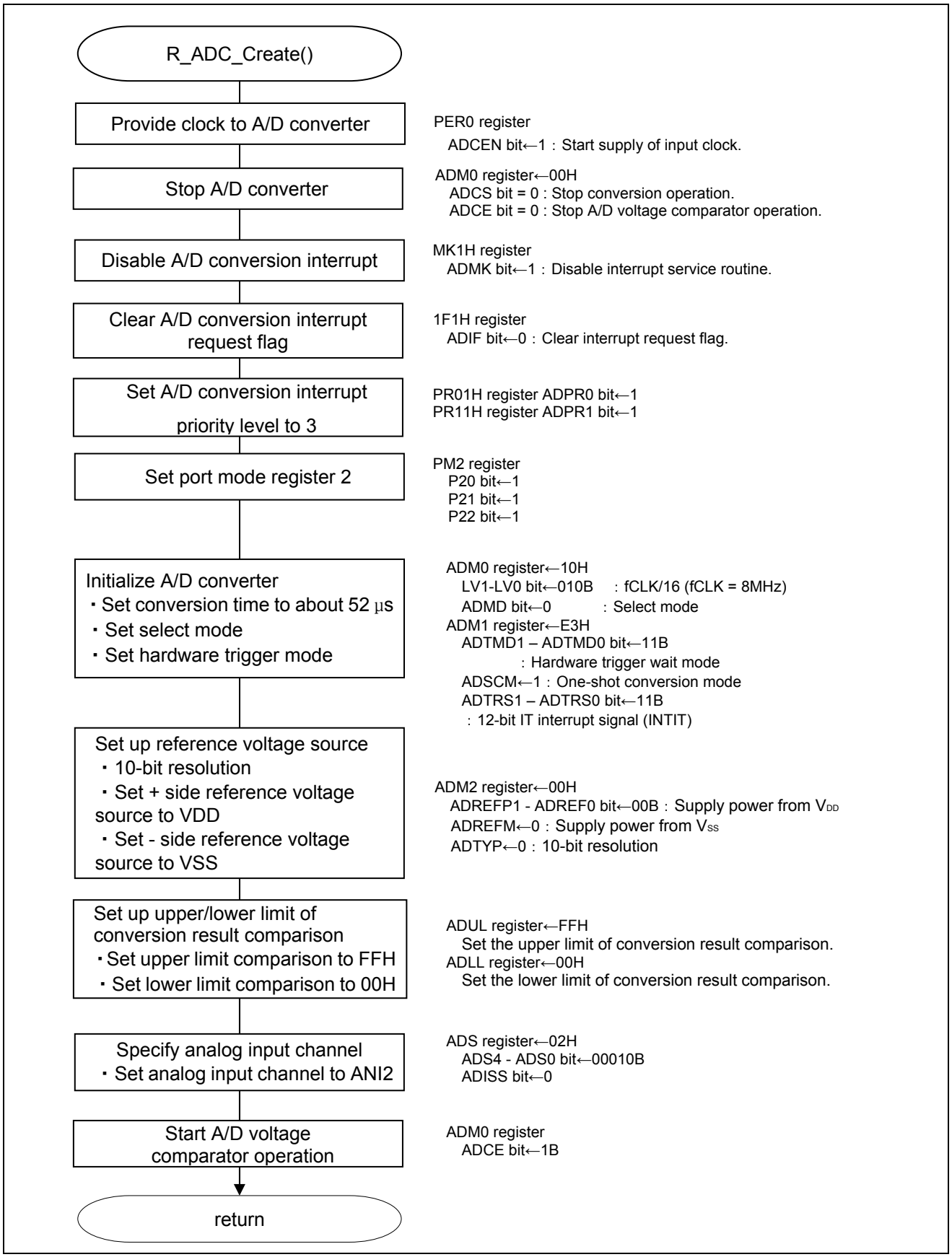


Figure 5.7 Initial Setting of the A/D Converter

Start providing a clock to the A/D converter

- Peripheral Enable Register 0 (PER0)
  Provide a clock to the A/D converter.

Symbol：PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	**1**	x	x	x	x	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Set A/D conversion mode and conversion time

- A/D Converter Mode Register 0 (ADM0)
  Control of A/D conversion operation
  Specification of the A/D conversion channel selection mode

Symbol：ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
0	**0**	**0**	**1**	**0**	**0**	**0**	**1**

Bit 7

ADCS	Control of A/D conversion operation
0	**Stops conversion operation**
1	Enables conversion operation

Bit 6

ADMD	Specification of the A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

Bit 5 – 1

ADM0					Mode	Conversion clock (f_{AD})	Number of A/D Power Supply Stabilization Wait Clock	Number of Conversion Clock	A/D Power Supply Stabilization Wait Time + Conversion Time	A/D Power Supply Stabilization Wait Time + Conversion Time at 10-Bit Resolution				
FR2	FR1	FR0	LV1	LV0						f_{CLK}= 1MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 16MHz	f_{CLK}= 32MHz
0	0	0	**0**	**0**	**Normal 1**	$f_{CLK}/64$	$8f_{AD}$	$19f_{AD}$ (The number of sampling clocks : $7f_{AD}$)	$1728/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	108µs	54µs
0	0	1				$f_{CLK}/32$			$864/f_{CLK}$			108µs	54µs	27µs
0	**1**	**0**				**$f_{CLK}/16$**			**$432/f_{CLK}$**		108µs	**54µs**	27µs	13.5µs
0	1	1				$f_{CLK}/8$			$216/f_{CLK}$		54µs	27µs	13.5µs	6.75µs
1	0	0				$f_{CLK}/6$			$162/f_{CLK}$		40.5µs	20.25µs	10.125µs	5.0625µs
1	0	1				$f_{CLK}/5$			$135/f_{CLK}$	135µs	33.75µs	16.85µs	8.4375µs	4.21875µs
1	1	0				$f_{CLK}/4$			$108/f_{CLK}$	108µs	27µs	13.5µs	6.75µs	3.375µs
1	1	1				$f_{CLK}/2$			$54/f_{CLK}$	54µs	13.5µs	6.75µs	3.375µs	Setting prohibited
0	0	0	0	1	Normal 2	$f_{CLK}/64$	$8f_{AD}$	$17f_{AD}$ (The number of sampling clocks : $5f_{AD}$)3.125	$1600/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	100µs	50µs
0	0	1				$f_{CLK}/32$			$800/f_{CLK}$			100µs	50µs	25µs
0	1	0				$f_{CLK}/16$			$400/f_{CLK}$		100µs	50µs	25µs	12.5µs
0	1	1				$f_{CLK}/8$			$200/f_{CLK}$		50µs	25µs	12.5µs	6.25µs
1	0	0				$f_{CLK}/6$			$150/f_{CLK}$		37.5µs	18.75µs	9.375µs	4.6875µs
1	0	1				$f_{CLK}/5$			$125/f_{CLK}$	125µs	31.25µs	15.625µs	7.8125µs	3.90625µs
1	1	0				$f_{CLK}/4$			$100/f_{CLK}$	100µs	25µs	12.5µs	6.25µs	3.125µs
1	1	1				$f_{CLK}/2$			$50/f_{CLK}$	50µs	12.5µs	6.25s	3.125µs	Setting prohibited

Bit 0

ADMD	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	**Enables A/D voltage comparator operation**

Set the A/D conversion end interrupt

- Interrupt Request Flag Register (IF1H)
  Clear the A/D conversion interrupt request flag.
- Interrupt Mask Flag Register (MK1H)
  Disable an A/D conversion interrupt.

Symbol：IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol：MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Set the A/D conversion interrupt priority level

- Priority Specification Flag Registers (PR11H and PR01H)
  Set to level 3 (low priority).

Symbol：PR11H

7	6	5	4	3	2	1	0
TMPR110	TRJPR10	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
x	x	x	x	x	x	x	**1**

Symbol：PR01H

7	6	5	4	3	2	1	0
TMPR010	TRJPR00	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
x	x	x	x	x	x	x	**1**

Bit 0

ADPR1	ADPR0	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

Set port mode register 2

- Port Mode Register 2 (PM2)
  Set port mode register 2 to input mode.

Symbol：PM2

7	6	5	4	3	2	1	0
PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
x	x	x	x	x	**1**	**1**	**1**

Bit 2

PM22	P22 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Bit 1

PM21	P21 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Bit 0

PM20	P20 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Set A/D conversion trigger mode

- A/D Converter Mode Register 1 (ADM1)
  Select the A/D conversion trigger.
  Select the A/D conversion mode.
  Select the hardware trigger signal.

Symbol：ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
1	**1**	**1**	x	x	x	**1**	**1**

Bit 7 - 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	x	Software trigger mode
1	0	Hardware trigger no-wait mode
1	**1**	**Hardware trigger wait mode**

Bit 5

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

Bit 1-0

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 01 count or capture interrupt signal (INTTM01)
0	1	Event signal selected by ELC
1	0	**Real-time clock interrupt signal (INTRTC)**
1	**1**	**12-bit interval timer interrupt signal (INTIT)**

Set up the reference voltage source

- A/D Converter Mode Register 2 (ADM2)
  Select the + side reference voltage source of the A/D converter.
  Select the – side reference voltage source of the A/D converter.
  Check the upper limit and lower limit conversion result values.
  Set up the SNOOZE mode.
  Set up the A/D conversion resolution.

Symbol：ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7 - 6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage (1.45 V)
1	1	Setting prohibited

Bit 5

ADREFM	Selection of the − side reference voltage source of the A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADRCK	Checking the upper limit and lower limit conversion result values
0	**The interrupt signal (INTAD) is output when the ADLL register≦the ADCR register≦the ADUL register.**
1	The interrupt signal (INTAD) is output when the ADCR register < the ADLL register (AREA 2) or the ADUL register < the ADCR register.

Bit 2

AWC	Specification of the SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Set up the conversion result comparison upper limit/lower limit

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Set up the conversion result comparison upper- and lower-limit values.

Symbol：ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol：ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Specify the input channel

- Analog input channel specification register (ADS)
  Specify the input channel for the analog voltage to be subjected to A/D conversion.

Symbol：ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	x	x	**0**	**0**	**0**	**1**	**0**

Bit 7,4-0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV_{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
0	**0**	**0**	**0**	**1**	**0**	**ANI2**	**P22/ANI2 pin**
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	0	1	1	1	ANI7	P27/ANI7 pin
0	0	1	0	0	0	ANI8	P150/ANI8 pin
0	0	1	0	0	1	ANI9	P151/ANI9 pin
0	0	1	0	1	0	ANI10	P152/ANI10 pin
0	0	1	0	1	1	ANI11	P153/ANI11 pin
0	0	1	1	0	0	ANI12	P154/ANI12 pin
0	0	1	1	0	1	ANI13	P155/ANI13 pin
0	0	1	1	1	0	ANI14	P156/ANI14 pin
0	1	0	0	0	0	ANI16	P03/ANI16 pin Note 1
0	1	0	0	0	1	ANI17	P02/ANI17 pin Note 2
0	1	0	0	1	0	ANI18	P147/ANI18 pin
0	1	0	0	1	1	ANI19	P120/ANI19 pin
0	1	0	1	0	0	ANI20	P100/ANI20 pin
1	0	0	0	0	0	—	Temperature sensor output voltage Note3
1	0	0	0	0	1	—	Internal reference voltage (1.45 V) Note3
Other than above						Setting prohibited	

Notes: 1. 30-, 32-pin products: P01/ANI16 pin
2. 30-, 32-pin products: P00/ANI17 pin
3. Operation is possible only in HS (high-speed main) mode.

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.6 Initial Setting of the 12-bit IT

Figure 5.8 shows the Initial Setting of the 12-bit IT.

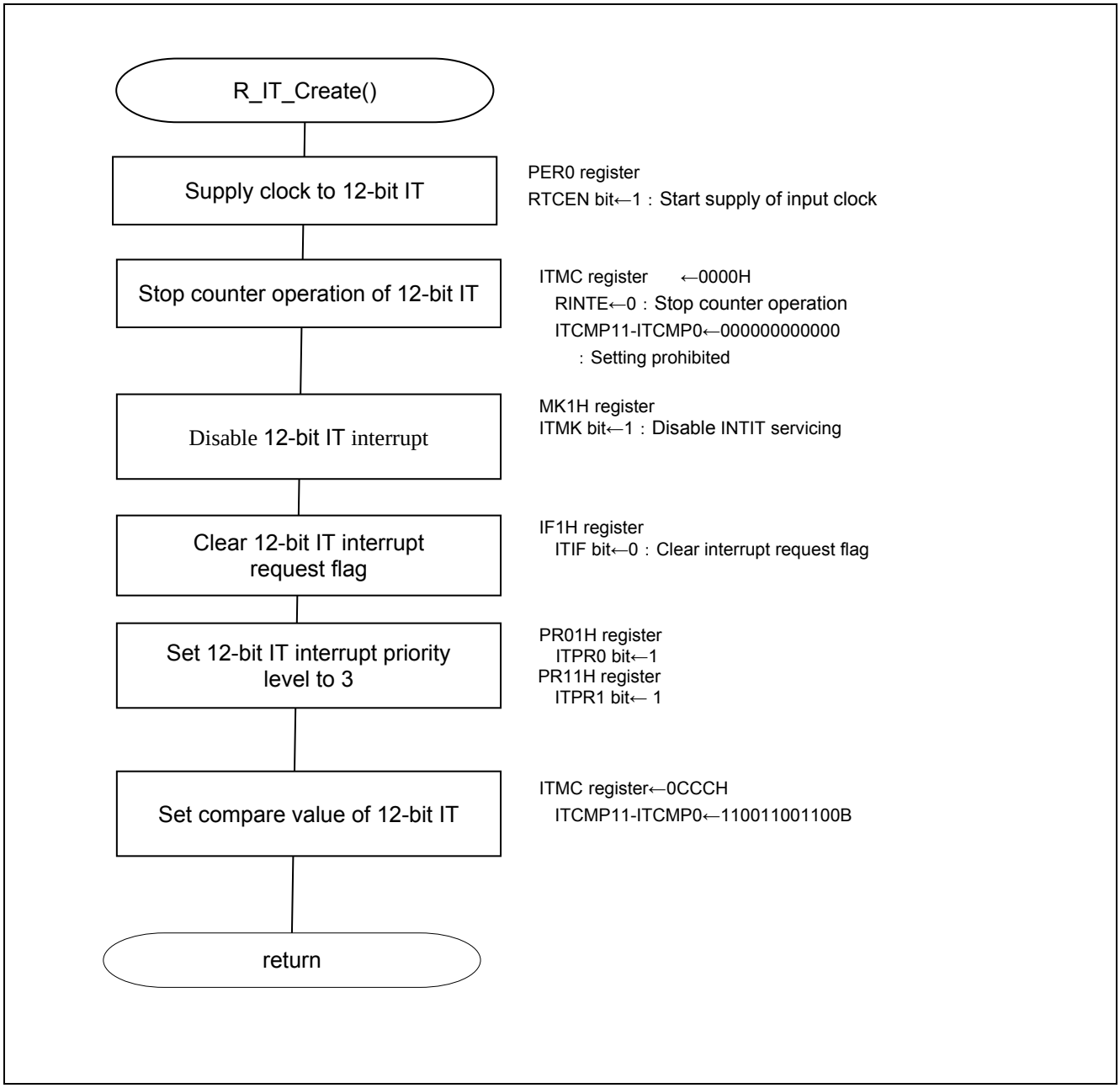


Figure 5.8 Initial Setting of the 12-bit IT

Start providing a clock to the 12-bit IT

- Peripheral enable register 0 (PER0)
  Provide a clock to the 12-bit IT.

Symbol：PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
1	x	x	x	x	x	x	x

Bit 7

RTCEN	Control of real-time clock (RTC) and 12-bit interval timer input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Counter operation of 12-bit IT and setting of compare value

- 12-bit interval timer control register (ITMC)
  Stop counter operation of 12-bit IT.
  Set compare value.

Symbol：ITMC

15	14	13	12	11 to 0
RINTE	0	0	0	ITCMP11 to ITCMP0
0	x	x	x	**110011001100**

Bit 15

RINTE	Control 12-bit IT operation
0	**Stop counter operation**
1	Start counter operation

Bit 11-5

ITCMP11 to ITCMP0	Specification of the 12-bit interval timer compare value
001H	**These bits generate a fixed-cycle interrupt (count clock cycles x (ITCMP setting + 1)).**
・・・	
CCCH	
・・・	
FFFH	
000H	Setting prohibited

Set up 12-bit IT interrupt

- Interrupt request flag register (IF1H)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Disable interrupt servicing.

Symbol：IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	**0**	x	x

Bit 2

ITIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol：MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	**1**	x	x

Bit 2

ITMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Set the 12-bit IT interrupt priority level

- Priority Specification Flag Registers (PR11H and PR01H)
  Set to level 3 (low priority).

Symbol：PR11H

7	6	5	4	3	2	1	0
TMPR110	TRJPR10	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
x	x	x	x	x	**1**	x	x

Symbol：PR01H

7	6	5	4	3	2	1	0
TMPR010	TRJPR00	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
x	x	x	x	x	**1**	x	x

Bit 2

ITPR1	ITPR0	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.7 Initial Setting of Timer RJ

Figure 5.9 shows the Initial Setting of Timer RJ.

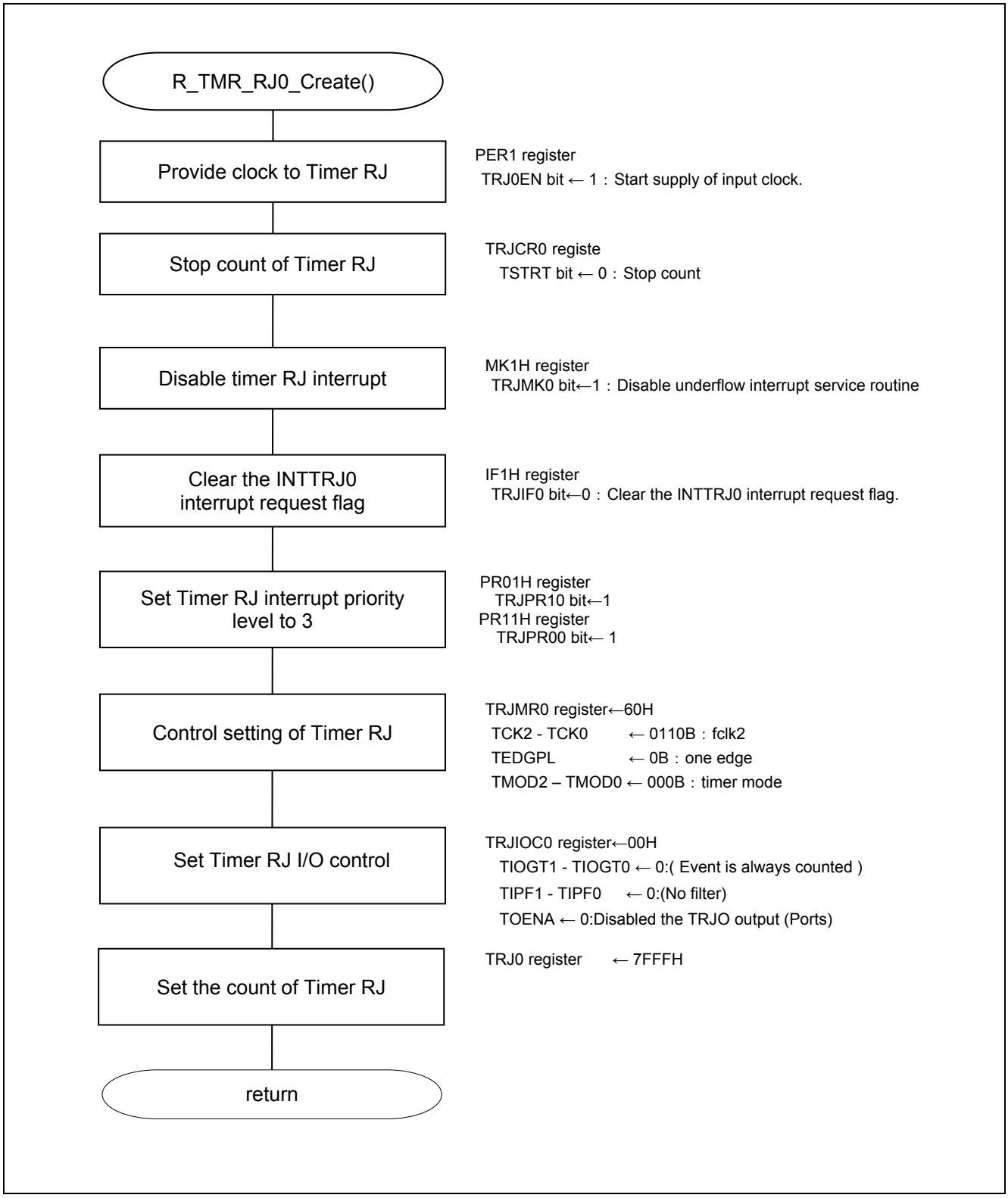


Figure 5.9 Initial Setting of the Timer RJ

Start providing a clock to Timer RJ

- Peripheral Enable Register 1 (PER1)
  Start providing a clock to Timer RJ.

Symbol：PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
x	x	x	x	x	x	x	**1**

Bit 0

TRJ0EN	Control of Timer RJ input clock supply
0	Stops input clock supply
1	**Enable input clock supply**

Start the Timer RJ count

- Timer RJ Control Register 0（TRJCR0）
  Start the Timer RJ count.

Symbol：TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSIF	TSTART
x	x	x	x	x	x	x	**0**

Bit 0

TSTART	Timer RJ count start
0	**Count stops**
1	Count starts

Set the Timer RJ interrupt

- Interrupt Mask Flag Register (MK1H)
  Enable the interrupt operation.
- Interrupt Request Flag Register (IF1H)
  Clear the interrupt request flag.

Symbol：MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	**1**	x	x	x	x	x	x

Bit 6

TRJMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol：IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	**0**	x	x	x	x	x	x

Bit 6

TRJIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Set the Timer RJ interrupt priority level

- Priority Specification Flag Registers (PR11H, PR01H)
  Set to level 3 (low priority).

Symbol：PR11H

7	6	5	4	3	2	1	0
TMPR110	TRJPR10	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
x	**1**	x	x	x	x	x	x

Symbol：PR01H

7	6	5	4	3	2	1	0
TMPR010	TRJPR00	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
x	**1**	x	x	x	x	x	x

Bit 6

TRJPR10	TRJPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

Set Timer RJ mode

- Timer RJ Mode Register 0 (TRJMR0)
  Set timer mode of f_{SUB}.

Symbol：TRJMR0

7	6	5	4	3	2	1	0
0	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
x	**1**	**1**	**0**	**0**	**0**	**0**	**0**

Bit 6-4

TCK2	TCK1	TCK0	Timer RJ count source select
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/8$
0	1	1	$f_{CLK}/2$
1	0	0	f_{IL}
1	0	1	Event input from ELC
1	**1**	**0**	**f_{SUB}**
Other than above			Setting prohibited

Bit 3

TEDGPL	TRJIO edge polarity select
0	**One edge**
1	Both edge

Bit 2-0

TMOD2	TMOD1	TMOD0	Timer RJ operating mode select
0	**0**	**0**	**Timer mode**
0	0	1	Pulse output mode
0	1	1	Event counter mode
1	0	0	Pulse width measurement mode
1	0	1	Pulse period measurement mode
Other than above			Setting prohibited

Set counter of Timer RJ

- Timer RJ Counter Register 0 (TRJ0)
  Set value of counter.

Symbol：TRJ0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit 15-0

Function
16-bit counter

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.8 Initial Setting of DTC

Figure 5.10 shows the Initial Setting of DTC.

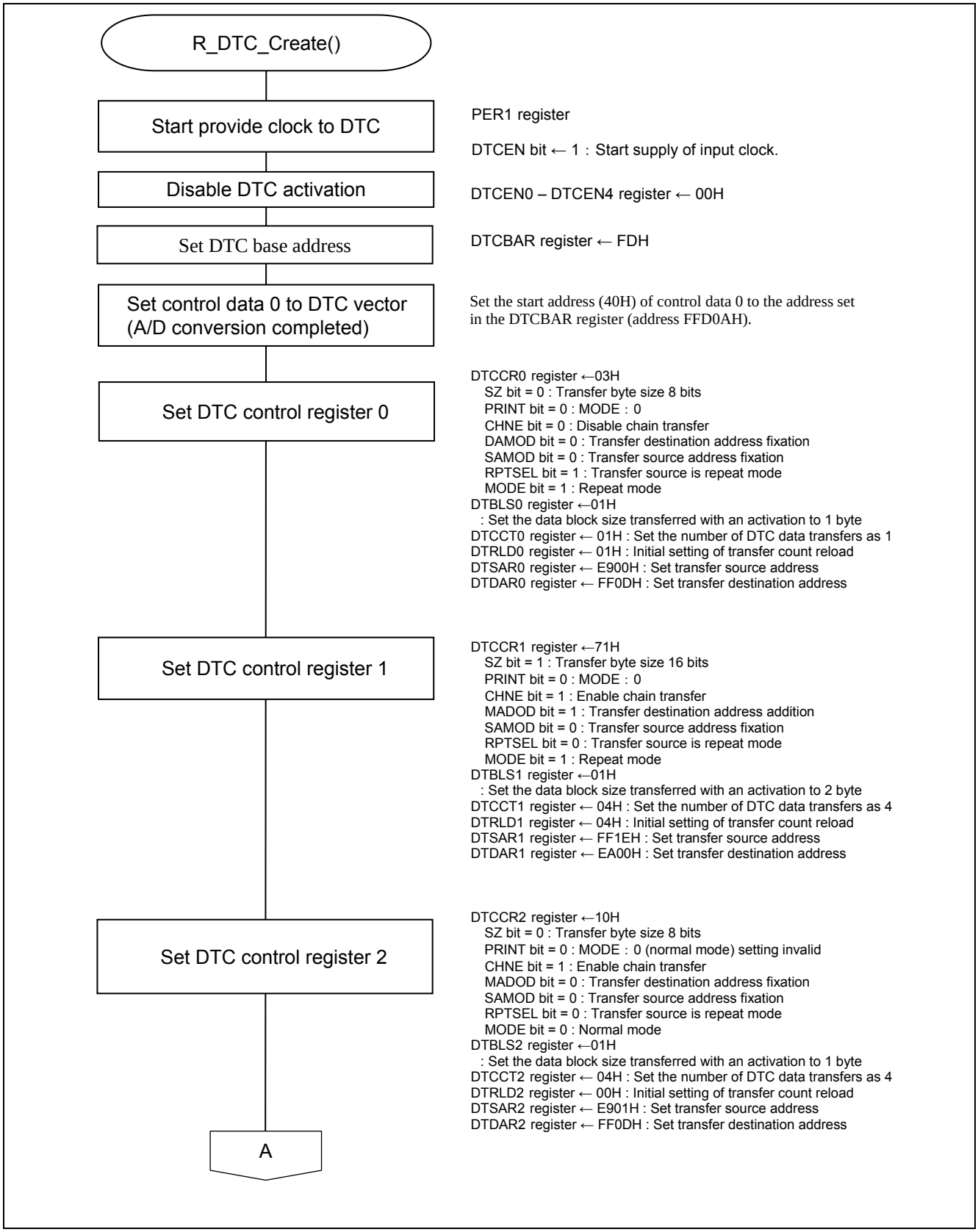


Figure 5.10 Initial Setting of the DTC(1/2)

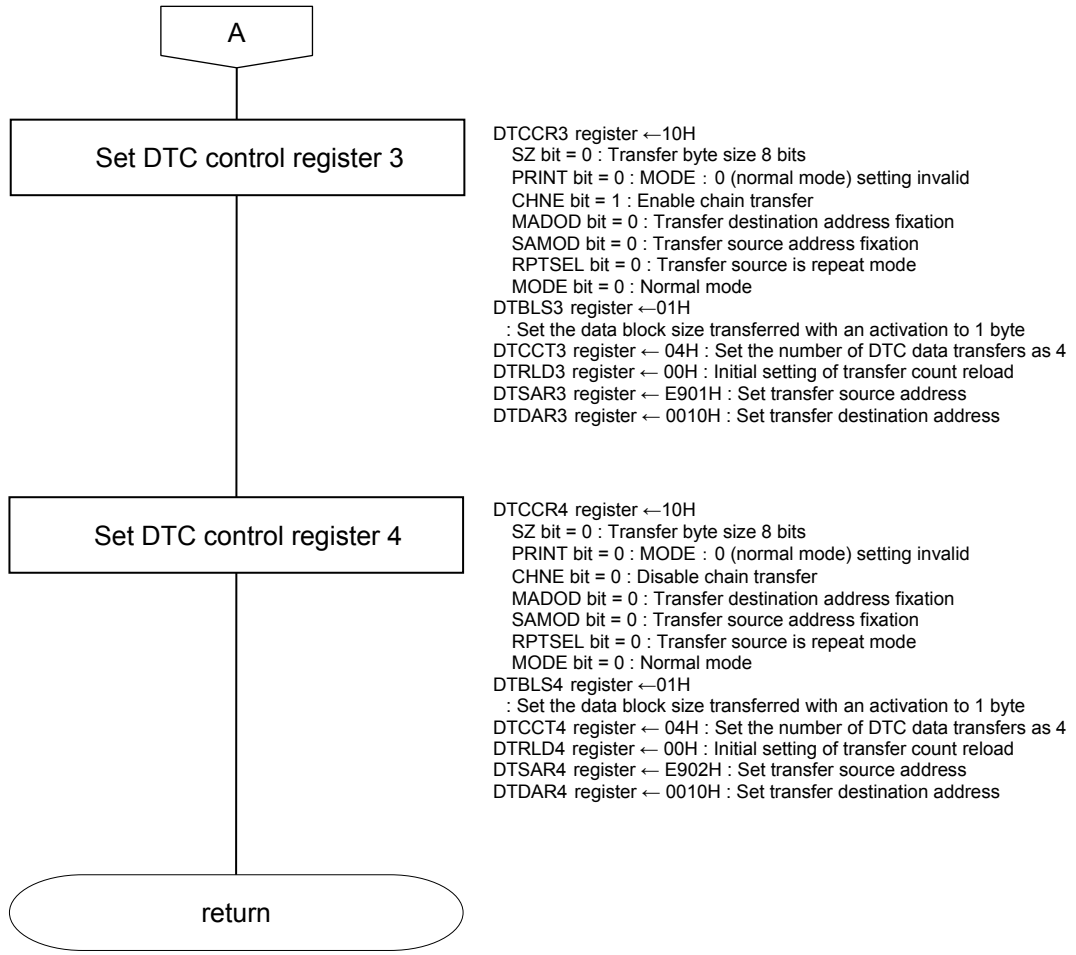


Figure 5.10 Initial Setting of the DTC(2/2)

Start providing a clock to the DTC

- Peripheral Enable Register 1 (PER1)
  Provide a clock to the DTC.

Symbol：PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TAU0EN
x	x	x	x	**1**	x	x	x

Bit 3

DTCEN	Control of DTC input clock supply
0	Stops input clock supply
1	**Enables input clock supply**

Disable DTC activation

- DTC Activation Enable Register i（DTCENi）(i=0～4)
  Disable DTC activation.

Symbol：DTCENi

7	6	5	4	3	2	1	0
DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7-0 (The follows list it in an example of bit 7.(contents same as for 7 bit - bits 0))

DTCENi7	DTC activation enable i7
0	**Activation disabled**
1	Activation enabled

Set the DTC base address

- DTC Base Address Register（DTCBAR）
  Set FDH to the DTC base address.

Symbol：DTCBAR

7	6	5	4	3	2	1	0
DTCBAR7	DTCBAR6	DTCBAR5	DTCBAR4	DTCBAR3	DTCBAR2	DTCBAR1	DTCBAR0
1	**1**	**1**	**1**	**1**	**1**	**0**	**1**

Set the DTC control register 0

・DTC Control Register 0（DTCCR0）

Set 8bits chain transfer disabled, repeat mode.

Symbol：DTCCR0

7	6	5	4	3	2	1	0
0	SZ	RPTINT	CHNE	DAMOD	SAMOD	PRTSEL	MODE
-	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Bit 6

SZ	Transfer Data size selection
0	**8 bits**
1	16 bits

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	**Interrupt generation disabled**
1	Interrupt generation enabled
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	**Chain transfers disabled**
1	Chain transfers enabled
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 3

DAMOD	Transfer destination address control
0	**Fixed**
1	Incremented
The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area).	

Bit 2

SAMOD	Transfer source address control
0	**Fixed**
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

PRTSEL	Repeat area selection
0	Transfer destination is the repeat area
1	**Transfer source is the repeat area**
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	Normal mode
1	**Repeat mode**

Set the DTC control register 1

- DTC Control Register 1（DTCCR1）
- Set 16bits chain transfer disabled, repeat mode.

Symbol：DTCCR1

7	6	5	4	3	2	1	0
0	SZ	RPTINT	CHNE	DAMOD	SAMOD	PRTSEL	MODE
-	**1**	**1**	**1**	**0**	**0**	**0**	**1**

Bit 6

SZ	Transfer Data size selection
0	**8 bits**
1	**16 bits**

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	Interrupt generation disabled
1	**Interrupt generation enabled**
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	Chain transfers disabled
1	**Chain transfers enabled**
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 3

DAMOD	Transfer destination address control
0	**Fixed**
1	Incremented
The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area).	

Bit 2

SAMOD	Transfer source address control
0	**Fixed**
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

PRTSEL	Repeat area selection
0	**Transfer destination is the repeat area**
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	Normal mode
1	**Repeat mode**

Set the DTC control register 2

- DTC Control Register 2（DTCCR2）
- Set 8bits chain transfer enabled, normal mode.

Symbol：DTCCR2

7	6	5	4	3	2	1	0
0	SZ	RPTINT	CHNE	DAMOD	SAMOD	PRTSEL	MODE
-	**0**	**0**	**1**	**0**	**0**	**0**	**0**

Bit 6

SZ	Transfer Data size selection
0	**8 bits**
1	16 bits

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	Interrupt generation disabled
1	Interrupt generation enabled
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	Chain transfers disabled
1	**Chain transfers enabled**
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 3

DAMOD	Transfer destination address control
0	**Fixed**
1	Incremented
The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area).	

Bit 2

SAMOD	Transfer source address control
0	**Fixed**
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

PRTSEL	Repeat area selection
0	Transfer destination is the repeat area
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	**Normal mode**
1	Repeat mode

Set the DTC control register 3

- DTC Control Register 3（DTCCR3）
- Set 8bits chain transfer enabled, normal mode.

Symbol：DTCCR3

7	6	5	4	3	2	1	0
0	SZ	RPTINT	CHNE	DAMOD	SAMOD	PRTSEL	MODE
-	**0**	**0**	**1**	**0**	**0**	**0**	**0**

Bit 6

SZ	Transfer Data size selection
0	**8 bits**
1	16 bits

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	Interrupt generation disabled
1	Interrupt generation enabled
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	Chain transfers disabled
1	**Chain transfers enabled**
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 3

DAMOD	Transfer destination address control
0	**Fixed**
1	Incremented
The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area).	

Bit 2

SAMOD	Transfer source address control
0	**Fixed**
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

PRTSEL	Repeat area selection
0	Transfer destination is the repeat area
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	**Normal mode**
1	Repeat mode

Set the DTC control register 4

- DTC Control Register 4（DTCCR4）
- Set 8bits chain transfer disabled, normal mode.

Symbol：DTCCR4

7	6	5	4	3	2	1	0
0	SZ	RPTINT	CHNE	DAMOD	SAMOD	PRTSEL	MODE
-	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 6

SZ	Transfer Data size selection
0	**8 bits**
1	16 bits

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	Interrupt generation disabled
1	Interrupt generation enabled
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	**Chain transfers disabled**
1	Chain transfers enabled
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 3

DAMOD	Transfer destination address control
0	**Fixed**
1	Incremented
The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area).	

Bit 2

SAMOD	Transfer source address control
0	**Fixed**
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

PRTSEL	Repeat area selection
0	Transfer destination is the repeat area
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	**Normal mode**
1	Repeat mode

Set DTC block size register 0

- DTC Block Size Register 0（DTBLS0）
- Set 1 byte to DTC block size.

Symbol：DTBLS0

7	6	5	4	3	2	1	0
DTBLS07	DTBLS06	DTBLS05	DTBLS04	DTBLS03	DTBLS02	DTBLS01	DTBLS00
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**

DTBLS0	Transfer Block Size	
	8-bit Transfer	16-bit Transfer
00H	256 bytes	512 bytes
01H	**1 byte**	2 bytes
02H	2 bytes	4 bytes
・ ・ ・	・ ・ ・	・ ・ ・
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Set DTC block size register 1

- DTC Block Size Register 1（DTBLS1）
- Set 2 bytes to DTC block size.

Symbol：DTBLS1

7	6	5	4	3	2	1	0
DTBLS17	DTBLS16	DTBLS15	DTBLS14	DTBLS13	DTBLS12	DTBLS11	DTBLS10
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**

DTBLS1	Transfer Block Size	
	8-bit Transfer	16-bit Transfer
00H	256 bytes	512 bytes
01H	1 byte	**2 bytes**
02H	2 bytes	4 bytes
・ ・ ・	・ ・ ・	・ ・ ・
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Set DTC block size register 2

- DTC Block Size Register 2（DTBLS2）
- Set 1 byte to DTC block size.

Symbol：DTBLS2

7	6	5	4	3	2	1	0
DTBLS27	DTBLS26	DTBLS25	DTBLS24	DTBLS23	DTBLS22	DTBLS21	DTBLS20
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**

DTBLS2	Transfer Block Size	
	8-bit Transfer	16-bit Transfer
00H	256 bytes	512 bytes
01H	**1 byte**	2 bytes
02H	2 bytes	4 bytes
・ ・ ・	・ ・ ・	・ ・ ・
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Set DTC block size register 3

- DTC Block Size Register 3（DTBLS3）
- Set 1 byte to DTC block size.

Symbol：DTBLS3

7	6	5	4	3	2	1	0
DTBLS37	DTBLS36	DTBLS35	DTBLS34	DTBLS33	DTBLS32	DTBLS31	DTBLS30
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**

DTBLS3	Transfer Block Size	
	8-bit Transfer	16-bit Transfer
00H	256 bytes	512 bytes
01H	**1 byte**	2 bytes
02H	2 bytes	4 bytes
・ ・ ・	・ ・ ・	・ ・ ・
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Set DTC block size register 4

- DTC Block Size Register 4（DTBLS4）
- Set 1 byte to DTC block size.

Symbol：DTBLS4

7	6	5	4	3	2	1	0
DTBLS47	DTBLS46	DTBLS45	DTBLS44	DTBLS43	DTBLS42	DTBLS41	DTBLS40
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**

DTBLS4	Transfer Block Size	
	8-bit Transfer	16-bit Transfer
00H	256 bytes	512 bytes
01H	**1 byte**	2 bytes
02H	2 bytes	4 bytes
・ ・ ・	・ ・ ・	・ ・ ・
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Set DTC transfer count register 0

- DTC Transfer Count Register 0 (DTCCT0)
- Set the transfer number of times in once.

Symbol：DTCCT0

7	6	5	4	3	2	1	0
DTCCT07	DTCCT06	DTCCT05	DTCCT04	DTCCT03	DTCCT02	DTCCT01	DTCCT00
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**

DTCCT0	Number of Transfers
00H	256 times
01H	**Once**
02H	2 times
・ ・ ・	・ ・ ・
FEH	254 times
FFH	255 times

Set DTC transfer count register 1

- DTC Transfer Count Register 1 (DTCCT1)
- Set the transfer number of times in four times.

Symbol：DTCCT1

7	6	5	4	3	2	1	0
DTCCT17	DTCCT16	DTCCT15	DTCCT14	DTCCT13	DTCCT12	DTCCT11	DTCCT10
0	**0**	**0**	**0**	**0**	**1**	**0**	**0**

DTCCT1	Number of Transfers
00H	256 times
01H	Once
02H	2 times
03H	3 times
04H	**4 times**
.	.
.	.
.	.
FEH	254 times
FFH	255 times

Set DTC transfer count register 2

- DTC Transfer Count Register 2 (DTCCT2)
- Set the transfer number of times in four times.

Symbol：DTCCT2

7	6	5	4	3	2	1	0
DTCCT27	DTCCT26	DTCCT25	DTCCT24	DTCCT23	DTCCT22	DTCCT21	DTCCT20
0	**0**	**0**	**0**	**0**	**1**	**0**	**0**

DTCCT2	Number of Transfers
00H	256 times
01H	Once
02H	2 times
03H	3 times
04H	**4 times**
.	.
.	.
.	.
FEH	254 times
FFH	255 times

Set DTC transfer count register 3

- DTC Transfer Count Register 3 (DTCCT3)
- Set the transfer number of times in four times.

Symbol：DTCCT3

7	6	5	4	3	2	1	0
DTCCT37	DTCCT36	DTCCT35	DTCCT34	DTCCT33	DTCCT32	DTCCT31	DTCCT30
0	**0**	**0**	**0**	**0**	**1**	**0**	**0**

DTCCT3	Number of Transfers
00H	256 times
01H	Once
02H	2 times
03H	3 times
04H	**4 times**
.	.
.	.
.	.
FEH	254 times
FFH	255 times

Set DTC transfer count register 4

- DTC Transfer Count Register 4 (DTCCT4)
- Set the transfer number of times in four times.

Symbol：DTCCT4

7	6	5	4	3	2	1	0
DTCCT47	DTCCT46	DTCCT45	DTCCT44	DTCCT43	DTCCT42	DTCCT41	DTCCT40
0	**0**	**0**	**0**	**0**	**1**	**0**	**0**

DTCCT4	Number of Transfers
00H	256 times
01H	Once
02H	2 times
03H	3 times
04H	**4 times**
.	.
.	.
.	.
FEH	254 times
FFH	255 times

Set DTC transfer count reload register 0

- DTC Transfer Count Reload Register 0 (DTRLD0)
- Set the reload number of times in once.

Symbol：DTRLD0

7	6	5	4	3	2	1	0
DTRLD07	DTRLD06	DTRLD05	DTRLD04	DTRLD03	DTRLD02	DTRLD01	DTRLD00
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Set DTC transfer count reload register 1

- DTC Transfer Count Reload Register 1 (DTRLD1)
- Set the reload number of times to 0 times.

Symbol：DTRLD1

7	6	5	4	3	2	1	0
DTRLD17	DTRLD16	DTRLD15	DTRLD14	DTRLD13	DTRLD12	DTRLD11	DTRLD10
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Set DTC transfer count reload register 2

- DTC Transfer Count Reload Register 2 (DTRLD2)
- Set the reload number of times to 0 times.

Symbol：DTRLD2

7	6	5	4	3	2	1	0
DTRLD27	DTRLD26	DTRLD25	DTRLD24	DTRLD23	DTRLD22	DTRLD21	DTRLD20
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Set DTC transfer count reload register 3

- DTC Transfer Count Reload Register 3 (DTRLD3)
- Set the reload number of times to 0 times.

Symbol：DTRLD3

7	6	5	4	3	2	1	0
DTRLD37	DTRLD36	DTRLD35	DTRLD34	DTRLD33	DTRLD32	DTRLD31	DTRLD30
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Set DTC transfer count reload register 4

- DTC Transfer Count Reload Register 4 (DTRLD4)
- Set the reload number of times to 0 times.

Symbol：DTRLD4

7	6	5	4	3	2	1	0
DTRLD47	DTRLD46	DTRLD45	DTRLD44	DTRLD43	DTRLD42	DTRLD41	DTRLD40
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Set DTC source address register 0

- DTC Source Address Register 0 (DTSAR0)
- Set “E900H” to DTC transfer source address.

Symbol：DTSAR0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR0 15	DTSAR0 14	DTSAR0 13	DTSAR0 12	DTSAR0 11	DTSAR0 10	DTSAR0 9	DTSAR0 8	DTSAR0 7	DTSAR0 6	DTSAR0 5	DTSAR0 4	DTSAR0 3	DTSAR0 2	DTSAR0 1	DTSAR0 0
1	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Set DTC source address register 1

- DTC Source Address Register 1 (DTSAR1)
- Set “FF1EH” to DTC transfer source address.

Symbol：DTSAR1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR1 15	DTSAR1 14	DTSAR1 13	DTSAR1 12	DTSAR1 11	DTSAR1 10	DTSAR1 9	DTSAR1 8	DTSAR1 7	DTSAR1 6	DTSAR1 5	DTSAR1 4	DTSAR1 3	DTSAR1 2	DTSAR1 1	DTSAR1 0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**

Set DTC source address register 2

- DTC Source Address Register 2 (DTSAR2)
- Set “E901H” to DTC transfer source address.

Symbol：DTSAR2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR2 15	DTSAR2 14	DTSAR2 13	DTSAR2 12	DTSAR2 11	DTSAR2 10	DTSAR2 9	DTSAR2 8	DTSAR2 7	DTSAR2 6	DTSAR2 5	DTSAR2 4	DTSAR2 3	DTSAR2 2	DTSAR2 1	DTSAR2 0
1	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Set DTC source address register 3

- DTC Source Address Register 3 (DTSAR3)
- Set “E901H” to DTC transfer source address.

Symbol：DTSAR3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR3 15	DTSAR3 14	DTSAR3 13	DTSAR3 12	DTSAR3 11	DTSAR3 10	DTSAR3 9	DTSAR3 8	DTSAR3 7	DTSAR3 6	DTSAR3 5	DTSAR3 4	DTSAR3 3	DTSAR3 2	DTSAR3 1	DTSAR3 0
1	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Set DTC source address register 4

- DTC Source Address Register 4 (DTSAR4)
- Set “E902H” to DTC transfer source address.

Symbol：DTSAR4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR4 15	DTSAR4 14	DTSAR4 13	DTSAR4 12	DTSAR4 11	DTSAR4 10	DTSAR4 9	DTSAR4 8	DTSAR4 7	DTSAR4 6	DTSAR4 5	DTSAR4 4	DTSAR4 3	DTSAR4 2	DTSAR4 1	DTSAR4 0
1	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

Set DTC destination address register 0

- DTC Destination Address Register 0 (DTDAR0）(j=0～23)
- Set “FF0DH” to DTC destination address.

Symbol：DTDAR0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR0 15	DTDAR0 14	DTDAR0 13	DTDAR0 12	DTDAR0 11	DTDAR0 10	DTDAR0 9	DTDAR0 8	DTDAR0 7	DTDAR0 6	DTDAR0 5	DTDAR0 4	DTDAR0 3	DTDAR0 2	DTDAR0 1	DTDAR0 0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**

Set DTC destination address register 1

- DTC Destination Address Register 1 (DTDAR1）
- Set “EA00H” to DTC destination address.

Symbol：DTDAR1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR1 15	DTDAR1 14	DTDAR1 13	DTDAR1 12	DTDAR1 11	DTDAR1 10	DTDAR1 9	DTDAR1 8	DTDAR1 7	DTDAR1 6	DTDAR1 5	DTDAR1 4	DTDAR1 3	DTDAR1 2	DTDAR1 1	DTDAR1 0
1	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Set DTC destination address register 2

- DTC Destination Address Register 2 (DTDAR2）
- Set “FF0DH” to DTC destination address.

Symbol：DTDAR2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR2 15	DTDAR2 14	DTDAR2 13	DTDAR2 12	DTDAR2 11	DTDAR2 10	DTDAR2 9	DTDAR2 8	DTDAR2 7	DTDAR2 6	DTDAR2 5	DTDAR2 4	DTDAR2 3	DTDAR2 2	DTDAR2 1	DTDAR2 0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**

Set DTC destination address register 3

- DTC Destination Address Register 3 (DTDAR3）
- Set “0010H” to DTC destination address.

Symbol：DTDAR3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR3 15	DTDAR3 14	DTDAR3 13	DTDAR3 12	DTDAR3 11	DTDAR3 10	DTDAR3 9	DTDAR3 8	DTDAR3 7	DTDAR3 6	DTDAR3 5	DTDAR3 4	DTDAR3 3	DTDAR3 2	DTDAR3 1	DTDAR3 0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

Set DTC destination address register 4

- DTC Destination Address Register 4 (DTDAR4）
- Set “0010H” to DTC destination address.

Symbol：DTDAR4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR4 15	DTDAR4 14	DTDAR4 13	DTDAR4 12	DTDAR4 11	DTDAR4 10	DTDAR4 9	DTDAR4 8	DTDAR4 7	DTDAR4 6	DTDAR4 5	DTDAR4 4	DTDAR4 3	DTDAR4 2	DTDAR4 1	DTDAR4 0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

5.7.9 Main Processing

Figure 5.11 shows the Main Processing.

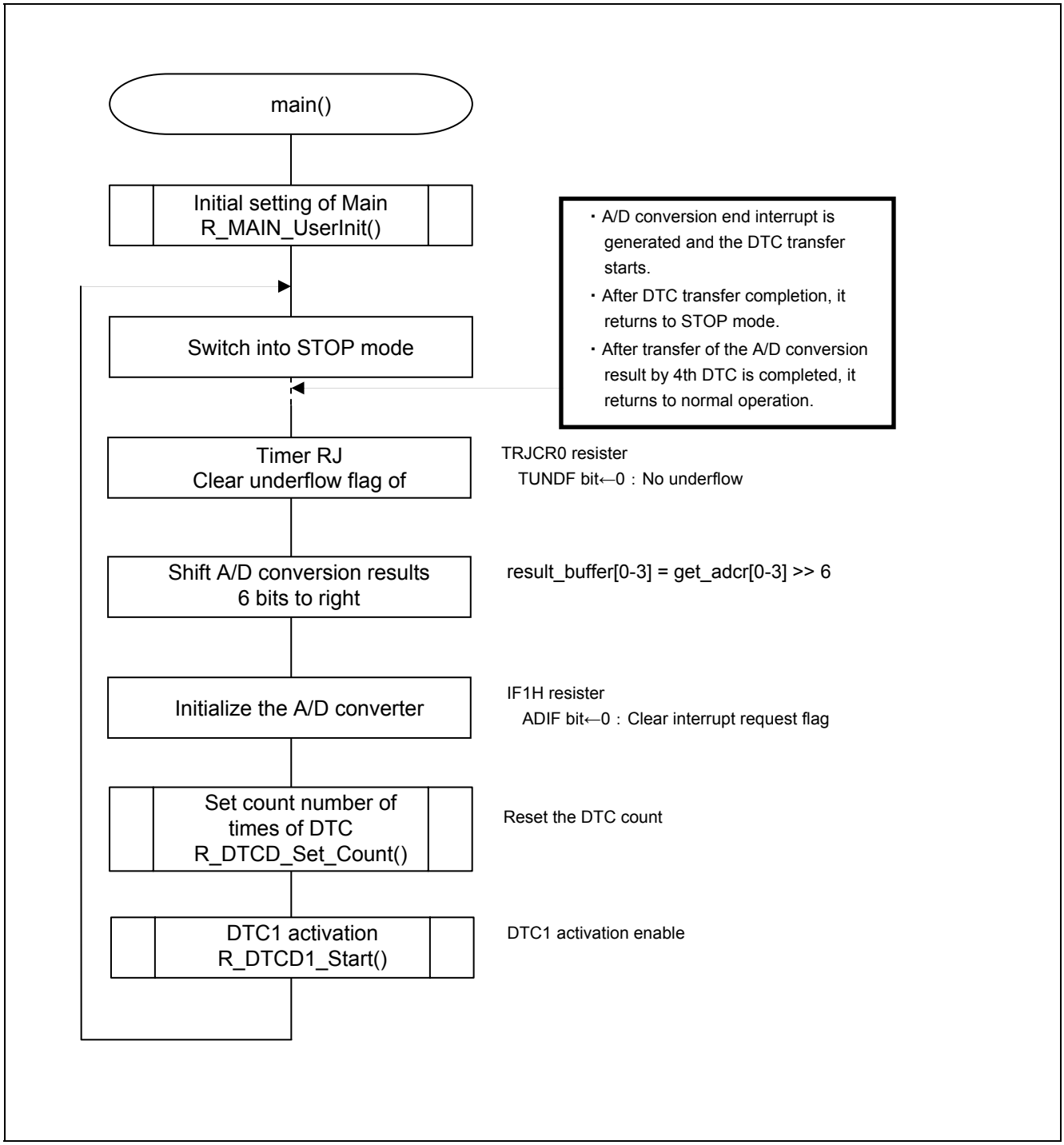


Figure 5.11 Main Processing

Clear underflow flag of Timer RJ

・Timer RJ Control Register 0（TRJCR0）

Clear the underflow flag of Timer RJ.

Symbol：TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSTF	TSTART
x	x	**0**	x	x	x	x	x

Bit 5

TUNDF	Timer RJ underflow flag
0	**No underflow**
1	**Underflow**

Set the A/D conversion end interrupt

・Interrupt Request Flag Register (IF1H)

Clear the interrupt request flag.

Symbol：IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

5.7.10 Initial setting of Main

Figure 5.12 shows the Initial setting of Main.

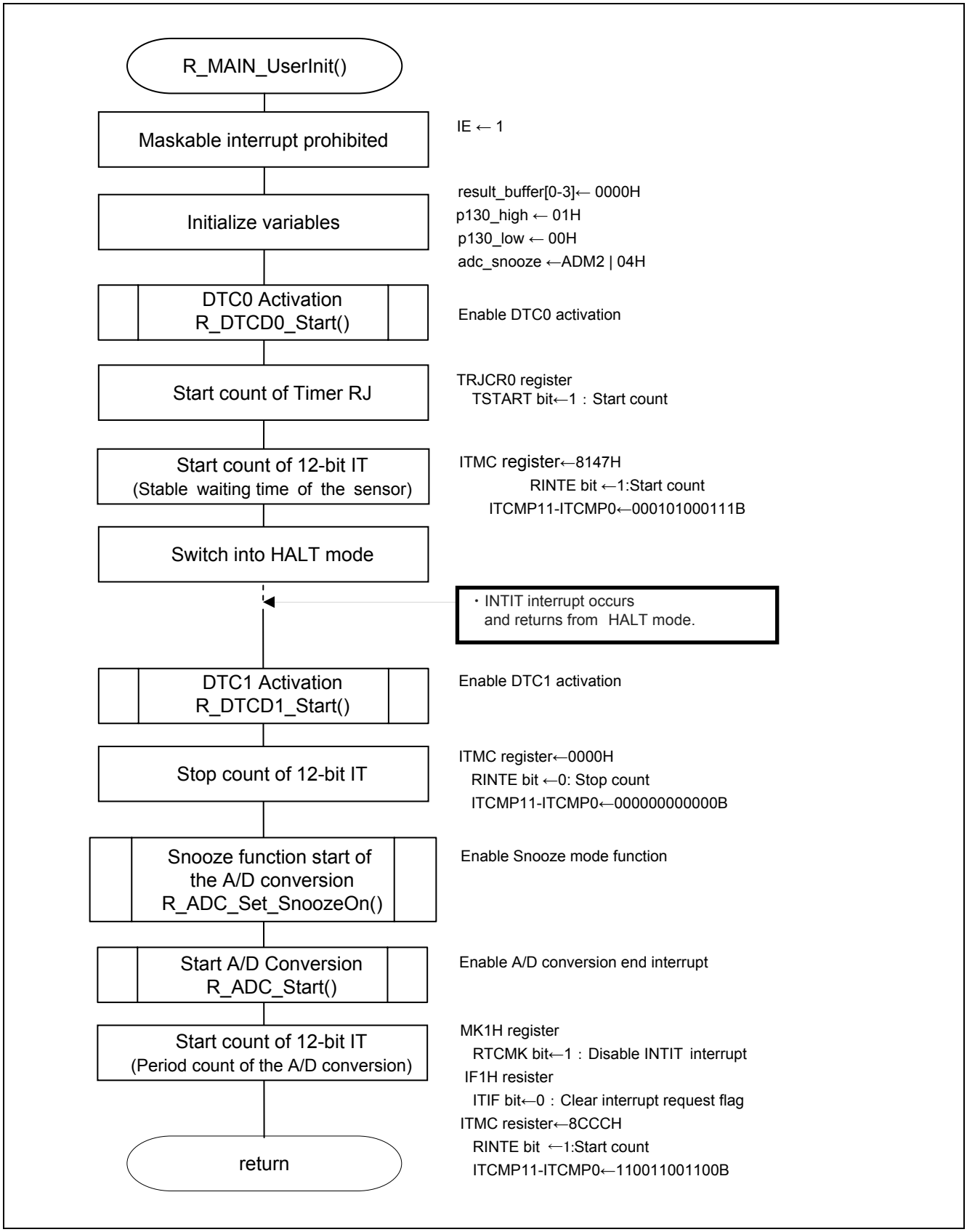


Figure 5.12 Initial setting of Main

Start count of Timer RJ

・Timer RJ Control Register 0（TRJCR0）
Start the count of Timer RJ.

Symbol：TRJCR0

7	6	5	4	3	2	1	0
0	0	TUNDF	TEDGF	0	TSTOP	TCSIF	TSTART
x	x	x	x	x	x	x	**1**

Bit 0

TSTART	Timer RJ count start
0	Count stops.
1	**Count starts.**

Start count of 12-bit IT (Stable waiting time of the sensor)

・12-bit interval timer control register (ITMC)
Start counter operation of 12-bit IT.

Symbol：ITMC

15	14	13	12	11 to 0
RINTE	0	RCLOE1	0	ITCMP11 to ITCMP0
1	x	x	x	**000101000111**

Bit 15

RINTE	12-bit interval timer operation control
0	Count operation stopped
1	**Count operation started**

Bit 11－5

ITCMP11 - ITCMP0	Specification of the 12-bit interval timer compare value
001H	**These bits generate a fixed-cycle interrupt (count clock cycles x (ITCMP setting + 1)).**
・・・	
147H	
・・・	
FFFH	
000H	Setting prohibit

Set up 12-bit IT interrupt

- Interrupt Request Flag Register (IF1H)
  Clear Interrupt Request Flag Register
- Interrupt mask flag register (MK1H)
  Disable interrupt servicing.

Symbol：IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	**0**	x	x

Bit 2

ITIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol：MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	**1**	x	x

Bit 2

ITMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Start count of 12-bit IT (Period count of the A/D conversion)

- 12-bit interval timer control register (ITMC)
  Start counter operation of 12-bit IT.

Symbol：ITMC

15	14	13	12	11 to 0
RINTE	0	RCLOE1	0	ITCMP 11 to ITCMP 0
1	x	x	x	**110011001100**

Bit 15

RINTE	12-bit interval timer operation control
0	Count operation stopped
1	**Count operation started**

Bit 11-5

ITCMP11 to ITCMP0	Specification of the 12-bit interval timer compare value
001H	**These bits generate a fixed-cycle interrupt (count clock cycles x (ITCMP setting + 1)).**
. . .	
CCCH	
. . .	
FFFH	
000H	Setting prohibited

5.7.11 DTC0 Activation

Figure 5.13 shows the DTC0 Activation.

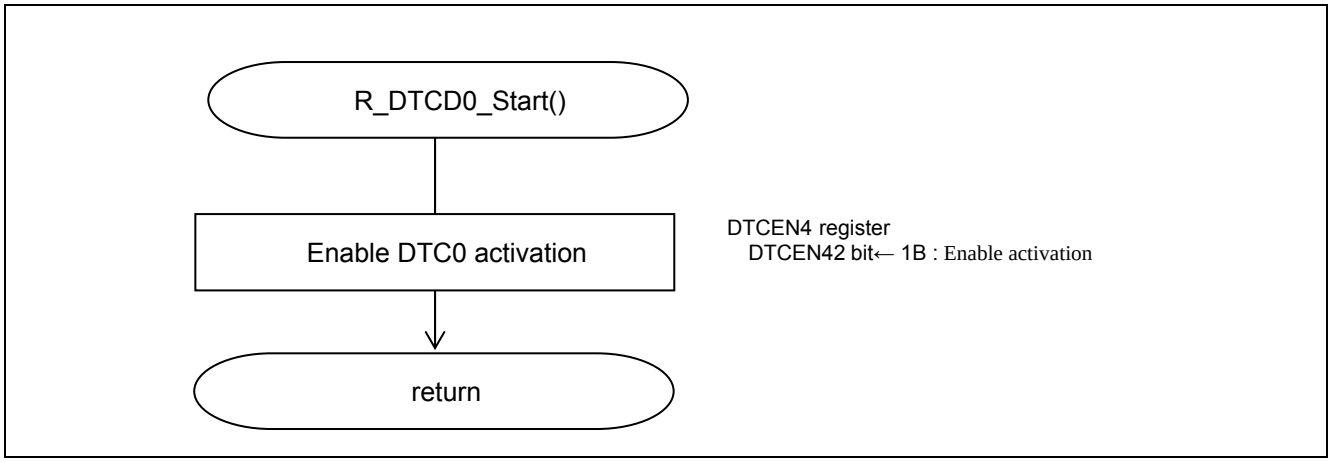


Figure 5.13 DTC0 Activation

Enable DTC0 activation

・DTC Activation Enable Register 4（DTCEN4）
Enable DTC activation.

Symbol：DTCEN4

7	6	5	4	3	2	1	0
DTCEN47	DTCEN46	DTCEN45	DTCEN44	DTCEN43	DTCEN42	DTCEN41	DTCEN40
0	**0**	**0**	**0**	**0**	**1**	**0**	**0**

Bit 2

DTCEN42	DTC activation enable 42
0	Activation disabled
1	**Activation enabled**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.12 DTC1 Activation

Figure 5.14 shows the DTC1 Activation.

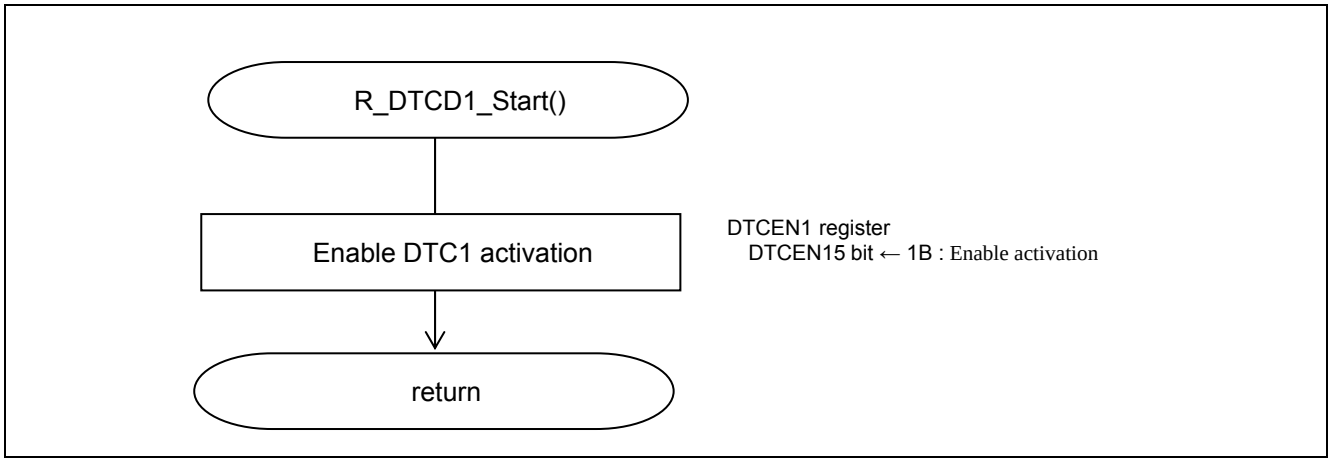


Figure 5.14 DTC1 Activation

Enable DTC1 activation

・DTC Activation Enable Register （DTCEN1）
Enable DTC activation.

Symbol：DTCEN1

7	6	5	4	3	2	1	0
DTCEN17	DTCEN16	DTCEN15	DTCEN14	DTCEN13	DTCEN12	DTCEN11	DTCEN10
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**

Bit 5

DTCEN15	DTC activation enable 15
0	Activation disabled
1	**Activation enabled**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.13 Permission to use SNOOZE mode function of A/D conversion

Figure 5.15 shows the permission to use SNOOZE mode function of A/D conversion.

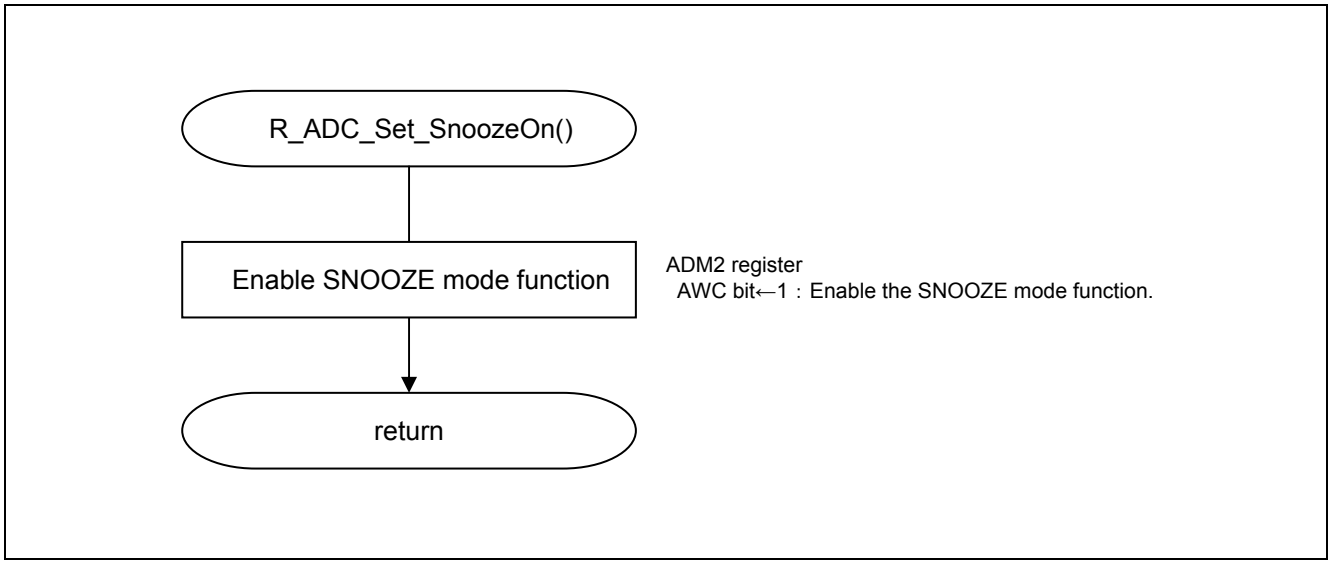


Figure 5.15 Permission to use SNOOZE mode function of A/D conversion

Start SNOOZE mode opertion

- A/D Converter Mode Register 2 (ADM2)
  Set up the SNOOZE mode.

Symbol：ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
x	x	x	x	x	**1**	x	x

Bit 2

AWC	Specification of the SNOOZE mode
0	Do not use the SNOOZE mode function.
1	**Use the SNOOZE mode function.**

5.7.14 Starting A/D Conversion

Figure 5.16 shows the Staring A/D Conversion.

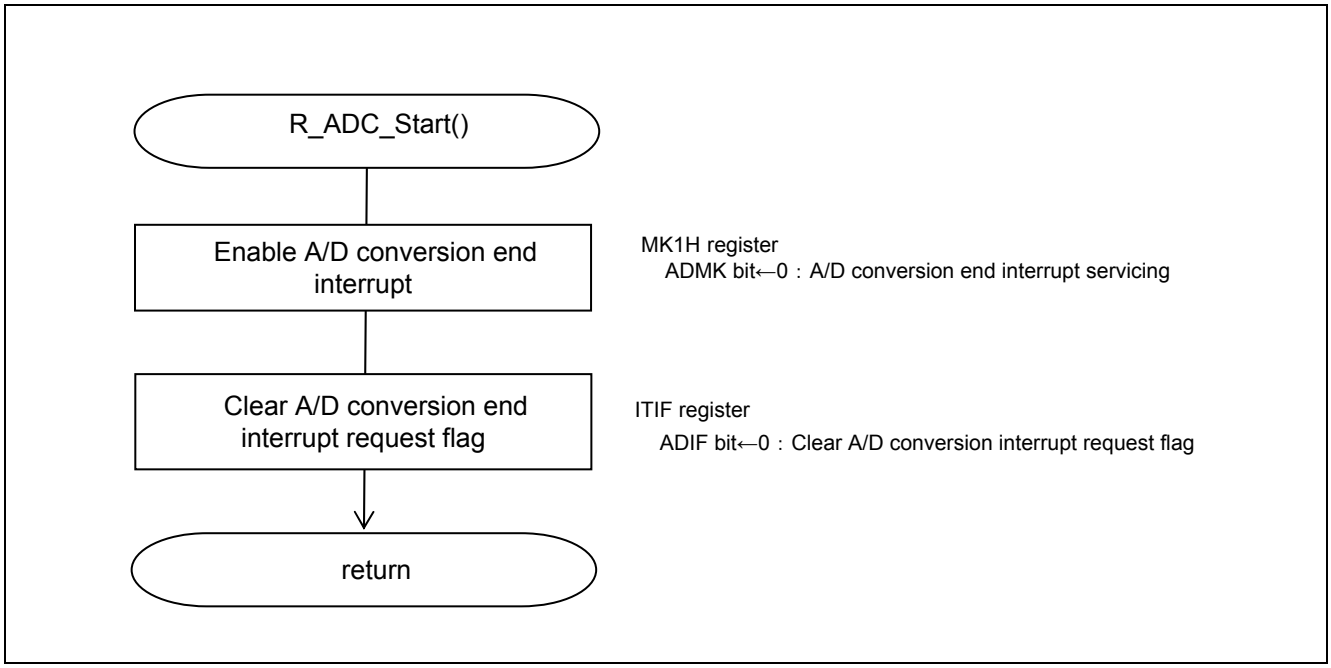


Figure 5.16 Starting A/D Conversion

Set up A/D conversion end interrupt

- Interrupt request flag register (IF1H)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Enable interrupt servicing

Symbol：IF1H

7	6	5	4	3	2	1	0
TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol：MK1H

7	6	5	4	3	2	1	0
TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	x	**0**

Bit 0

ADMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	**Interrupt servicing disabled**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.7.15 Setting count number of times of DTC

Figure 5.17 shows the Setting count number of times of DTC.

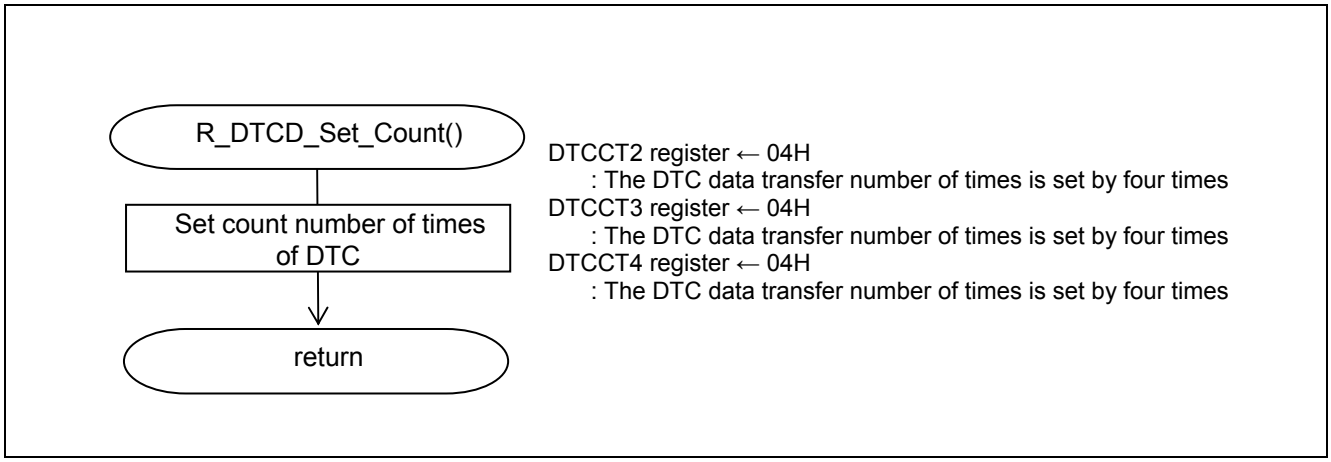


Figure 5.17 Setting count number of times of DTC

Set DTC transfer count register i (i=2~4)

- DTC Transfer Count Register i（DTCCTi）
  Set one time to the DTC transfer count register.

Symbol：DTCCTi

7	6	5	4	3	2	1	0
DTCCTi7	DTCCTi6	DTCCTi5	DTCCTi4	DTCCTi3	DTCCTi2	DTCCTi1	DTCCTi0
0	**0**	**0**	**0**	**0**	**1**	**0**	**0**

DTCCTi	Number of Transfers
00H	256 times
01H	Once
02H	2 times
03H	3 times
04H	**4 times**
・	・
FEH	254 times
FFH	255 times

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

RL78/G14 Group User's Manual: Hardware（R01UH0186E）

RL78 Family User's Manual: Software（R01US0015E）

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/G14 A/D conversion using DTC realizes the low-power consumption of the system

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 01, 2015	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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