RL78/G13

Timer Array Unit (Pulse Interval Measurement) CC-RL

R01AN2702EJ0300
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Introduction

This application note describes how the timer array unit (TAU) measures time intervals between pulses. This unit measures the time elapsed between pulses which arrive at the timer input pin (TI00). Then, it stores the measured value in the on-chip RAM.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note describes the measurement of time intervals between input pulses on channel 0 of the timer array unit 0 (TAU0). Each time a valid edge is detected on the timer input pin (TI00), the count value of the timer is captured to measure the pulse interval. The measurement result is stored in the on-chip RAM.

Table 1.1 shows the required peripheral functions and their uses. Figure 1.1 presents an overview of the pulse interval measurement.

Table 1.1 Required Peripheral Functions and Their Uses

Peripheral Function	Use
Timer array unit 0 (TAU0) channel 0	Measurement of the interval of the pulse input to the timer input pin (TI00)
TI00	Input pin for pulse signals

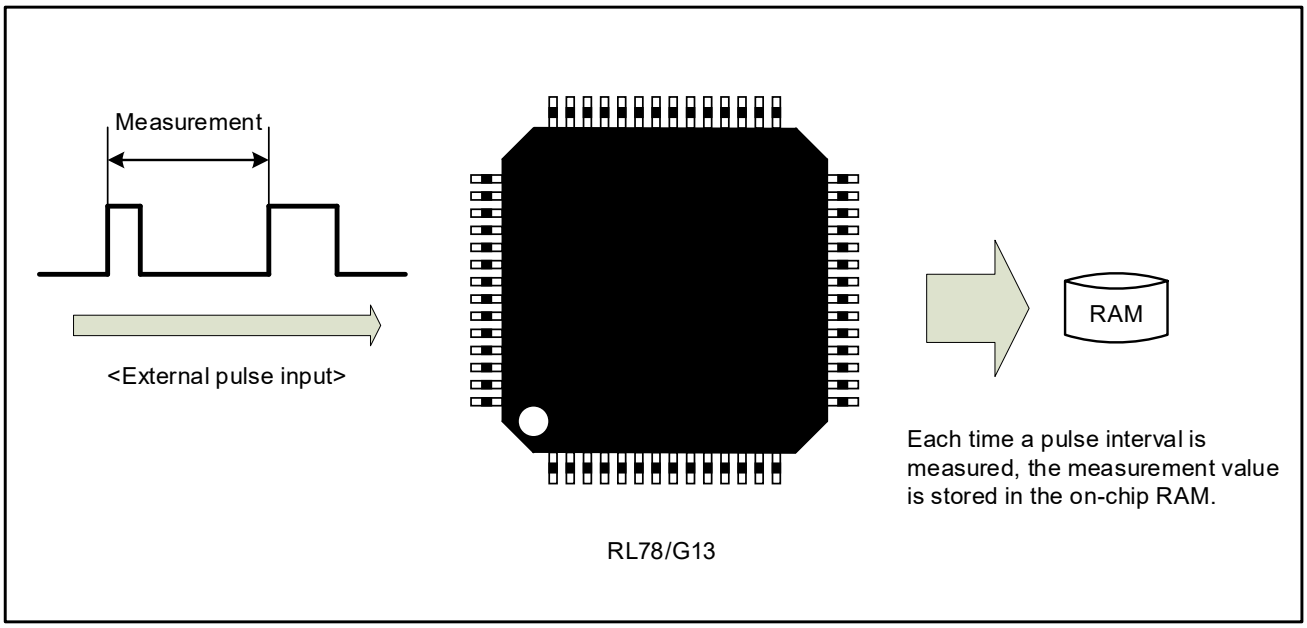

Figure 1.1 Overview of Pulse Interval Measurement

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
MCU used	RL78/G13 (R5F100LEA)
Board used	RL78/G13 (R5F100LE) Target Board (QB-R5F100LE-TB)
Operating frequency	High-speed on-chip oscillator clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	3.3 V (can be operated at 2.7 V to 5.5 V) LVD detection voltage: Reset mode At rising edge TYP. 2.81 V (2.76 V to 2.87 V) At falling edge TYP. 2.75 V (2.70 V to 2.81 V)
Integrated development environment (CS+)	CS+ V8.06.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.10.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2 studio V2021-07 (21.7.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.10.00 from Renesas Electronics Corp.
Code Generator Plug-in	CS+ Code Generator for RL78 (CS+ for CC) V2.21.00 from Renesas Electronics Corp.

3. Related Application Note

The application note that is related to this application note is listed below for reference.

- RL78/G13 Initialization CC-RL (R01AN2575E) Application Note
- RL78/G13 Timer Array Unit (Pulse Interval Measurement (Both edges)) CC-RL (R01AN4259E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for the application note.

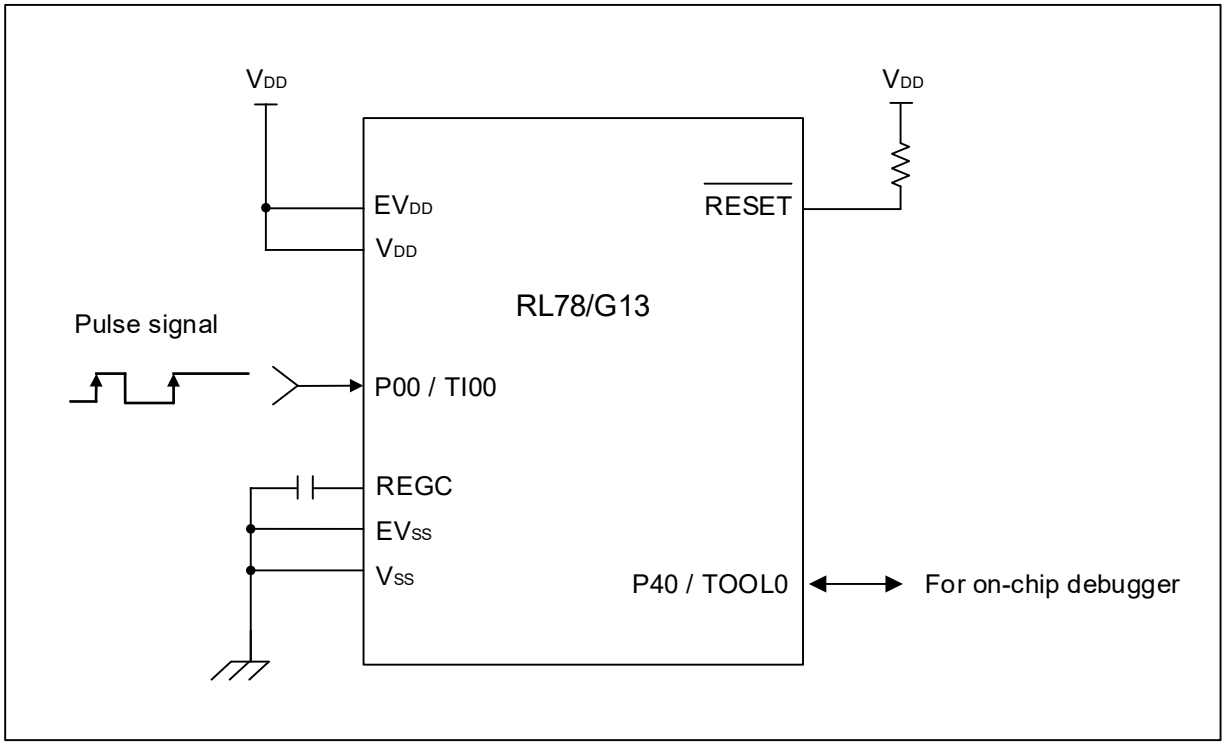

Figure 4.1 Hardware Configuration

Notes: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to VDD or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 Pin to be Used

Table 4.1 shows the pin to be used and its function.

Table 4.1 Pin to be Used and Its Function

Pin Name	I/O	Description
P00 / TI00	Input	Timer input pin of Timer array unit 0 channel 0

5. Description of the Software

5.1 Operation Outline

In this sample code, each time a rising edge (valid edge) is detected on the timer input pin (TI00), the counter value of the timer is captured and the pulse interval of the pulse input to the timer input pin (TI00) is measured.

To measure the pulse interval accurately, the capture end interrupts (INTTM00) of Timer array unit 0 channel 0 after the first capture end interrupt are used. When capture end interrupts occur after the first capture end interrupt, the measured pulse intervals are stored in the variable in the on-chip RAM.

(1) Initialize Timer Array Unit 0 (TAU0).

- Use the P00/TI00 pin for the inputting capture trigger.
- Set the operation clock of TAU0 channel 0 to f_{CLK}.
- Set TAU0 channel 0 to the capture mode.
- Set the TI00 pin input valid edge to “Rising edge”.
- Set the capture trigger of TAU0 channel 0 to “Valid edge of the TI00 pin input”.
- Use the capture end interrupt (INTTM00) from TAU0 channel 0.

(2) Set the TS00 bit of the timer channel start register 0 (TS0) to 1 to enable count operation. This clears the timer count register (TCR00) to 0000H and starts counting.

(3) Switch to a HALT mode and wait for a detection of a valid edge.

(4) When a valid edge is detected, the count value of the TCR00 register is captured to the timer data register (TDR00), at the same time, the TCR00 register is cleared to 0000H, and the capture end interrupt (INTTM00) is requested, and then a HALT mode is released. After a HALT mode is released, the capture end interrupt request flag is cleared. The first capture value of the TDR00 register is invalid and cannot be used.

(5) Set the numbers of measurement times of the pulse interval.

(6) Enable interrupt requests.

(7) Switch to a HALT mode and wait for a detection of a valid edge.

(8) When a valid edge is detected, a HALT mode is released, and in the capture end interrupt processing, the capture value of the TDR00 register is temporarily stored in the on-chip RAM, and then the captured value is stored in the variable in the on-chip RAM.

(9) Repeat steps (7) to (8) until pulse intervals are measured eight times.

(10) After the measurement of the setting number is finished, set the TT00 bit of the timer channel stop register 0 (TT0) to 1 to disable count operation, and switch to a HALT mode.

5.2 List of Option Byte Settings

Table 5.1 shows the option byte settings. Set the values that are most suited to your system as necessary.

Table 5.1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 010C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 010C1H	01111111B	LVD detection voltage: reset mode At rising edge TYP. 2.81 V (2.76 V to 2.87 V) At falling edge TYP. 2.75 V (2.70 V to 2.81 V)
000C2H / 010C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 010C3H	10000100B	Enables on-chip debugging

5.3 List of Constants

Table 5.2 lists the constant that is used in this sample program.

Table 5.2 Constant for the Sample Program

Constant	Setting	Description
_0001_TAU_OVERFLOW_OCCURS	0x0001U	Detects an overflow

5.4 List of Variables

Table 5.3 lists the global variables.

Table 5.3 Global Variables

Type	Variable Name	Description	Function Used
uint8_t	g_times	Number of times to measure the pulse interval	main r_tau0_channel0_interrupt
__saddr uint32_t	g_pulse_width[8]	Storage of measurement values of pulse intervals	main r_tau0_channel0_interrupt
volatile uint32_t	g_tau0_ch0_width	Temporary storage of the measurement value of pulse interval	r_tau0_channel0_interrupt t

5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_TAU0_Channel0_Start	Timer Array Unit 0 channel 0 start processing
R_TAU0_Channel0_Stop	Timer Array Unit 0 channel 0 stop processing
r_tau0_channel0_interrupt	Timer Array Unit 0 channel 0 INTTM00 interrupt processing

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] R_TAU0_Channel0_Start	
Outline	Timer Array Unit 0 channel 0 start processing
Header	#include "r_cg_macrodriver.h" #include "r_cg_timer.h" #include "r_cg_userdefine.h"
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel0_Stop	
Outline	Timer Array Unit 0 channel 0 stop processing
Header	#include "r_cg_macrodriver.h" #include "r_cg_timer.h" #include "r_cg_userdefine.h"
Declaration	void R_TAU0_Channel0_stop(void)
Explanation	This function stops count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tau0_channel0_interrupt	
Outline	Timer Array Unit 0 channel 0 INTTM00 interrupt processing
Header	#include "r_cg_macrodriver.h" #include "r_cg_timer.h" #include "r_cg_userdefine.h"
Declaration	static void __near r_tau0_channel0_interrupt(void)
Explanation	This function stores the measured value of the pulse time interval into g_pulse_width[].
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

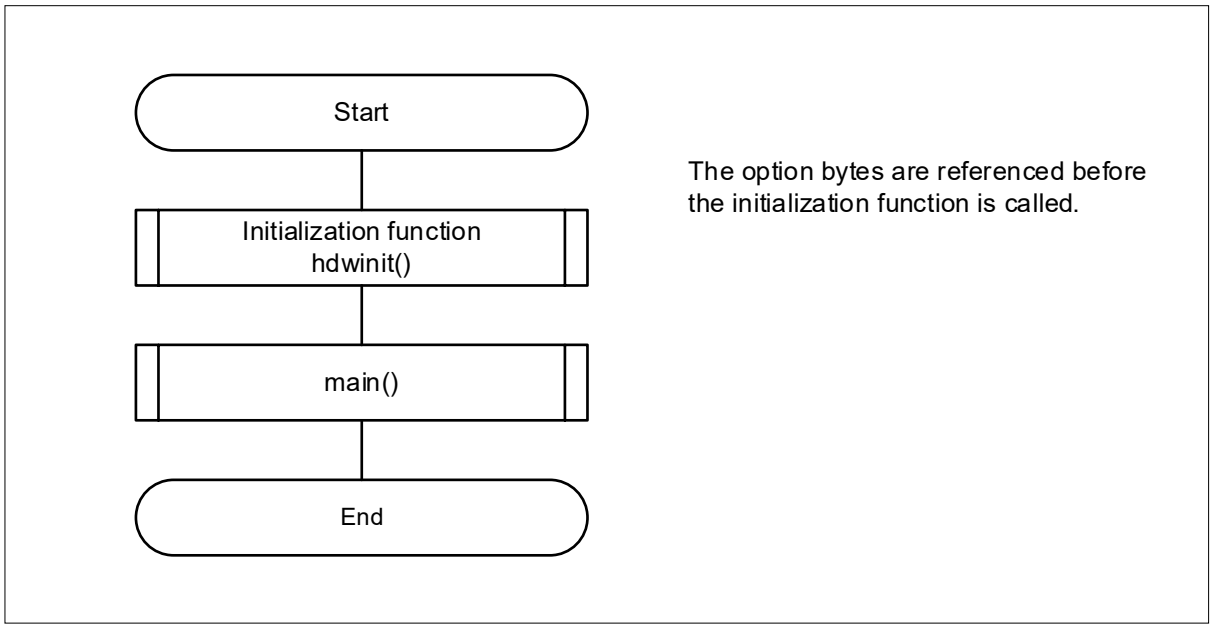

Figure 5.1 Overall Flow

Note: Startup routine is executed before and after the initialization function.

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

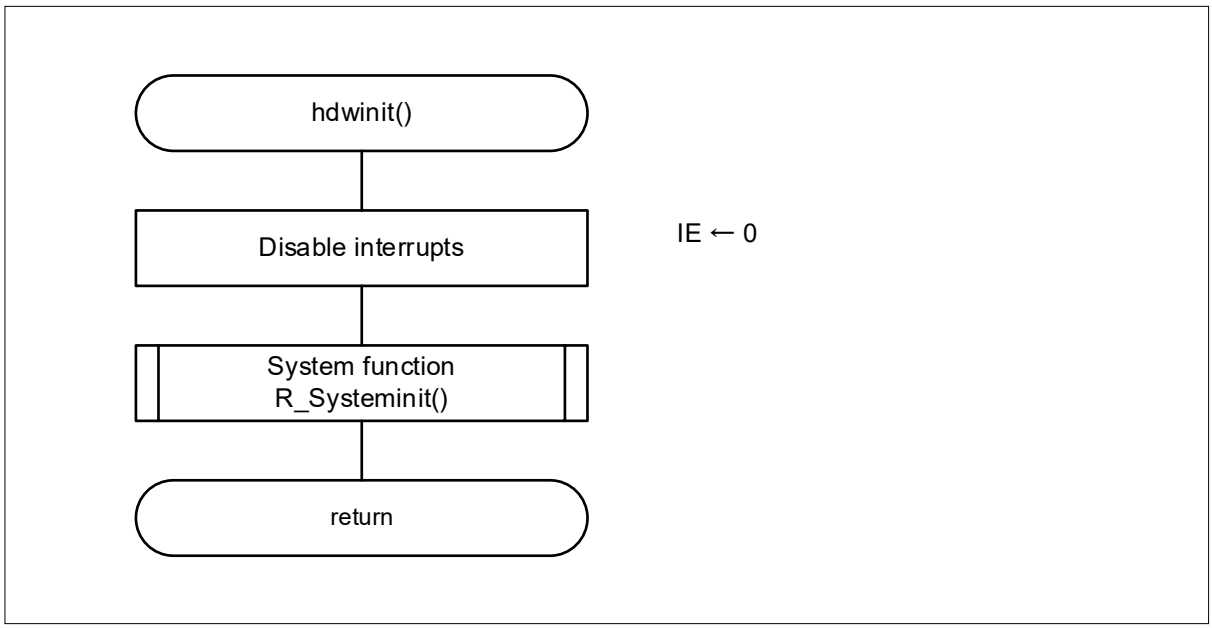

Figure 5.2 Initialization Function

5.7.2 System Function

Figure 5.3 shows the flowchart for the system function.

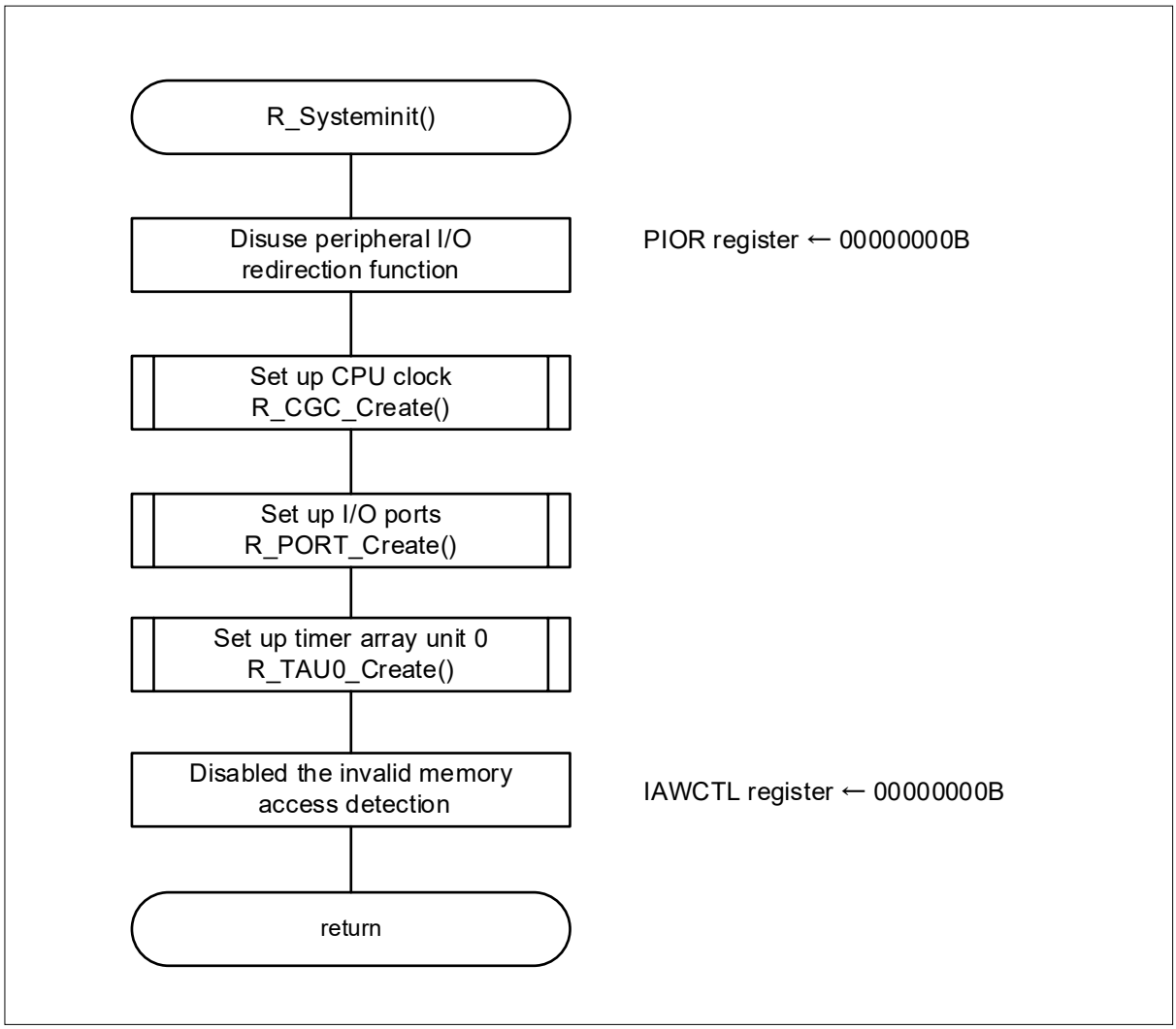

Figure 5.3 System Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

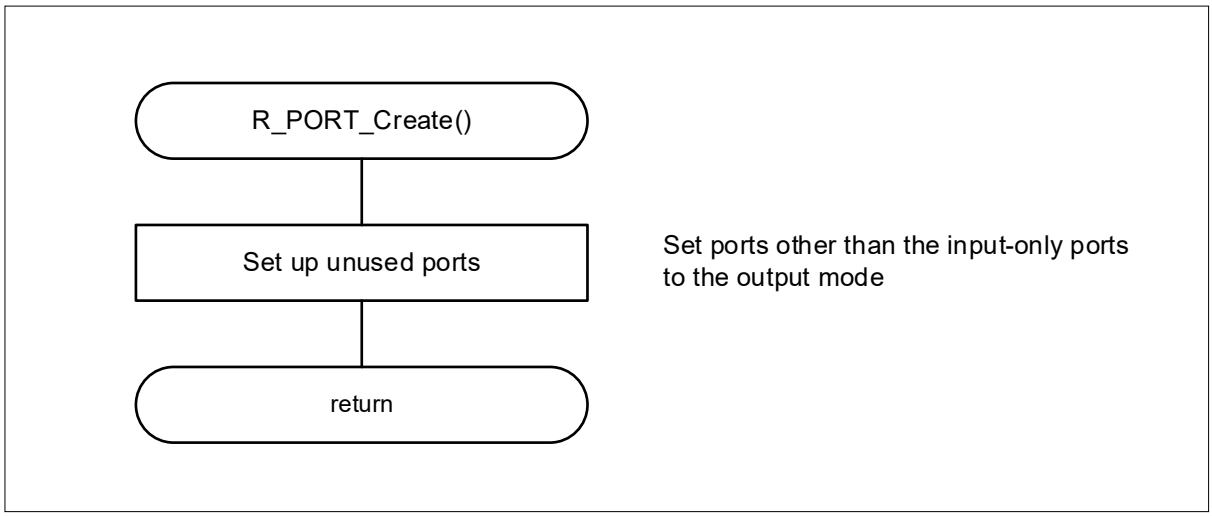

Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

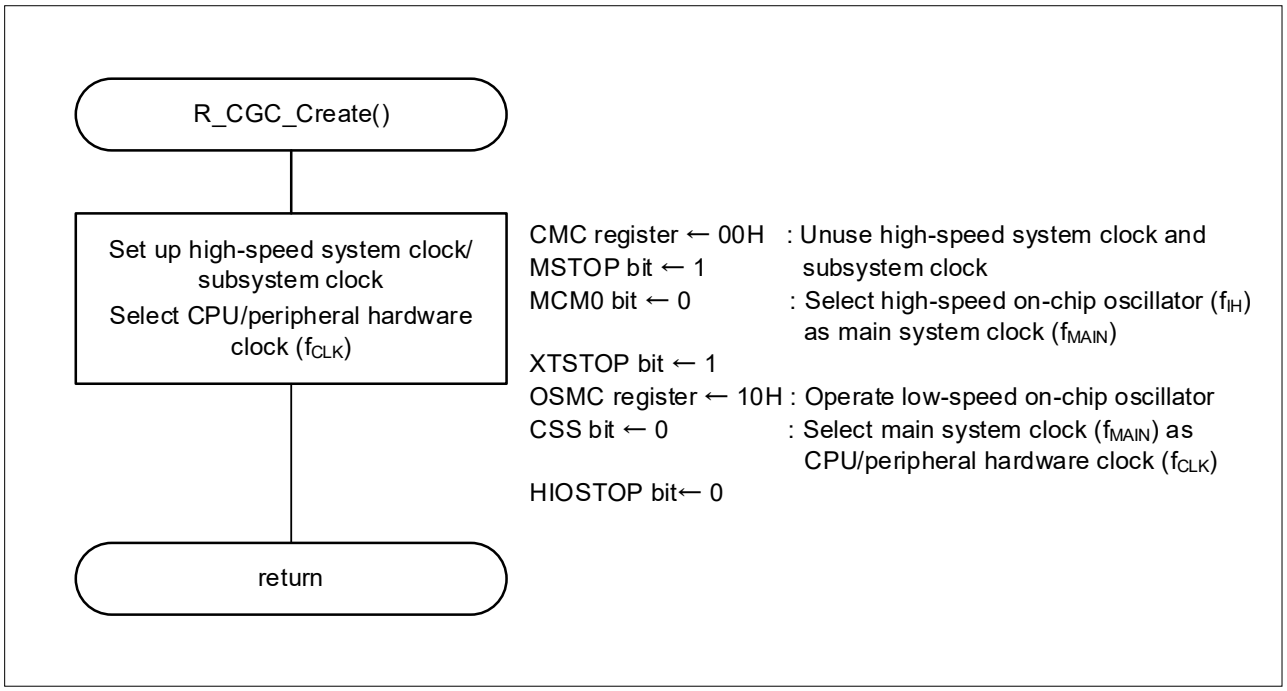

Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 Timer Array Unit 0 Setup

Figure 5.6 shows the flowchart for setting up the timer array unit 0 (TAU0).

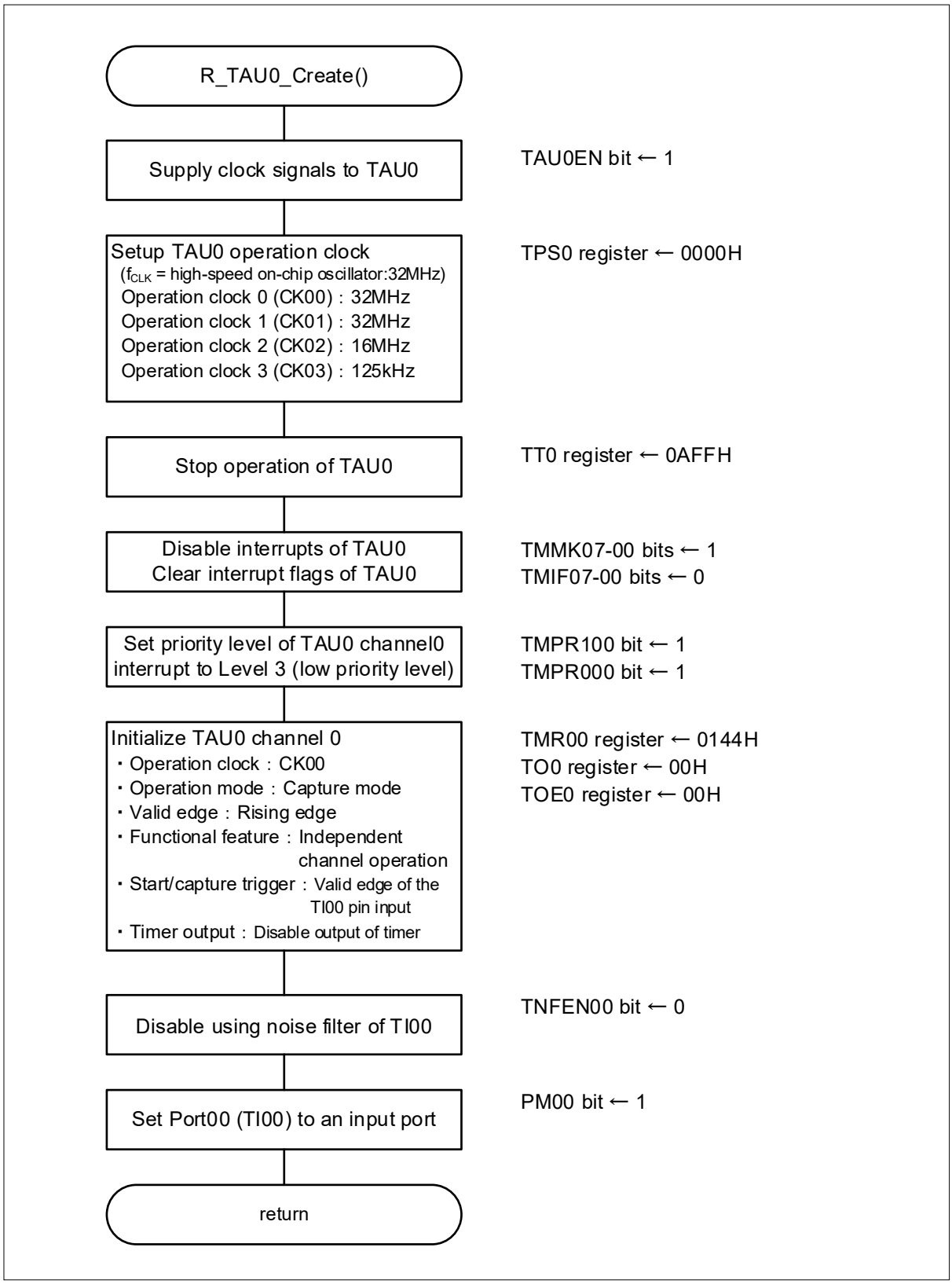

Figure 5.6 Timer Array Unit 0 Setup

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)
  Supply clock signals to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
0	0	0	0	0	0	0	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the clock frequency

- Timer clock select register 0 (TPS0)
  Select the CK00 operation clock.

  Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	**0**	**0**	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	**2 MHz**	**5 MHz**	**10 MHz**	**20 MHz**	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Controlling the channel trigger operation

- Timer channel stop register 0 (TT0)
  Select the TAU0 stop trigger.

  Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TT H03	0	TT H01	0	TT 07	TT 06	TT 05	TT 04	TT 03	TT 02	TT 01	TT 00
0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	**1**

Bits 7 to 0

TT0n	Operation stop trigger (n=0-7)
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).**

Bits 11 and 9

TTH0n	Operation stop trigger (n=1,3 8-bit timer mode)
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00)
  Specify the operation mode, edge, trigger, channel and clocks.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**1**	**0**	**1**	0	0	**0**	**1**	**0**	**0**

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock f_{MCK} specified with the CKS000 and CKS001 bits**
1	Valid edge of the input signal from the TI00 pin

Bits 10 to 8

STS 002	STS 001	STS 000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	**0**	**1**	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**1**	**0**	**1**	0	0	**0**	**1**	**0**	**0**

Bits 7 and 6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	**1**	**Rising edge**
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bits 3 to 0

MD 003	MD 002	MD 001	MD 000	Channel 0 operation mode setup
0	0	0	0	Interval timer mode. Does not generate a timer interrupt at the start of count operation.
			1	Interval timer mode. Generates a timer interrupt at the start of count operation.
0	**1**	**0**	**0**	**Capture mode** **Does not generate a timer interrupt at the start of count operation.**
			1	Capture mode Generates a timer interrupt at the start of count operation.
0	1	1	0	Event counter mode Does not generate a timer interrupt at the start of count operation.
1	0	0	0	One-count mode Disables the start trigger during count operation.
			1	One-count mode Enables the start trigger during count operation.
1	1	0	0	Capture & one-count mode Does not generate a timer interrupt at the start of count operation. Disables the start trigger during count operation.

5.7.6 Main Processing

Figure 5.7 shows the flowchart for main processing.

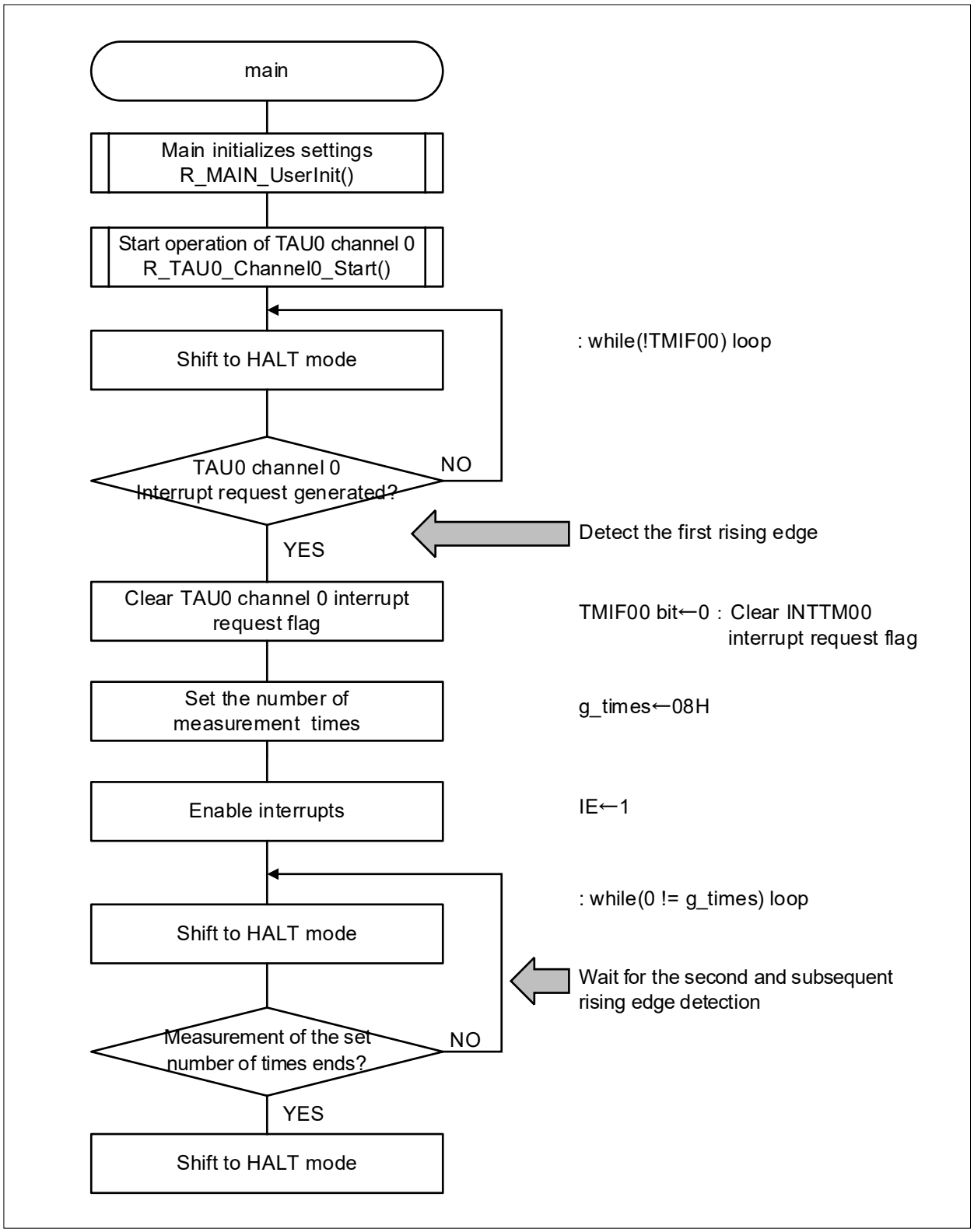

Figure 5.7 Main Processing

5.7.7 Main Initializes Settings

Figure 5.8 shows the flowchart for the main initializes settings.

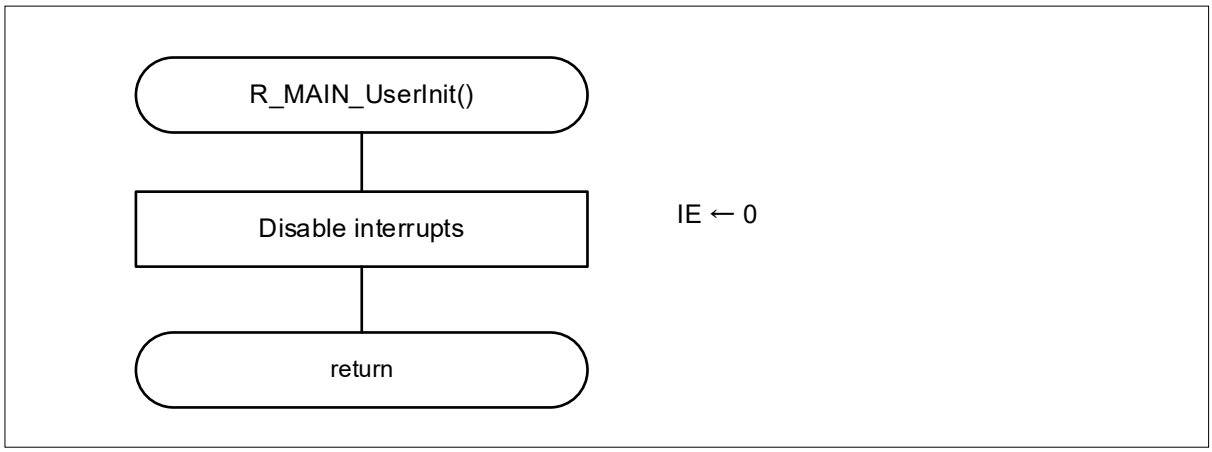

Figure 5.8 Main Initializes Settings

5.7.8 Timer Array Unit 0 Channel 0 Start Processing

Figure 5.9 shows the flowchart for starting the operation of channel 0 of the timer array unit 0.

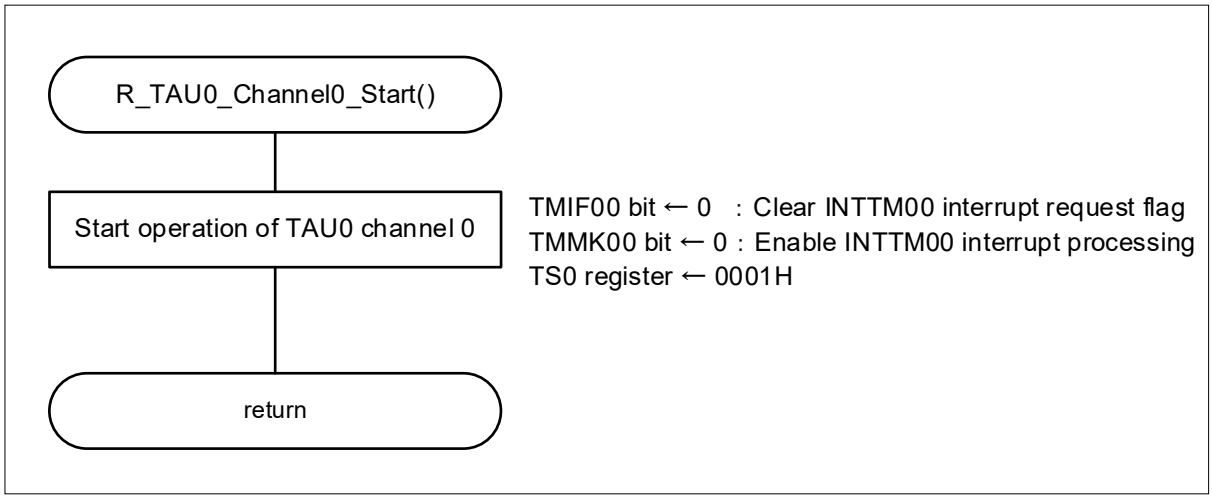

Figure 5.9 Timer Array Unit 0 Channel 0 Start Processing

Configuring the interrupt request flag

- Clear the timer interrupt request flag.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
0/1	0/1	0/1	**0**	0/1	0/1	0/1	0/1

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the interrupt mask

- Unmask timer interrupts.

Symbol: MK1L

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
0/1	0/1	0/1	**0**	0/1	0/1	0/1	0/1

Bit 4

TMMK00	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the timer channel startup

- Enable timer count operation.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TS H03	0	TS H01	0	TS 07	TS 06	TS 05	TS 04	TS 03	TS 02	TS 01	TS 00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.9 INTTM0 Interrupt Processing

Figure 5.10 shows the flowchart for INTTM00 interrupt processing.

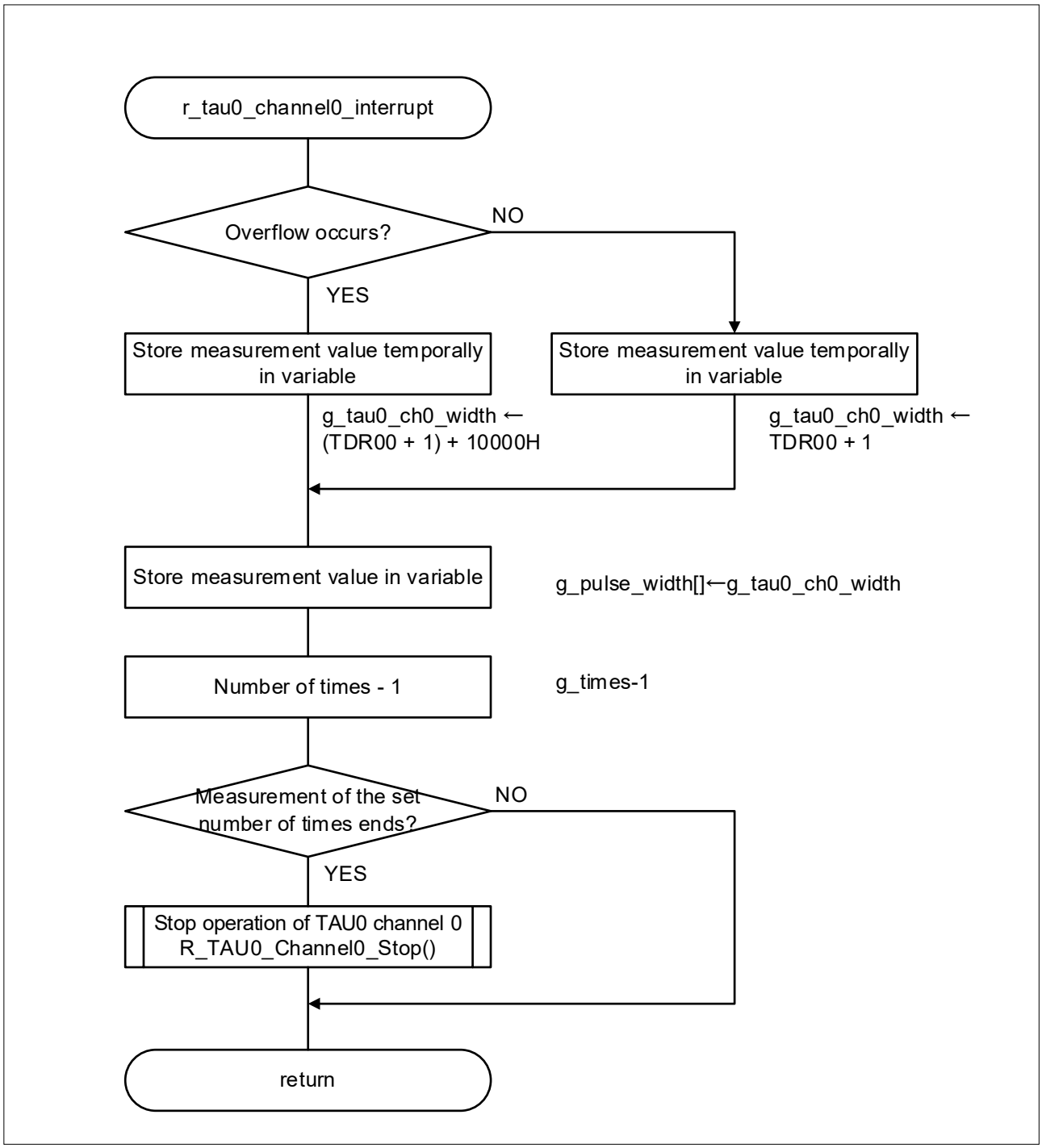

Figure 5.10 INTTM00 Interrupt Processing

5.7.10 Timer Array Unit 0 Channel 0 Stop Processing

Figure 5.11 shows the flowchart for stop the operation of the channel 0 of the timer array unit.

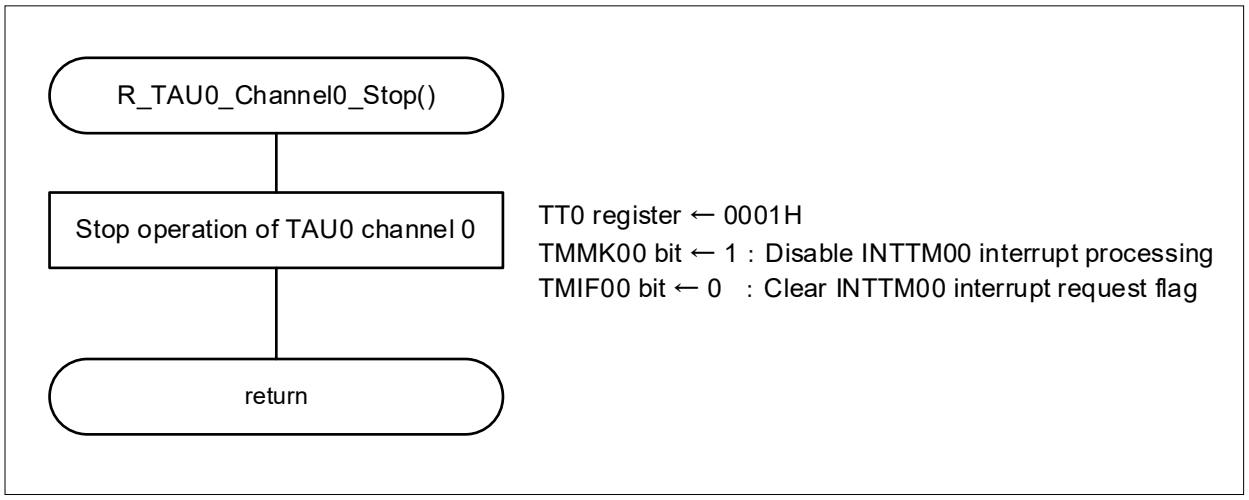

Figure 5.11 Timer Array Unit 0 Channel 0 Stop Processing

Configuring the timer channel stop

- Stop timer count operation.

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TT H03	0	TT H01	0	TT 07	TT 06	TT 05	TT 04	TT 03	TT 02	TT 01	TT 00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**

Bit 0

TT00	Operation stop trigger of channel 0
0	No trigger operation
1	**The TE00 bit is cleared to 0 and the count operation stopped.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

RL78/G13 User's Manual: Hardware (R01UH0146J)
RL78 family user's manual software (R01US0015J)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun.01, 2015	-	First Edition
2.00	Jul. 01, 2015	4	Table2.1: Added e2 studio
3.00	Aug 16, 2021	Throughout	Change from Timer Array Unit to Timer Array Unit 0
		4	Change of 2. Operation Check Conditions
		4	Change of 3. Related Application Note
		5	Change of Description in Table 4.1 Pin to be Used and Its Function
		6	Change of 5.1 Operation Outline
		7	Change of 5.2 List of Option Byte Settings
		7	Change of Description in Table 5.3 Global Variables
		8	Change of Table 5.4 Functions
		8	Change of outlines in 5.6 Function Specifications
		11	Change of Figure 5.4 I/O Port Setup
		12	Change of Figure 5.5 CPU clock Setup
		13	Change of Figure 5.6 Timer Array Unit 0 Setup
		15	Change of the table of Configuration the clock frequency
		15	Change of the table of Controlling the channel trigger operation
		18	Change of Figure 5.7 Main Processing
		19	Change of the title of 5.7.8
		19	Change of Figure 5.9 Timer Array Unit 0 Channel 0 Start Processing
		22	Change of Figure 5.10 INTTM00 Interrupt Processing
		23	Change of the title of 5.7.10
		23	Change of Figure 5.11 Timer Array Unit 0 Channel 0 Stop Processing

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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