

RL78/G13

Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

R01AN0460EJ0200

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Introduction

This application note describes how the serial array unit (SAU) performs master transmission and reception by 3-wire serial I/O communication (CSI). Using the CSI, this unit transmits data 0x05 and 0x50 alternately to the slave and receives data from the slave.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specifications

The serial array unit (SAU) described in this application note performs master transmission and reception by 3-wire serial I/O communication (CSI). As the CSI master, this unit supplies clock signals to the slave, transmits data 0x05 and 0x50 alternately to the slave, and receives data from the slave.

Table 1.1 lists the peripheral functions to be used and their uses. Figure 1.1 presents an overview of CSI operation.

Figures 1.2 and 1.3 show timing charts for explaining the CSI communication.

Table 1.1 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Serial array unit 0 channel 0	CSI00 master transmission/reception
Timer array unit 0 channel 0	Interval timer operation

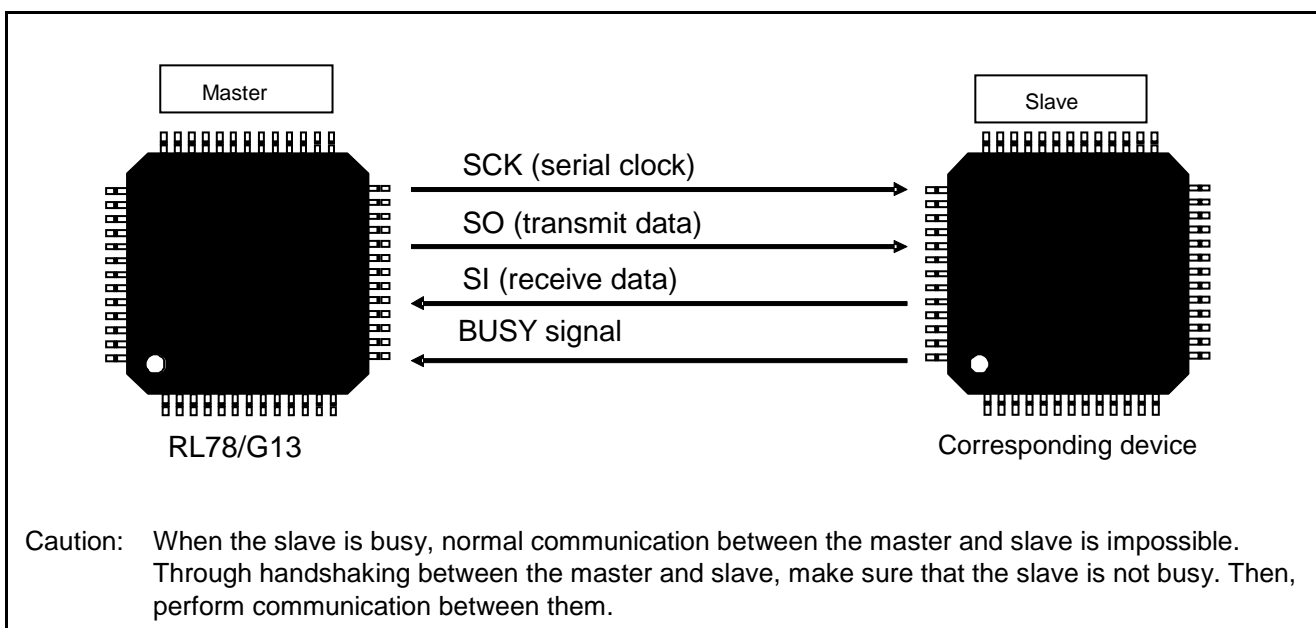


Figure 1.1 Overview of CSI Operation

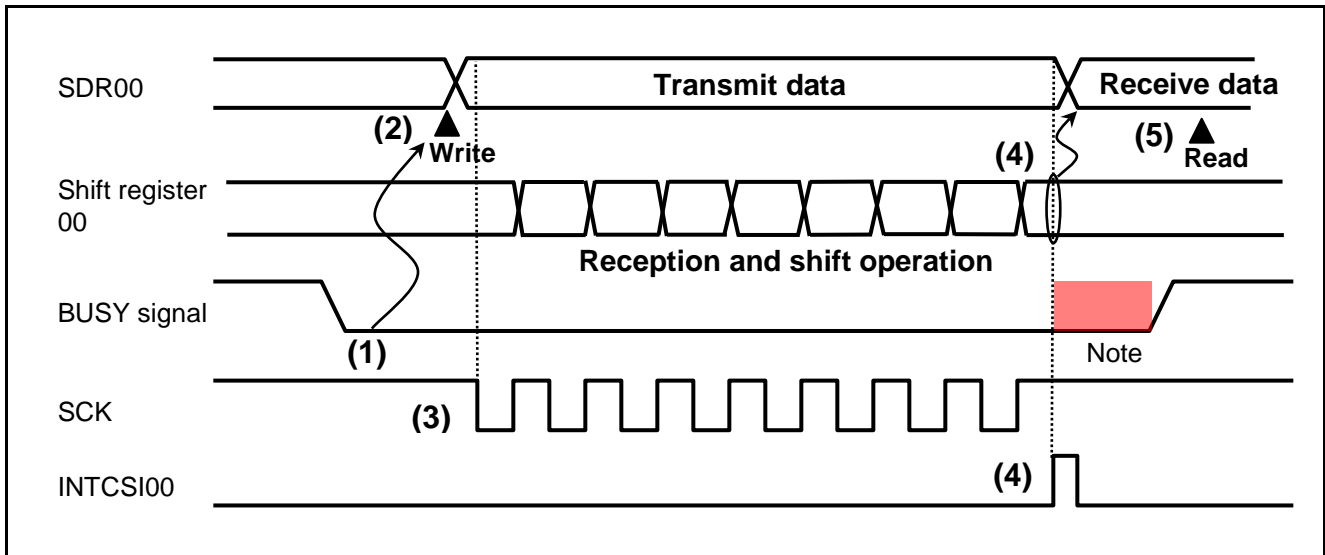


Figure 1.2 Handshake Operation and Communication

- (1) [Software processing] Make sure that the slave is not busy.
- (2) [Software processing] Write transmit data to the SDR00 register and then start CSI00 transmission/reception.
- (3) [Hardware processing] Write data to the SDR00 register, output serial clock signals, and then enter the communication status.
- (4) [Hardware processing] Transfer receive data from the shift register 00 to the SDR00 register and then generate a transfer end interrupt.
- (5) [Software processing] Read the receive data from the SDR00 register.

Note: If the transmission/reception is restarted before the BUSY signal from the slave rises, the expected results may not be obtained. As an example of master operation to prevent this phenomenon, the timing chart (Figure 1.3) shows operation using the falling edge of the BUSY signal.

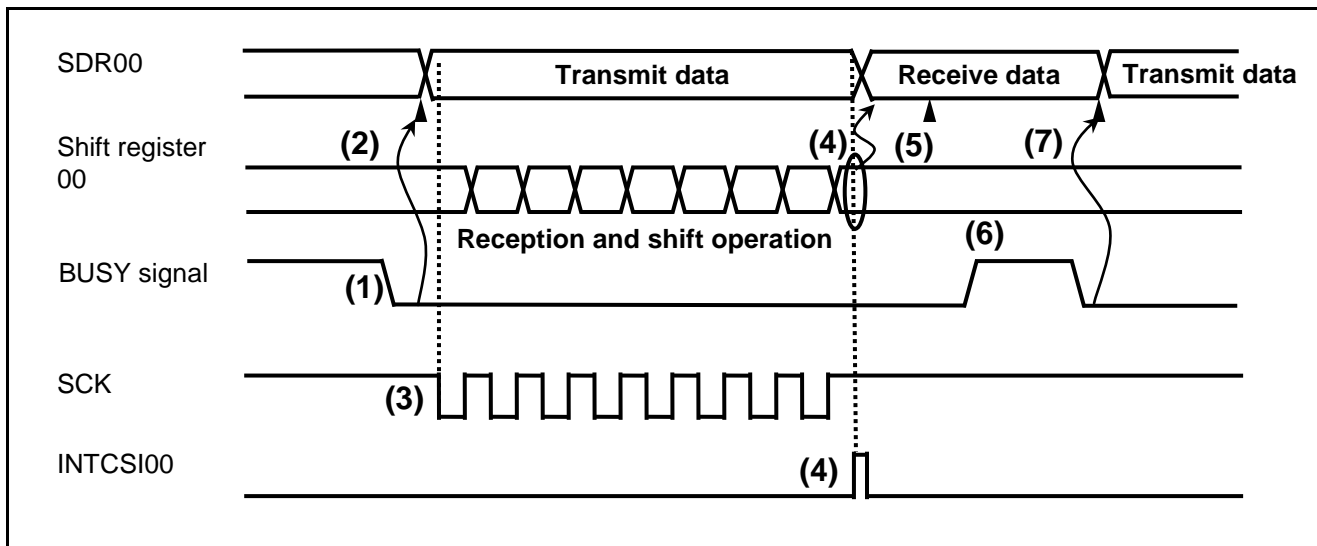


Figure 1.3 Example of BUSY Signal Edge Detection in the Master

- BUSY signal edge detection

In this example, the master starts communication upon detection of the falling edge of the BUSY signal from the slave.

- (1) [Software processing in the slave] Write the next transmit data to the master and make the BUSY signal fall.
- (2) [Software processing in the master] Detect the falling edge of the BUSY signal and write transmit data to the SDR00 register.
- (3) [Hardware processing in the master] Start transmission/reception and then output serial clock (SCK) signals.
- (4) [Hardware processing in the master] After completion of the transfer, set the value of shift register 00 in the SDR00 register and then generate a transfer end interrupt (INTCSI00).
- (5) [Software processing in the master] Read the receive data from the SDR00 register.
- (6) [Software processing in the master] Wait until the falling edge of the BUSY signal is detected. ^{Note}
- (7) [Software processing in the master] Detect the falling edge of the BUSY signal and then write the transmit data to the SDR00 register.

Note: If the BUSY signal is held at the high level for a short period, the software may be unable to detect the edge. In this case, input the BUSY signal to an external interrupt pin (such as the INTP0 pin) so that the hardware detects the edge.

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	<ul style="list-style-type: none">High-speed on-chip oscillator (HOCO) clock: 32 MHzCPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (VLVI): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CubeSuite+)	CubeSuite+ V1.00.01 from Renesas Electronics Corp.
C compiler (CubeSuite+)	CA78K0R V1.20 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2.0.1.3 from Renesas Electronics Corp.
C compiler (e2studio)	KPIT GNURL78-ELF Toolchain V13.02 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V1.30.2
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V1.30.2

3. Related Application Note

The application note that is related to this application note is listed below for reference.

- RL78/G13 Initialization (R01AN0451EJ0100) Application Note
- RL78/G13 Timer Array Unit Interval Timer (R01AN0456J) Application Note
- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Slave Transmission/Reception) (R01AN0461EJ0100) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

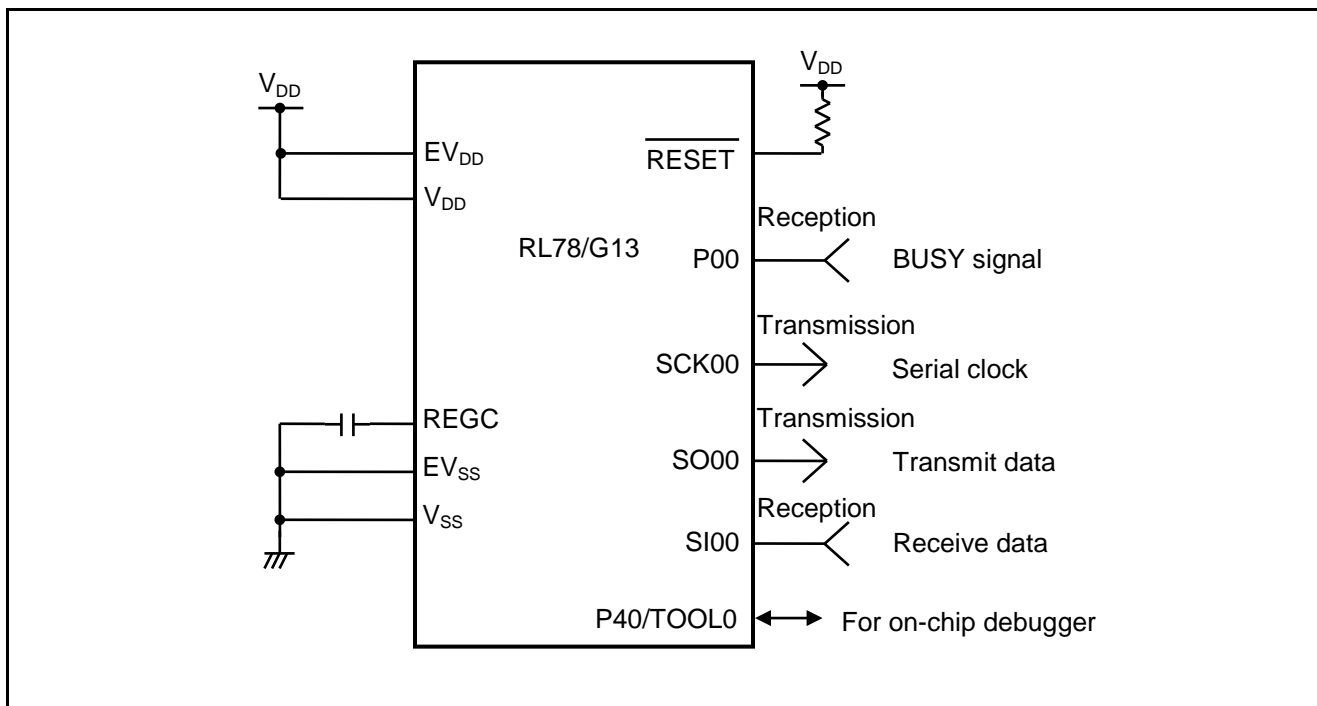


Figure 4.1 Hardware Configuration

- Cautions:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
 2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD} , respectively.
 3. V_{DD} must be held at not lower than the reset release voltage (V_{LVI}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P10/SCK00/SCL00	Output	Serial clock output pin
P11/SI00/RxD0/TOOL RxD/SDA00	Input	Data reception pin
P12/SO00/TxD0/TOOLTxD	Output	Data transmission pin
P00/ANI17/TI00/TxD1	Input	BUSY signal detection pin

5. Description of the Software

5.1 Operation Outline

The sample program covered in this application note transmits and receives data to and from the corresponding device (slave) via the CSI (master transmission/reception). It supplies clock signals to the slave, transmits data (0x05 or 0x50) to the slave, and receives data from the slave at intervals of about 10 ms. This communication is performed in full-duplex mode.

(1) Initialize SAU0.

<Conditions for setting>

- Use SAU0 channel 0 as the CSI.
- Set the serial clock frequency to about 312,500 Hz.
- Select the single transfer mode as the operation mode.
- Select type 1 as the phase between data and clock signals.
- Set data transfer order to the MSB first.
- The length of data should be 8 bits.
- A serial transfer end interrupt (INTCSI00) should occur in single transfer mode.
- Use the P10/SCK00 pin for clock output and set the initial output value to 1.
- Use the P12/SO00 pin for data output and set the initial output value to 1.
- Use the P11/SI00 pin for data input.
- Enable output for serial communication.

(2) Controlling the communication interval (10 ms) uses the interval timer function of the timer array unit (TAU) channel 0. The system starts the interval timer and then executes a HALT instruction. When the system is in HALT mode, it waits for the occurrence of a timer interrupt (INTTM00).

(3) When a timer count end interrupt occurs and moreover the system exits the HALT mode, the system checks whether communication is possible. If the communication is possible, the system transmits/receives data. If no communication is underway and moreover the slave is not busy, the system determines that communication is possible and transmits/receives data.

(4) When data transmission/reception is already completed or if communication is impossible, the system executes the HALT instruction again. Then, the system enters HALT mode to wait for the occurrence of a timer interrupt (INTTM00).

Caution: For information about timer array unit setup, refer to the RL78/G13 Timer Array Unit Interval Timer (R01AN0456J) Application Note.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode, 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
_0001_TAU_CH0_START_TRG_ON	0x0001U	Enables TAU0 channel 0 operation.
_0100_SAU_CH0_CLOCK_OUTPUT_1	0x0100U	Sets the serial clock output value for SAU0 channel 0.
_0001_SAU_CH0_DATA_OUTPUT_1	0x0001U	Sets the serial data output value for SAU0 channel 0.
_0001_SAU_CH0_OUTPUT_ENABLE	0x0001U	Enables output for SAU0 channel 0 serial communication.
_0001_SAU_CH0_START_TRG_ON	0x0001U	Starts SAU0 channel 0 operation.
_0001_SAU_OVERRUN_ERROR	0x0001U	Acquires the overrun error detection flag for SAU0 channel 0.

5.4 List of Variables

Table 5.3 lists the global variables that are used in this sample program.

Table 5.3 Global Variables for the Sample Program

Type	Variable Name	Contents	Function Used
unsigned char	tx_data	Serial transmit data	main()
unsigned char	rx_data	Serial receive data	main()
uint8_t	gp_Csi00RxAddress	CSI00 receive buffer address	R_CSI00_Send_Receive() R_CSI00_Interrupt()
uint8_t	gp_Csi00TxAddress	CSI00 transmit buffer address	R_CSI00_Send_Receive() R_CSI00_Interrupt()
uint16_t	g_Csi00TxCnt	CSI00 transmit data size	R_CSI00_Send_Receive() R_CSI00_Interrupt()

5.5 List of Functions

Table 5.4 summarizes the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_TAU0_Channel0_Start	Starts TAU0 channel 0 operation.
R_CSI00_Start	Starts CSI00 operation.
R_CSI00_Send_Receive	CSI00 data transmission/reception function
R_CSI00_Interrupt	CSI00 transfer end interrupt function

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] R_TAU0_Channel0_Start

Synopsis	TAU0 channel 0 operation start
Header	r_cg_macrodriver.h, r_cg_timer.h, and r_cg_userdefine.h
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function releases a mask of TAU0 channel 0 count end interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_CSI00_Start

Synopsis	CSI00 operation start
Header	r_cg_macrodriver.h, r_cg_serial.h, and r_cg_userdefine.h
Declaration	void R_CSI00_Start(void)
Explanation	This function starts SAU0 channel 0 as CSI00 and sets it to a communication standby state.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_CSI00_Send_Receive

Synopsis	CSI00 data transmission/reception function
Header	r_cg_macrodriver.h, r_cg_serial.h, and r_cg_userdefine.h
Declaration	MD_STATUS R_CSI00_Send_Receive(uint8_t *txbuf, uint16_t txnum, and uint8_t *rxbuf)
Explanation	This function sets up CSI00 data transmission/reception.
Arguments	uint8_t *txbuf : [Transmit data buffer address] uint16_t txnum : [Transmit data buffer size] uint8_t *rxbuf : [Receive data buffer address]
Return value	[MD_OK]: Transmission/reception setup completed [MD_ARGERROR]: Transmission/reception setup unsuccessful
Remarks	None

[Function Name] R_CSI00_Interrupt

Synopsis	CSI00 transfer end interrupt function
Header	r_cg_macrodriver.h, r_cg_serial.h, and r_cg_userdefine.h
Declaration	__interrupt void R_CSI00_Interrupt(void)
Explanation	If there is data not transmitted, this function reads receive data and then starts transmitting the data not transmitted. Otherwise, this function reads receive data.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

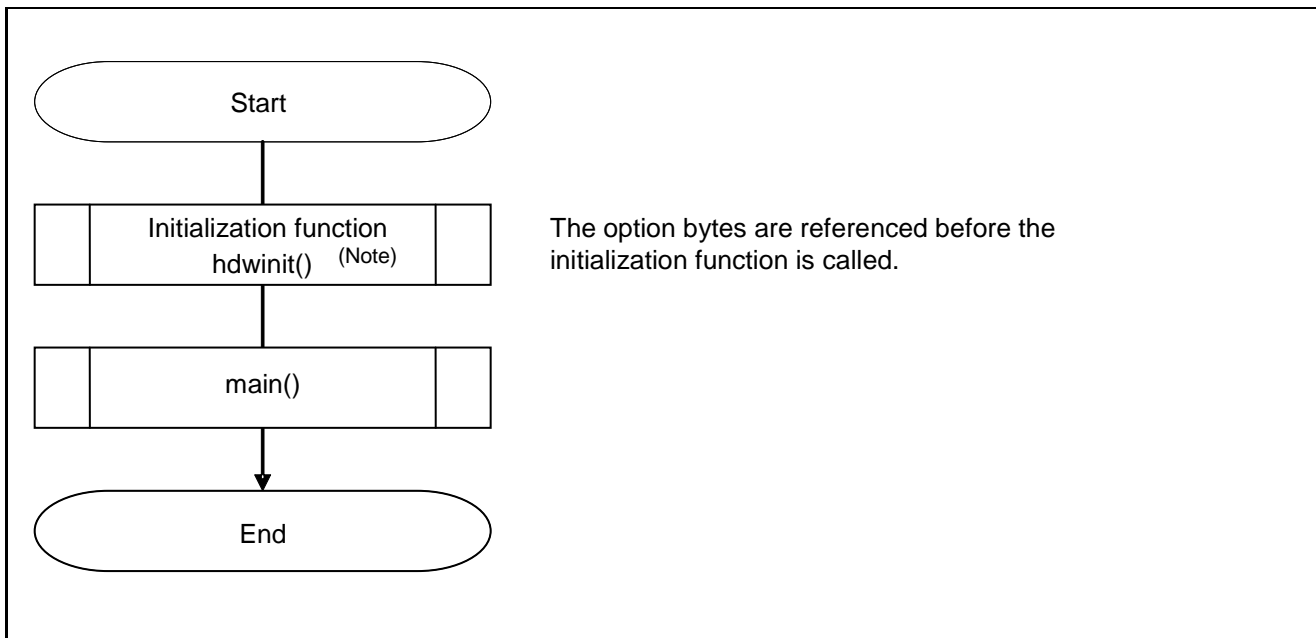


Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

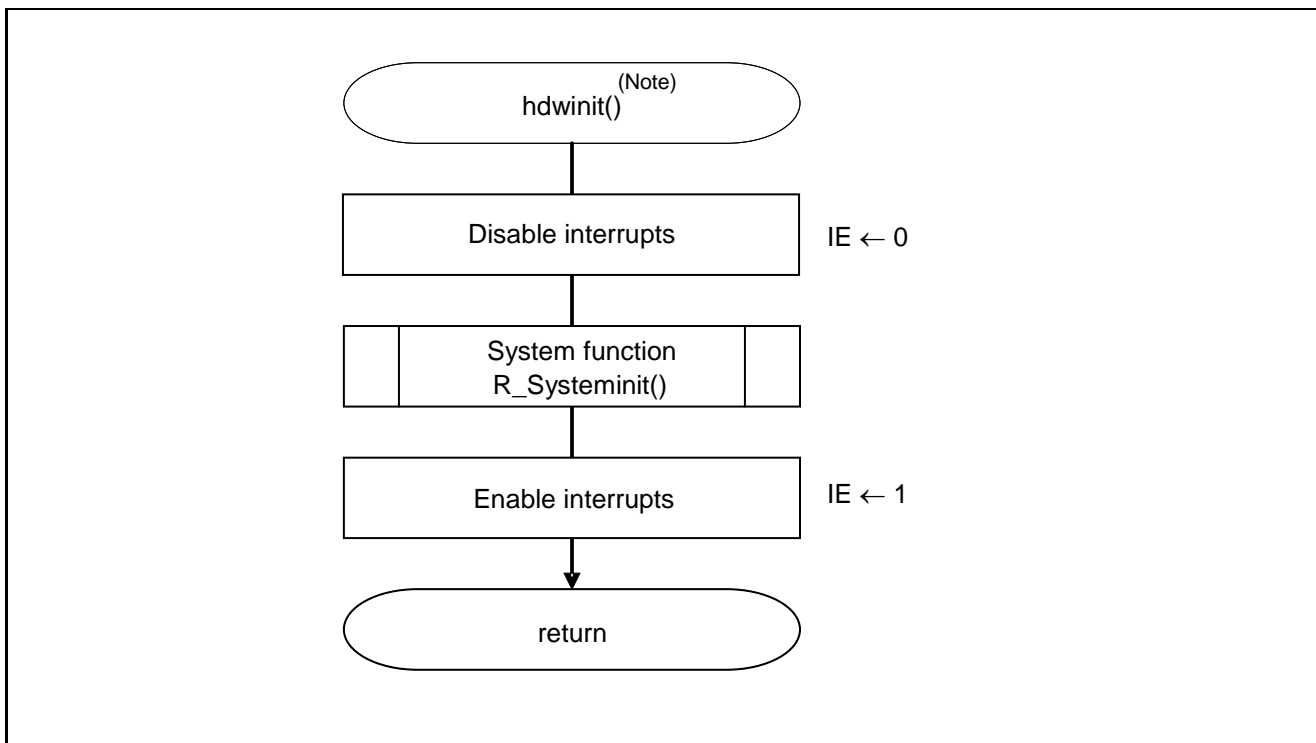


Figure 5.2 Initialization Function

Note: The `__low_level_init` function initializes the system in the IAR Workbench IDE-Oriented sample code.

5.7.2 System Function

Figure 5.3 shows the flowchart for the system function.

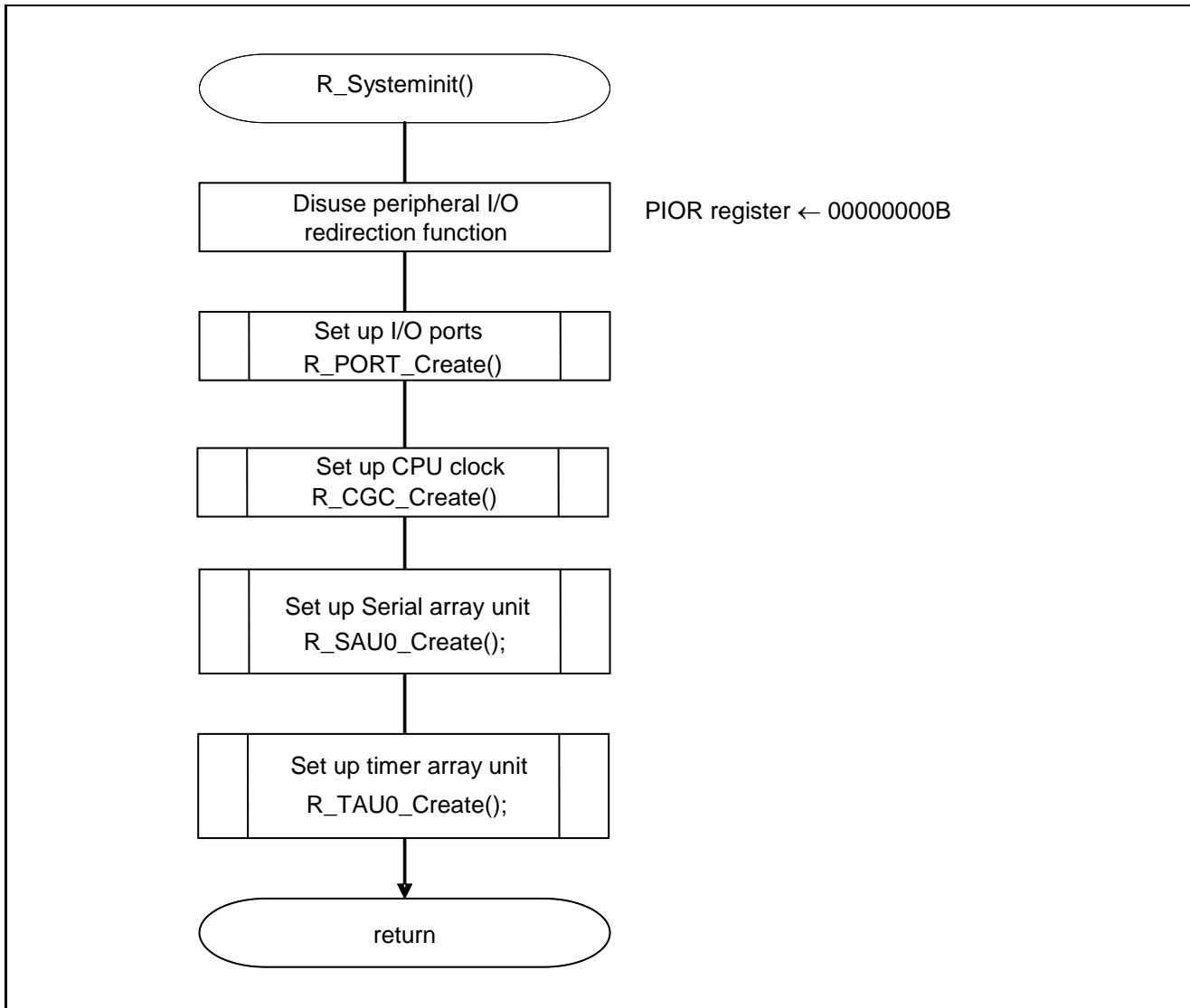


Figure 5.3 System Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for I/O port setup.

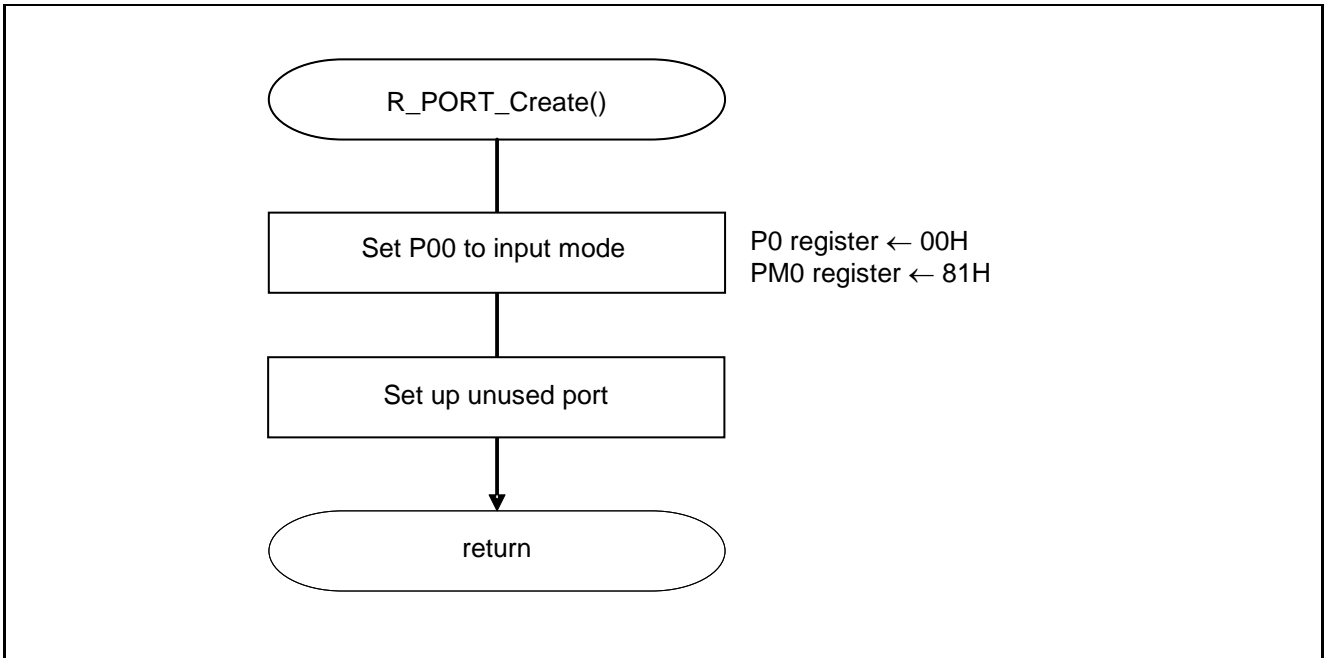


Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Setting up the BUSY signal detection ports

- Port register 0 (P0)
- Port mode register 0 (PM0)
Select an I/O mode and output latch for each port.

Symbol: P0

7	6	5	4	3	2	1	0
0	P06	P05	P04	P03	P02	P01	P00
0	x	x	x	x	x	x	0

Bit 0

P00	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Symbol: PM0

7	6	5	4	3	2	1	0
1	PM06	PM05	PM04	PM03	PM02	PM01	PM00
1	x	x	x	x	x	x	1

Bit 0

PM00	PM11 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

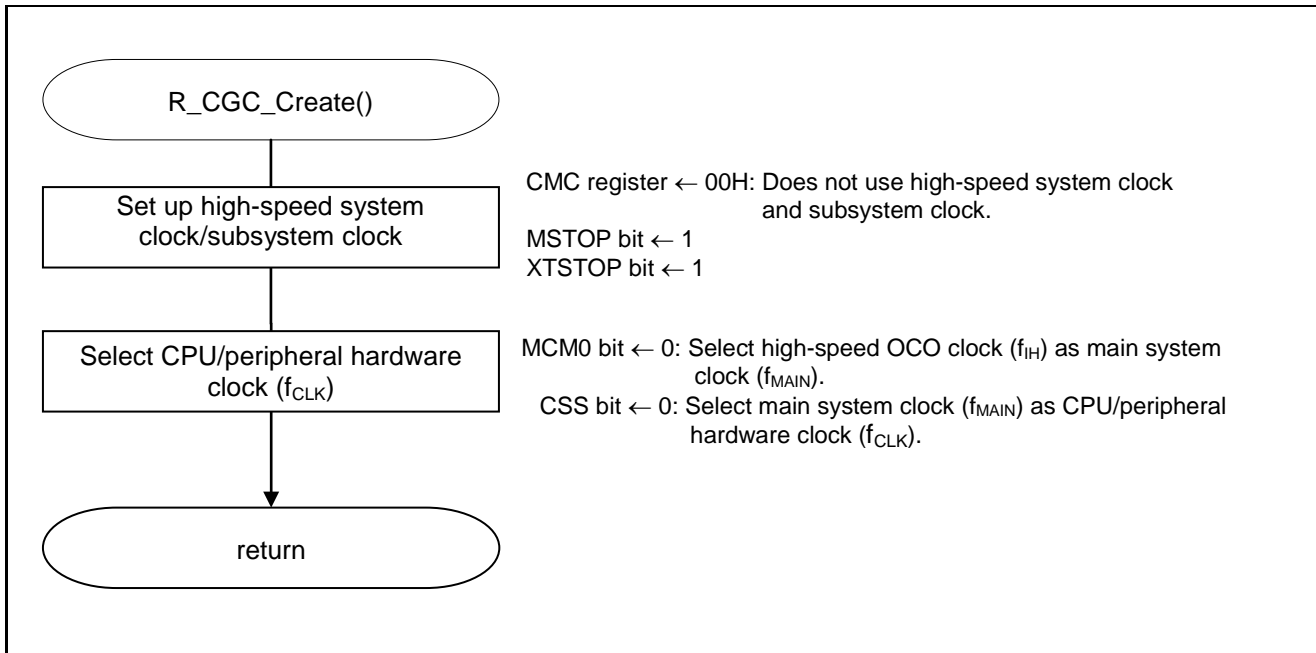


Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100).

5.7.5 SAU0 Setup

Figure 5.6 shows the flowchart for SAU0 setup.

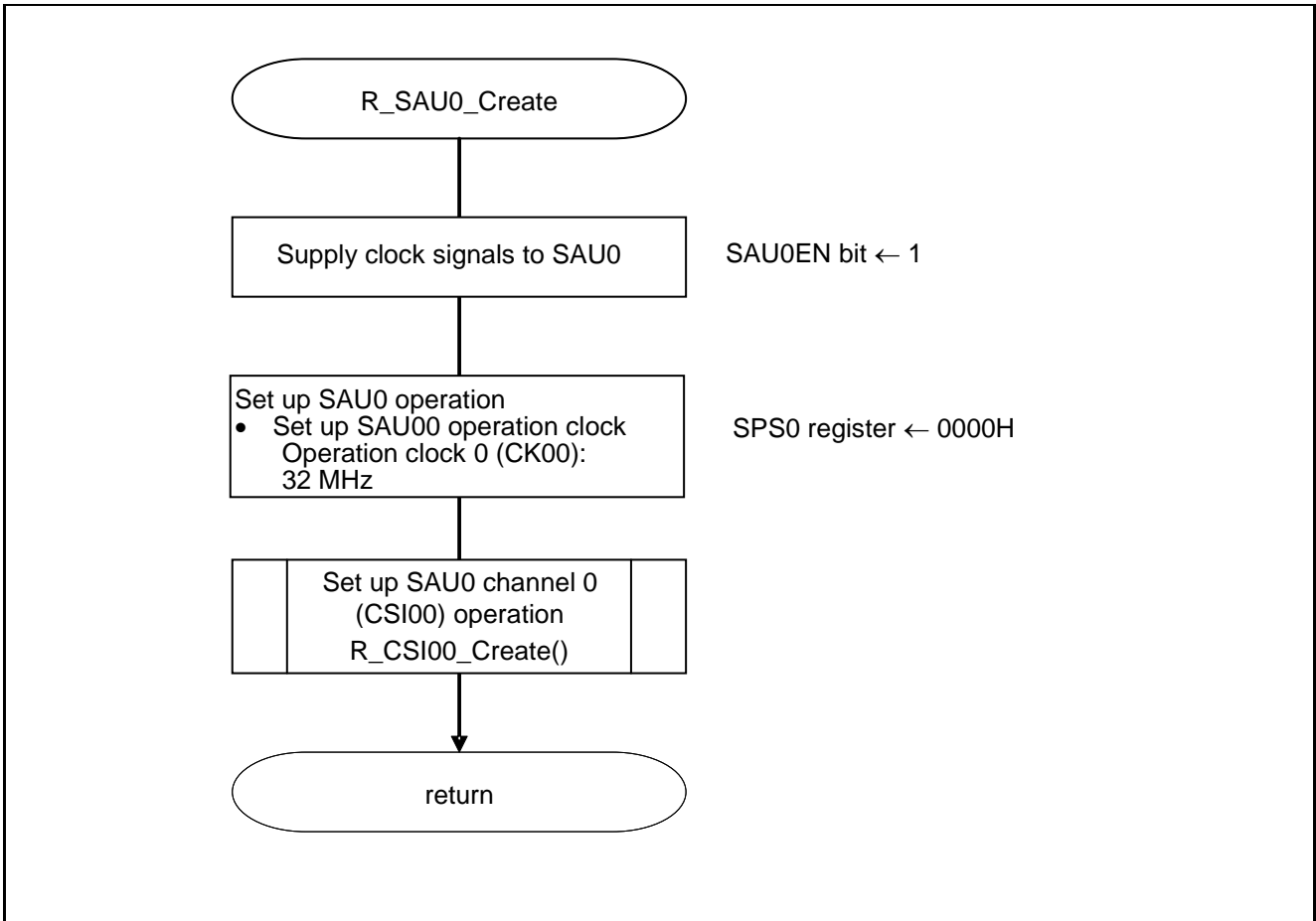


Figure 5.6 SAU0 Setup

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Enabling supply of clock signals to the SAU

- Peripheral enable register 0 (PER0)
Enable supply of clock signals to SAU0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	1	x	x

Bit 2

SAU0EN	Control of serial array unit 0 and input clock supply
0	Stops input clock supply.
1	Enables input clock supply.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Selecting a serial clock

- Serial clock select register 0 (SPS0)
Select an operation clock for SAU0.

Symbol: SPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	0	0	0	0	0	0	x	x	x	x	0	0	0	0

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
				f_{CLK}	$f_{CLK} =$ 2 MHz	$f_{CLK} =$ 5 MHz	$f_{CLK} =$ 10 MHz	$f_{CLK} =$ 20 MHz	$f_{CLK} =$ 32 MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	313 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156 kHz	313 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	78.1 kHz	156 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	39.1 kHz	78.1 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.77 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	31.3 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	2.44 kHz	4.88 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	977 Hz

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 SAU0 Channel 0 (CSI00) Operation Setup

Figure 5.7 shows the flowchart for setting up SAU0 channel 0 (CSI00) operation.

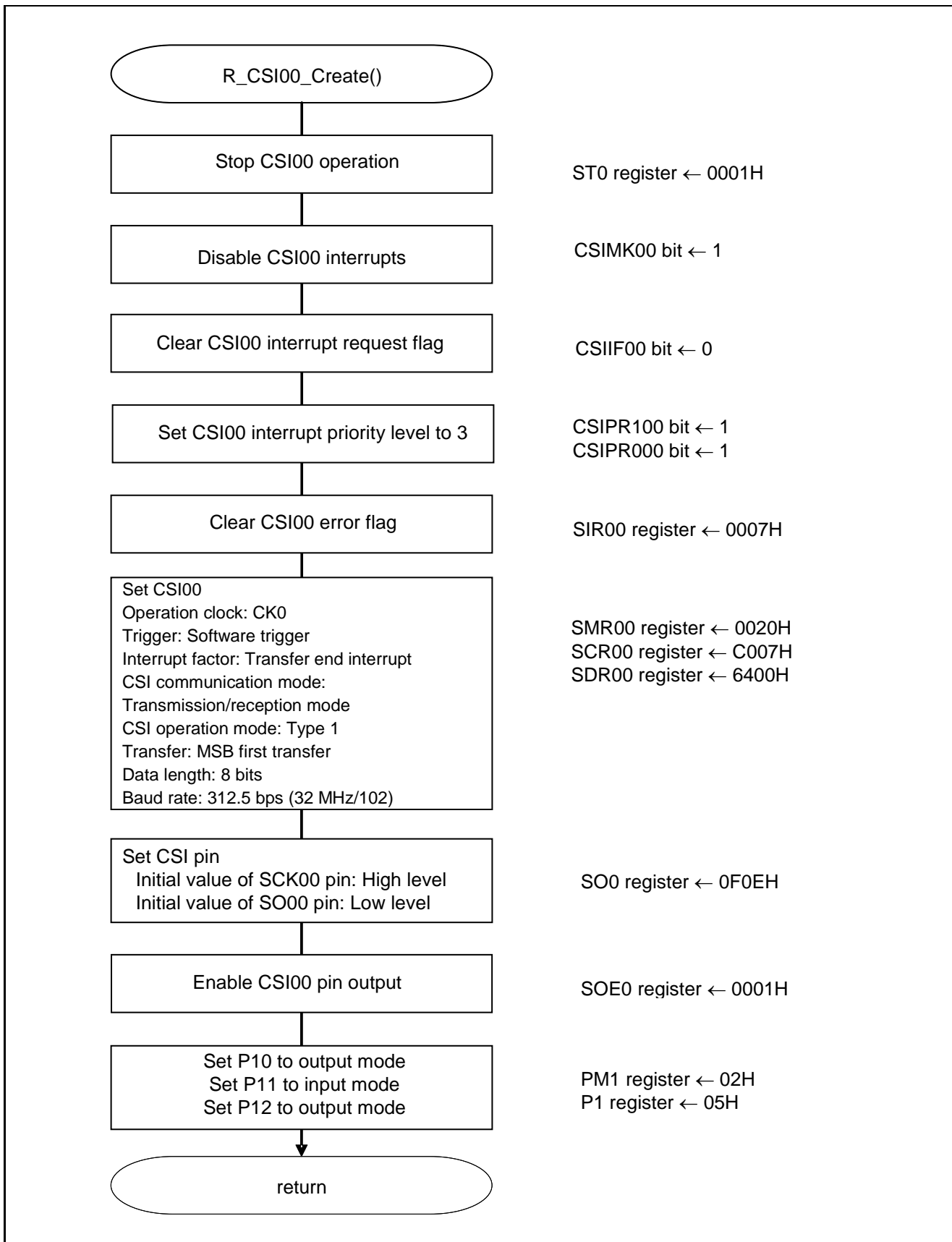


Figure 5.7 SAU0 Channel 0 (CSI00) Operation Setup

Stopping serial channel 0

- Serial channel stop register 0 (ST0)
Stop communication/count operation of serial channel 0.

Symbol: ST0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	ST0 3	ST0 2	ST0 1	ST0 0
0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	1

Bit 0

ST00	Operation stop trigger of channel 0
0	No trigger operation
1	Clears the SE00 bit to 0 and stops the communication operation.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Setting a transfer end interrupt priority level

- Priority specification flag register 00H (PR00H)
- Priority specification flag register 10H (PR10H)
Set the interrupt priority level.

Symbol: PR00H

7	6	5	4	3	2	1	0
SREPR00 TMPR001 H	SRPR00 CSIPR001 IICPR001	STPR00 CSIPR000 IICPR000	DMAPR01	DMAPR00	SREPR02 TMPR011 H	SRPR02 CSIPR021 IICPR021	STPR02 CSIPR020 IICPR020
x	x	1	x	x	x	x	x

Symbol: PR10H

7	6	5	4	3	2	1	0
SREPR10 TMPR101 H	SRPR10 CSIPR101 IICPR101	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12 TMPR111 H	SRPR12 CSIPR121 IICPR121	STPR12 CSIPR120 IICPR120
x	x	1	x	x	x	x	x

Bit 5

CSIPR00 0	CSIPR10 0	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Clearing the CSI00 error flags

- Serial flag clear trigger register 00 (SIR00)
Clear the SAU0 channel 0 error flags.

Symbol: SIR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	FEC T00	PEC T00	OVCT 00
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit 2

FECT0 0	Clear trigger of framing error flag of channel 0
0	Not cleared
1	Clears the FEF00 bit of the SSR00 register to 0.

Bit 1

PECT0 0	Clear trigger of parity error flag of channel 0
0	Not cleared
1	Clears the PEF00 bit of the SSR00 register to 0.

Bit 0

OVCT0 0	Clear trigger of overrun error flag of channel 0
0	Not cleared
1	Clears the OVF00 bit of the SSR00 register to 0.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Setting up the SAU0 channel 0 operation mode

- Serial mode register 00 (SMR00)
 - Select an operation clock (f_{MCK}).
 - Specify whether to make the serial clock (f_{SCK}) input available.
 - Set the start trigger and operation mode.
 - Select an interrupt source.

Symbol: SMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CK S00	CC S00	0	0	0	0	0	STS 00	0	SIS 000	1	0	0	MD 002	MD 001	MD 000
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit 15

CKS00	Selection of operation clock (f_{MCK}) of channel n
0	Operation clock CK00 set by the SPS0 register
1	Operation clock CK01 set by the SPS0 register

Bit 14

CCS00	Selection of transfer clock (f_{TCLK}) of channel n
0	Divided operation clock f_{MCK} specified by the CKS00 bit
1	Clock input f_{SCK} from the SCK00 pin (slave transfer in CSI mode)

Bit 8

STS00	Selection of start trigger source
0	Only software trigger is valid
1	Valid edge of the RxDq pin (selected for UART reception)

Bits 2 and 1

MD002	MD001	Setting of operation mode of channel 0
0	0	CSI mode
0	1	UART mode
1	0	Simplified I ² C mode
1	1	Setting prohibited

Bit 0

MD000	Selection of interrupt source of channel 0
0	Transfer end interrupt
1	Buffer empty interrupt

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Setting up the SAU0 channel 0 operation mode

- Serial communication operation setting register 00 (SCR00)
 - Select an operation clock (f_{MCK}).
 - Specify whether to make the serial clock (f_{SCK}) input available.
 - Set up the start trigger and operation mode.
 - Select an interrupt source.

Symbol: SCR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE00	RX E00	DA P00	CK P00	0	EO C00	PTC 001	PTC 000	DIR 00	0	SLC 001	SLC 000	0	1	DLS 001	DLS 000
1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits 15 and 14

TXE00	RXE00	Setting of operation mode of channel n
0	0	Disable communication.
0	1	Reception only
1	0	Transmission only
1	1	Transmission/reception

Bits 13 and 12

DAP00	CKP00	Selection of data and clock phase in CSI mode	Type
0	0		1
0	1		2
1	0		3
1	1		4

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: SCR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE00	RX E00	DA P00	CK P00	0	EO C00	PTC 001	PTC 000	DIR 00	0	SLC 001	SLC 000	0	1	DLS 001	DLS 000
1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit 7

DIR00	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	Inputs/outputs data with LSB first.

Bits 1 and 0

DLS00	DLS00	Setting of data length in CSI and UART modes
1	0	
0	0	9-bit data length (stored in bits 0 to 8 of the SDR00 register) (can be set in UART0 mode only.)
1	0	7-bit data length (stored in bits 0 to 6 of the SDR00 register)
1	1	8-bit data length (stored in bits 0 to 7 of the SDR00 register)
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Selecting an operation clock frequency divisor

- Serial data register 00 (SDR00)
Set the division ratio of the operation clock (f_{MCK}) frequency.

Symbol: SDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits 15 to 9

SDR00[15:9]							Transfer clock setting by dividing the operation clock (f_{MCK})
0	0	0	0	0	0	0	$f_{MCK}/2$
0	0	0	0	0	0	1	$f_{MCK}/4$
0	0	0	0	0	1	0	$f_{MCK}/6$
0	0	0	0	0	1	1	$f_{MCK}/8$
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
0	1	1	0	0	1	0	$f_{MCK}/102$
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	$f_{MCK}/254$
1	1	1	1	1	1	1	$f_{MCK}/256$

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Specifying the output values for the SCK00 and SO00 pins

- Serial output register 0 (SO0)
Specify the output values for the serial data output pin and serial clock output pin.

Symbol: SO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CK O03	CK O02	CK O01	CK O00	0	0	0	0	SO 03	SO 02	SO 01	SO 00
0	0	0	0	x	x	x	1	0	0	0	0	x	x	x	0

Bit 8

CKO00	Serial clock output of channel 0
0	Serial clock output value is "0".
1	Serial clock output value is "1".

Bit 0

SO00	Serial data output of channel 0
0	Serial clock output value is "0".
1	Serial clock output value is "1".

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Enabling output of serial communication operation

- Serial output enable register 0 (SOE0)
Enable output of serial communication operation.

Symbol: SOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SO E03	SO E02	SO E01	SO E00
0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	1

Bit 0

SOE00	Serial output enable/stop of channel 0
0	Stops output by serial communication operation.
1	Enables output by serial communication operation.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Setting up the ports of the SCK00, SO00 and SI00 pins

- Port register 1 (P1)
- Port mode register 1 (PM1)
Select an input/output mode and output latch for each port.

Symbol: P1

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
x	x	x	x	x	1	x	1

Bit 2

P12	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Bit 0

P10	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	x	x	x	x	0	1	0

Bit 2

PM12	P12 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 1

PM11	P11 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 0

PM10	P10 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 TAU0 Setup

Figure 5.8 shows the flowchart for setting up TAU0.

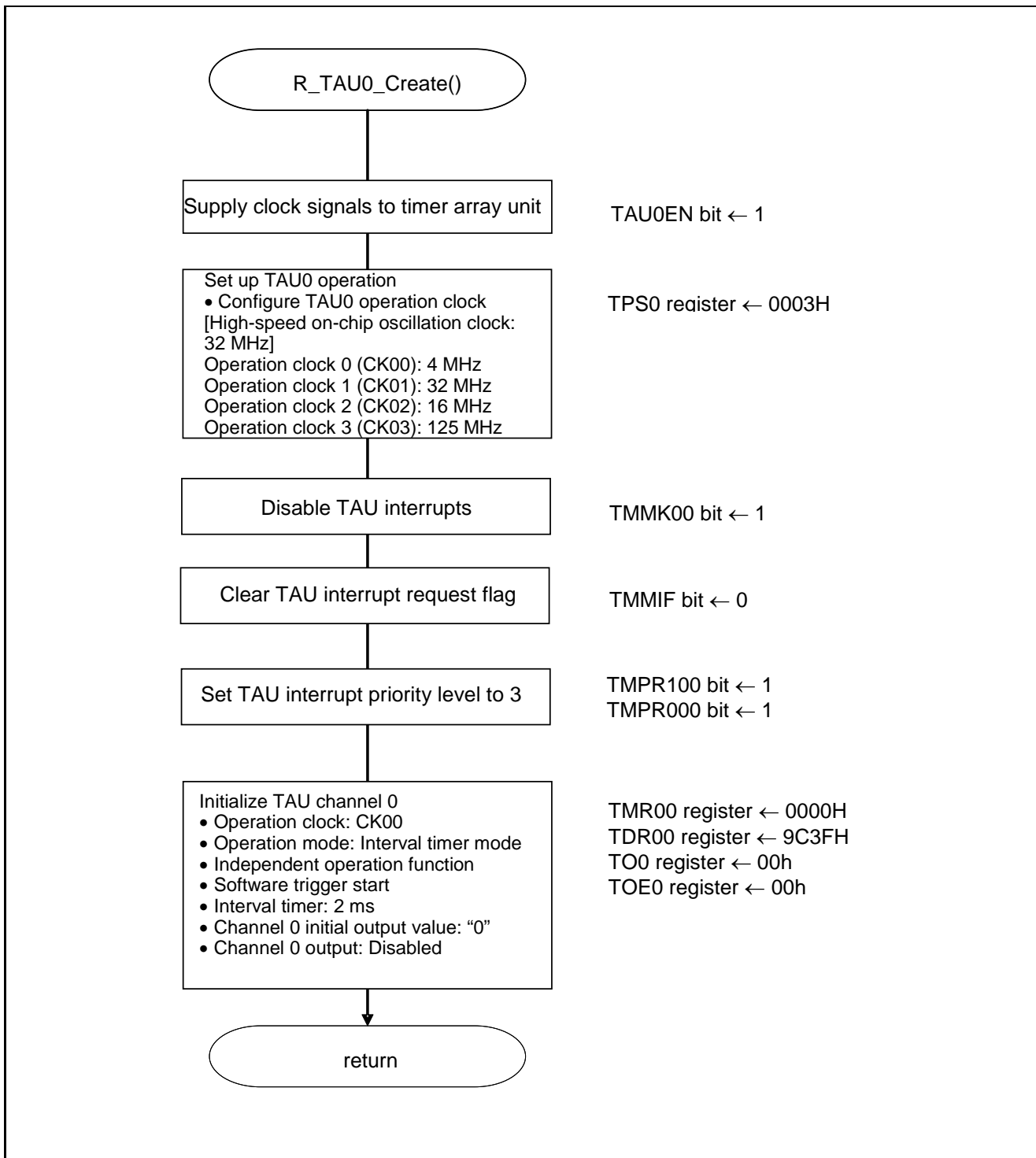


Figure 5.8 TAU0 Setup

Caution: For information about TAU0 setup (R_TAU0_Create()), refer to the section entitled "Flowcharts" in RL78/G13 Timer Array Unit (Interval Timer) Application Note (R01AN0456EJ0100).

5.7.8 Main Processing

Figure 5.9 shows the flowchart for main processing.

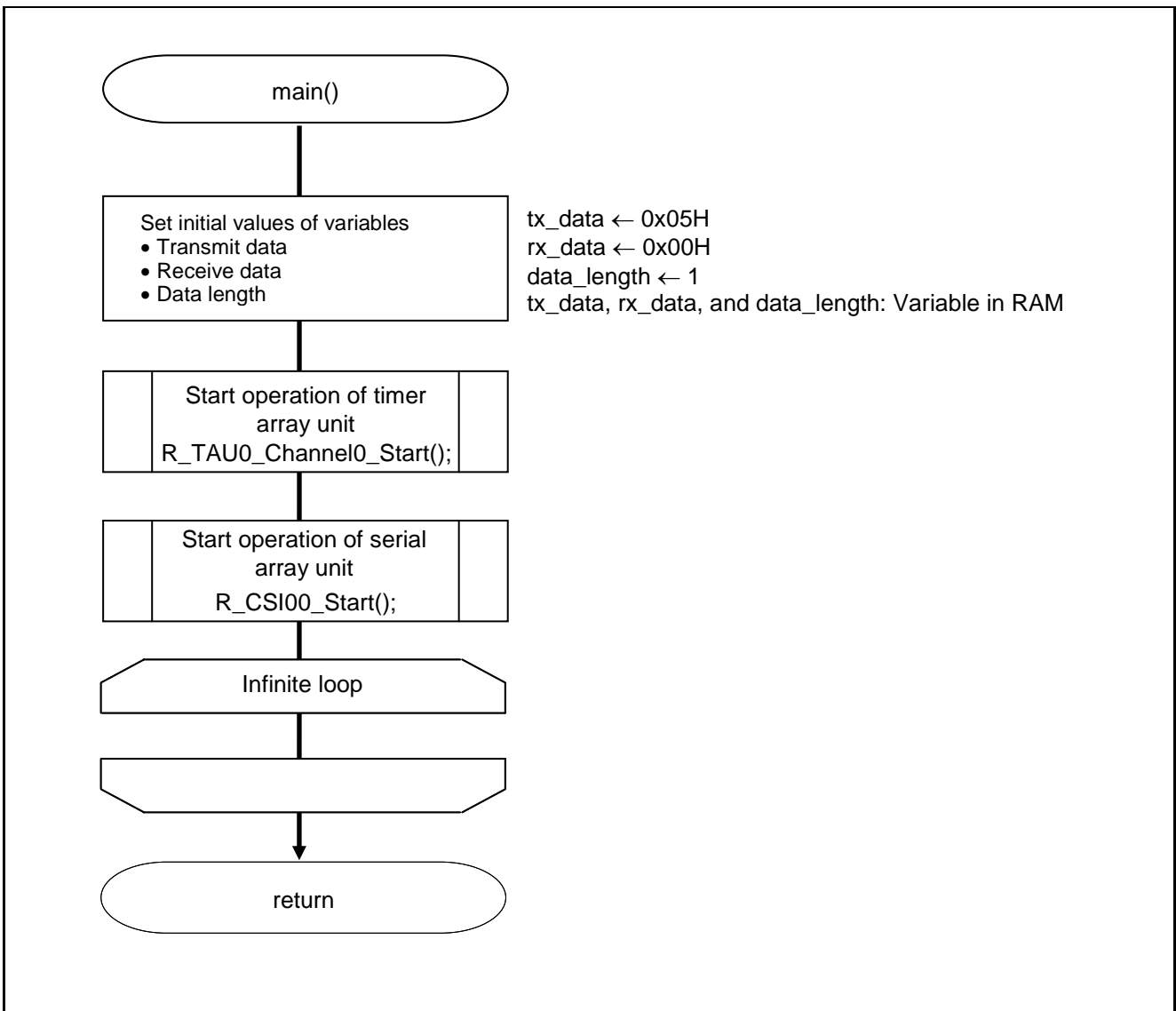


Figure 5.9 Main Processing

5.7.9 TAU0 Channel 0 Startup

Figure 5.10 shows the flowchart for starting the operation of TAU0 channel 0.

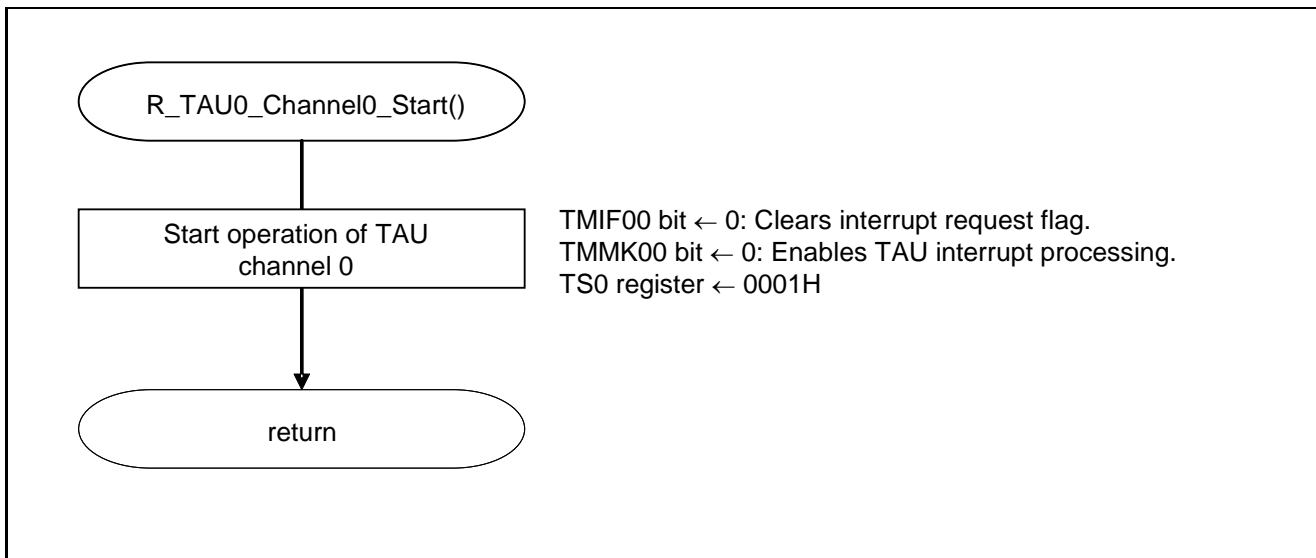


Figure 5.10 TAU0 Channel 0 Startup

Caution: For information about TAU0 setup (R_TAU0_Create()), refer to the section entitled "Flowcharts" in RL78/G13 Timer Array Unit Interval Timer Application Note (R01AN456J).

5.7.10 SAU0 Channel 0 Startup

Figure 5.11 shows the flowchart for starting the operation of SAU0 channel 0 (CSI00).

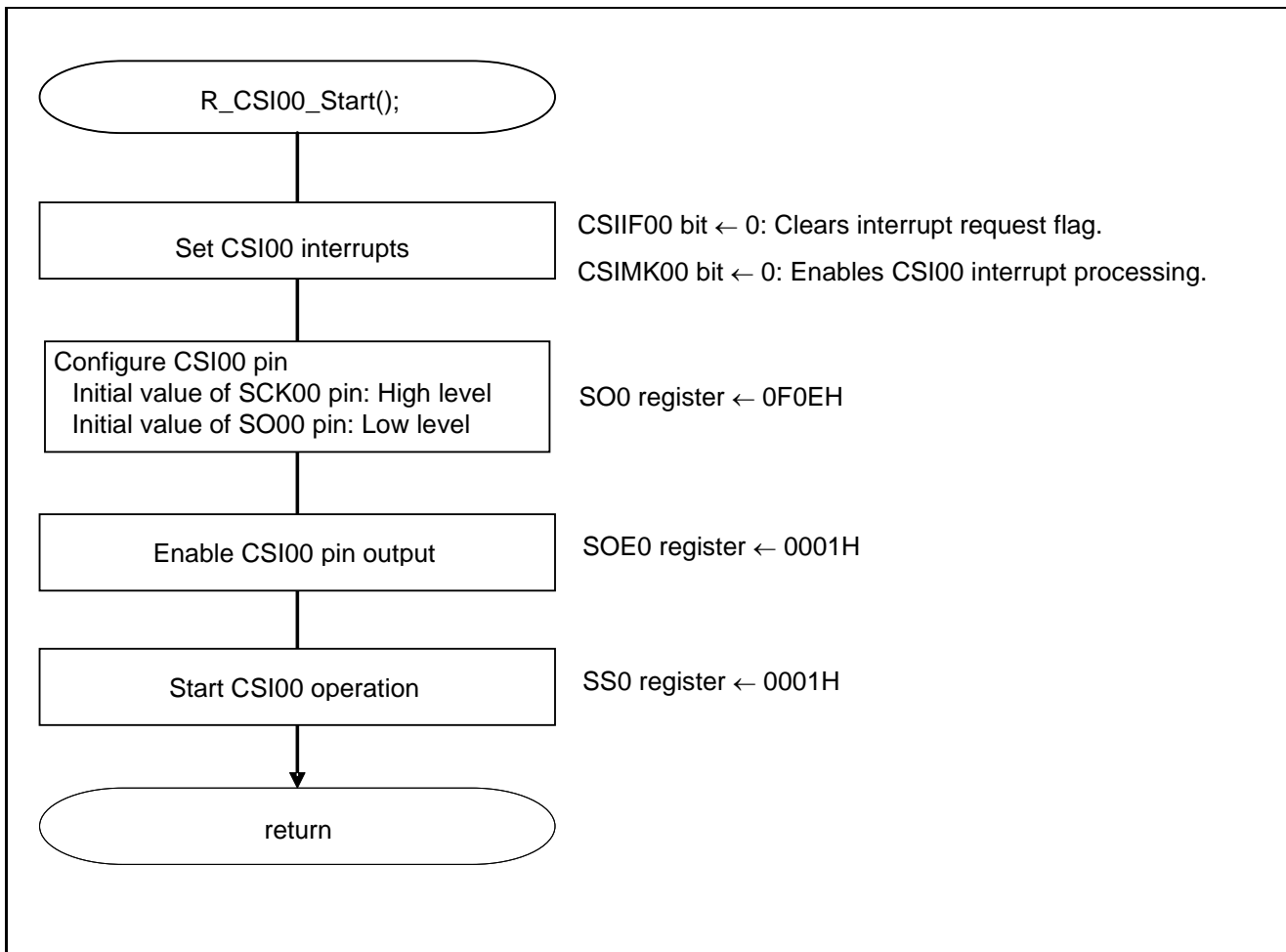


Figure 5.11 SAU0 Channel 0 (CSI00) Startup

Setting the transfer end interrupt

- Interrupt request flag register 0H (IF0H)
Clear the interrupt request flag.
- Interrupt mask flag register 0H (MK0H)
Enable interrupt processing.

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIF01 IICIF01	STIF0 CSIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIF21 IICIF21	STIF2 CSIF20 IICIF20
x	x	0	x	x	x	x	x

Bit 5

CSIF00	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
x	x	1	x	x	x	x	x

Bit 5

CSIMK0	Interrupt processing control
0	Enables interrupt processing.
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Enabling serial communication

- Serial channel start register 0 (SS0)
Enable serial communication/count operation.

Symbol: SS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SS0 3	SS0 2	SS0 1	SS0 0
0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	1

Bit 0

SS00	Operation start trigger of channel 0
0	No trigger operation
1	Sets the SE00 bit to 1 and enters the communication wait status.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Remark: When the SS0 register is read, 0000H is always read.

5.7.11 Infinite Loop in Main Processing

Figure 5.12 shows the flowchart for an infinite loop in the main processing.

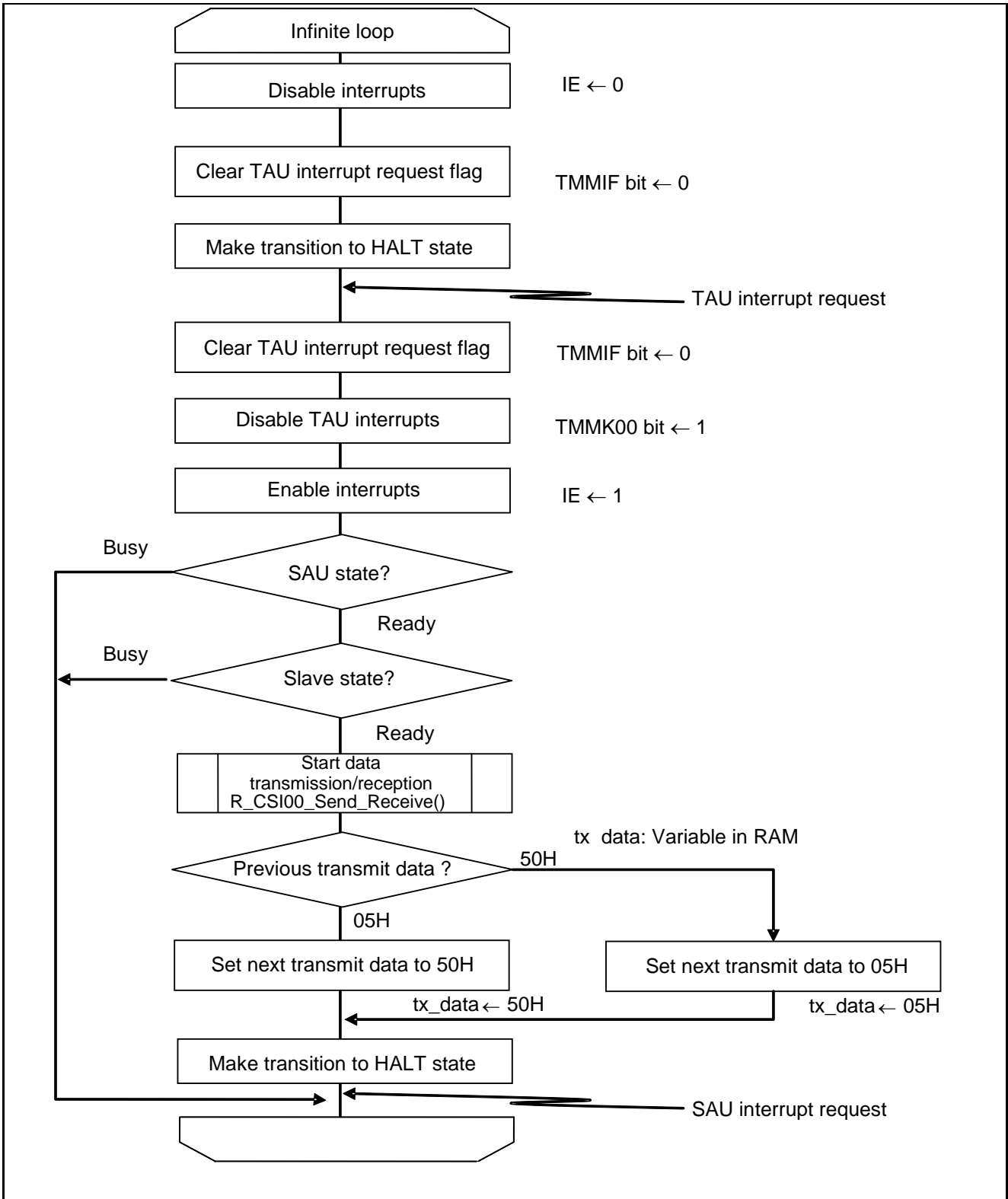


Figure 5.12 Infinite Loop in Main Processing

RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)

Confirming the communication state

- Serial status register 00 (SSR00)
Indicate the communication status and error occurrence status of serial array unit channel 0.

Symbol: SSR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	TSF 00	BFF 00	0	0	FEF 00	PEF 00	OV F00
0	0	0	0	0	0	0	0	0	0/1	x	0	0	x	x	x

Bit 6

TSF00	Communication status indication flag of channel n
0	Communication is stopped or suspended.
1	Communication is in progress.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.12 CSI00 Data Transmission/Reception Start

Figure 5.13 shows the flowchart for starting CSI00 data transmission/reception.

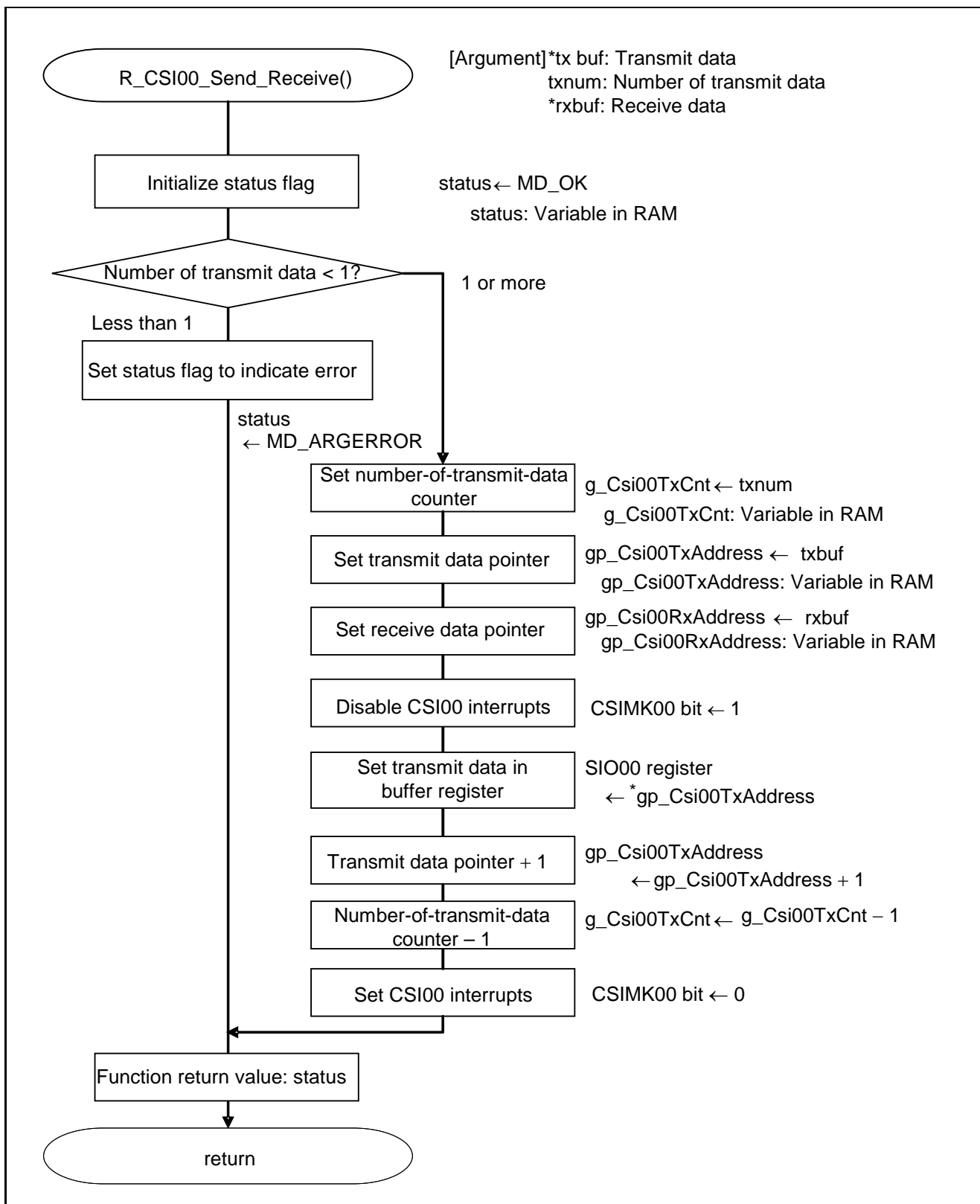
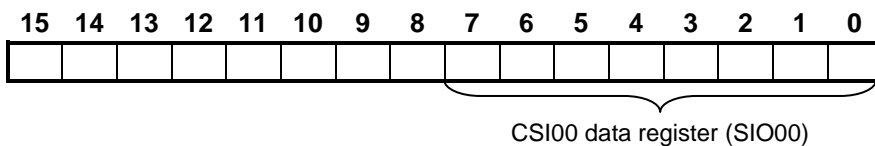


Figure 5.13 CSI00 Data Transmission/Reception Start

Setting transmit data

- Serial data register 00 (SDR00)
Set transmit data and start transmitting the data.

Symbol: SDR00



Write transmit data to the lower eight bits.

These eight bits should be accessed as the CSI00 register.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.13 CSI00 Transfer End Interrupt Processing

Figure 5.14 shows the flowchart for CSI00 transfer end interrupt processing.

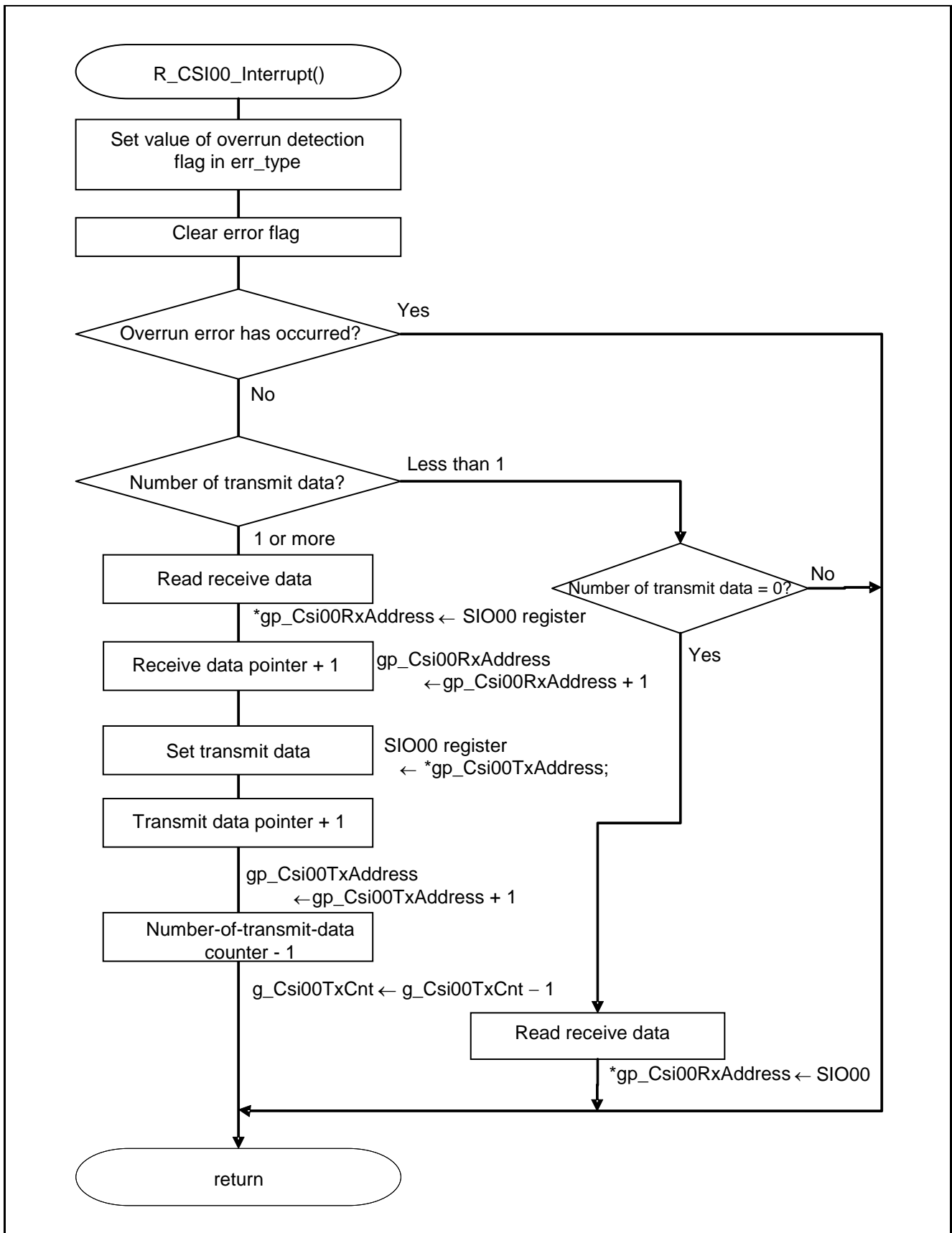


Figure 5.14 CSI00 Transfer End Interrupt Processing

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

User's Manual:

RL78/G13 User's Manual: Hardware (R01UH0146EJ)

RL78 Family User's Manual: Software (R01US0015EJ)

The latest version can be downloaded from the Renesas Electronics website.

Technical Updates/Technical News

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REVISION HISTORY	RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception)
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Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2011	—	First edition issued
2.00	Dec. 27, 2013	6	Table 2.1: Added e2studio and IAR information
		13	Added note Figure 5.2: Fixed typo in function name
		14	Figure 5.3: Fixed typo in in function name

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal.
Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

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