

RL78/G13, RL78/G23

Migration Guide from RL78/G13 to RL78/G23

Introduction

This application note describes the differences in peripheral functions between RL78/G13 and RL78/G23.

Target Device

RL78/G13, RL78/G23

For detailed information on peripheral functions and electrical characteristics, refer to the User's Manual: Hardware and Technical Updates.

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Differences in peripheral functions between RL78/G13 and RL78/G23


Table 1.1 and Table 1.3 show the main differences in peripheral functions between RL78/G13 and RL78/G23.

However, differences due to changes in the settings of the CPU core, peripheral functions, and clock generation circuit are not considered. For details, refer to the User's Manual: Hardware of each product.

Table 1.1 Differences in peripheral functions between RL78/G13 and RL78/G23 (1/3)

Item	RL78/G13	RL78/G23	
	Function name	Function name	Main differences from RL78/G13
Ports	Port Functions	Port Functions	- Added output current control port. - Enhanced low-level output current for some pins.
Flash operation mode switching	—	Operation State Control	Additional function
Clocks	Clock Generator	Clock Generator	- Added middle-speed on-chip oscillator. - Changed frequency (fIL) of low-speed on-chip oscillator to 32.768kHz.
Timers	Timer Array Unit	Timer Array Unit	Added an event input from ELCL.
	Realtime Clock	Realtime Clock	None
	12-bit Interval Timer	32-bit Interval Timer	Changed function (Capable of measuring up to 4,660 hours.)
Clock Output/Buzzer Output	Clock Output/Buzzer Output Controller	Clock Output/Buzzer Output Controller	None
Watchdog Timers (WDT)	Watchdog Timer	Watchdog Timer	Changed overflow time.
A/D Converter	A/D Converter	A/D Converter	- Added 12-bit resolution. - Capable of selecting Digital I/O or analog input for each pin. (This pin function selection applies also to ANI0 to ANI15 pins.)

Note : Additional peripheral functions : Changed peripheral functions

: Deleted peripheral functions —: There is no corresponding function.

Caution. For details on peripheral functions, usage and electrical characteristics, refer to the User's Manual: Hardware.

Table 1.2 Differences in peripheral functions between RL78/G13 and RL78/G23 (2/3)

Item	RL78/G13	RL78/G23	
	Function name	Function name	Main differences from RL78/G13
D/A Converter	—	D/A Converter	Additional function
Comparator	—	Comparator	Additional function
Serial Interface (Clock Asynchronous, Clock Synchronous)	Serial Array Unit	Serial Array Unit	Added UART loopback function
		UARTA	Additional function
I ² C bus interface	IICA	IICA	Added all address match function
Remote Control Signal Receiver	—	Remote Control Signal Receiver (REMC)	Additional function
Accumulator (computing unit)	Multiplier and Divider/Multiply-Accumulator	—	Deleted item (Added multiply & accumulate instructions.)
Data Transfer Functions	DMA (Direct Memory Access) Controller	DTC (Data Transfer Controller)	Changed function
linkage operation between peripheral functions without CPU	—	Logic and Event Link Controller (ELCL)	Additional function

Note : Additional peripheral functions : Changed peripheral functions


 : Deleted peripheral functions —: There is no corresponding function.

Caution. For details on peripheral functions, usage and electrical characteristics, refer to the User's Manual: Hardware.

Table 1.3 Differences in peripheral functions between RL78/G13 and RL78/G23 (3/3)

Item	RL78/G13	RL78/G23	
	Function name	Function name	Main differences from RL78/G13
Interrupts	Interrupt Functions	Interrupt Functions	Changed interrupt sources.
	Key Interrupt Function	Key Interrupt Function	- Added a function to select key Interrupt detection pins. - Added a function to select detection edge.
Reduced system operating current	Standby Function	Standby Function	- Added a function that starting of high-speed on-chip oscillator is at high speed. - Added a function to stop power supply to RAM.
Resets	Reset Function	Reset Function	Added a function to confirm that a power-on reset has occurred.
	Power-On-Reset Circuit	Power-On-Reset Circuit	Changed reset processing time.
Voltage Detector (LVD)	Voltage Detector	Voltage Detector	- Equipped with 2 channels. - Changed detection voltage values.
Safety Functions	Safety Functions	Safety Functions	- Added a function to prevent Flash rewriting when CPU goes out of control. - Added a function to detect digital output signal level for I/O pins. - Added UART loopback function.
Security function, encryption function	—	Security Function	Additional function
Processing execution function independent of CPU	—	SNOOZE Mode Sequencer	Additional function
Capacitive touch/proximity sensor	—	Capacitive Sensing Unit	Additional function
Regulator	Regulator	Regulator	Changed an output voltage value of internal regulator.
Option Function Select Areas	Option Bytes	Option Bytes	Changed functions of WDT, LVD, and Flash operating modes.
Flash Memory	Flash Memory	Flash Memory	Changed specifications, such as block size.
On-Chip Debugging	On-Chip Debugging	On-Chip Debugging	Changed dedicated emulators.
BCD Correction Circuit	BCD Correction Circuit	BCD Correction Circuit	None

Note : Additional peripheral functions : Changed peripheral functions

: Deleted peripheral functions —: There is no corresponding function.

Caution. For details on peripheral functions, usage and electrical characteristics, refer to the User's Manual: Hardware.

2. Comparison of RL78/G13 and RL78/G23 registers





Table 2.1 to Table 2.19 show register comparison between RL78/G13 and RL78/G23 for peripheral functions other than additions, changes and deletions described in chapter "1. Differences in peripheral functions between RL78/G13 and RL78/G23". For details of each register function, refer to the User's Manual: Hardware.

Also, the registers and bits mounted on the microcontroller differ depending on the product. For the registers and bits mounted in each product, refer to the User's Manual: Hardware.

2.1 Port Functions

Table 2.1 Registers Controlling Port Function (1/2)

RL78/G13	RL78/G23	
Register name	Register name	Remark
Port mode registers (PMxx)	Port mode registers (PMxx)	Addition of PM121 and PM122 bits to PM12 register
Port registers (Pxx)	Port registers (Pxx)	None
Pull-up resistor option registers (PUxx)	Pull-up resistor option registers (PUxx)	Addition of PU121 and PU122 bits to PU12 register
Port input mode registers (PIMx)	Port input mode registers (PIMxx)	Addition of PIM33 bit to PIM3 register. Addition of PIM41 bit to PIM4 register. Addition of PIM71 bit to PIM7 register. Addition of PIM84 bit to PIM8 register.
Port output mode registers (POMx)	Port output mode registers (POMxx)	Addition of POM34 bit to POM3 register. Addition of POM42 bit to POM4 register. Addition of POM72 bit to POM7 register. Addition of POM83 bit to POM8 register. Addition of POM120 bit to POM12 register.
—	Port digital input disable registers (PDIDISxx)	New addition
Port mode control registers (PMCxx)	Port mode control A registers (PMCAxx)	Changed applicable pins
—	Port mode control T registers (PMCTxx)	New addition
—	Port mode control E registers (PMCExx)	New addition
A/D port configuration register (ADPC)	—	Deleted item

Note : The register name is unchanged. : Additional contents : Changed contents
: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

Table 2.2 Registers Controlling Port Function (2/2)

RL78/G13	RL78/G23	
Register name	Register name	Remark
Peripheral I/O redirection register (PIOR)	Peripheral I/O redirection register (PIOR)	None
Global digital input disable register (GDIDIS)	Global digital input disable register (GDIDIS)	None
—	Output current control enable register (CCDE)	New addition
—	Output current select registers (CCSx)	New addition
—	Port overdrive register (PTDC)	New addition
—	Port function output enable registers (PFOEx)	New addition
—	Port mode select register (PMS)	New addition

Note : The register name is unchanged. : Additional contents : Changed contents

: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.2 Clock Generator

Table 2.3 Registers Controlling Clock Generator

RL78/G13	RL78/G23	
Register name	Register name	Remark
Clock operation mode control register (CMC)	Clock operation mode control register (CMC)	Addition of XTSEL bit to bit 3
System clock control register (CKC)	System clock control register (CKC)	Addition of MCM1 bit to bit 0. Addition of MCS1 bit to bit 1.
Clock operation status control register (CSC)	Clock operation status control register (CSC)	Addition of MIOEN bit to bit 1
Oscillation stabilization time counter status register (OSTC)	Oscillation stabilization time counter status register (OSTC)	None
Oscillation stabilization time select register (OSTS)	Oscillation stabilization time select register (OSTS)	None
Peripheral enable register 0 (PER0)	Peripheral enable register 0 (PER0)	Change of bit 7 to RTCWEN bit
—	Peripheral enable register 1 (PER1)	New addition
Subsystem clock supply mode control register (OSMC)	Subsystem clock supply mode control register (OSMC)	Addition of HIPREC bit to bit 0. Change of bits 1 and 2 to undefined values.
—	Subsystem clock select register (CKSEL)	New addition
High-speed on-chip oscillator frequency select register (HOCODIV)	High-speed on-chip oscillator frequency select register (HOCODIV)	None
—	Middle-speed on-chip oscillator frequency select register (MOCODIV)	New addition
—	High-speed system clock division register (MOSCDIV)	New addition
High-speed on-chip oscillator trimming register (HIOTRM)	High-speed on-chip oscillator trimming register (HIOTRM)	None
—	Middle-speed on-chip oscillator trimming register (MIOTRM)	New addition
—	Low-speed on-chip oscillator trimming register (LIOTRM)	New addition
—	Standby mode release setting register (WKUPMD)	New addition

Note : The register name is unchanged : Additional contents : Changed contents

: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.3 Timer Array Unit

Table 2.4 Registers Controlling Timer Array Unit

RL78/G13	RL78/G23	
Register name	Register name	Remark
Peripheral enable register 0 (PER0)	Peripheral enable register 0 (PER0)	No change for bits 0 and 1 (TAU0EN, TAU1EN) used to set this peripheral function. However, bit 7 is changed to RTCWEN bit.
—	Peripheral reset control register 0 (PRR0)	New addition
Timer clock select register m (TPSm)	Timer clock select register m (TPSm)	None
Timer mode register mn (TMRmn)	Timer mode register mn (TMRmn)	None
Timer status register mn (TSRmn)	Timer status register mn (TSRmn)	None
Timer channel enable status register m (TEm)	Timer channel enable status register m (TEm)	None
Timer channel start register m (TSM)	Timer channel start register m (TSM)	None
Timer channel stop register m (TTm)	Timer channel stop register m (TTm)	None
Timer input select register 0 (TIS0)	Timer input select register 0 (TIS0)	None
—	Timer input select register 1 (TIS1)	New addition
Timer output enable register m (TOEm)	Timer output enable register m (TOEm)	None
Timer output register m (TOm)	Timer output register m (TOm)	None
Timer output level register m (TOLm)	Timer output level register m (TOLm)	None
Timer output mode register m (TOMm)	Timer output mode register m (TOMm)	None
Input switch control register (ISC)	Input switch control register (ISC)	Addition of ISC2 to ISC7 bits to bits 2 to 7.
Noise filter enable registers 1, 2 (NFEN1, NFEN2)	Noise filter enable registers 1, 2 (NFEN1, NFEN2)	None
Port mode control register (PMCxx)	Port mode control A register (PMCAxx)	Change of applicable pins
—	Port mode control T register (PMCTxx)	New addition
—	Port mode control E register (PMCExx)	New addition
Port mode register (PMxx)	Port mode register (PMxx)	Addition of PM121 and PM122 bits to PM12 register.
Port register (Pxx)	Port register (Pxx)	None
—	Port function output enable register 0 (PFOE0)	New addition

Note : The register name is unchanged. : Additional contents : Changed contents

: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.4 Realtime Clock

Table 2.5 Registers Controlling the Realtime Clock

RL78/G13	RL78/G23	
Register name	Register name	Remark
Peripheral enable register 0 (PER0)	Peripheral enable register 0 (PER0)	Bit 7 is changed to RTCWEN bit.
Subsystem clock supply mode control register (OSMC)	Subsystem clock supply mode control register (OSMC)	No change for bit 4 (WUTMMCK0) used to set this peripheral function. However, HIPREC bit is added to bit 0. Bits 1 and 2 are changed to undefined values .
Realtime clock control register 0 (RTCC0)	Realtime clock control register 0 (RTCC0)	Addition of RTC128EN bit to bit 4
Realtime clock control register 1 (RTCC1)	Realtime clock control register 1 (RTCC1)	None
Second count register (SEC)	Second count register (SEC)	None
Minute count register (MIN)	Minute count register (MIN)	None
Hour count register (HOUR)	Hour count register (HOUR)	None
Day count register (DAY)	Day count register (DAY)	None
Day-of-week count register (WEEK)	Day-of-week count register (WEEK)	None
Month count register (MONTH)	Month count register (MONTH)	None
Year count register (YEAR)	Year count register (YEAR)	None
Time error correction register (SUBCUD)	Time error correction register (SUBCUD)	None
Alarm minute register (ALARMWWM)	Alarm minute register (ALARMWWM)	None
Alarm hour register (ALARMWH)	Alarm hour register (ALARMWH)	None
Alarm day-of-week register (ALARMWW)	Alarm day-of-week register (ALARMWW)	None
Port mode register 3 (PM3)	Port mode register 3 (PM3)	No change for bit 0 (PM30) used to set this peripheral function. However, PM32 to PM37 bits are added to bits 2 to 7.
Port register 3 (P3)	Port register 3 (P3)	None

Note : The register name is unchanged. : Additional contents : Changed contents

: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.5 Clock Output/Buzzer Output Controller

Table 2.6 Registers Controlling Clock Output/Buzzer Output Controller

RL78/G13	RL78/G23	
Register name	Register name	Remark
Clock output select registers n (CKSn)	Clock output select registers n (CKSn)	None
Port mode registers 1, 3, 5, 14 (PM1, PM3, PM5, PM14)	Port mode registers 1, 3, 5, 14 (PM1, PM3, PM5, PM14)	None
Port registers 1, 3, 5, 14 (P1, P3, P5, P14)	Port registers 1, 3, 5, 14 (P1, P3, P5, P14)	None
—	Port mode control T registers (PMCTxx)	New addition
—	Port mode control E registers (PMCExx)	New addition

Note : The register name is unchanged. : Additional contents : Changed contents

: Deleted contents —: There is no corresponding register.


Caution. For details of each register function, refer to the User's Manual: Hardware.

2.6 Watchdog Timer

Table 2.7 Register Controlling Watchdog Timer

RL78/G13	RL78/G23	
Register name	Register name	Remark
Watchdog timer enable register (WDTE)	Watchdog timer enable register (WDTE)	None

Note : The register name is unchanged. : Additional contents : Changed contents

: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.7 A/D Converter

Table 2.8 Registers Controlling A/D Converter

RL78/G13	RL78/G23	
Register name	Register name	Remark
Peripheral enable register 0 (PER0)	Peripheral enable register 0 (PER0)	No change for bit 5 (ADCEN) used to set this peripheral function. However, bit 7 is changed to RTCWEN bit.
—	Peripheral reset control register 0 (PRR0)	New addition
A/D converter mode register 0 (ADM0)	A/D converter mode register 0 (ADM0)	None
A/D converter mode register 1 (ADM1)	A/D converter mode register 1 (ADM1)	Addition of ADTRS2 bit to bit 2. Addition of ADLSP bit to bit 3.
A/D converter mode register 2 (ADM2)	A/D converter mode register 2 (ADM2)	Bit 0 is changed to ADTYP0 bit. Addition of ADTYP1 bit to bit 1.
10-bit A/D conversion result register (ADCR)	12-bit/10-bit A/D conversion result register (ADCRn)	- Changed the register name. - Added 12-bit resolution A/D conversion.
8-bit A/D conversion result register (ADCRH)	8-bit A/D conversion result register (ADCRnH)	Changed applicable pins
Analog input channel specification register (ADS)	Analog input channel specification register (ADS)	None
Conversion result comparison upper limit setting register (ADUL)	Conversion result comparison upper limit setting register (ADUL)	None
Conversion result comparison lower limit setting register (ADLL)	Conversion result comparison lower limit setting register (ADLL)	None
A/D test register (ADTES)	A/D test register (ADTES)	None
A/D port configuration register (ADPC)	—	Deleted item.
Port mode control registers 0, 3, 10, 11, 12, and 14 (PMC0, PMC3, PMC10, PMC11, PMC12, PMC14)	Port mode control A registers 0, 3, 10, 11, 12, and 14 (PMCA0, PMCA3, PMCA10, PMCA11, PMCA12, PMCA14)	Changed applicable pins
—	Port mode control T registers 0, 3 (PMCT0, PMCT3)	New addition
—	Port mode control E registers 0, 3 (PMCE0, PMCE3)	New addition
Port mode registers 0, 2, 3, 10, 11, 12, 14, and 15 (PM0, PM2, PM3, PM10, PM11, PM12, PM14, PM15)	Port mode registers 0, 2, 3, 10, 11, 12, 14, and 15 (PM0, PM2, PM3, PM10, PM11, PM12, PM14, PM15)	Addition of PM121 and PM122 bits to PM12 register.

Note : The register name is unchanged. : Additional contents : Changed contents





: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.8 Serial Array Unit

Table 2.9 Registers Controlling Serial Array Unit (1/2)

RL78/G13	RL78/G23	
Register name	Register name	Remark
Peripheral enable register 0 (PER0)	Peripheral enable register 0 (PER0)	No change for bits 2 and 3 (SAU0EN, SAU1EN) used to set this peripheral function. However, bit 7 is changed to RTCWEN bit.
—	Peripheral reset control register 0 (PRR0)	New addition
Serial clock select register m (SPSm)	Serial clock select register m (SPSm)	None
Serial mode register mn (SMRmn)	Serial mode register mn (SMRmn)	None
Serial communication operation setting register mn (SCRmn)	Serial communication operation setting register mn (SCRmn)	None
Serial data register mn (SDRmn)	Serial data register mn (SDRmn)	None
Serial flag clear trigger register mn (SIRmn)	Serial flag clear trigger register mn (SIRmn)	None
Serial status register mn (SSRmn)	Serial status register mn (SSRmn)	None
Serial channel start register m (SSm)	Serial channel start register m (SSm)	None
Serial channel stop register m (STm)	Serial channel stop register m (STm)	None
Serial channel enable status register m (SEm)	Serial channel enable status register m (SEm)	None
Serial output enable register m (SOEm)	Serial output enable register m (SOEm)	None
Serial output level register m (SOLm)	Serial output level register m (SOLm)	None
Serial output register m (SOM)	Serial output register m (SOM)	None
Serial standby control register m (SSCm)	Serial standby control register m (SSCm)	None
Input switch control register (ISC)	Input switch control register (ISC)	Addition of ISC2 to ISC7 bits to bits 2 to 7.
Noise filter enable register 0 (NFEN0)	Noise filter enable register 0 (NFEN0)	None

Note : The register name is unchanged. : Additional contents : Changed contents
: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

Table 2.10 Registers Controlling Serial Array Unit (2/2)

RL78/G13	RL78/G23	
Register name	Register name	Remark
Port input mode registers 0, 1, 4, 5, 8, 14 (PIM0, PIM1, PIM4, PIM5, PIM8, PIM14)	Port input mode registers 0, 1, 4, 5, 8, 14 (PIM0, PIM1, PIM4, PIM5, PIM8, PIM14)	Addition of PIM41 bit to PIM4 register. Addition of PIM84 bit to PIM8 register.
Port output mode registers 0, 1, 4, 5, 7 to 9, 14 (POM0, POM1, POM4, POM5, POM7 to POM9, POM14)	Port output mode registers 0, 1, 4, 5, 7 to 9, 14 (POM0, POM1, POM4, POM5, POM7 to POM9, POM14)	Addition of POM42 bit to POM4 register. Addition of POM72 bit to POM7 register. Addition of POM83 bit to POM8 register.
Port mode control registers 0, 3, 14 (PMC0, PMC3, PMC14)	Port mode control A registers 0, 3, 14 (PMCA0, PMCA3, PMCA14)	Changed applicable pins
—	Port mode control T registers 0, 3 (PMCT0, PMCT3)	New addition
—	Port mode control E register 0 (PMCE0)	New addition
—	Port function output enable registers (PFOEx)	New addition
Port mode registers 0, 1, 3 to 5, 7 to 9, 14 (PM0, PM1, PM3 to PM5, PM7 to PM9, PM14)	Port mode registers 0, 1, 3 to 5, 7 to 9, 14 (PM0, PM1, PM3 to PM5, PM7 to PM9, PM14)	None
Port registers 0, 1, 3 to 5, 7 to 9, 14 (P0, P1, P3 to P5, P7 to P9, P14)	Port registers 0, 1, 3 to 5, 7 to 9, 14 (P0, P1, P3 to P5, P7 to P9, P14)	None
—	UART loopback select register (ULBS)	New addition

Note : The register name is unchanged. : Additional contents : Changed contents

: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.9 Serial Interface IICA

Table 2.11 Registers Controlling Serial Interface IICA

RL78/G13	RL78/G23	
Register name	Register name	Remark
Peripheral enable register 0 (PER0)	Peripheral enable register 0 (PER0)	No change for bits 6 and 4 (IICA1EN, IICA0EN) used to set this peripheral function. However, bit 7 is changed to RTCWEN bit.
—	Peripheral reset control register 0 (PRR0)	New addition
IICA control register n0 (IICCTLn0)	IICA control register n0 (IICCTLn0)	None
IICA status register n (IICSn)	IICA status register n (IICSn)	None
IICA flag register n (IICFn)	IICA flag register n (IICFn)	None
IICA control register n1 (IICCTLn1)	IICA control register n1 (IICCTLn1)	Addition of SVADISn bit to bit 6.
IICA low-level width setting register n (IICWLn)	IICA low-level width setting register n (IICWLn)	None
IICA high-level width setting register n (IICWHn)	IICA high-level width setting register n (IICWHn)	None
Port mode register 6 (PM6)	Port mode register 6 (PM6)	None
Port register 6 (P6)	Port register 6 (P6)	None

Note : The register name is unchanged. : Additional contents : Changed contents

: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.10 Interrupt Functions

Table 2.12 Registers Controlling Interrupt Functions

RL78/G13	RL78/G23	
Register name	Register name	Remark
Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, IF3L)	Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, IF3L, IF3H)	Addition of IF3H register. Change of the contents of IF0H, IF1L, IF1H (ITIF → ITLIF bit), IF2L (PIF10 → FLIF bit), IF2H and IF3L.
Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L)	Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L, MK3H)	Addition of MK3H register. Change of the contents of MK0H, MK1L, MK1H (ITMK → ITLMK bit), MK2L (PMK10 → FLMK bit), MK2H and MK3L.
Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L)	Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR03H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR13L, PR13H)	Addition of PR03H and PR13H. Change of the contents of PR00H, PR10H, PR01L, PR11L, PR01H, PR11H (ITPR0, ITPR1 → ITLPR0, ITLPR1 bit), PR02L, PR12L (PPR010, PPR110 → FLPR0, FLPR1 bit), PR02H, PR12H, PR03L and PR13L.
External interrupt rising edge enable registers (EGP0, EGP1)	External interrupt rising edge enable registers (EGP0, EGP1)	None
External interrupt falling edge enable registers (EGN0, EGN1)	External interrupt falling edge enable registers (EGN0, EGN1)	None
Program status word (PSW)	Program status word (PSW)	None

Note : The register name is unchanged. : Additional contents : Changed contents





: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.11 Key Interrupt Function

Table 2.13 Register Controlling the Key Interrupt

RL78/G13	RL78/G23	
Register name	Register name	Remark
—	Key return control register (KRCTL)	New addition
Key return mode register (KRM)	Key return mode register 0 (KRM0)	Changed applicable pins
—	Key return flag register (KRF)	New addition
Port mode register 7 (PM7)	Port mode register 7 (PM7)	None





Note : The register name is unchanged. : Additional contents : Changed contents
: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.12 Standby Function

Table 2.14 Registers Controlling Standby Function

RL78/G13	RL78/G23	
Register name	Register name	Remark
Subsystem clock supply mode control register (OSMC)	Subsystem clock supply mode control register (OSMC)	Addition of HIPREC bit to bit 0. Bits 1 and 2 are changed to undefined values.
Oscillation stabilization time counter status register (OSTC)	Oscillation stabilization time counter status register (OSTC)	None
Oscillation stabilization time select register (OSTS)	Oscillation stabilization time select register (OSTS)	None
—	Standby mode release setting register (WKUPMD)	New addition
—	Memory power reduction control register (PSMCR)	New addition

Note : The register name is unchanged. : Additional contents : Changed contents
: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.13 Reset Function

Table 2.15 Registers for Confirming Reset Sources

RL78/G13	RL78/G23	
Register name	Register name	Remark
Reset control flag register (RESF)	Reset control flag register (RESF)	None
—	Power-on-reset status register (PORSR)	New addition
—	Peripheral reset control register 0 (PRR0)	New addition
—	Peripheral reset control register 1 (PRR1)	New addition

Note : The register name is unchanged. : Additional contents : Changed contents

: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.14 Power-On-Reset Circuit

There is no register that controls the power-on-reset circuit.

2.15 Voltage Detector

Table 2.16 Registers Controlling Voltage Detector

RL78/G13	RL78/G23	
Register name	Register name	Remark
User option byte 000C1H/ 010C1H (Settings related to LVD.)	User option byte 000C1H/ 040C1H (Settings related to LVD.)	Changed functions of option bytes. Changed address when using the boot swap operation.
Voltage detection register (LVIM)	Voltage detection register (LVIM)	Bit 0 has been changed to LVD0F bit. Bit 1 has been changed to LVD1F bit. Bit 2 has been changed to DLVD0F bit. Bit 3 has been changed to DLVD1F bit.
—	LVD detection flag clearing register (LVDFCLR)	New addition
Voltage detection level register (LVIS)	Voltage detection level register (LVIS)	Bit 0 is changed to LVD1V0 bit. Bit 1 is changed to LVD1V1 bit. Bit 2 is changed to LVD1V2 bit. Bit 3 is changed to LVD1V3 bit. Bit 4 is changed to LVD1V4 bit. Bit 6 is changed to LVD1SEL bit. Bit 7 is changed to LVD1EN bit.

Note : The register name is unchanged : Additional contents : Changed contents





: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.16 Safety Functions

Table 2.17 Registers Used by Safety Functions

RL78/G13	RL78/G23	
Register name	Register name	Remark
Flash memory CRC control register (CRC0CTL)	Flash memory CRC control register (CRC0CTL)	None
Flash memory CRC operation result register (PGCRCL)	Flash memory CRC operation result register (PGCRCL)	None
CRC input register (CRCIN)	CRC input register (CRCIN)	None
CRC data register (CRCD)	CRC data register (CRCD)	None
—	Code flash memory guard register (GFLASH0)	New addition
—	Data flash memory guard register (GFLASH1)	New addition
—	Flash security area guard register (GFLASH2)	New addition
RAM parity error control register (RPECTL)	RAM parity error control register (RPECTL)	None
Invalid memory access detection control register (IAWCTL)	Invalid memory access detection control register (IAWCTL)	None
—	Guard register of IAWCTL register (GIWCTL)	New addition
Timer input select register 0 (TIS0)	Timer input select register 0 (TIS0)	None
A/D test register (ADTES)	A/D test register (ADTES)	None
Analog input channel specification register (ADS)	Analog input channel specification register (ADS)	None
—	Port mode select register (PMS)	New addition
—	UART loopback select register (ULBS)	New addition

Note : The register name is unchanged. : Additional contents : Changed contents
: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

2.17 Regulator





There is no register that controls the regulator.

2.18 Option Bytes

There is no register that controls the option bytes. The function of option bytes is set using the option byte area. Table 2.18 shows a comparison of RL78/G13 and RL78/G23 option byte areas.

Table 2.18 Option Byte Area

RL78/G13	RL78/G23	
Option byte area (Normal/Boot swap operation)	Option byte area (Normal/Boot swap operation)	Remark
000C0H-000C3H / 010C0H-010C3H	000C0H-000C3H / 040C0H-040C3H	Changed functions of option bytes. Changed address when using the boot swap operation.
User option bytes 000C0H-000C2H / 010C0H-010C2H	User option bytes 000C0H-000C2H / 040C0H-040C2H	
000C0H / 010C0H (Settings related to WDT.)	000C0H / 040C0H (Settings related to WDT.)	
000C1H / 010C1H (Settings related to LVD.)	000C1H / 040C1H (Settings related to LVD.)	
000C2H / 010C2H (Settings related to flash and HOCO.)	000C2H / 040C2H (Settings related to flash and HOCO.)	
On-chip debug option byte 000C3H / 010C3H	On-chip debug option byte 000C3H / 040C3H	

Note : The option bytes name is unchanged. : Additional contents : Changed contents
: Deleted contents —: There is no corresponding register.

Caution. For details of the function of each option bytes, refer to the User's Manual: Hardware.





2.19 On-Chip Debugging

There is no register that controls the on-chip debugging function.

2.20 BCD Correction Circuit

Table 2.19 Register Used by BCD Correction Circuit

RL78/G13	RL78/G23	
Register name	Register name	Remark
BCD correction result register (BCDADJ)	BCD correction result register (BCDADJ)	None

Note : The register name is unchanged. : Additional contents : Changed contents
: Deleted contents —: There is no corresponding register.

Caution. For details of each register function, refer to the User's Manual: Hardware.

3. Other changes and notes

3.1 RL78/G23 instruction set

"Multiply and accumulation register (MACR)", which is used in the multiply and accumulation instructions, is added on RL78/G23. (The MACR register is composed of multiply and accumulation register (H)/(L): MACRH/MACRL).

4. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146)

RL78/G23 User's Manual: Hardware (R01UH0896)

RL78 Family User's Manual: Software (R01US0015)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.13.21	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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