RL78/G13

DMA Controller (PWM Output) CC-RL

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Introduction

This application note explains how to use the PWM output function of the timer array unit (TAU) through the DMA controller. The sample application covered in this application note controls the brightness of an LED using the PWM output function. It starts the DMA controller using the timer interrupt from channel 2 of the timer array unit 0 as the trigger. The application transfers data from the on-chip RAM to the TDR01 register of the TAU0 through the DMA controller. The brightness of the LED is controlled by changing the duty factor of the PWM output.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

The sample application covered in this application note generates PWM output by operating channel 0 of the timer array unit 0 (TAU0) as the master and channel 1 as a slave in simultaneous operation. The PWM output is connected to LED1 (for PWM output) to control the brightness of the LED.

Channel 2 of the TAU0 (with an interval time of 500 ms) and the DMA controller are used to change the duty factor of the PWM output at regular intervals. The output to LED2 (for status update) is inverted at the timing when the duty factor is changed.

Table 1.1 shows peripheral functions to be used and their uses. Figure 1.1 presents an overview of the PWM output operation. Table 1.2 shows the relationship between the duty factors of the PWM output and the brightness of the LED. Figure 1.2 is a timing chart which outlines the PWM output operation.

Table 1.1 Peripheral Functions to be Used and their Uses

Peripheral Function	Use
Timer array unit 0	This unit is used to set the PWM function by operating channel 0 and channel 1 in simultaneous operation and deliver a PWM output from the TO01 pin. Channel 2 is set up as an interval timer to generate timer interrupts (INTTM02) at regular intervals (500 ms).
DMA Controller	INTTM02 is selected as the DMA start source and the duty factor of the PWM output is changed when an INTTM02 occurs.

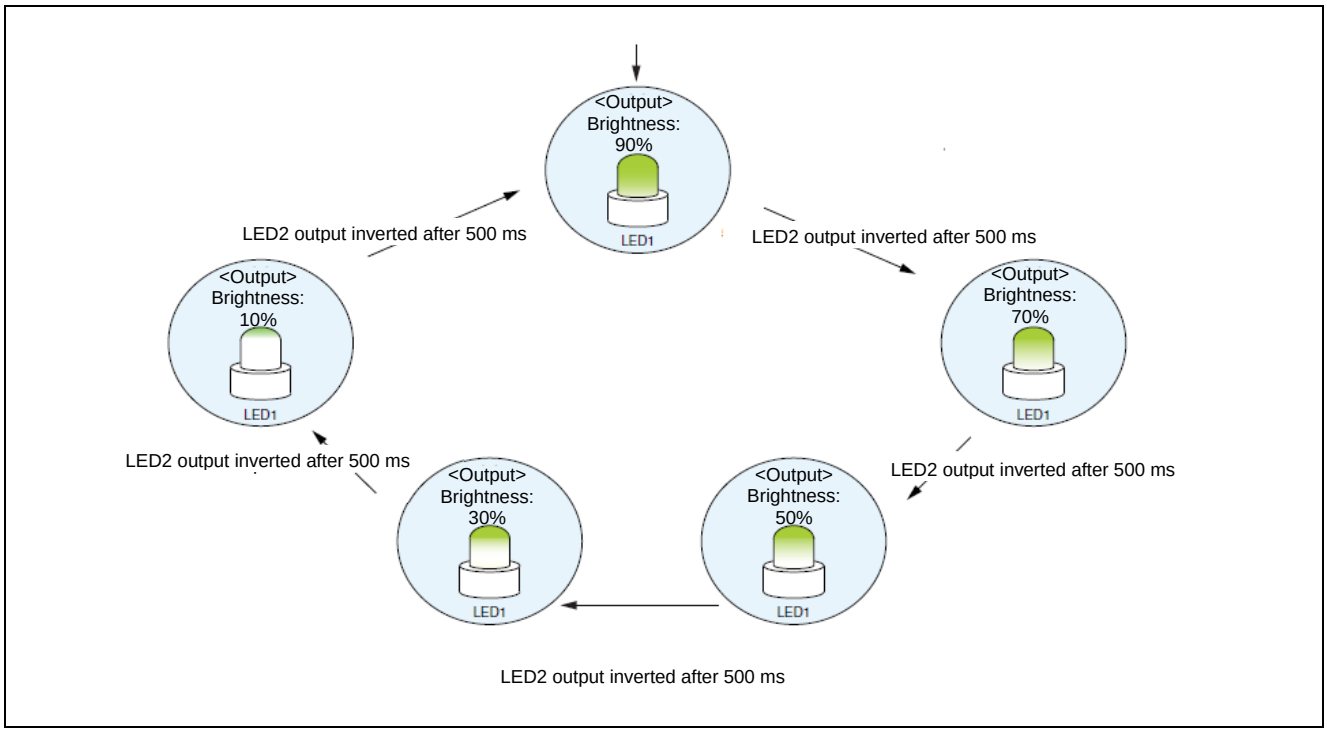
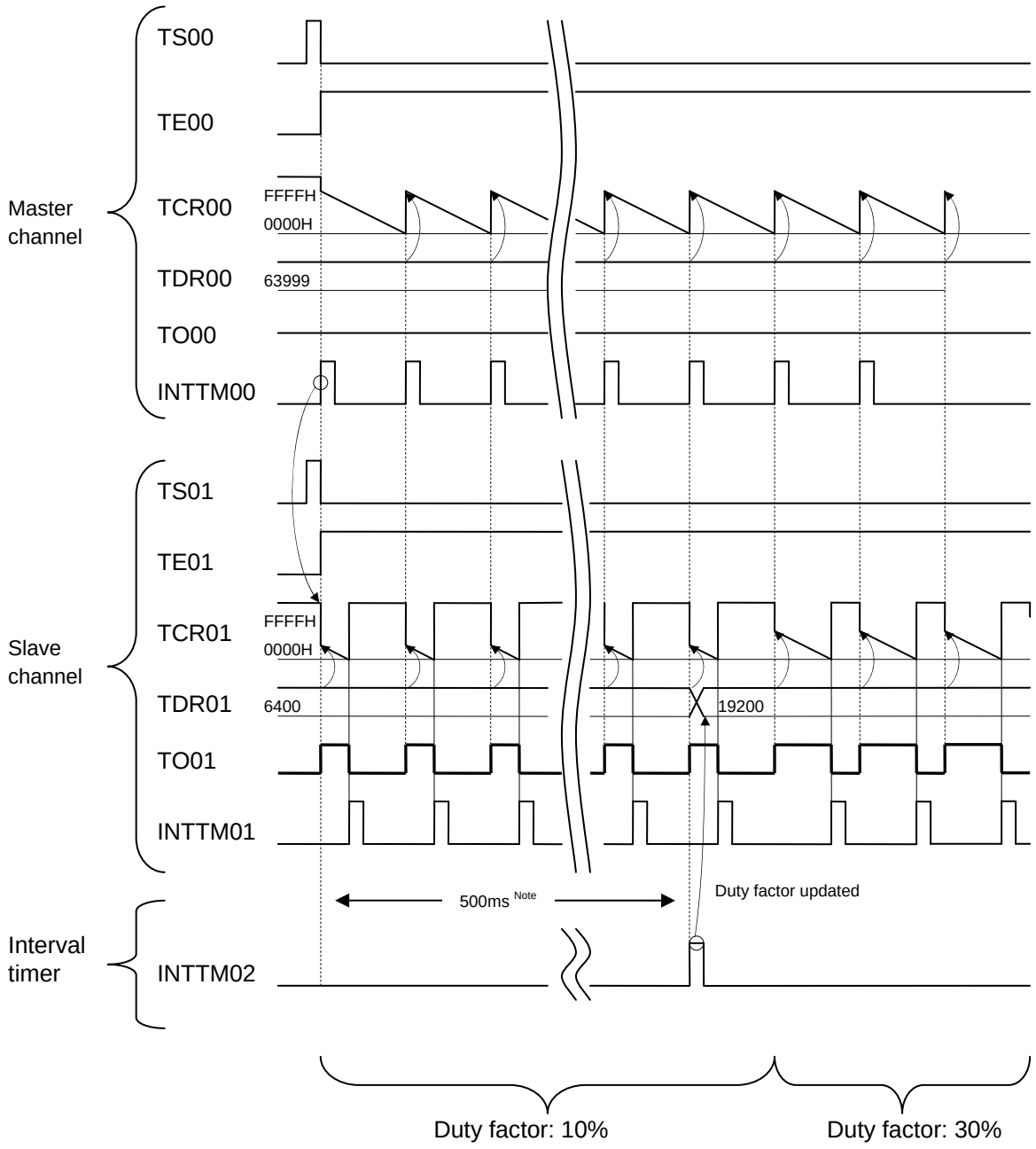


Figure 1.1 Overview of PWM Output Operation

Note: The first change in the duty factor of the PWM output occurs in one second after power is turned on.

Table 1.2 Relationship between Duty Factors of PWM Output and Brightness of LED

Duty factor	Brightness of LED1
10%	90%
30%	70%
50%	50%
70%	30%
90%	10%



Note: The first change in the duty factor of the PWM output occurs in one second after power is turned on.

Figure 1.2 Timing Chart which Outlines PWM Output Operation

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.

3. Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G13 Initialization (R01AN2575E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

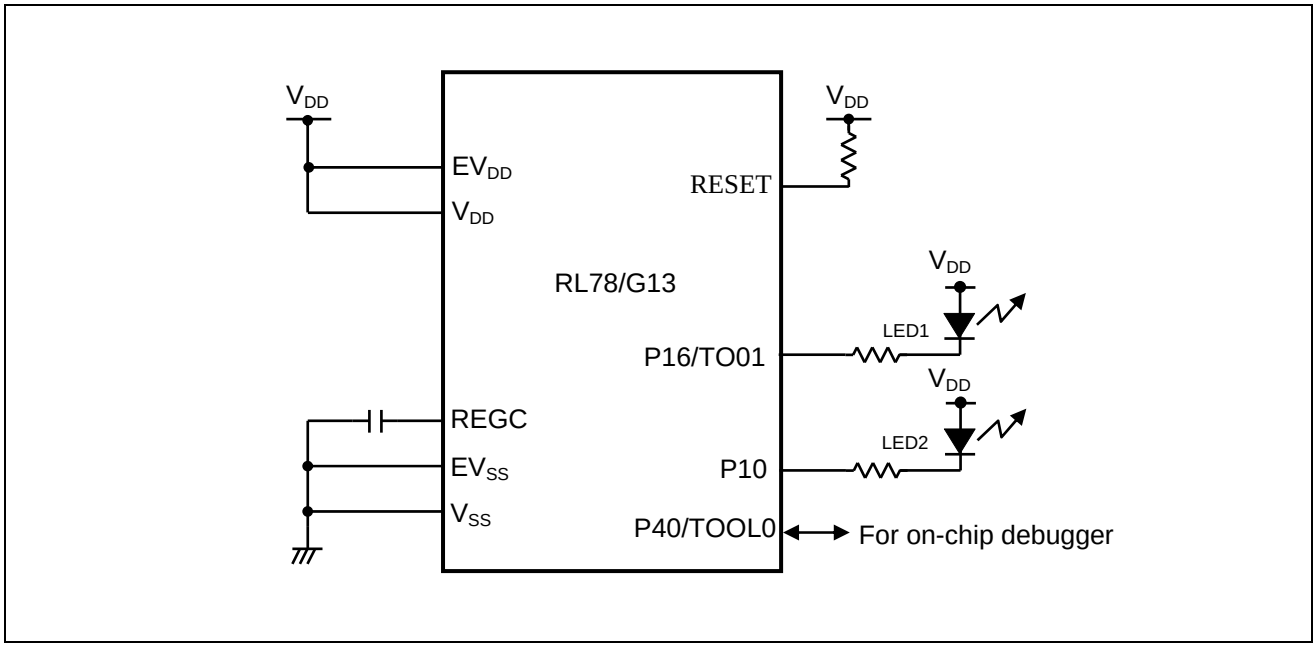


Figure 4.1 Hardware Configuration

Caution: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P16/TO01	Output	PWM output port
P10	Output	LED port to indicate the update of the duty factor.

5. Software Description

5.1 Operation Outline

The sample application covered in this application note uses the PWM function by operating channels 0 and 1 of the TAU0 in simultaneous operation. The PWM output from P16/TO01 is used to control the brightness of LED1.

The application uses channel 2 of the TAU0 (with an interval time of 500 ms) and the DMA controller to change the duty factor of the PWM output at certain intervals. The output to LED2 (for status update) is inverted at the timing when the duty factor is changed.

(1) Initialize the DMA controller.
<Conditions for setting>

- Set the DMA transfer direction to "on-chip RAM to SFR."
- Use a timer interrupt (INTTM02) from timer channel 2 as the DMA start source.
- Set the transfer data size to 16 bits.
- Set the DMA transfer destination to timer data register 01 (TDR01).
- Set the DMA transfer source to the start address of the variable dma_buffer [].
- Set the number of times of DMA transfer to 5.

(2) Initialize the TAU0.
<Conditions for setting>

- Set the P16/TO01 pin to a PWM output.
- Set channel 0 of the TAU0 to 2-ms cycle interval timer mode.
- Set channel 1 of the TAU0 to one-count mode.
- Use channel 2 of the TAU0 in 500-ms interval timer mode.
- Initialize the duty factor of the PWM output to 10%.
- Use a timer interrupt (INTTM02) from channel 2 of the TAU0.

(3) Start operation by setting both the operation enable trigger bits for channels 0 and 1 of the TAU0 simultaneously to 1. Also, set the operation enable trigger bit of channel 2 of the TAU0 to 1.
(4) Execute a HALT instruction and wait for a timer interrupt (INTTM02) from channel 2 of the TAU0 and a transfer end interrupt (INTDMA0) from channel 0 of the DMA controller.
(5) Cancel the HALT mode when timer interrupts (INTTM02) occur at intervals of 500 ms.
(6) Increase the duty factor from 10% to 90% (10% → 30% → 50% → 70% → 90%) in units of 20% each time a timer interrupt (INTTM02) from channel 2 of the TAU0 occurs.
(7) When the duty factor reaches 90%, the DMA controller is set up again so that it repeats transfer starting at a duty factor of 10% by a subsequent DMA transfer end interrupt (INTDMA0) of channel 0 of the DMA controller.
(8) After the processing of the timer interrupt (INTTM02) from channel 2 of the TAU0 is completed and after the processing of the transfer end interrupt (INTDMA0) from channel 0 of the DMA controller is completed, the application reexecutes the HALT instruction and waits for a timer interrupt (INTTM02) from channel 2 of the TAU0 and a transfer end interrupt (INTDMA0) from channel 0 of the TAU0.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
DUTY_FACTOR_BASE	640	Value of 1% duty factor
DUTY_PATTERN_NUM	5	Number of duty factor patterns
_0002_TAU_CH1_OUTPUT_ENABLE	0x0002U	TOE0 value to enable the TO01
_0001_TAU_CH0_START_TRG_ON	0x0001U	TS0 value to enable channel 0 of TAU0
_0002_TAU_CH1_START_TRG_ON	0x0002U	TS0 value to enable channel 1 of TAU0
_0004_TAU_CH2_START_TRG_ON	0x0004U	TS0 value to enable channel 2 of TAU0
_0005_DMA0_BYTE_COUNT	0x0005U	Number of times of DMA transfer by channel 0

5.4 List of Variables

Table 5.3 lists the global variable that is used by this sample program.

Table 5.3 Global Variable

Type	Variable Name	Contents	Function Used
uint16_t	duty_array[DUTY_PATTERN_NUM]	Array of duty factor patterns	R_DMAC0_Create_UserInit() R_DMAC0_Interrupt()

5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_DMAC0_Start	DMA0 transfer enabling
R_TAU0_Channel0_Start	PWM timer count start processing
R_TAU0_Channel2_Start	Timer count start processing to change duty factor
r_dmac0_interrupt	DMA0 transfer end interrupt
r_tau0_channel2_interrupt	Timer interrupt of timer channel 2

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] R_DMAC0_Start

Synopsis	DMA0 transfer enabling
Header	r_cg_dmac.h
Declaration	void R_DMAC0_Start(void);
Explanation	This function starts controlling DMA transfer. It performs the following operations: • Clears the DMA transfer end interrupt request. • Enables DMA transfer end interrupts. • Enables DMA transfer and transitions to the DMA transfer trigger wait mode.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel0_Start

Synopsis	PWM timer count start processing
Header	r_cg_timer.h
Declaration	void R_TAU0_Channel0_Start(void);
Explanation	This function enables channel 1 for timer outputs. It starts channels 0 and 1 for counting.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel2_Start

Synopsis	Timer count start processing to change duty factor
Header	r_cg_timer.h
Declaration	void R_TAU0_Channel2_Start(void);
Explanation	This function clears the timer interrupt flag of channel 2. It enables the timer interrupt of channel 2. It starts channel 2 for counting.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_dmac0_interrupt

Synopsis	DMA0 transfer end interrupt
Header	r_cg_dmac.h
Declaration	static void __near r_dmac0_interrupt(void);
Explanation	This interrupt processing is performed when the specified number of times of DMA transfer is finished. It resets the on-chip RAM address and the number of times of DMA transfer.
Arguments	None
Return value	None
Remarks	None

Function Name] r_tau0_channel2_interrupt

Synopsis	Timer interrupt of timer channel 2
Header	r_cg_timer.h
Declaration	static void __near r_tau0_channel2_interrupt(void);
Explanation	This function inverts the polarity of the output from P10.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

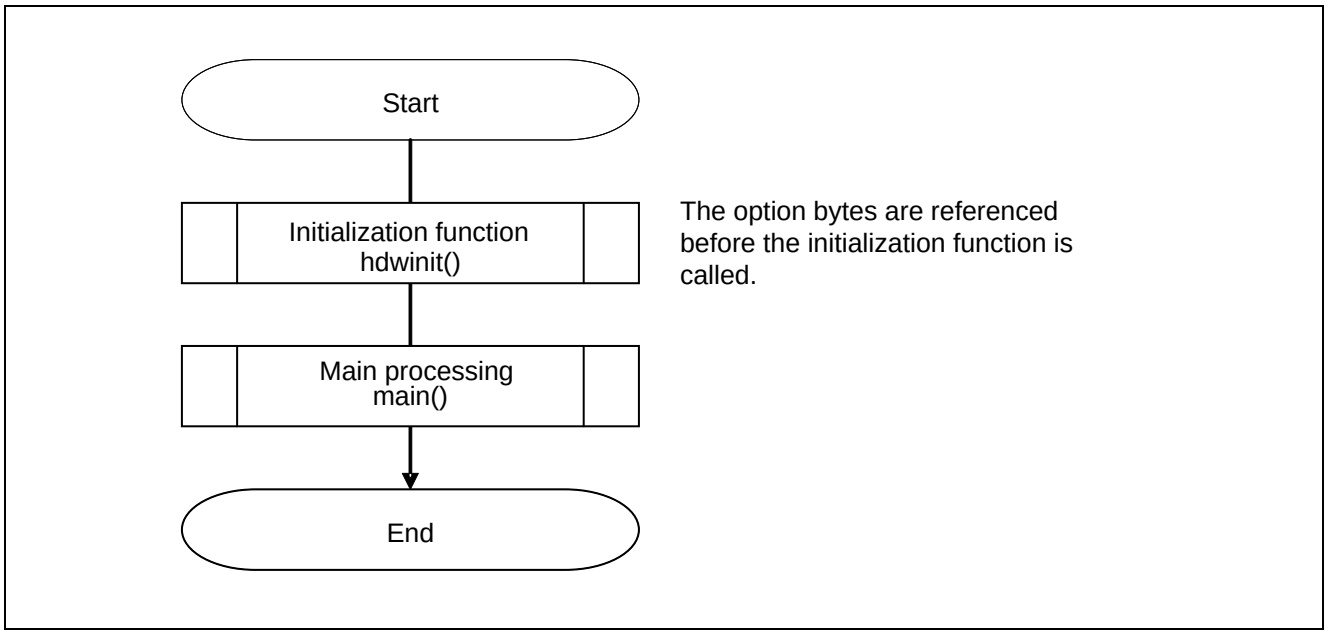


Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

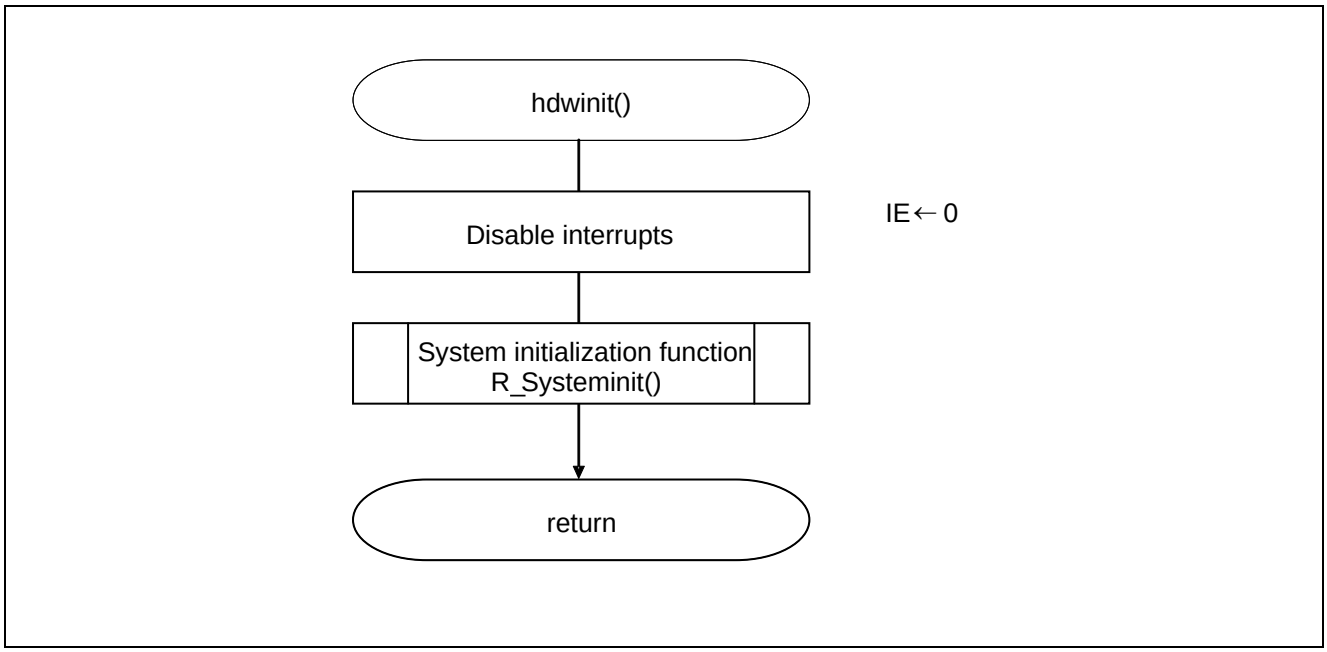


Figure 5.2 Initialization Function

5.7.2 System Function

Figure 5.3 shows the flowchart for the system function.

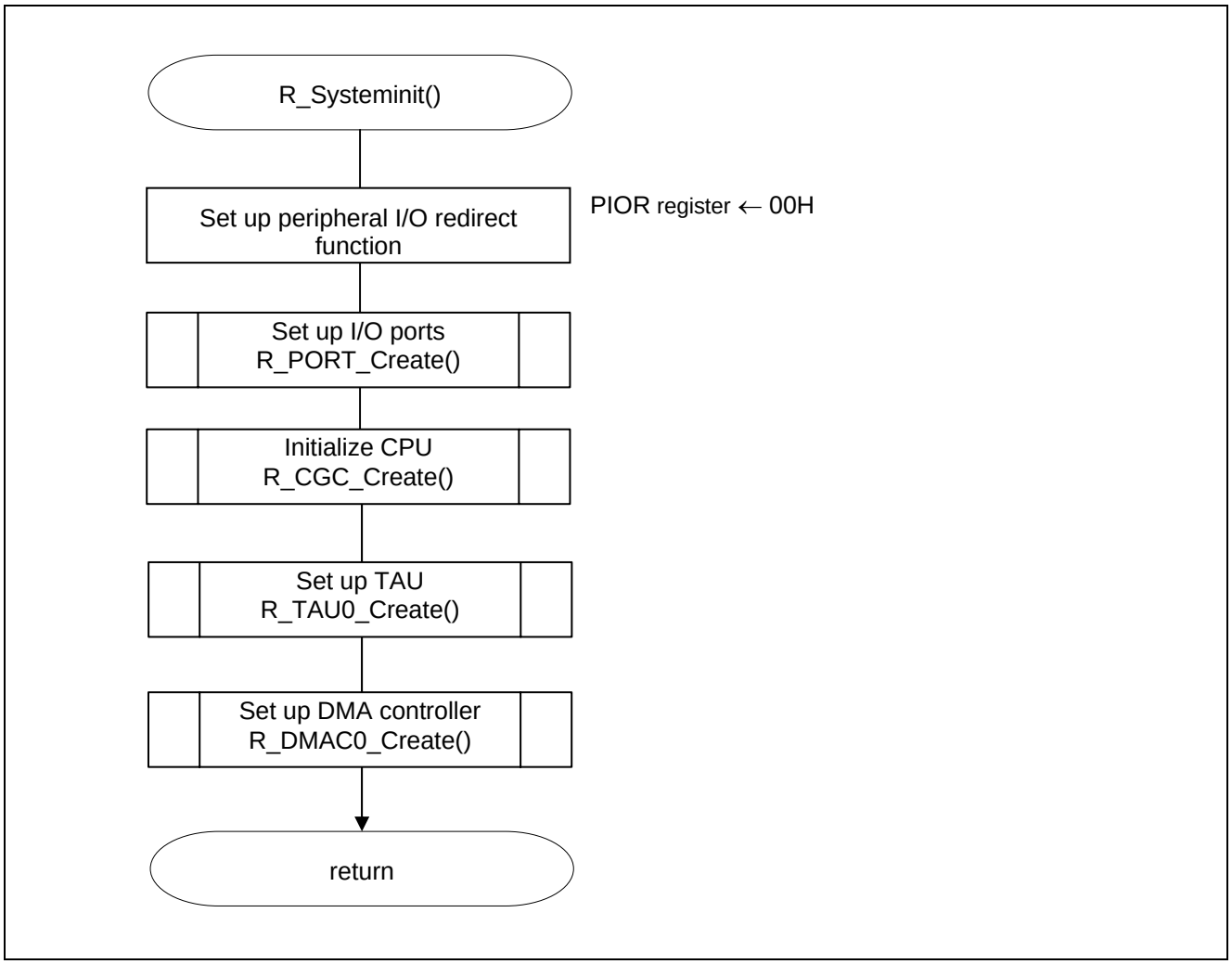


Figure 5.3 System Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for I/O port setup.

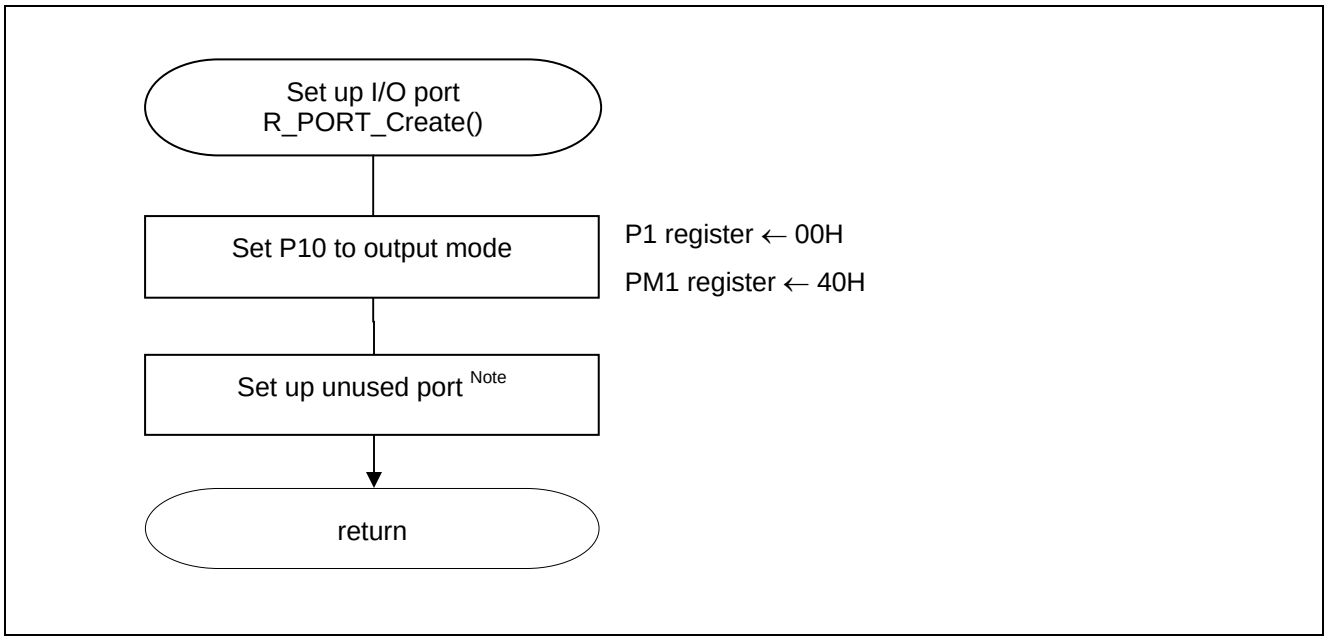


Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the pin for the LED for indicating the duty factor update status

- Port register 1 (P1)
- Port mode register 1 (PM1)

Symbol: P1

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
0	0	0	0	0	0	0	**0**

Bit 0

P10	P10 pin output data control (in output mode)
0	**Output 0**
1	Output 1

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
0	1	0	0	0	0	0	**0**

Bit 0

PM10	P10 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

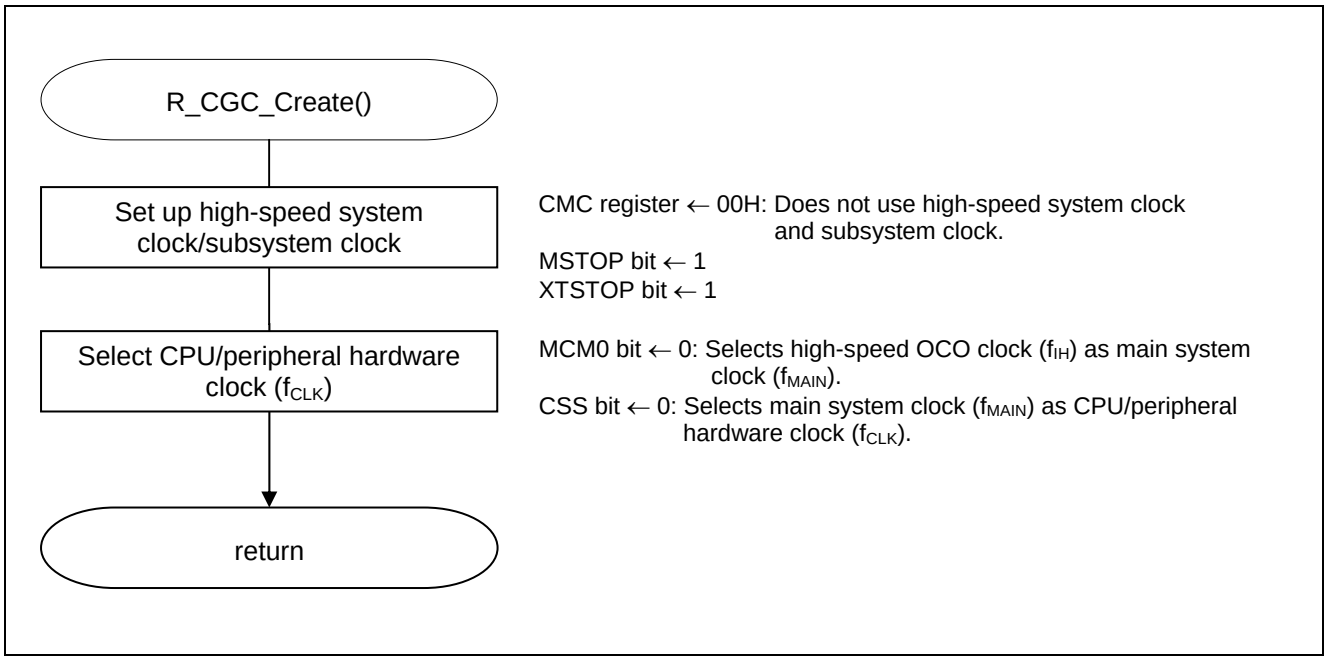


Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 TAU0 Setup

Figures 5.6 and 5.7 show the flowchart for setting up the TAU0.

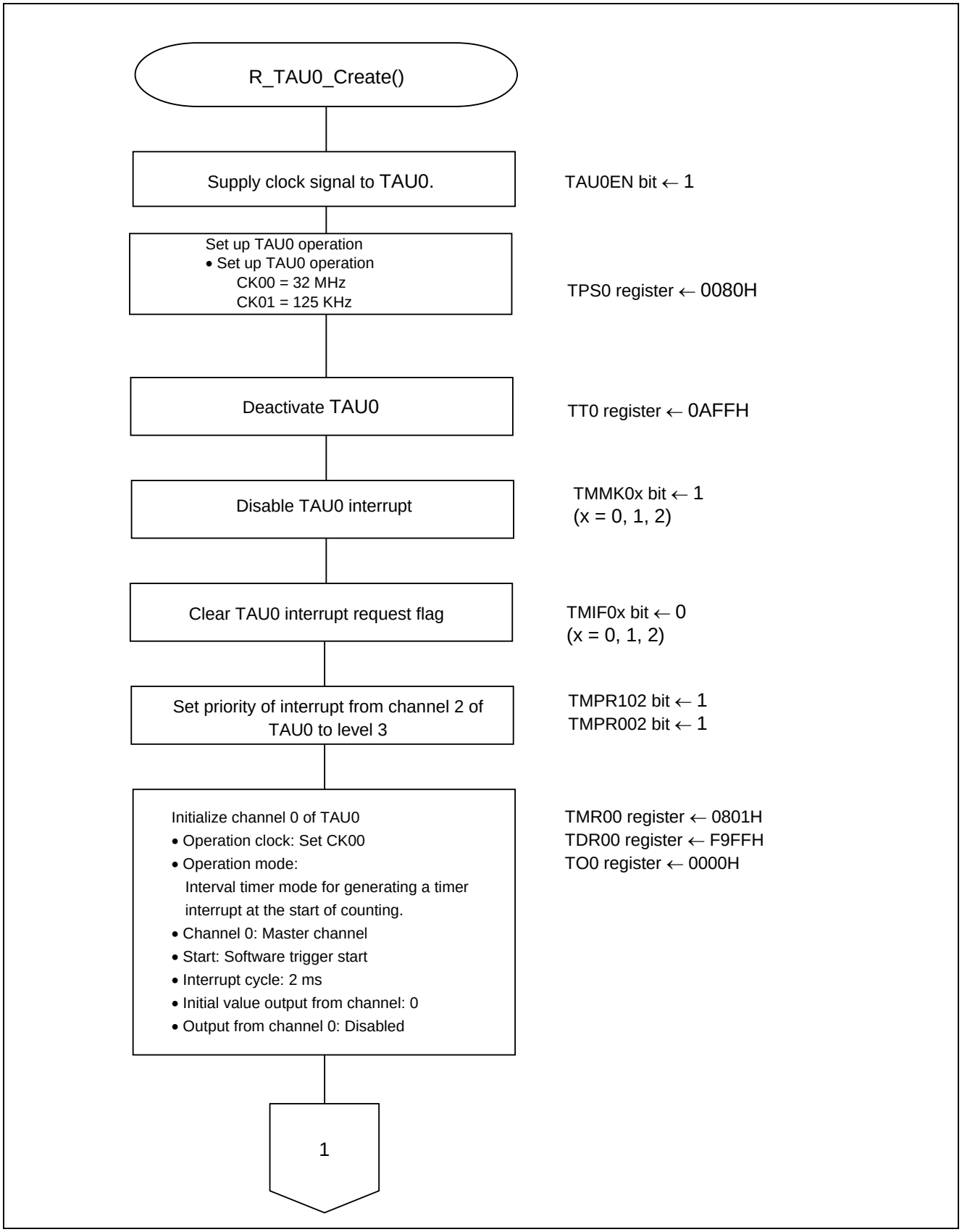


Figure 5.6 TAU0 Setup (1/2)

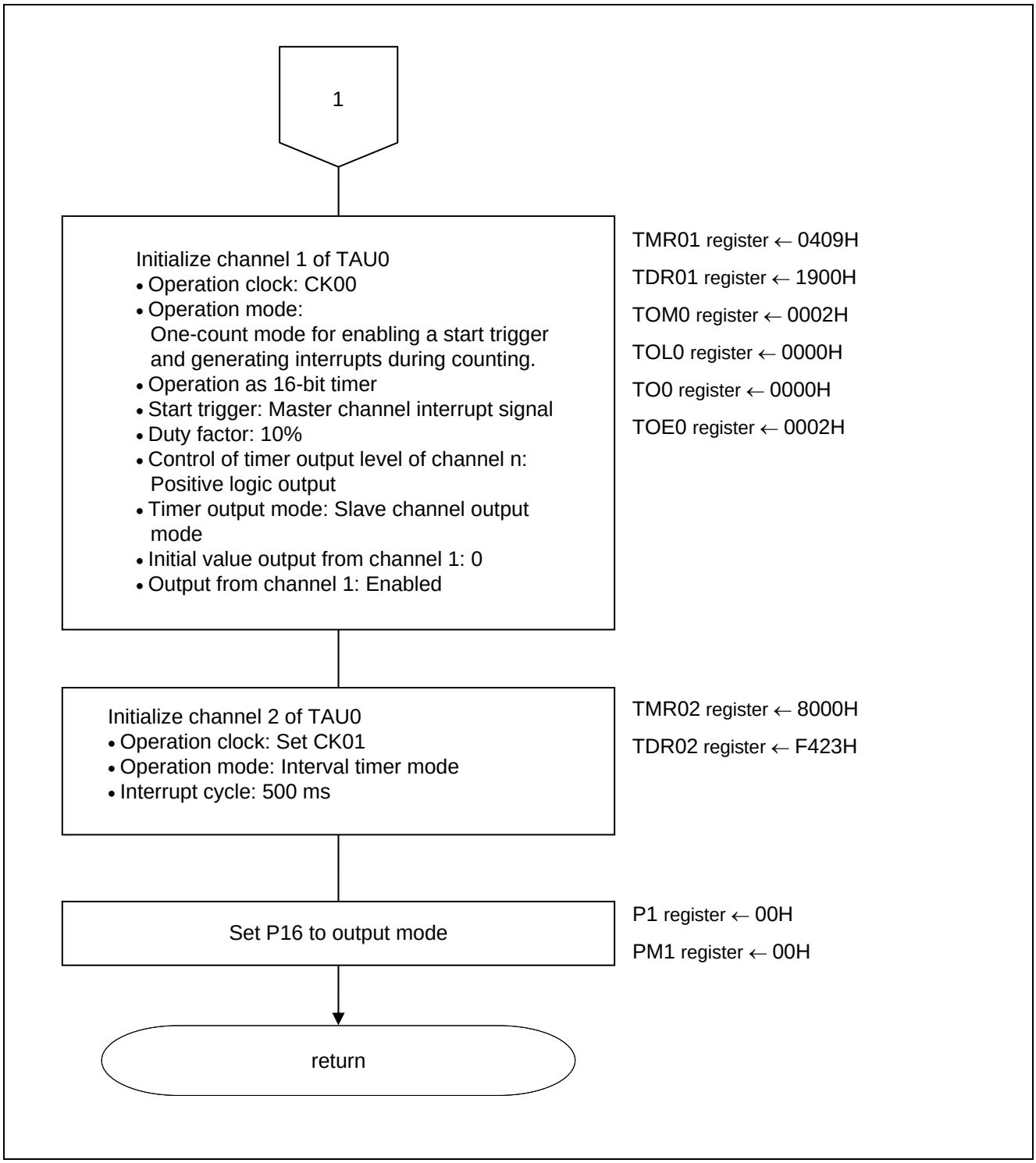


Figure 5.7 TAU0 Setup (2/2)

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Timer Array Unit (PWM Output) Application Note (R01AN2589E).

5.7.6 Initializing DMA Controller

Figure 5.8 shows the flowchart for initializing the DMA controller.

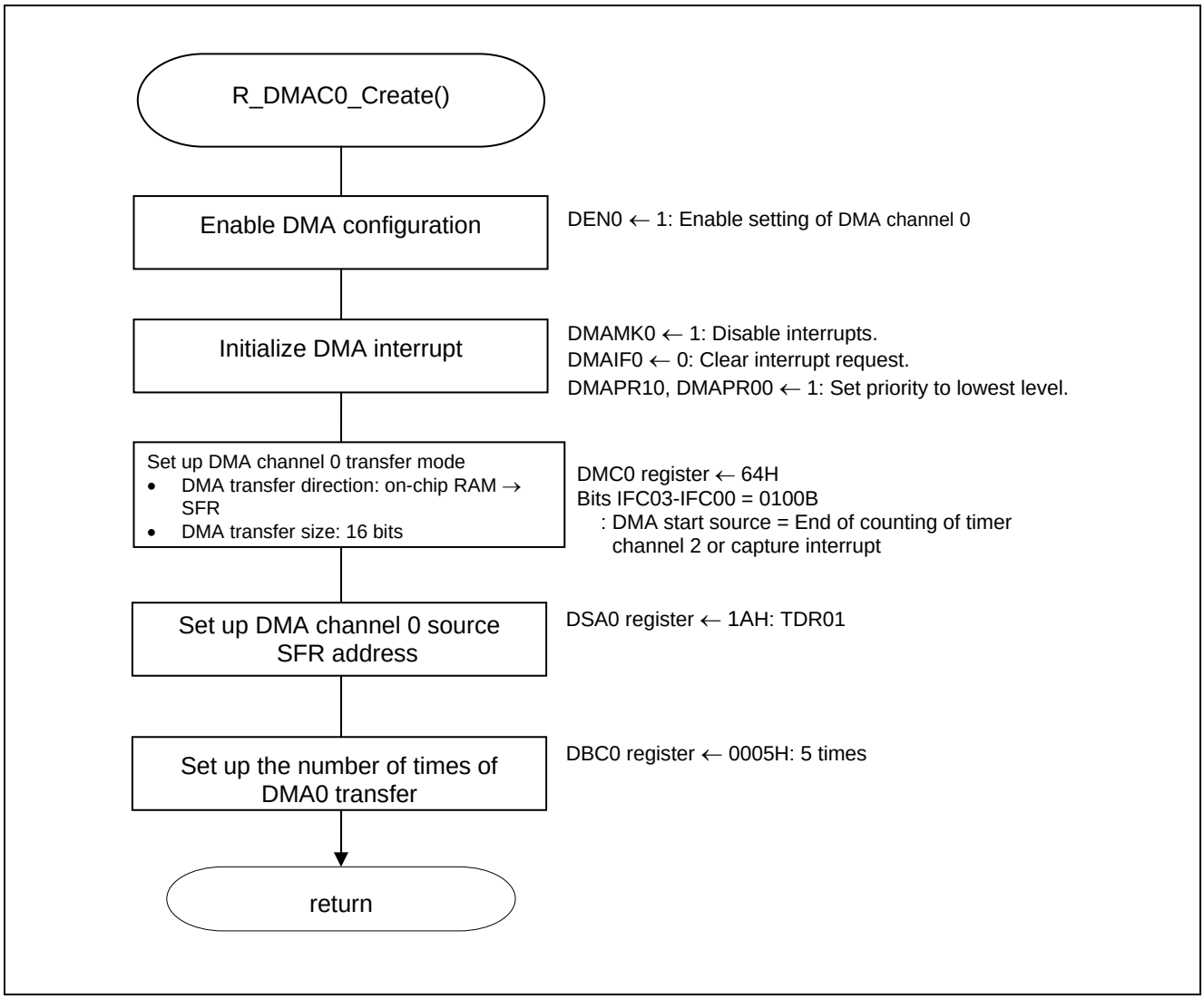


Figure 5.8 Initializing DMA Controller

Disabling DMA channel 0

- DMA operation control register (DRC0)

Symbol: DRC0

7	6	5	4	3	2	1	0
DEN0	0	0	0	0	0	0	DST0
1	0	0	0	0	0	0	**0**

Bit 7

DEN0	DMA operation enable flag
0	**Disables DMA channel 0 (stops operating clock of DMA).** **Disables DMA setup processing.**
1	**Enables DMA channel 0.** **Enables DMA setup processing.**

Bit 0

DST0	DMA transfer mode flag
0	**DMA transfer of DMA channel 0 is completed.**
1	DMA transfer of DMA channel 0 is not completed (still under execution).

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Initialization for DMA transfer end interrupts

- Interrupt request flag register (IF0H)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0H)
  Clear interrupt mask.
- Priority specification flag register (PR00H, PR10H)
  Interrupt level: Level 3 (lowest level)

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
x	x	x	x	**0**	x	x	x

Bit 3

DMAIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01 H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11 H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
x	x	x	x	**1**	x	x	x

Bit 3

DMAMK0	Interrupt processing control
0	Enables interrupt processing.
1	**Disables interrupt processing.**

Symbol: PR00H

7	6	5	4	3	2	1	0
SREPR00 TMPR001 H	SRPR00 CSIPR001 IICPR001	STPR00 CSIPR000 IICPR000	DMAPR01	DMAPR00	SREPR02 TMPR011 H	SRPR02 CSIPR021 IICPR021	STPR02 CSIPR020 IICPR020
x	x	x	x	**1**	x	x	x

Symbol: PR10H

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SREPR10 TMPR101 H	SRPR10 CSIPR101 IICPR101	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12 TMPR111 H	SRPR12 CSIPR121 IICPR121	STPR12 CSIPR120 IICPR120
x	x	x	x	**1**	x	x	x

Bit 3

DMAPR10	DMAPR00	Priority level selection
0	0	Specify level 0 (highest level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (lowest level)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 transfer mode

- DMA mode control register (DMC0)
  Set DMA transfer direction from on-chip RAM to SFR.
  Set transfer data size to 16 bits.
  Specify DMA transfer on DMA start request.
  Select CSI00 transfer end/buffer empty interrupt as DMA start source.

Symbol: DMC0

7	6	5	4	3	2	1	0
STG0	DRS0	DS0	DWAIT0	IFC03	IFC02	IFC01	IFC00
x	**1**	**1**	**0**	**0**	**1**	**0**	**0**

Bit 6

DRS0	Selection of DMA transfer direction
0	SFR to on-chip RAM
1	**On-chip RAM to SFR**

Bit 5

DS0	Specification of transfer data size for DMA transfer
0	8 bits
1	**16 bits**

Bit 4

DWAIT0	Pending of DMA transfer
0	**Executes DMA transfer upon DMA start request (no held pending).**
1	Holds DMA start request pending if any.

Bits 3 to 0

IFC03	IFC02	IFC01	IFC00	Selection of DMA start source	
				Trigger Signal	Description
0	0	0	0	-	Disables DMA transfer by interrupt. (Only software trigger is enabled.)
0	0	0	1	INTAD	A/D conversion end interrupt
0	0	1	0	INTTM00	End of timer channel 0 count end or capture end interrupt
0	0	1	1	INTTM01	End of timer channel 1 count end or capture end interrupt
0	**1**	**0**	**0**	**INTTM02**	**End of timer channel 2 count end or capture end interrupt**
0	1	0	1	INTTM03	End of timer channel 3 count end or capture end interrupt
0	1	1	0	INTST0/INTCSI00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt
0	1	1	1	INTSR0/INTCSI01	UART0 reception transfer end interrupt/CSI01 transfer end or buffer empty interrupt
1	0	0	0	INTST1/INTCSI10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt
1	0	0	1	INTSR1/INTCSI11	UART1 reception transfer end interrupt/CSI11 transfer end or buffer empty interrupt
1	0	1	0	INTST2/INTCSI20	UART2 transmission transfer end or buffer empty interrupt/CSI20 transfer end or buffer empty interrupt
1	0	1	1	INTSR2/INTCSI21	UART2 reception transfer end interrupt/CSI21 transfer end or buffer empty interrupt
Other than above				Setting prohibited	

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up SFR for DMA channel 0 transfer

- DMA SFR address register 0 (DSA0)
  Set SFR for the source of DMA transfer

  Symbol: DSA0

7	6	5	4	3	2	1	0
0	**0**	**0**	**1**	**1**	**0**	**1**	**0**

  Set the lower 8 bits of TDR01 (SFR address: 0xFFF1A).

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 source RAM address

- DMA RAM address register 0 (DRA0)
  Set the RAM address of DMA transfer source.

  Symbol: DRA0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 transfer count

- DMA byte count register 0 (DBC0)
  Specify DMA transfer count.

  Symbol: DBC0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**

  Set the number of times of DMA transfer to 5.

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 Main Processing

Figure 5.9 shows the flowchart for main processing.

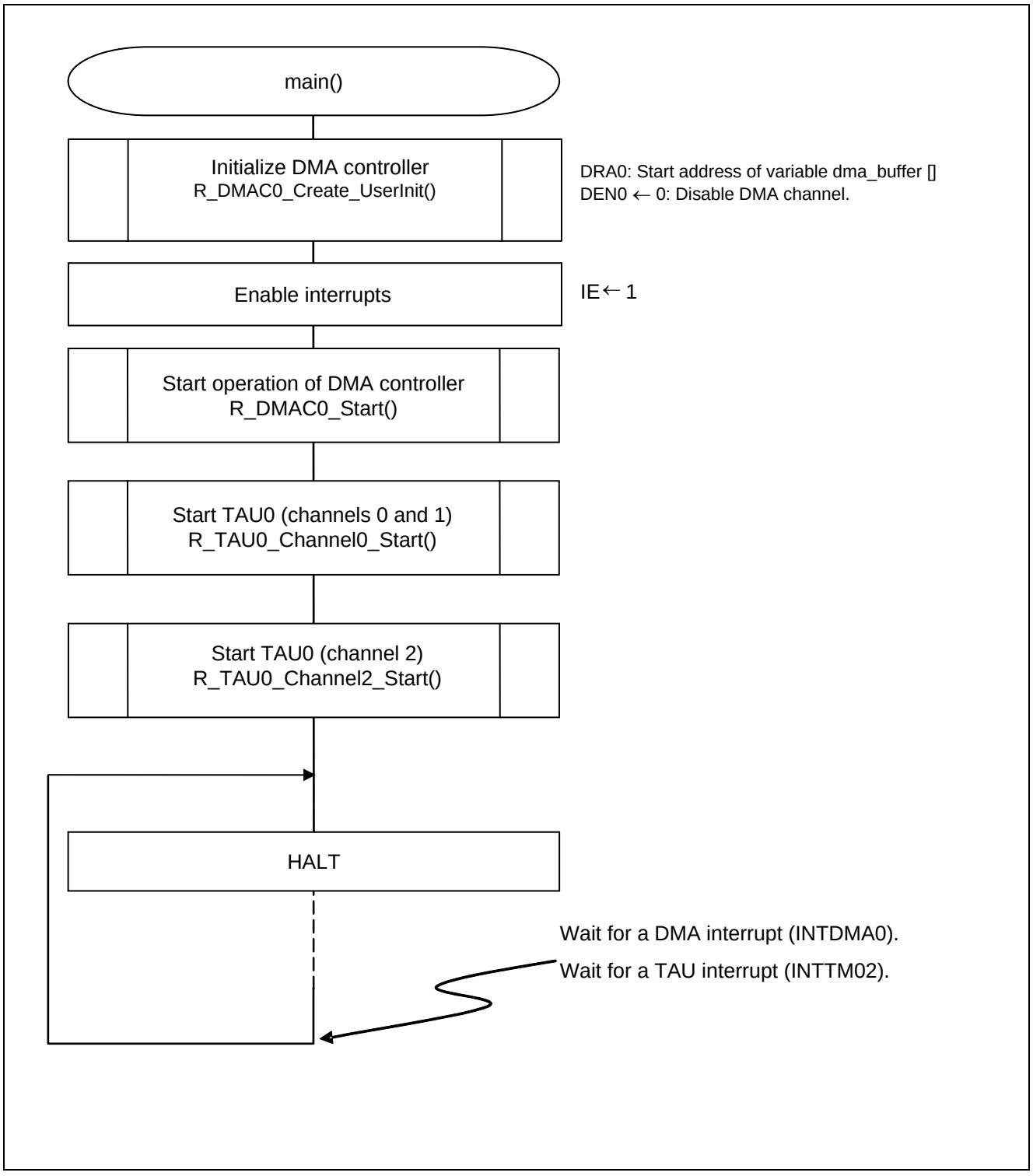


Figure 5.9 Main Processing

5.7.8 DMA Transfer Enable Processing

Figure 5.11 shows the flowchart for the DMA transfer enable processing.

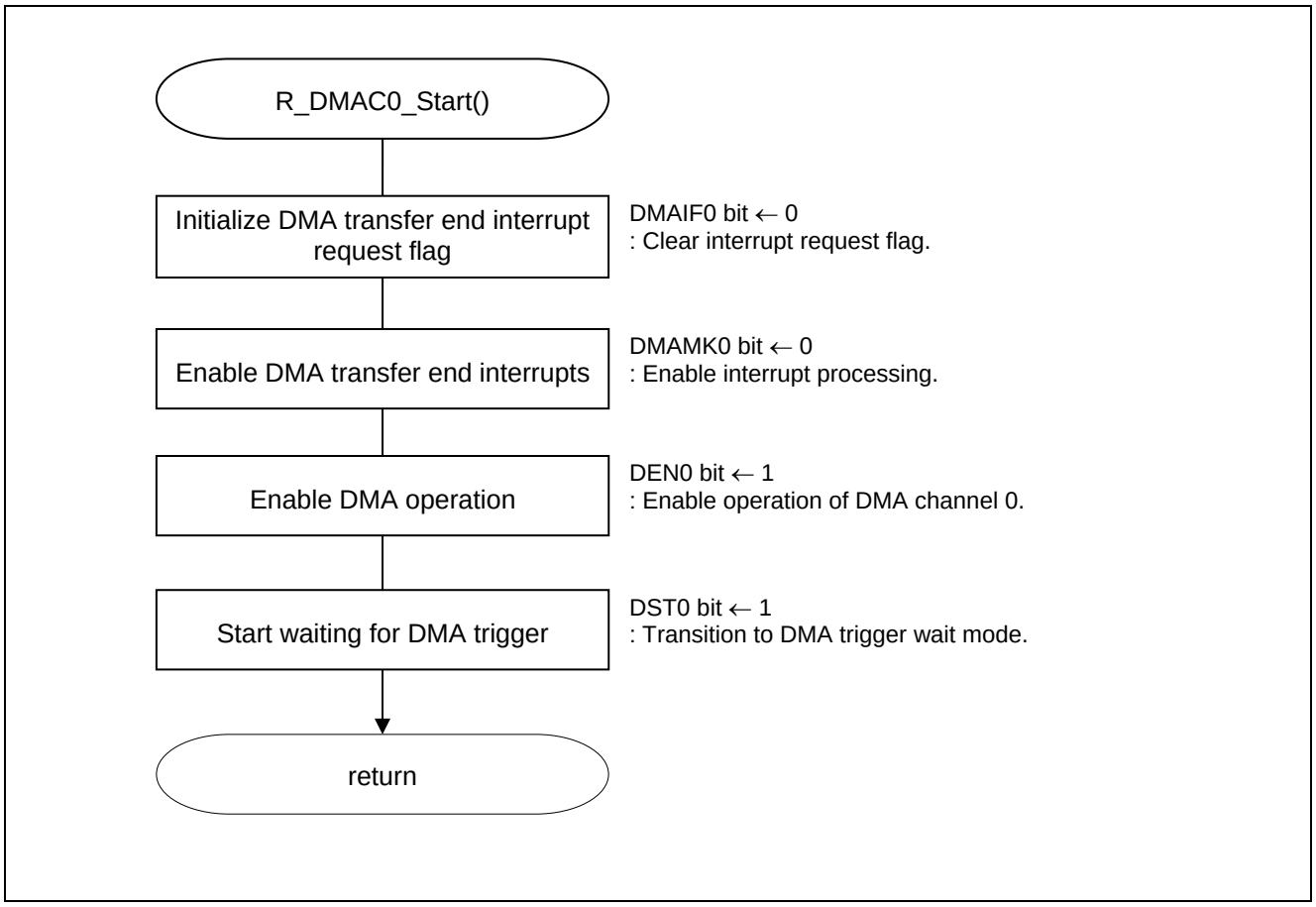


Figure 5.11 DMA Transfer Enable Processing

Preparing for enabling DMA transfer end interrupts

- Interrupt request flag register (IF0H)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0H)
  Clear interrupt mask.

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
x	x	x	x	**0**	x	x	x

Bit 3

DMAIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
x	x	x	x	**0**	x	x	x

Bit 3

DMAMK0	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 operation trigger wait mode

- DMA operation control register (DRC0)

Symbol: DRC0

7	6	5	4	3	2	1	0
DEN0	0	0	0	0	0	0	DST0
1	0	0	0	0	0	0	**1**

Bit 7

DEN0	DMA operation enable flag
0	Disables operation of DMA channel 0 (stops operating clock of DMA). Disables DMA setup processing.
1	**Enables operation of DMA channel 0.** **Enables DMA setup processing.**

Bit 0

DST0	DMA transfer mode flag
0	DMA transfer of DMA channel 0 DMA is completed.
1	**DMA transfer of DMA channel 0 is not completed (still under execution).**

The DMA trigger wait mode is entered by setting DST0 to 1 after enabling DMA operation (DEN0 = 1).

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.9 Starting TAU0 (Channels 0 and 1)

Figure 5.11 shows the flowchart for starting the TAU0 (channels 0 and 1).

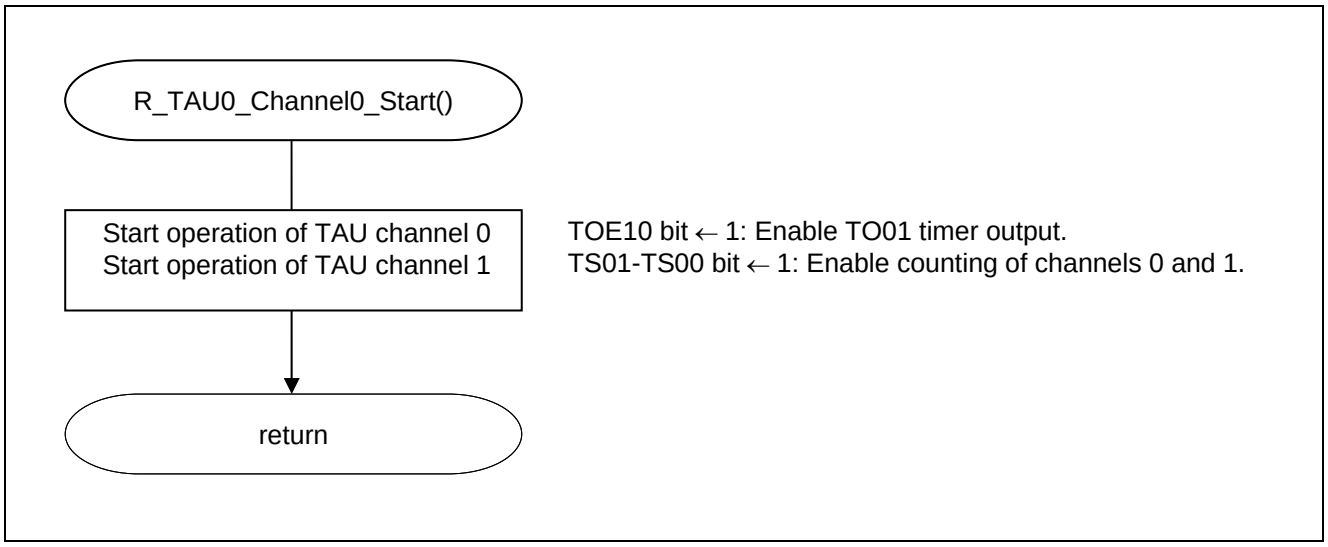


Figure 5.11 Starting TAU0 (Channels 0 and 1)

Caution: For details on the procedure for setting up the TAU0 (R_TAU0_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Timer Array Unit (PWM Output) Application Note (R01AN2589E).

5.7.10 Starting TAU0 (Channel 2)

Figure 5.12 shows the flowchart for starting the TAU0 (channel 2).

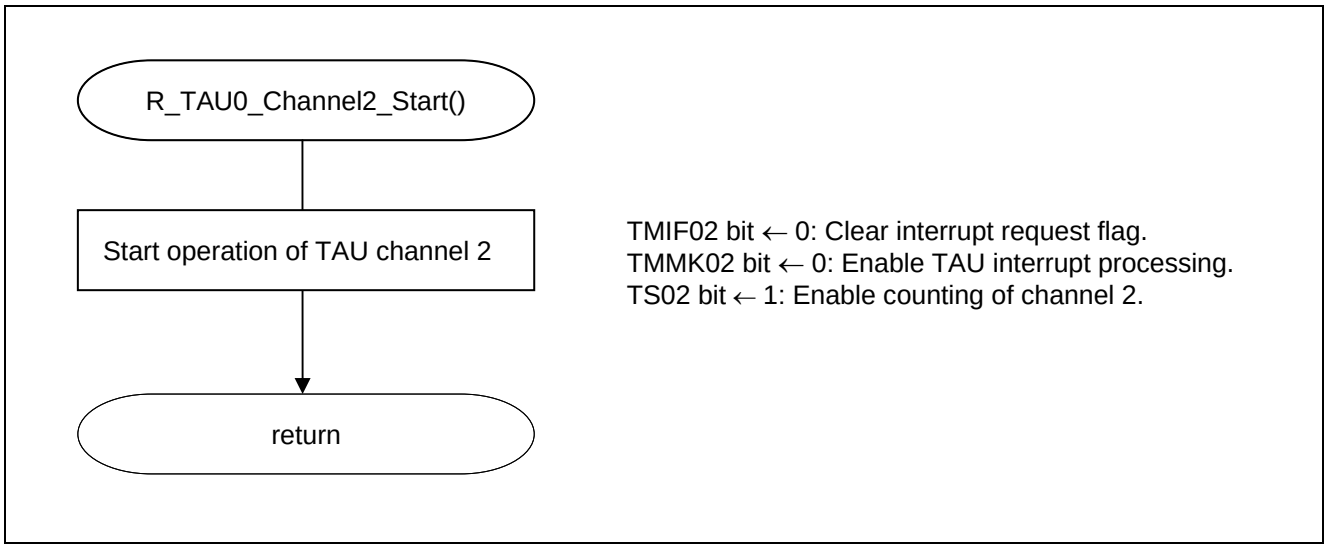


Figure 5.12 Starting TAU0 (Channel 2)

Caution: For details on the procedure for setting up the TAU0 (R_TAU0_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Timer Array Unit (PWM Output) Application Note (R01AN2589E).

5.7.11 TAU0 Timer Interrupt Processing (Channel 2)

Figure 5.13 shows the flowchart for the TAU0 timer interrupt processing (channel 2).

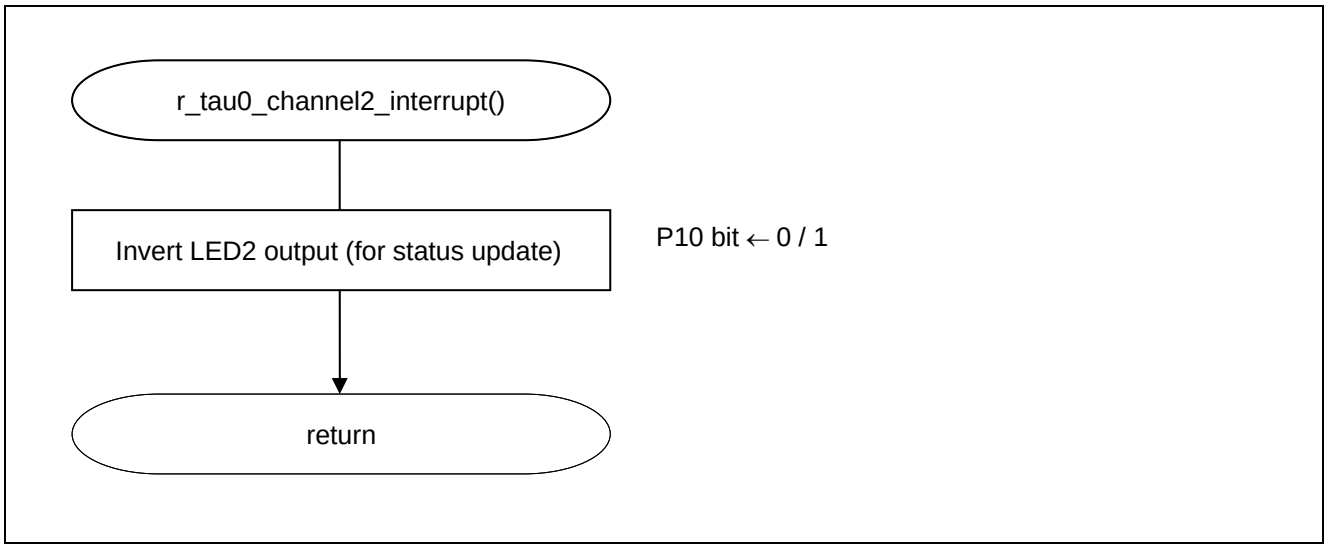


Figure 5.13 TAU0 Timer Interrupt Processing (Channel 2)

5.7.12 DMA Transfer End Interrupt Processing

Figure 5.14 shows the flowchart for the DMA transfer end interrupt processing.

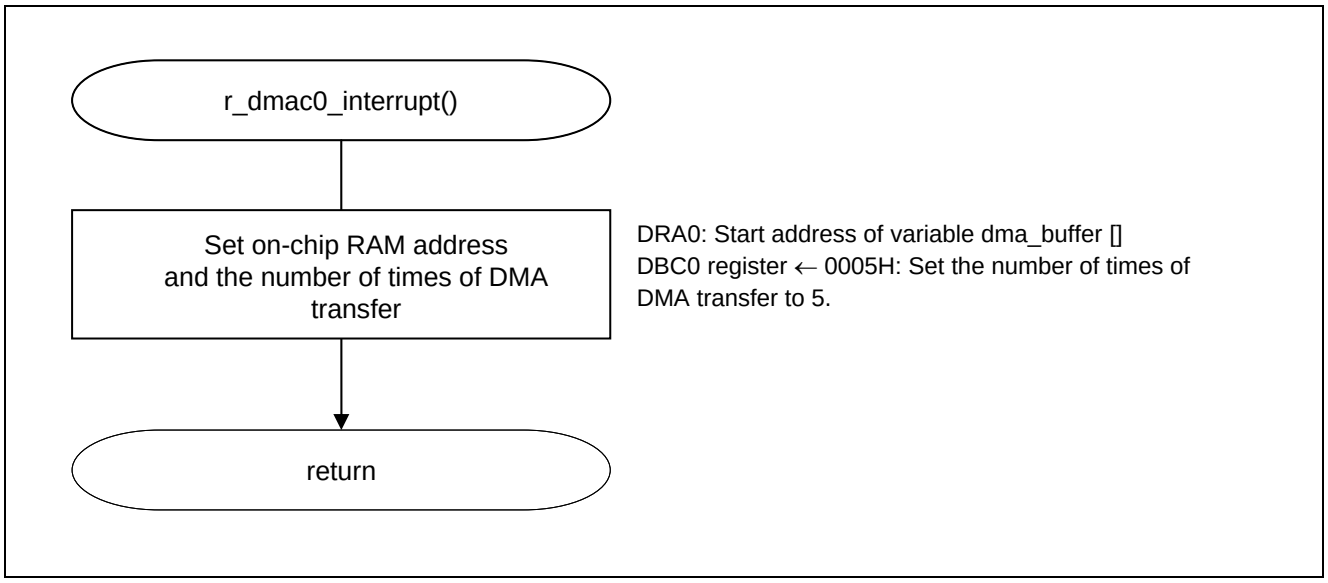


Figure 5.14 DMA Transfer End Interrupt Processing

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

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Revision Record	RL78/G13 DMA Controller (PWM Output)

Rev.	Date	Description	
		Page	Summary
1.00	May 28, 2015	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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