RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: Serial Interface IIC0 to Serial Interface IICA

Introduction

This application note describes how to migrate the serial Interface IIC0 of the 78K0/Kx2 to the serial Interface IICA of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of Serial Interface IIC0 and Serial Interface IICA

Table 1.1 shows the functions of the Serial Interface IIC0, and Table 1.2 shows the functions of the Serial Interface IICA.

Table 1.1 Functions of the Serial Interface IIC0

Function	Explanation
I^2C bus mode (multimaster supported)	This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCL0) line and a serial data bus (SDA0) line. This mode complies with the I^2C bus format and the master device can generated “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I^2C bus.

Note. Do not use serial interface IIC0 and the multiplier/divider simultaneously, because various flags corresponding to interrupt request sources are shared among serial interface IIC0 and the multiplier/divider.

Remarks1. The multiplier/divider is mounted only onto the 78K0/Kx2 microcontroller products whose flash memory is at least 48KB.

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user’s manuals (hardware).

Table 1.2 Functions of the Serial Interface IICA

Function	Explanation
I^2C bus mode (multimaster supported)	This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLAn) line and a serial data bus (SDAAn) line. This mode complies with the I^2C bus format and the master device can generated “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I^2C bus.

Remarks1. For RL78/G13, n: Channel number (n = 0, 1)

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user’s manuals (hardware).

2. Difference between Serial Interface IIC0 and Serial Interface IICA

Table 2.1 and Table 2.2 shows the differences between the IIC0.

Table 2.1 Differences between IIC (1/2)

Item	78K0/Kx2 Serial Interface IIC0	RL78/G13 Serial Interface IICAn
Communication operation	- Master operation in single master system - Master operation in multimaster system - Slave operation	- Master operation in single master system - Master operation in multimaster system - Slave operation
Byte format	8 bits, MSB first	8 bits, MSB first
Slave address	7 bits, 10 bits	7 bits, 10 bits
Extension code	When the higher 4 bits of the receive address are either “0000” or “1111”, the extension code reception flag (EXC0) is set to 1 for extension code reception and an interrupt request (INTIIC0) is issued at the falling edge of the eighth clock.	When the higher 4 bits of the receive address are either “0000” or “1111”, the extension code reception flag (EXCn) is set to 1 for extension code reception and an interrupt request (INTIICAn) is issued at the falling edge of the eighth clock.
Function	- Start condition - Stop condition - Acknowledge - Synchronization / Arbitration - Clock stretch - Software reset (manual) - START byte (manual) - Exit from communication	- Start condition - Stop condition - Acknowledge - Synchronization / Arbitration - Clock stretch - Software reset (manual) - START byte (manual) - Exit from communication
Fastest transfer rate	- Standard mode: 100kbps - Fast mode: 400kbps	- Standard mode: 100 kbps - Fast mode: 400 kbps - Fast-mode Plus: 1 Mbps
Transfer clock for I^2C bus (Note1)	$f_{SCL} = 1/ (m \times T + t_R + t_F)$	$f_{SCL} = f_{MCK} / \{IICWL + IICWH + f_{MCK} (t_R + t_F)\}$
Selection Clock Setting	- Normal mode: f_W = 2.00MHz to 8.38MHz - High-speed mode: f_W = 4.00MHz to 8.38MHz - If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{XH}): f_W = 3.8MHz to 4.2MHz	- Standard mode (Note2) $f_{CLK} \geq$ 1MHz - Fast mode (Note2) $f_{CLK} \geq$ 3.5MHz - Fast mode plus (Note2) $f_{CLK} \geq$ 10MHz

Note1. For 78K0/Kx2,
T = 1/fw, m = 12, 18, 24, 44, 66, 86, t_R: SCL0 rise time, t_F: SCL0 fall time

For details, refer to the appropriate user’s manuals (hardware).

For RL78/G13
f_{MCK}: IICA operation clock frequency,
t_R: SDAAn and SCLAn signal rising times, t_F: SDAAn and SCLAn signal falling times
IICWL, IICWH:
Settings depend on whtether the mode used is Standard-mode, Fast-mode, or Fast-mode Plus.

For details, refer to the appropriate user’s manuals (hardware).

Note2. The fastest operation frequency of the IICA operation clock (f_{MCK}) is 20MHz (max.).
Set bit 0 (PRSn) of the IICA control register n1 (IICCTLn1) to "1" only when the f_{CLK} exceeds 20 MHz.

Remarks1. For RL78/G13, n: Channel number (n = 0,1)

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user’s manuals (hardware).

Table 2.2 Differences between IIC (2/2)

Item	78K0/Kx2 Serial Interface IIC0	RL78/G13 Serial Interface IICAn
Status flag	- Master status check - Detection of arbitration loss - Detection of extension code reception - Detection of matching addresses - Detection of transmit/receive status - Detection of acknowledge - Detection of start condition - Detection of stop condition - I^2C bus status flag	- Master status check - Detection of arbitration loss - Detection of extension code reception - Detection of matching addresses - Detection of transmit/receive status - Detection of acknowledge - Detection of start condition - Detection of stop condition - I^2C bus status flag
Stop operation	IICC0 register Set IICE0 bit to 0	IICCTLn0 register Set IICEn bit to 0
Enable operation	IICC0 register Set IICE0 bit to 1	IICCTLn0 register Set IICEn bit to 1
Start condition trigger	IICC0 register Set STT0 bit to 1	IICCTLn0 register Set STTn bit to 1
Stop condition trigger	IICC0 register Set SPT0 bit to 1	IICCTLn0 register Set SPTn bit to 1
Start transmission operation	- Master transmission Write data to IIC0 register only after a start condition is generated in bus-released status (IICBSY0 = 0) or master communication status (MSTS0 = 1). - Slave transmission Write data to IICC0 register in transmission status (TRC0 = 1). For 2nd and the following byte transmission, write data only after acknowledge detection (ACKD0 = 1).	- Master transmission Write data to IIC0 register only after a start condition is generated in bus-released status (IICBSYn = 0) or master communication status (MSTSn = 1). - Slave transmission Write data to IICC0 register in transmission status (TRCn = 1). For 2nd and the following byte transmission, write data only after acknowledge detection (ACKDn = 1).
Start reception operation	Release the wait status (WREL0 = 1) to receive data. After receiving data, read the value from IIC0 register.	Release the wait status (WRELn = 1) to receive data. After receiving data, read the value from IIC0 register.
Interrupt occur timing	- Falling edge of eighth or ninth clock of the serial clock (set by WTIM0 bit) (Note) - Interrupt request generated when a stop condition is detected (set by SPIE0 bit)	- Falling edge of eighth or ninth clock of the serial clock (set by the WTIMn bit) (Note) - Interrupt request generated when a stop condition is detected (set by the SPIEn bit)
Communication reservation	IICF0 register Set IICRSV0 bit to 0	IICFn register Set IICRSVn bit to 0
Wake up in STOP mode	Operable only when the external clock from EXSCL0 pin is selected as the serial clock	IICCTLn1 register Set WUPn bit to 1
Clock pin	SCL0 pin	SCLAn pin
transmission / reception pin	SDA0 pin	SDAAn pin

Note. When slave operation, the received address does not match the contents of the slave address register and extension code is not received, neither interrupt nor a wait occurs.

Remarks1. For RL78/G13, n: Channel number (n = 0, 1)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

3. Comparison between Registers

Table 3.1 and Table 3.2 compares the registers for the 78K0/Kx2 Serial interface IIC0 and the registers for the RL78/G13 Serial interface IICAn.

Table 3.1 Comparison between Registers (1/2)

Item	78K0/Kx2	RL78/G13
Clock supply to serial interface IICAn	None	PER0 register IICAnEN bit
IIC shift register	IIC0 register	IICAn register
Slave address register	SVA0 register	SVAn register
I^2C operation enable	IICC0 register IICE0 bit	IICCTLn0 register IICEn bit
Exit from communications	IICC0 register LREL0 bit	IICCTLn0 register LRELn bit
Wait cancellation	IICC0 register WREL0 bit	IICCTLn0 register WRELn bit
Enable/disable generation of interrupt request when stop condition is detected	IICC0 register SPIE0 bit	IICCTLn0 register SPIEn bit
Control of wait and interrupt request generation	IICC0 register WTIM0 bit	IICCTLn0 register WTIMn bit
Acknowledgment control (Note)	IICC0 register ACKE0 bit	IICCTLn0 register ACKEn bit
Start condition trigger	IICC0 register STT0 bit	IICCTLn0 register STTn bit
Stop condition trigger	IICC0 register SPT0 bit	IICCTLn0 register SPTn bit
Master device status	IICS0 register MSTS0 bit	IICSn register MSTSn bit
Detection of arbitration loss	IICS0 register ALD0 bit	IICSn register ALDn bit
Detection of extension code reception	IICS0 register EXC0 bit	IICSn register EXCn bit
Detection of matching addresses	IICS0 register COI0 bit	IICSn register COIn bit
Detection of transmit/receive status	IICS0 register TRC0 bit	IICSn register TRCn bit
Detection of acknowledge	IICS0 register ACKD0 bit	IICSn register ACKDn bit
Detection of start condition	IICS0 register STD0 bit	IICSn register STDn bit
Detection of stop condition	IICS0 register SPD0 bit	IICSn register SPDn bit

Note. When the device serves as a slave and the addresses match, an acknowledge is generated regardless of the set value.

Remarks1. For RL78/G13, n: Channel number (n = 0, 1)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 3.2 Comparison between Registers (2/2)

Item	78K0/Kx2	RL78/G13
STT0 clear flag	IICF0 register STCF bit	IICFn register STCFn bit
I^2C bus status flag	IICF0 register IICBSY bit	IICFn register IICBSYn bit
Initial start enable trigger	IICF0 register STCEN bit	IICFn register STCENn bit
Communication reservation function disable bit	IICF0 register IICRSV bit	IICFn register IICRSVn bit
Operation of address match wakeup function in STOP mode	None	IICCTLn1 register WUPn bit
Detection of SCL0 pin level	IICCL0 register CLD0 bit	IICCTLn1 register CLDn bit
Detection of SDA0 pin level	IICCL0 register DAD0 bit	IICCTLn1 register DADn bit
Operation mode switching	IICCL0 register SMC0 bit	IICCTLn1 register SMCn bit
Digital filter operation control	IICCL0 register DFC0 bit	IICCTLn1 register DFCn bit
IIC operation clock selection	IICCL0 register CL00 bit, CL01 bit IICX0 register CLX0 bit	IICCTLn1 register PRSn bit
IICA low-level width setting register	None	IICWLn register
IICA high-level width setting register	None	IICWHn register

Remarks1. For RL78/G13, n: Channel number (n = 0, 1)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

4. Sample Code for Serial Interface IICA

The sample code for Serial Interface IICA is explained in the following application notes.

- RL78/G13 Serial Interface IICA (for Master Transmission/Reception) CC-RL (R01AN2759)
- RL78/G13 Serial Interface IICA (for Slave Transmission/Reception) CC-RL (R01AN2760)

5. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Data	Description	
		Page	Summary
1.00	Nov.11, 2019	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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