RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: Serial interfaces CSI10 and CSI11 to Serial Array Unit

Introduction

This application note describes how to migrate the Serial interfaces CSI10 and CSI11 of the 78K0/Kx2 to the serial array unit (SAU) of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of Serial interfaces CSI10 and CSI11 and Serial array unit

Table 1.1 shows the functions of the Serial interfaces CSI10 and CSI11, and Table 1.2 shows the functions of the serial array unit (SAU).

Table 1.1 Functions of Serial interfaces CSI10 and CSI11

Function	Explanation
3-wire serial I/O mode	Clock synchronous communication function by 3 lines of serial clock (SCK1n) and serial data (SI1n, SO1n).

Table 1.2 Functions of Serial Array Unit

Function	Explanation
3-wire serial I/O	This is a clocked communication function that uses three lines: serial clock (SCK) and serial data (SI and SO) lines.
UART	This is a start-stop synchronization function using two lines: serial data transmission (TXD) and serial data reception (RXD) lines.
Simplified I^2C (only master function with a single master)	This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA).
LIN Communication (Note)	LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol designed to reduce the cost of an automobile network.

Note. The LIN-bus is accepted in UART2 (channels 0 and 1 of unit 1)

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Each of the serial interfaces CSI10 and CSI11 of the 78K0/Kx2 incorporates one channel of 3-line serial I/O (CSI). Figure 1.1 shows a block diagram of the serial interfaces CSI10 and CSI11.

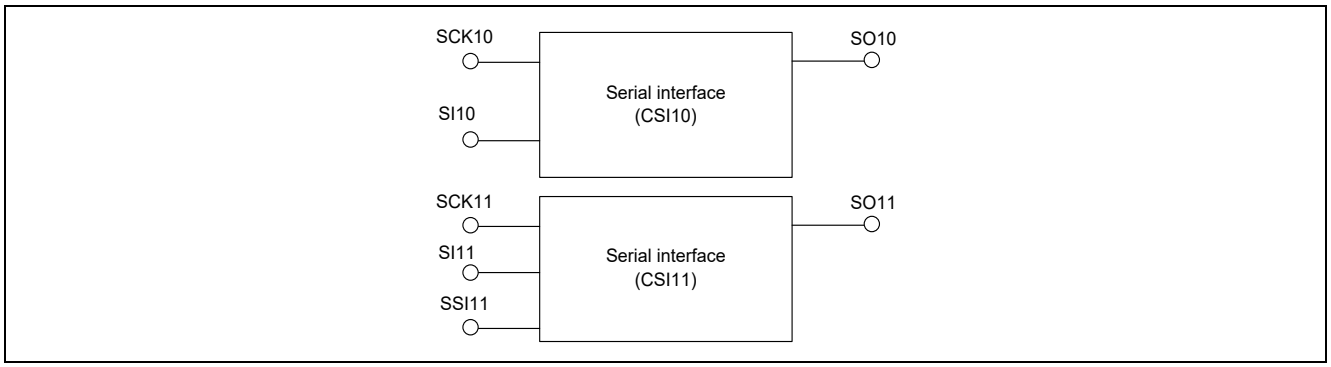

Figure 1.1 Block Diagram of Serial interfaces CSI10 and CSI11

A single serial array unit (SAU) in the RL78/G13 has up to four serial channels. Each channel can achieve 3-wire serial (CSI), UART, and simplified I^{2}C communication.

Figure 1.2 shows a CSI block diagram of the serial array unit 0 (SAU0) of the RL78/G13.

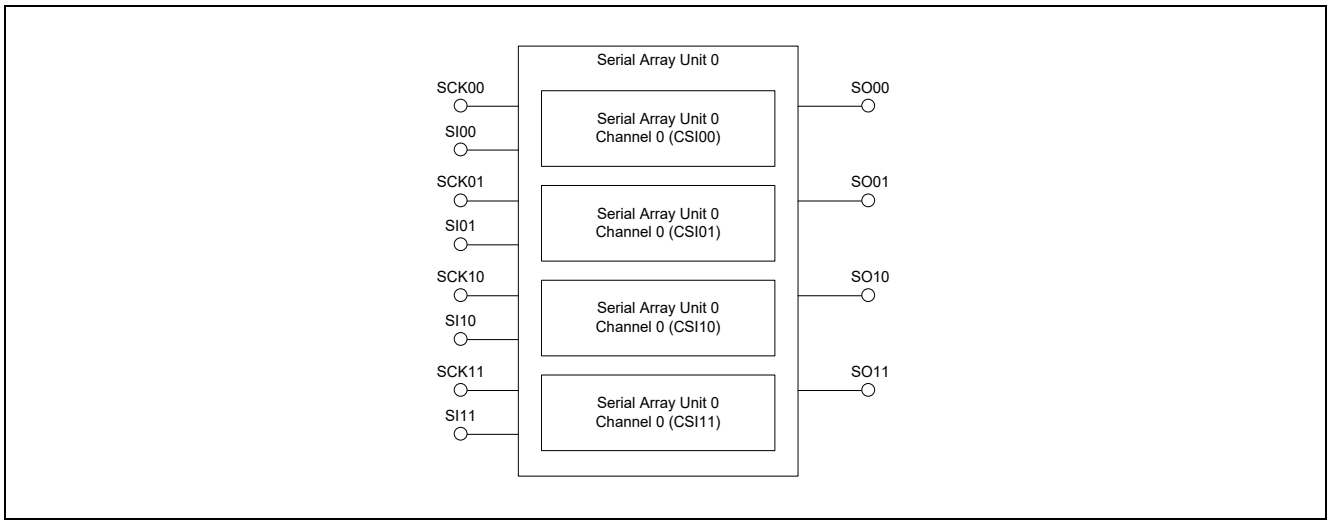

Figure 1.2 Block Diagram of Serial Array Unit 0 (SAU0) CSI

Table 1.3 shows the SAU functions corresponding to the Serial interfaces CSI10 and CSI11.

Table 1.3 Correspondence between Functions

78K0/Kx2 Serial interfaces CSI10 and CSI11	RL78/G13 Serial Array Unit (SAU)
3-wire serial I/O mode	3-wire serial I/O
-	UART
-	Simplified I^{2}C

The 3-wire serial I/O mode of the Serial interfaces CSI10 and CSI11 correspond to the 3-wire serial I/O of the SAU.

2. Difference between Serial interfaces CSI10 and CSI11 and Serial Array Unit

Table 2.1 and Table 2.2 shows the differences between the 3-wire serial I/O mode.

Table 2.1 Differences between 3-wire serial I/O mode (1/2)

Item	78K0/Kx2 Serial interfaces CSI10, CSI11	RL78/G13 Serial Array Unit (SAU) CSImn
Transfer data length	8 bits	7 bits / 8 bits
Maximum transfer rate	- During master communication 6.25 MHz (Note1) - During slave communication 2.5 MHz	- During master communication 16 MHz (CSI00 only) (Note2), 8 MHz (CSImn) (Note3) - During slave communication 4 MHz
First bit specification	CSIM1n register DIR1n = 0: MSB first DIR1n = 1: LSB first	SCRmn register DIRmn = 0: MSB first DIRmn = 1: LSB first
Selection of data and clock phase	CSIC1n register Combination of CKP1n and DAP1n bits	SCRmn register Combination of CKPmn and DAPmn bits
Disables operation	CSIM1n register CSIE1n = 0	STm register STmn = 1
Enables operation	CSIM1n register CSIE1n = 1	SSm register SSmn = 1
Setting of operation mode	CSIM1n register TRMD1n bit = 1: Transmit/receive mode TRMD1n bit = 0: Receive mode	SCRmn register TXEmn = 1, RXEmn = 1: Transmission/reception TXEmn = 1, RXEmn = 0: Transmission only TXEmn = 0, RXEmn = 1: Reception only
Transmit buffer register	SOTB1n register	Lower 8 bits of SDRmn register (SIOp)
Receive data register	SIO1n register	Lower 8 bits of SDRmn register (SIOp)
Data transmission is started (Master mode)	Write transmit data to SOTB1n register (When TRMD1n = 1)	Write transmit data to SIOp register (When TXEmn = 1)
Data reception is started (Master mode)	- Write transmit data to SOTB1n register (When TRMD1n = 1) - Read reception data from SIO1n register. (When TRMD1n = 0)	- Write transmit data to SIOp register (When TXEmn = 1, RXEmn = 1) - Write FFH as dummy data to SDRmn register (When TXEmn = 0, RXEmn = 1)

Note1. (A) and (A2) Grade Products are 5MHz.

Note2. Target products G (Industrial applications) is 4MHz.

Note3. Target products G (Industrial applications) is 2MHz.

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 2.2 Differences between 3-wire serial I/O mode (2/2)

Item	78K0/Kx2 Serial interfaces CSI10, CSI11	RL78/G13 Serial Array Unit (SAU) CSImn
Interrupt	Transmission completion interrupt	SMRmn register MDmn0 = 0: Transfer end interrupt MDmn0 = 1: Buffer empty interrupt
Interrupt occur timing	After transfer of transmit/receive data is completed.	- MDmn0 = 0 After transfer of transmit/receive data is completed. - MDmn0 = 1 When data is transferred from the SDRmn register to the shift register.
Communication status flag	CSIM1n register CSOT1n = 0: Communication is stopped. CSOT1n = 1: Communication is in progress.	SSRmn register TSFmn = 0: Communication is stopped or suspended. TSFmn = 1: Communication is in progress.
Buffer register status indication flag	None	SSRmn register BFFmn = 0: Valid data is not stored in the SDRmn register. BFFmn = 1: Valid data is stored in the SDRmn register.
Overrun error detection flag	None	SSRmn register OVFmn = 0: No error occurs. OVFmn = 1: An error occurs.
Serial clock I/O pin	SCK1n pin	SCKmn pin
Serial data input pin	SI1n pin	SImn pin
Serial data output pin	SO1n pin	SOmn pin
Serial interface chip select input pin	SSI11 pin (CSI11 only)	None (Substituted by port manipulation)

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

3. Comparison between Registers

Table 3.1 and Table 3.2 compares the registers for the 78K0/Kx2 Serial interfaces CSI10 and CSI11 and the registers for the RL78/G13 Serial Array Unit used as CSImn.

Table 3.1 Comparison between Registers (1/2)

Item	78K0/Kx2	RL78/G13
Clock supply to serial array unit	None	PER0 register SAUmEN bit
Disables operation	CSIM1n register CSIE1n bit	STm register STmn bit
Enables operation	CSIM1n register CSIE1n bit	SSm register SSmn bit
Mode control Selection	CSIM1n register TRMD1n bit	SCRmn register TXEmn bit, RXEmn bit
First bit specification	CSIM1n register DIR1n bit	SCRmn register DIRmn bit
Communication status flag	CSIM1n register CSOT1n bit	SSRmn register TSFmn bit
SSI11 pin use selection	CSIM11 register SSE11 bit	None
Selection of clock phase	CSIC1n register CKP1n bit	SCRmn register CKPmn bit
Selection of data phase	CSIC1n register DAP1n bit	SCRmn register DAPmn bit
Serial clock selection	CSIC1n register CKS1n2 - CKS1n0 bits	SMRmn register CKSmn bit, CCSmn bit SPSm register PRSmk3 - PRSmk0 bits Upper 7 bits of SDRmn register
Transmit buffer register	SOTB1n register	Lower 8 bits of SDRmn register
Receive register	SIO1n register	Lower 8 bits of SDRmn register
Start trigger selection	None	SMRmn register Set STSmn bit to 0
Controls inversion of level of receive data of channel n in UART mode	None	SMRmn register Set SISmn bit to 0
Setting of operation mode of channel n	None	SMRmn register Set MDmn2 bit to 0, MDmn1 bit to 0
Selection of interrupt source of channel n	None	SMRmn register MDmn0 bit
Mask control of error interrupt signal	None	SCRmn register EOCmn bit

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 3.2 Comparison between Registers (2/2)

Item	78K0/Kx2	RL78/G13
Setting of parity bit in UART mode	None	SCRmn register Set PTCmn1 bit to 0, PTCmn0 bit to 0
Setting of stop bit in UART mode	None	SCRmn register Set SLCmn1 bit to 0, SLCmn0 bit to 0
Setting of data length in CSI and UART modes	None	SCRmn register DLSmn1 bit, DLSmn0 bit
Clear trigger of framing error flag	None	SIRmn register FECTmn (not used)
Clear trigger of parity error flag	None	SIRmn register PECTmn (not used)
Clear trigger of overrun error flag	None	SIRmn register OVCTmn bit
Buffer register status indication flag	None	SSRmn register BFFmn bit
Framing error detection flag	None	SSRmn register FEFmn (not used)
Parity/ACK error detection flag	None	SSRmn register PEFmn (not used)
Overrun error detection flag	None	SSRmn register OVFmn bit
Indication of operation enable/stop status	None	SEm register SEmn bit
Serial output enable/stop	None	SOEm register SOEmn bit
Clock output value setting when operation is disabled	None	SOm register CKOmn bit
Data output value setting when operation is disabled	None	SOm register SOmn bit
Selects inversion of the level of the transmit data	None	SOLm register Set SOLmn bit to 0
Selection of whether to enable or disable the generation of communication error interrupts in the SNOOZE mode	None	SSCm register SSECm bit
Setting of the SNOOZE mode	None	SSCm register SWCm bit
Switching channel 7 input of timer array unit	None	ISC register Set ISC1 bit to 0
Switching external interrupt (INTP0) input	None	ISC register Set ISC0 bit to 0
Use of noise filter	None	NFEN0 register Set SNFENn0 bit to 0

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

4. Sample Code for Serial Array Unit

The sample code for Serial Array Unit is explained in the following application notes.

- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception) CC-RL (R01AN2547)
- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Slave Transmission/Reception) CC-RL (R01AN2711)
- RL78/G13 Low-power Consumption Operation (CSI in SNOOZE Mode) CC-RL (R01AN2762)

5. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Data	Description	
		Page	Summary
1.00	Jul.05, 2019	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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