RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: Power-on-Clear Circuit, Low-Voltage Detector

Introduction

This application note describes how to migrate the Power-on-Clear Circuit, Low-Voltage Detector of the 78K0/Kx2 to Power-on-reset Circuit, Voltage Detector of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences in Function Overview

1.1 Difference between Power-on-Clear Circuit and Power-on-reset Circuit

Table 1.1 overviews the differences between the functions of the Power-on-Clear Circuit (POC) of the 78K0/Kx2 and the Power-on-reset Circuit (POR) of the RL78/G13.

Table 1.1 Differences between Functions（Power-on-Clear Circuit and Power-on-reset Circuit）

Item	78K0/Kx2 Power-on-Clear Circuit (POC)	RL78/G13 Power-on-reset Circuit (POR)
Operation Mode	- 1.59V POC mode - 2.7V/1.59 V POC mode	1.51V/1.50V POR mode only
Detection voltage	- V_{POC} = 1.59 V (1.44V to 1.74V) - V_{VDDPOC} = 2.70 V (2.50V to 2.90V)	When power supply voltage is rising: V_{POR} = 1.51V (1.45V to 1.57V) When power supply voltage is falling: V_{PDR} = 1.50V (1.44V to 1.56V)
Minimum pulse width	MIN. 200 us	MIN. 300 us
Power supply voltage rising slope	MIN. 0.5V/ms (Note1)	MAX. 54 V/ms
Supply Voltage Rise Time	- When RESET input is not used: MAX. 3.6ms (V_{DD}:0V to 1.8V (Note2)) - When RESET input is used: MAX. 1.9ms (Releasing RESET input to V_{DD}: 1.8V (Note2))	None (Note3)

Note1. With the standard and (A) grade products, if the voltage rises to 1.8 V at a rate slower than 0.5 V/ms (MIN.) on power application, input a low level to the RESET pin after power application and before the voltage reaches 1.8 V, or set the 2.7 V/1.59 V POC mode by using an option byte (POCMODE = 1). With the (A2) grade products, if the voltage rises to 2.7 V at a rate slower than 0.75 V/ms (MIN.) on power application, input a low level to the RESET pin after power application and before the voltage reaches 2.7 V.

Note2. For the (A2) grade products, replace 1.8 V by 2.7 V.

Note3. Keep the reset state by using the external reset or voltage detector (LVD) until the power supply voltage (V_{DD}) rises to the operating voltage range specified by the electric characteristics.

With the RL78/G13, set the flash operation mode by using an option byte according to the main system clock frequency (f_{MAIN}) and the power supply voltage (V_{DD}) used.

Table 1.2 shows the RL78/G13 flash operation mode setting.

Table 1.2 RL78/G13 Setting of flash operation mode

Operation mode	Operating Frequency Range (f_{MAIN})	Operating Voltage Range (V_{DD})
LV (low voltage main) mode	1 MHz to 4 MHz	1.6 V to 5.5 V
LS (low speed main) mode	1 MHz to 8 MHz	1.8 V to 5.5 V
HS (high speed main) mode	1 MHz to 16 MHz	2.4 V to 5.5 V
	1 MHz to 32 MHz	2.7 V to 5.5 V

1.2 Difference between Low-Voltage Detector and Voltage Detector

Table 1.3 overviews the differences between the functions of the Low-Voltage Detector (LVI) of the 78K0/Kx2 and the Voltage Detector (LVD) of the RL78/G13.

Table 1.3 Differences between Functions (Low-Voltage Detector and Voltage Detector)

Item	78K0/Kx2 Low-Voltage Detector (LVI)	RL78/G13 Voltage Detector (LVD)
Target of detection	Supply voltage (V_{DD}) or Input voltage from an external input pin (EXLVI)	Supply voltage (V_{DD})
Detection levels	16 levels (Note)	14 levels
Minimum pulse width	MIN. 200 us	MIN. 300 us
Operation mode select	- Interrupt - Reset	- Interrupt mode - Reset mode - Interrupt & reset mode
Setting of detection voltage	Set the appropriate value to the LVIS register by using the software.	Set the appropriate value to the option byte in the code flash area. In interrupt and reset mode, set the voltage detection operation mode and detection level to the LVIS register by using software.

Note. (A2) grade products: 10 levels

2. Register Compatibilities

2.1 Option Byte Comparison between Power-on Clear Circuit and Power-on Reset Circuit

Table 2.1 compares the option byte of the 78K0/Kx2 power-on clear circuit (POC) and that of the RL78/G13 power-on reset circuit (POR).

Table 2.1 Option Byte Comparison between Power-on Clear Circuit and Power-on Reset Circuit

Item	78K0/Kx2 Power-on-Clear Circuit (POC)	RL78/G13 Power-on-reset Circuit (POR)
POC mode selection	Address: 0081H / 1081H (Note1) POCMODE (Note2)	None

Note1. Only when using the boot swap function.

Note2. POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming.

2.2 Register Comparison between Low-Voltage Detector and Voltage Detector

Table 2.2 compares the registers of the 78K0/Kx2 low-voltage detector (LVI) and those of the RL78/G13 voltage detector (LVD).

Table 2.2 Register Comparison between Low-Voltage Detector and Voltage Detector

Item	78K0/Kx2 Low-Voltage Detector (LVI)	RL78/G13 Voltage Detector (LVD)
Enables or disables operation	LVIM register LVION bit	Address: 000C1H / 010C1H (Note1) VPOC2 bit, LVIMDS0 bit
Voltage detection selection	LVIM register LVISEL bit	None
Select operation mode	LVIM register LVIMD bit	Address: 000C1H / 010C1H (Note1) LVIMDS1 bit, LVIMDS0 bit
Voltage detection flag	LVIM register LVIF bit	LVIM register LVIF bit
Select voltage detection level	LVIS register	Address: 000C1H / 010C1H (Note2) VPOC1, VPOC0 bit, LVIS1 bit, LVIS0 bit
Enable or disable rewriting the voltage detection level register (LVIS)	None	LVIM register LVISEN bit
Mask status flag of LVD output	None	LVIM register LVIOMSK bit
Operation mode of voltage detection	None	LVIS register LVIMD bit (Note3)
LVD detection level	None	LVIS register LVILV bit

Note1. If the corresponding register is the option byte, the address of the option byte is shown.

Note2. Only when using the boot swap function.

Note3. Writing “0” can only be allowed in the interrupt & reset mode. Do not set in other cases.

3. Sample Code for Voltage Detector

The sample code for the Voltage Detector is explained in the following application notes.

・RL78/G13 Voltage Detector (Reset Mode) CC-RL (R01AN2834)

4. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 28, 2019.	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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