RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: Interrupt Functions

Introduction

This application note describes how to migrate the Interrupt Functions of the 78K0/Kx2 to the Interrupt Functions of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. 78K0/Kx2 and RL78/G13 interrupt functions 3

2. Difference between Interrupt functions 4

3. Comparison between Registers 5

4. Comparison between Interrupt Priorities....6

5. Sample Code for Interrupt Function....11

6. Documents for Reference 11

Revision History....12

1. 78K0/Kx2 and RL78/G13 interrupt functions

Table 1.1 shows the Interrupt functions in the 78K0/Kx2, and Table 1.2 shows the Interrupt functions in the RL78/G13.

Table 1.1 78K0/Kx2 interrupt functions

Function	Explanation
Maskable interrupts	These interrupts undergo mask control. Maskable interrupts can be divided into a high interrupt priority group and a low interrupt priority group by setting the priority specification flag registers. Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the priority of vectored interrupt servicing. A standby release signal is generated and STOP and HALT modes are released.
Software interrupt	This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

Table 1.2 RL78/G13 interrupt functions

Function	Explanation
Maskable interrupts	These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers. Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the default priority of vectored interrupt servicing. A standby release signal is generated and STOP, HALT, and SNOOZE modes are released.
Software interrupt	This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

Table 1.3 shows the correspondence between interrupt functions.

Table 1.3 Correspondence between Functions

78K0/Kx2 Interrupt functions	RL78/G13 Interrupt functions
Maskable interrupts 78K0/KF2: External interrupts: 9 ch, Internal interrupts: 20 ch	Maskable interrupts 80-pin: External interrupts:13, Internal interrupts:37 128-pin: External interrupts:13, Internal interrupts:41
Software interrupt (BRK instruction)	Software interrupt (BRK instruction)
Reset Interrupt Source: Reset input, Power-on clear, Low-voltage detection, WDT overflow	Reset Interrupt Source: RESET pin input, Power-on-reset, Voltage detection, Overflow of watchdog timer, Execution of illegal instruction, Illegal-memory access, RAM parity error

2. Difference between Interrupt functions

Table 2.1 shows the differences between the Interrupt functions.

Table 2.1 Difference between Interrupt functions

Item	78K0/Kx2 Interrupt functions	RL78/G13 Interrupt functions
Interrupt Type	- Maskable Interrupt - Software Interrupt - Reset	- Maskable Interrupt - Software Interrupt - Reset
Maskable interrupt sources	29 (Note1)	54 (Note2)
External sources	9 (Note1)	13 (Note2)
Internal sources	20 (Note1)	41 (Note2)
Software interrupt sources	1	1
Reset sources	4	7
Interrupt priority specification	2 levels	4 levels
Priority of interrupt currently being serviced	Program Status Word (PSW) bit 2: 0 bit 1: ISP	Program Status Word (PSW) bit 2: ISP1 bit 1: ISP0
Time from Generation of Maskable Interrupt Until Servicing	- When High priority level (xxPRx = 0) 7 clocks to 32 clocks - When Low priority level (xxPRx = 1) 8 clocks to 33 clocks (1 clock = 1/f_{CPU})	9 clocks to 16 clocks (1 clock = 1/f_{CLK})
Interrupt request hold instructions	Yes (Note3)	Yes (Note3)
Interrupt Request Flag	XXIFX bit	XXIFX bit
Interrupt servicing control	XXMKX bit	XXMKX bit
Priority level selection	XXPRX bit	XXPR1X bit, XXPR0X bit
Return instruction from the vectored interrupt (RETI)	Use a return instruction from the vectored interrupt	Use a return instruction from the vectored interrupt
Return instruction from the software interrupt generated with the BRK instruction (RETB)	Use a return instruction from the software interrupt generated with the BRK instruction. (Vector Table Address: 003EH, 003FH)	Use a return instruction from the software interrupt generated with the BRK instruction. (Vector Table Address: 0007EH, 0007FH)

Note1. For 78K0/KF2 80-pin products

Note2. For RL78/G13 128 pin products

Note3. For details, refer to the appropriate user's manuals (hardware).

Remark. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

3. Comparison between Registers

Table 3.1 compares the registers for the Interrupt functions of the 78K0/Kx2 and the RL78/G13.

Table 3.1 Comparison between Registers

Item	78K0/Kx2	RL78/G13
Interrupt request flag registers	IF0L register, IF0H register IF1L register, IF1H register	IF0L register, IF0H register IF1L register, IF1H register IF2L register, IF2H register IF3L register
Interrupt mask flag registers	MK0L register, MK0H register MK1L register, MK1H register	MK0L register, MK0H register MK1L register, MK1H register MK2L register, MK2H register MK3L register
Priority specification flag registers	PR0L register, PR0H register PR1L register, PR1H register	PR00L register, PR00H register PR01L register, PR01H register PR02L register, PR02H register PR03L register PR10L register, PR10H register PR11L register, PR11H register PR12L register, PR12H register PR13L register
External interrupt rising edge enable register	EGP register	EGP0 register, EGP1 register
External interrupt falling edge enable register	EGN register	EGN0 register, EGN1 register
Program status word	PSW	PSW

Remark. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

4. Comparison between Interrupt Priorities

Table 4.1 to Table 4.4 compare the default priorities of the 78K0/Kx2 and RL78/G13 maskable interrupts.

Table 4.1 Comparison between Interrupt Priorities (1/4)

Item	78K0/Kx2			RL78/G13		
Type	Maskable interrupt			Maskable interrupt		
Default Priority	Name	Trigger	Vector Table Address	Name	Trigger	Vector Table Address
0	INTLVI	Low-voltage detection (Note1)	0004H	INTWDTI	Watchdog timer interval (Note2) (75% of overflow time + 1/2f_{IL})	00004H
1	INTP0	Pin input edge detection	0006H	INTLVI	Voltage detection (Note3)	00006H
2	INTP1		0008H	INTP0	Pin input edge detection	00008H
3	INTP2		000AH	INTP1		0000AH
4	INTP3		000CH	INTP2		0000CH
5	INTP4		000EH	INTP3		0000EH
6	INTP5		0010H	INTP4		00010H
7	INTSRE6	UART6 reception error generation	0012H	INTP5		00012H
8	INTSR6	End of UART6 reception	0014H	INTST2 /INTCSI20 /INTIIC20	UART2 transmission transfer end or buffer empty interrupt /CSI20 transfer end or buffer empty interrupt/IIC20 transfer end	00014H
9	INTST6	End of UART6 transmission	0016H	INTSR2 /INTCSI21 /INTIIC21	UART2 reception transfer end /CSI21 transfer end or buffer empty interrupt/IIC21 transfer end	00016H
10	INTCSI10/ INTST0	End of CSI10 communication /end of UART0 transmission	0018H	INTSRE2	UART2 reception communication error occurrence	00018H
				INTTM11H	End of timer channel 11 count or capture (at higher 8-bit timer operation)	
11	INTTMH1	Match between TMH1 and CMP01 (when compare register is specified)	001AH	INTDMA0	End of DMA0 transfer	0001AH
12	INTTMH0	Match between TMH0 and CMP00 (when compare register is specified)	001CH	INTDMA1	End of DMA1 transfer	0001CH

Note1. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is cleared to 0.

Note2. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

Note3. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is cleared to 0.

Remark. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Table 4.2 Comparison between Interrupt Priorities (2/4)

Item	78K0/Kx2			RL78/G13		
Type	Maskable interrupt			Maskable interrupt		
Default Priority	Name	Trigger	Vector Table Address	Name	Trigger	Vector Table Address
13	INTTM50	Match between TM50 and CR50 (when compare register is specified)	001EH	INTST0 /INTCSI00 /INTIIC00	UART0 transmission transfer end or buffer empty interrupt /CSI00 transfer end or buffer empty interrupt/IIC00 transfer end	0001EH
14	INTTM000	- Match between TM00 and CR000 (when compare register is specified) - TI010 pin valid edge detection (when capture register is specified)	0020H	INTSR0 /INTCSI01 /INTIIC01	UART0 reception transfer end/CSI01 transfer end or buffer empty interrupt /IIC01 transfer end	00020H
15	INTTM010	- Match between TM00 and CR010 (when compare register is specified), - TI000 pin valid edge detection (when capture register is specified)	0022H	INTSRE0	UART0 reception communication error occurrence	00022H
				INTTM01H	End of timer channel 01 count or capture (at higher 8-bit timer operation)	
16	INTAD	End of A/D conversion	0024H	INTST1 /INTCSI10 /INTIIC10	UART1 transmission transfer end or buffer empty interrupt /CSI10 transfer end or buffer empty interrupt/IIC10 transfer end	00024H
17	INTSR0	End of UART0 reception or reception error generation	0026H	INTSR1 /INTCSI11 /INTIIC11	UART1 reception transfer end/CSI11 transfer end or buffer empty interrupt/IIC11 transfer end	00026H
18	INTWTI	Watch timer reference time interval signal	0028H	INTSRE1	UART1 reception communication error occurrence	00028H
				INTTM03H	End of timer channel 03 count or capture (at higher 8-bit timer operation)	
19	INTTM51 (Note3)	Match between TM51 and CR51 (when compare register is specified)	002AH	INTIICA0	End of IICA0 communication	0002AH
20	INTKR	Key interrupt detection	002CH	INTTM00	End of timer channel 00 count or capture	0002CH
21	INTWT	Watch timer overflow	002EH	INTTM01	End of timer channel 01 count or capture (at 16-bit/lower 8-bit timer operation)	0002EH

Remark. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Table 4.3 Comparison between Interrupt Priorities (3/4)

Item	78K0/Kx2			RL78/G13		
Type	Maskable interrupt			Maskable interrupt		
Default Priority	Name	Trigger	Vector Table Address	Name	Trigger	Vector Table Address
22	INTP6	Pin input edge detection	0030H	INTTM02	End of timer channel 02 count or capture	00030H
23	INTP7		0032H	INTTM03	End of timer channel 03 count or capture (at 16-bit/lower 8-bit timer operation)	00032H
24	INTIIC0/ INTDMU	End of IIC0 communication/ end of multiply/divide operation	0034H	INTAD	End of A/D conversion	00034H
25	INTCSI11	End of CSI11 communication	0036H	INTRTC	Fixed-cycle signal of real-time clock/alarm match detection	00036H
26	INTTM001	Match between TM01 and CR001 (when compare register is specified), TI011 pin valid edge detection (when capture register is specified)	0038H	INTIT	Interval signal of 12-bit interval timer detection	00038H
27	INTTM011	Match between TM01 and CR011 (when compare register is specified), TI001 pin valid edge detection (when capture register is specified)	003AH	INTKR	Key return signal detection	0003AH
28	INTACSI	End of CSIA0 communication	003CH	INTST3 /INTCSI30 /INTIIC30	UART3 transmission transfer end or buffer empty interrupt /CSI30 transfer end or buffer empty interrupt/IIC30 transfer end	0003CH
29	–	–	–	INTSR3 /INTCSI31 /INTIIC31	UART3 reception transfer end /CSI31 transfer end or buffer empty interrupt/IIC31 transfer end	0003EH
30	–	–	–	INTTM13	End of timer channel 13 count or capture (at 16-bit/lower 8-bit timer operation)	00040H
31	–	–	–	INTTM04	End of timer channel 04 count or capture	00042H
32	–	–	–	INTTM05	End of timer channel 05 count or capture	00044H
33	–	–	–	INTTM06	End of timer channel 06 count or capture	00046H
34	–	–	–	INTTM07	End of timer channel 07 count or capture	00048H

Remark. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Table 4.4 Comparison between Interrupt Priorities (4/4)

Item	78K0/Kx2			RL78/G13		
Type	Maskable interrupt			Maskable interrupt		
Default Priority	Name	Trigger	Vector Table Address	Name	Trigger	Vector Table Address
35	–	–	–	INTP6	Pin input edge detection	0004AH
36	–	–	–	INTP7		0004CH
37	–	–	–	INTP8		0004EH
38	–	–	–	INTP9		00050H
39	–	–	–	INTP10		00052H
40	–	–	–	INTP11		00054H
41	–	–	–	INTTM10	End of timer channel 10 count or capture	00056H
42	–	–	–	INTTM11	End of timer channel 11 count or capture (at 16-bit/lower 8-bit timer operation)	00058H
43	–	–	–	INTTM12	End of timer channel 12 count or capture	0005AH
44	–	–	–	INTSRE3	UART3 reception communication error occurrence	0005CH
				INTTM13H	End of timer channel 13 count or capture (at higher 8-bit timer operation)	
45	–	–	–	INTMD	End of division operation / Overflow of multiply-accumulation result occurs	0005EH
46	–	–	–	INTIICA1	End of IICA1 communication	00060H
47	–	–	–	INTFL	Reserved (Note)	00062H
48	–	–	–	INTDMA2	End of DMA2 transfer	00064H
49	–	–	–	INTDMA3	End of DMA3 transfer	00066H
50	–	–	–	INTTM14	End of timer channel 14 count or capture	00068H
51	–	–	–	INTTM15	End of timer channel 15 count or capture	0006AH
52	–	–	–	INTTM16	End of timer channel 16 count or capture	0006CH
53	–	–	–	INTTM17	End of timer channel 17 count or capture	0006EH

Note. Used for the flash self-programming library and data flash library.

Remark. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Table 4.5 compares the software interrupts of the 78K0/Kx2 and RL78/G13.

Table 4.5 Comparison between software interrupt

78K0/Kx2			RL78/G13		
Software Interrupt			Software Interrupt		
Name	Trigger	Vector Table Address	Name	Trigger	Vector Table Address
BRK	Execution of BRK instruction	003EH	BRK	Execution of BRK instruction	0007EH

Table 4.6 compares the reset sources of the 78K0/Kx2 and RL78/G13.

Table 4.6 Comparison between reset source

78K0/Kx2			RL78/G13		
Reset			Reset		
Name	Trigger	Vector Table Address	Name	Trigger	Vector Table Address
RESET	Reset input	0000H	RESET	RESET pin input	00000H
POC	Power-on clear		POR	Power-on-reset	
LVI	Low-voltage detection (Note1)		LVD	Voltage detection (Note2)	
WDT	WDT overflow		WDT	Overflow of watchdog timer	
–	–	–	TRAP	Execution of illegal instruction (Note3)	
–	–	–	IAW	Illegal-memory access	
–	–	–	RPE	RAM parity error	

Note1. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is set to 1.

Note2. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is set to 1.

Note3. When the instruction code in FFH is executed. Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Remark. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

5. Sample Code for Interrupt Function

The sample code for the interrupt functions is explained in the following application notes.

- RL78/G13 Key Interrupt Function CC-RL (R01AN2700)

6. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

  The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.12, 2019.	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.