RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: A/D Converter

Introduction

This application note describes how to migrate the A/D Converter of the 78K0/Kx2 to that of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of A/D Converter of 78K0/Kx2 and A/D Converter of RL78/G13

Table 1.1 shows the functions of the A/D Converter of 78K0/Kx2, and Table 1.2 shows the functions of the A/D Converter of RL78/G13.

Table 1.1 Functions of 78K0/Kx2 A/D Converter

Function	Explanation
A/D conversion	The A/D converter converts an analog input signal into a digital value, and consists of up to eight channels (ANI0 to ANI7) with a resolution of 10 bits. 10-bit resolution A/D conversion is carried out repeatedly for one analog input channel selected from ANI0 to ANI7. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated. The A/D converter has the 10-bit A/D conversion result register (ADCR), which holds the A/D conversion result in its upper ten bits, and also the 8-bit A/D conversion result register (ADCRH), which holds the A/D conversion result in its upper eight bits.

Table 1.2 Functions of RL78/G13 A/D Converter

Function	Explanation
A/D conversion	The A/D converter is used to convert analog input signals into digital values, and is configured to control analog inputs, including up to 26 channels of A/D converter analog inputs (ANI0 to ANI14 and ANI16 to ANI26). The A/D converter has select mode and also scan mode. In select mode, one of the analog input channels is selected and A/D-converted. In scan mode, four consecutive analog input channels among ANI0-ANI14 are A/D-converted sequentially. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated. In addition, the converter can handle hardware triggers and has one-shot conversion mode as well as sequential conversion mode. The A/D converter has the 10-bit A/D conversion result register (ADCR), which holds the A/D conversion result in its upper ten bits, and also the 8-bit A/D conversion result register (ADCRH), which holds the A/D conversion result in its upper eight bits. Besides, 10-bit or 8-bit resolution can be selected. A hardware trigger signal in STOP mode can release STOP mode and so A/D conversion can be performed without operating the CPU (SNOOZE mode).

The A/D converter incorporated in the 78K0/Kx2 has the sample-and-hold circuit, series resistor string, voltage comparator, successive approximation register, and A/D conversion result registers.

Figure 1.1 shows a block diagram of the A/D Converter in the 78K0/Kx2.

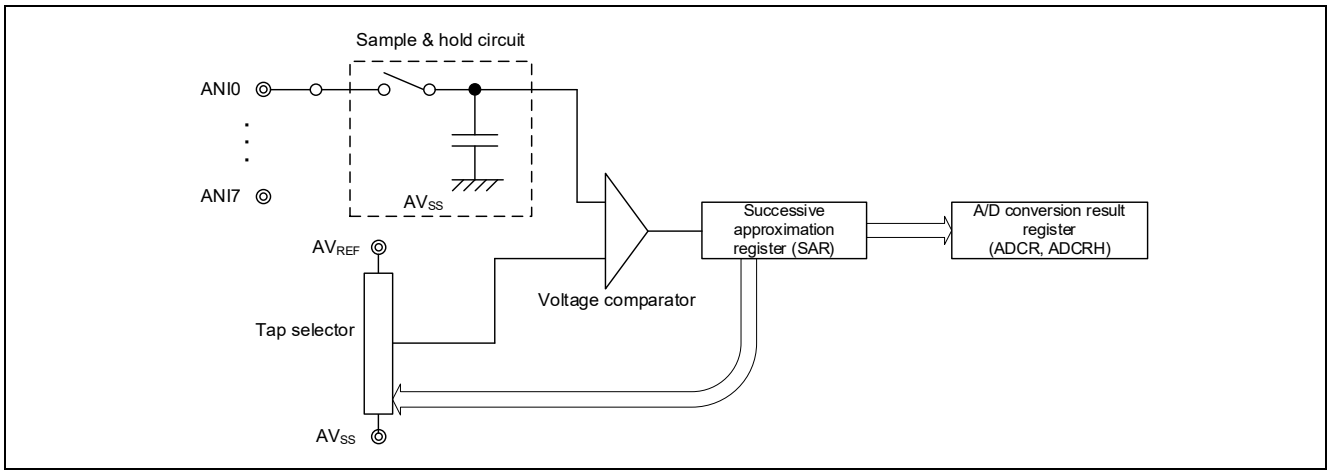

Figure 1.1 Block Diagram of A/D Converter (78K0/Kx2)

The A/D converter incorporated in the RL78/G13 has the sample-and-hold circuit, A/D voltage comparator, Comparison voltage generator, successive approximation register, and A/D conversion result registers.

For the comparison voltage generator, either VDD and VSS pin pair or AVREFP and AVREFM pin pair can be selected to use.

Figure 1.2 shows a block diagram of the A/D Converter in the RL78/G13.

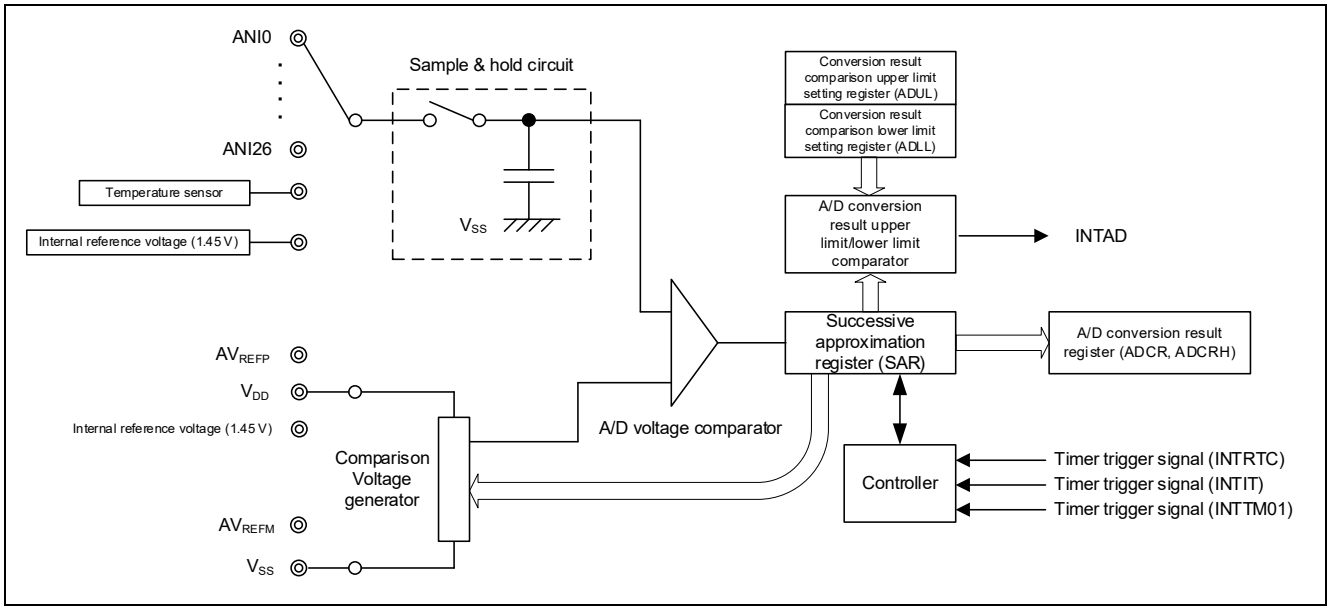

Figure 1.2 Block Diagram of A/D Converter (RL78/G13)

Table 1.3 shows the A/D converter functions of 78K0/Kx2 and RL78/G13.

Table 1.3 Correspondence between Functions

78K0/Kx2 A/D Converter	RL78/G13 A/D Converter
10-bit resolution A/D conversion	10-bit/8-bit resolution A/D conversion
-	A/D conversion channel selection mode (Select mode / Scan mode)
-	Sampling clock selection
-	A/D conversion trigger mode (Software trigger mode / Hardware trigger mode)
-	A/D conversion mode (Sequential conversion mode / One-shot conversion mode)
-	Selection of the + side reference voltage source (V_{DD} / AV_{REFP} / Internal reference voltage)
-	Selection of the – side reference voltage (VSS / AV_{REFM})
-	Checking the upper limit and lower limit conversion result values
-	SNOOZE mode
-	A/D test

The A/D Converter of 78K0/Kx2 corresponds to the A/D Converter (10-bit resolution, Select mode, Software trigger mode, Sequential conversion mode) of the RL78/G13.

2. Difference between A/D Converter

Table 2.1 and Table 2.2 shows the differences between the A/D Converter.

Table 2.1 Differences between A/D Converter (1/2)

Item	78K0/Kx2 A/D Converter	RL78/G13 A/D Converter
Conversion Time (min.)	6.1μs (Note1)	2.125μs (Note2)
Overall error (min.)	±0.4%FSR (Note3)	±3.5LSB (Note4)
Resolution	10bit	10bit/ 8bit
Analog input channel (max.)	8ch	26ch
Enables conversion operation	ADM register ADCS = 1	ADM0 register ADCS = 1
Stops conversion operation	ADM register ADCS = 0	ADM0 register ADCS = 0
Enables comparator operation	ADM register ADCE = 1 (Note5)	ADM0 register ADCE = 1 (Note5)
Stops comparator operation	ADM register ADCE = 0	ADM0 register ADCE = 0
A/D conversion result register	ADCR, ADCRH register	ADCR, ADCRH register
Channel selection mode	None	- Select mode - Scan mode
Conversion operation mode	None	- One-shot conversion mode - Sequential conversion mode

Note1. For 78K0/Kx2, 4.0V≦AV_{REF}≦5.5V

Note2. For RL78/G13, 3.6 V≦V_{DD}≦5.5 V, 10-bit resolution
The target for conversion : ANI0-ANI14, ANI16-ANI26

Note3. When the resolution is 10 bits, equivalent to ± 4 LSB. 1 LSB = $1/2^{10}$ = 1/1024 = 0.098 %FSR.

Note4. For RL78/G13, 1.8 V ≤ V_{DD} = AV_{REFP} ≤ 5.5 V,
When reference voltage (+) = AV_{REFP}/ANI0, reference voltage (-) = AV_{REFM}/ANI1, target pin: ANI2-ANI14.

Note5. When the ADCS bit is set to 1 after 1 μs or more has elapsed from the time ADCE bit is set to 1, the conversion result at that time has priority over the first conversion result. Otherwise, ignore data of the first conversion.

Remark. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 2.2 Differences between A/D Converter (2/2)

Item	78K0/Kx2 A/D Converter	RL78/G13 A/D Converter
Operation voltage mode	- LV0 = 0 (Note1) - LV0 = 1 (Note2)	- Standard 1 / standard 2 mode (Note3) - Low voltage 1 / low voltage 2 mode (Note4)
Sampling time	Static	Standard 1 / Low voltage 1 mode Sampling clock cycles: 7 x f_{AD} Standard 2 / Low voltage 2 mode Sampling clock cycles: 5 x f_{AD}
Selection of the A/D conversion trigger mode	None	- Software trigger mode - Hardware trigger no-wait mode - Hardware trigger wait mode
Selection of the hardware trigger signal	None	- End of timer channel 01 count or capture interrupt signal (INTTM01) - Real-time clock interrupt signal (INTRTC) - 12-bit interval timer interrupt signal (INTIT)
+ side reference voltage source	AV_{REF}	- Supplied from P20/AV_{REFP}/ANI0 - Supplied from V_{DD} - Supplied from the internal reference voltage (1.45V) (Note5)
- side reference voltage source	AV_{SS}	- Supplied from P21/AV_{REFM}/ANI1 - Supplied from V_{SS}
Checking the upper limit and lower limit conversion result values	None	- The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register - The interrupt signal (INTAD) is output when the ADCR register < the ADLL register or the ADUL register < the ADCR register
Timing of interrupt request generation	Interrupt request signal (INTAD) is generated when AD conversion is completed and the result is transferred to the AD conversion result register.	Interrupt request signal (INTAD) is generated when AD conversion is completed and the result is transferred to the AD conversion result register.
Setting of SNOOZE mode	None	Yes
A/D test	None	Yes
Analog input (A) / digital I/O (D) switching	Bitwise switching by ADPC register (Note6)	Bitwise switching by ADPC register (Note7)

Note1. Can be selected when 2.7 V ≦ AV_{REF} ≦ 5.5 V.

Note2. Can be selected when 2.3 V≦AV_{REF}≦5.5 V.

Note3. Can be selected when 2.7 V≦V_{DD}≦5.5 V.

Note4. Can be selected when 1.6 V≦V_{DD}≦5.5 V.

Note5. This setting can be used only in HS (high-speed main) mode.

Note6. For 78K0/Kx2, **ANI7** to **ANI0** are used as analog inputs (A) in this order.

Note7. For RL78/G13, **ANI0** to **ANI26** are used as analog inputs (A) in this order.

Remark. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

3. Register Compatibilities

Table 3.1 compares the registers for the 78K0/Kx2 A/D Converter and the registers for the RL78/G13 A/D Converter.

Table 3.1 Comparison between Registers

Item	78K0/Kx2	RL78/G13
Clock supply to A/D Converter	None	PER0 register ADCEN bit
A/D conversion operation control	ADM register ADCS bit	ADM0 register ADCS bit
Comparator operation contro	ADM register ADCE bit	ADM0 register ADCE bit
A/D Conversion Time Selection	ADM register FR2 - FR0 bit LV1 bit, LV0 bit	ADM register FR2 - FR0 bit LV1 bit, LV0 bit
10-bit A/D conversion result register	ADCR register	ADCR register
8-bit A/D conversion result register	ADCRH register	ADCRH register
Analog input channel specification register	ADS register ADS2 - ADS0 bit	ADS register ADISS bit, ADS4 - ADS0 bit
A/D port configuration register	ADPC register ADPC3 - ADPC0 bit	ADPC register ADPC3 - ADPC0 bit
Specification of the A/D conversion channel selection mode	None	ADM0 register ADMD bit
Selection of the A/D conversion trigger mode	None	ADM1 register ADTMD1 bit, ADTMD0 bit
Specification of the A/D conversion mode	None	ADM1 register ADSCM bit
Selection of the hardware trigger signal	None	ADM1 register ADTRS1 bit, ADTRS0 bit
Selection of the + side reference voltage source of the A/D converter	None	ADM2 register ADREFP1 bit, ADREFP0 bit
Selection of the – side reference voltage of the A/D converter	None	ADM2 register ADREFM bit
Checking the upper limit and lower limit conversion result values	None	ADM2 register ADRCK bit
Specification of the SNOOZE mode	None	ADM2 register AWC bit
Selection of the A/D conversion resolution	None	ADM2 register ADTYP bit
Conversion result comparison upper limit setting register	None	ADUL register
Conversion result comparison lower limit setting register	None	ADLL register
A/D test register	None	ADTES register ADTES1 bit, ADTES0 bit

Remark. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

4. Sample Code for A/D Converter

The sample code for A/D Converter is explained in the following application notes.

- RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) CC-RL (R01AN2581)
- RL78/G13 A/D Converter (SNOOZE Mode) CC-RL (R01AN2804)

5. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Data	Description	
		Page	Summary
1.00	Sep.09, 2019.	-	First edition issued

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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