RL78/G11, R8C/32C Group

Migration Guide from R8C to RL78: A/D Converter

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Abstract

This application note describes how to implement, in the RL78/G11 A/D converter, the various operations equivalent to the operation modes provided by the R8C/32C group A/D converter. The operation modes include: one-shot mode, repeat mode 0, repeat mode 1, single sweep mode, and repeat sweep mode.

Target Devices

RL78/G11, R8C/32C Group

When applying this application note to other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU. For the specifications and electrical characteristics of the MCU, refer to the appropriate User's Manual: Hardware and technical updates.

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1. Migration from R8C Family to RL78 Family

This chapter describes how to allow the RL78/G11 to support the various operation modes provided by the R8C/32C group A/D converter (one-shot mode, repeat mode 0, repeat mode 1, single sweep mode, and repeat sweep mode).

Table 1.1 shows the operation modes of the R8C/32C group A/D converter, and Table 1.2 shows the operation modes of the RL78/G11 A/D converter.

The R8C/32C group A/D converter performs A/D conversion according to one of the operation modes selected from the operation modes listed in Table 1.1. The RL78/G11 A/D converter performs A/D conversion according to the combination of the A/D conversion channel selection mode and A/D conversion operation mode listed in Table 1.2.

The R8C/32C group and RL78/G11 have different number of registers for storing A/D conversion results.

The R8C/32C group has several registers for storing A/D conversion results, which correspond to selected pins. Specifically, one register or eight registers can be used for one pin.

On the other hand, the RL78/G11 has only one register for storing the A/D conversion results.

Therefore, for sequential A/D conversion by the RL78/G11, the A/D conversion results need to be read by using the interrupts or DTC before the next A/D conversion ends.

In addition, the R8C/32C group and RL78/G11 store the A/D conversion results in different forms.

In 10-bit resolution A/D conversion, both MCUs store the A/D conversion results in 2-byte registers. With the R8C/32C group, the A/D conversion results are stored in the lower 10 bits in the A/D conversion result register (ADi). However, With the RL78/G11, the A/D conversion results are stored in the upper 10 bits in the A/D conversion result register (ADCR). Therefore, to allow the RL78/G11 to handle the A/D conversion results in the same form as the R8C/32C group, it is necessary to shift the A/D conversion results to the right by six bits through software.

In 8-bit resolution A/D conversion, both MCUs store the A/D conversion results in 1-byte registers. With the R8C/32C group, the A/D conversion results are stored in the lower 8 bits in the A/D conversion result register (ADi). With the RL78/G11, the A/D conversion results are sotored in the upper 8 bits in the A/D conversion result register (ADCR).

Table 1.1 Operation Modes of R8C/32C Group A/D Converter (outline)

R8C/32C Group A/D Converter		
Operation Mode	Function	A/D Conversion Result Register
One-shot mode	A/D conversion is performed once on the input voltage of one pin.	A/D conversion result register corresponding to the selected pin
Repeat mode 0	A/D conversion is repeatedly performed on the input voltage of one pin.	
Repeat mode 1	A/D conversion is repeatedly performed on the input voltage of one pin.	Eight A/D conversion result registers (A/D conversion results are repeatedly stored in the consecutive registers according to the number of conversions.)
Single sweep mode	A/D conversion is performed once each on the input voltage of two or four pins.	A/D conversion result registers corresponding to the selected pins
Repeat sweep mode	A/D conversion is repeatedly performed on the input voltage of two or four pins.	

Table 1.2 Operation Modes of RL78/G11 A/D Converter (outline)

RL78/G11 A/D Converter		
Operation Mode	Operation Mode Specification	Function
A/D conversion channel selection mode	Select mode	A/D conversion is performed on the analog input of one selected channel.
	Scan mode	A/D conversion is performed on the analog input of four channels (ANI0-ANI3) in order.
A/D conversion operation mode	One-shot conversion mode	A/D conversion is performed once on the selected channel.
	Sequential conversion mode	A/D conversion is sequentially performed on the selected channels until it is stopped by software.

Table 1.3 shows the operation modes of the R8C/32C group and the corresponding combinations of the A/D conversion channel selection modes and A/D conversion operation modes of the RL78/G11.

Table 1.3 Correspondence among A/D Operation Modes

R8C/32C Group	RL78/G11	
Operation Mode	A/D Conversion Channel Selection Mode	A/D Conversion Operation Mode
One-shot mode	Select Mode	One-shot conversion mode
Repeat mode 0		Sequential conversion mode
Repeat mode 1		
Single sweep mode	Scan mode	One-shot conversion mode
Repeat sweep mode		Sequential conversion mode

2. Differences between RL78/G11 and R8C/32C Group

2.1 A/D Converter Specifications

Table 2.1 and Table 2.2 show the differences in the specifications of the A/D converters.

Table 2.1 Differences in Specifications of A/D Converters (1/2)

Item	R8C/32C Group	RL78/G11
A/D converter operating voltage range	2.2 V ≤ Vref = AVcc ≤ 5.5 V (unavailable in wait mode, STOP mode, low-power read mode, and when flash memory is stopped)	• When standard 1/standard 2 mode is selected, 2.7 V ≤ V_{DD} ≤ 5.5 V • When low voltage 1/low voltage 2 mode is selected, 1.6 V ≤ V_{DD} ≤ 5.5 V
Reference voltage	Vref (2.2 V to AVcc)	Selected from V_{DD}, AV_{REFP} (1.6 V to V_{DD}), and internal reference voltage (1.45 V).
Analog input voltage	0 V to Vref	• Reference voltage = AV_{REFP} ANI2, ANI3: 0 V to AV_{REFP} ANI16 to ANI22: 0 V to AV_{REFP} • Reference voltage = V_{DD} ANI0 to ANI3: 0 V to V_{DD} ANI16 to ANI22: 0 V to EV_{DD} • Reference voltage = internal reference voltage 0 to V_{BGR}
Operating clock frequency (conversion clock frequency)	fAD, fAD/2, fAD/4, fAD/8, (fAD = f1 or fOCO-F)	f_{CLK}/64, f_{CLK}/32, f_{CLK}/16, f_{CLK}/8, f_{CLK}/6, f_{CLK}/5, f_{CLK}/4, f_{CLK}/2 f_{CLK} (CPU/peripheral hardware clock frequency)
Resolution	8 or 10 bits	8 or 10 bits
Operation mode (A/D conversion mode)	• One-shot mode • Repeat mode 0 • Repeat mode 1 • Single sweep mode • Repeat sweep mode	Defined by combination of A/D conversion channel selection mode (select mode, scan mode) and A/D conversion operation mode (sequential conversion mode, one-shot conversion mode).
Analog input pins	• 4 pins AN8 to AN11	• 3 pins (10-pin product) ANI0 to ANI2 • 8 pins (16-pin product) ANI0 to ANI3, ANI18, ANI20 to ANI22 • 10 pins (20-pin product) ANI0 to ANI3, ANI16 to ANI18, ANI20 to ANI22 • 11 pins (24-pin, 25-pin product) ANI0 to ANI3, ANI16 to ANI22

Table 2.2 Differences in Specifications of A/D Converters (2/2)

Item	R8C/32C Group	RL78/G11
A/D conversion trigger	• Software trigger • Timer RC • External trigger (ADTRG)	• Software trigger • Hardware trigger (Note 1)
Hardware trigger operation mode selection	Impossible	Possible (hardware trigger no-wait mode, hardware trigger wait mode)
A/D conversion time	44 ϕAD cycles min.	Selectable by using ADM0 register.
Number of pins that can be simultaneously used	1, 2, or 4 pins (Note 2)	1 or 4 pins (Note 2)
Number of registers for storing A/D conversion results	8 (AD0 to AD7)	1 (Note 3)
Operation in STOP mode	Impossible	Possible (SNOOZE mode function)
On-chip reference voltage/ internal reference voltage	1.34 V (TYP.)	1.45 V (TYP.)
A/D disconnection detection assistance function	Provided	Not provided
Temperature sensor	Not provided	Provided
Test mode	Not provided	Provided

Note 1. As a hardware trigger, one of the following signals can be selected: end of timer channel 1 count or capture interrupt singal (INTTM01), event signal selected by ELC, realtime clock interrupt singal (INTRTC), and 12-bit interval timer interrupt singal (INTIT).
The ELC can select events from among external interrupt edge detection (INTP0 to INTP6), key return signal detection (INTKR), 12-bit interval timer interrupt singal detection (INTIT), 8-bit interval timer channel 00 compare match or 16-bit interval timer channel 0 compare match (cascaded) (INTIT00), 8-bit interval timer channel 01 compare match (INTIT01), end of TAU count/capture (INTTM00 to INTTM03), comparator detection (INTCMP0 and INTCMP1), and TMKB trigger output (INTTMKB0).

Note 2. Depends on the operation mode.

Note 3. The RL78/G11 can only hold the A/D conversion results of one A/D conversion. When performing A/D conversion consecutively, read the A/D conversion results by using the DTC or the equivalent before the next A/D conversion ends.
For how to read the A/D conversion results by using the DTC, refer to the application note, RL78/G14 Transferring A/D Conversion Result Using the DTC CC-RL (R01AN2574).

2.2 Comparison of Registers

Table 2.3 shows the registers of the R8C/32C group and the RL78/G11 used for setting the various items.

Table 2.3 Register Comparison

Item to be Set	R8C/32C Group	RL78/G11
On-chip reference voltage	• OCVREFCR register • ADCON1 register ADEX0 bit	• ADM2 register ADREFP1, ADREFP0 bits ADREFM bit • ADS register
Registers for storing A/D conversion results	AD0 to AD7 registers	• ADCR register (10 bits) or ADCRH register (8 bits) selected
Clock frequency division ratio	ADMOD register CKS1, CKS0 bits	ADM0 register FR2 to FR0 bits
Clock source	ADMOD register CKS2 bit	—
A/D operation mode	ADMOD register MD2 to MD0 bits	• ADM0 register ADMD bit • ADM1 register ADSCM bit
A/D conversion trigger	ADMOD register ADCAP1, ADCAP0 bits	ADM1 register ADTMD1, ADTMD0 bits ADTRS1, ADTRS0 bits
Analog input pins	ADINSEL register CH2 to CH0 bits SCAN0 bit ADGSEL1, ADGSEL0 bits	• ADS register • PMC0, PMC2, PMC3, PMC5 registers • PM0, PM2, PM3, PM5 registers
A/D converter operation control	• ADCON0 register ADST bit • ADCON1 register ADSTBY bit	ADM0 register ADCS bit ADCE bit
Resolution	ADCON1 register BITS bit	ADM2 register ADTYP bit
A/D disconnection detection assistance control	ADCON1 register ADDDAEN bit ADDDAEL bit	—
A/D input clock control	—	PER0 register ADCEN bit
A/D conversion time mode	—	ADM0 register LV1, LV0 bits
A/D conversion result comparison upper and lower limit setting	—	• ADUL register • ADLL register
Upper and lower limit conversion result value checking	—	ADM2 register ADRCK bit
SNOOZE mode	—	ADM2 register AWC bit
Temperature sensor output	—	ADS register
A/D test mode	—	ADTES register ADTES1, ADTES0 bits

—: No applicable registers provided.

2.3 Absolute Accuracy

As the counterpart of the absolute accuracy of the R8C/32C group, the overall error is defined for the RL78/G11.

2.3.1 Characteristics of R8C/32C Group

Table 2.4 shows the absolute accuracy of the R8C/32C group.

Table 2.4 Absolute Accuracy of R8C/32C Group

Item		Test Conditions		Specified Values			Units
				Min.	Typ	Max.	
Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN8 to AN11 input	—	—	±3	LSB
		V_{ref} = AV_{CC} = 3.3 V	AN8 to AN11 input	—	—	±5	LSB
		V_{ref} = AV_{CC} = 3.0 V	AN8 to AN11 input	—	—	±5	LSB
		V_{ref} = AV_{CC} = 2.2 V	AN8 to AN11 input	—	—	±5	LSB
	8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN8 to AN11 input	—	—	±2	LSB
		V_{ref} = AV_{CC} = 3.3 V	AN8 to AN11 input	—	—	±2	LSB
		V_{ref} = AV_{CC} = 3.0 V	AN8 to AN11 input	—	—	±2	LSB
		V_{ref} = AV_{CC} = 2.2 V	AN8 to AN11 input	—	—	±2	LSB

2.3.2 Characteristics of RL78/G11

Table 2.5 shows the overall error of the RL78/G11 under the following conditions.

$AV_{REF}(+)$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF}(-)$ = AV_{REFM}/ANI1 (ADREFM = 1) selected,

Target ANI pins: ANI2, ANI3 (ANI pins to which V_{DD} is supplied)

Table 2.5 Overall Error of RL78/G11

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Units
Overall error (Note)	AINL	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB

Note Quantization error (±1/2 LSB) is not included.

2.4 Selecting Analog Input Pins for Each Operation Mode

With the R8C/32C group, two or four analog input pins can be selected as the analog input pins in single sweep mode and repeat sweep mode. On the other hand, with the RL78/G11, only four analog input pins can be selected as the analog input pins in scan mode.

2.4.1 R8C/32C Group

Table 2.6 shows the analog input pins that can be used in each operation mode of the R8C/32C group.

Table 2.6 Usable Analog Input Pins for R8C/32C Group

Operation Mode	Usable Input Pins
One-shot mode, repeat mode 0, repeat mode 1	1 pin selected from AN8 to AN11 and OCVREF.
Single sweep mode, repeat sweep mode	AN8 and AN9 (2 pins), or AN8 to AN11 (4 pins)

2.4.2 RL78/G11

Table 2.7 shows the analog input pins that can be used in each channel selection mode of the RL78/G11.

Table 2.7 Usable Analog Input Pins for RL78/G11

Channel Selection Mode	Usable Input Pins
Select mode	1 pin selected from ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, temperature sensor output voltage, and PGAOUT pins.
Scan mode	4 pins ANI0 to ANI3

When ports are used as analog input pins for the RL78/G11, it is necessary to set the appropriate port-related registers including the PMC registers. For information, refer to section, Register Settings When Using Alternate Function, of the RL78/G11 User's Manual: Hardware.

2.5 Interrupt Operation

In repeat mode 1, single sweep mode, and repeat sweep mode of the R8C/32C group, an interrupt is generated when the A/D conversion on all the selected pins ends; however, with the RL78/G11, an interrupt is generated each time the A/D conversion on one pin ends.

3. Migration of A/D Converters by Using Sample Code Provided

This sample program implements in the RL78/G11, the R8C/32C group A/D converter operations by the method shown in Table 3.1.

For details on the sample program, refer to the following chapters.

Table 3.1 Migration from R8C/32C Group to RL78/G11 by Using This Sample Program

R8C/32C Group	RL78/G11		
Operation Mode	A/D Conversion Channel Selection Mode	A/D Conversion Operation Mode	Method of Transferring A/D Conversion Results
One-shot mode	Select mode	One-shot conversion mode	Interrupt processing
Repeat mode 0		Sequential conversion mode	Interrupt processing
Repeat mode 1			DTC transfer
Single sweep mode	Scan mode	One-shot conversion mode	DTC transfer
Repeat sweep mode		Sequential conversion mode	DTC transfer

4. Example of Migration from One-Shot Mode

4.1 Specifications

To implement R8C/32C one-shot mode in the RL78/G11, the AD converter (software trigger, select, one-shot conversion mode) is used. The A/D conversion results are stored in the RAM by interrupt processing.

The analog input voltage of one pin selected from the ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, temperature sensor output, and PGAOUT pins is A/D-converted in select mode and one-shot conversion mode, and the A/D conversion result values are stored in the RAM assigned by software processing. Specifically, A/D conversion on the selected one pin is performed; When A/D conversion ends, the conversion result is stored in the 10-bit A/D conversion result register (ADCR), and an A/D conversion end interrupt request is generated. Finally, the A/D conversion result is transferred from the ADCR register to the RAM by interrupt processing.

Table 4.1 shows the peripheral function used and the purpose of use, and Figure 4.1 shows the operation summary.

Table 4.1 Peripheral Function Used and Purpose of Use (example of migration from one-shot mode)

Peripheral Function	Purpose of Use
A/D converter	Performs A/D conversion on the analog input voltage.

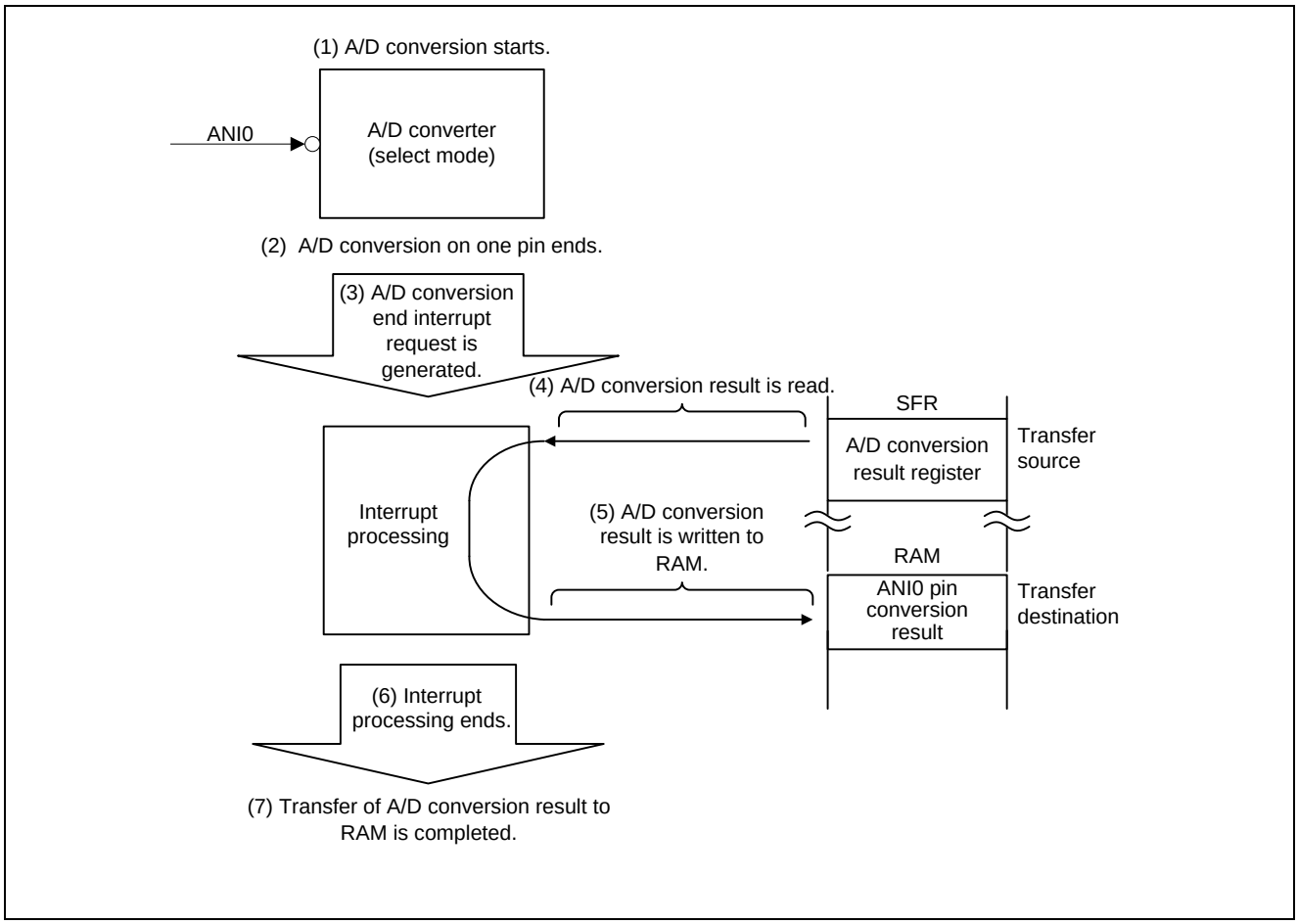


Figure 4.1 Operation Summary (example of migration from one-shot mode)

4.2 Conditions for Confirming Operations

The sample code operations described in this application note are confirmed under the following conditions.

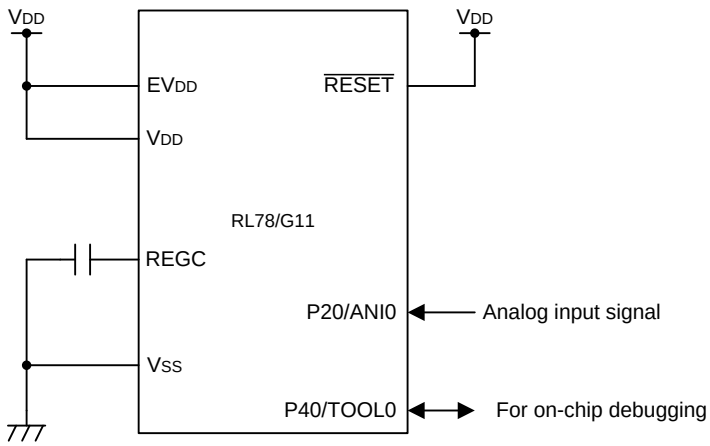
Table 4.2 Conditions for Confirming Operations (example of migration from one-shot mode)

Item	Description
Microcontroller used	RL78/G11 (R5F1056A)
Operating frequency	• High-speed on-chip oscillator clock (f_{IH}): 24 MHz • CPU/peripheral hardware clock (f_{CLK}): 24 MHz
Operating voltage	5.0 V (can be operated from 3.6 V to 5.5 V) LVD operation (V_{LVD}): Reset mode; rise 3.13 V/fall 3.06 V
Integrated development environment (CS+)	CS+ for CC V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.4.0.015 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.

4.3 Hardware Descriptions

4.3.1 Hardware Configuration Example

Figure 4.2 shows an example of the hardware configuration used for this application.



Note 1: The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied. Input-only ports should be each connected to V_{DD} or V_{SS} via a resistor.

Note 2: Any pin whose name begins with EV_{DD} should be connected to V_{DD}.

Note 3: V_{DD} should be equal to or greater than the reset-release voltage (V_{LVD}) specified for the LVD.

Figure 4.2 Hardware Configuration (example of migration from one-shot mode)

4.3.2 List of Pins Used

Table 4.3 lists the pin used and its function.

Table 4.3 Pin Used and Its Function (example of migration from one-shot mode)

Pin Name	I/O	Function
P20/ANI0	Input	A/D converter input (ANI0)

4.4 Software Descriptions

4.4.1 Operation Summary

With this sample program, the A/D conversion on one pin is performed in select mode, and the conversion result is stored in the RAM by A/D conversion end interrupt processing.

Upon completion of the A/D conversion on the ANI0 pin, an A/D conversion end interrupt is generated. In interrupt processing, the A/D conversion result is transferred from the transfer source addresses (ADCR register (FFF1EH, FFF1FH)) to the transfer destination addresses (variable g_ad_value (FF900H to FF901H)). In addition, the A/D conversion result transferred is relocated in the lower 10 bits before being stored in the buffer for storing the A/D conversion results of ANI0 (variable g_ad_an0_value).

Table 4.4 shows the A/D converter settings.

Table 4.4 A/D Converter Settings (example of migration from one-shot mode)

Item to be Set	Settings
Conversion clock frequency (f_{AD})	f_{CLK}/8
A/D conversion mode	• A/D conversion trigger mode: Software trigger • A/D conversion channel selection mode: Select mode • A/D conversion operation mode: One-shot conversion mode
Resolution	10 bits
Analog input channel	ANI0
A/D conversion result comparison upper limit (ADUL register)	FFH
A/D conversion result comparison lower limit (ADLL register)	00H
Upper and lower limit conversion result checking	INTAD generated when ADLL register ≤ ADCR register ≤ ADUL register

(1) The initial setting is made for the A/D converter.
(2) The ADCS bit in the ADM0 register is set to 1 (conversion enabled) to start A/D conversion.
(3) Upon completion of the A/D conversion on the ANI0 pin, an A/D conversion end interrupt is generated.
(4) In interrupt processing, the A/D conversion result is read from the ADCR register and transferred to the RAM (variable g_ad_value).
Also, the A/D conversion result (variable g_ad_value) is shifted to the right by 6 bits (relocated in the lower 10 bits) and stored in the variable g_ad_an0_value.

Figure 4.3 shows the A/D conversion timing and Figure 4.4 shows the relationship between the ADCR register and RAM.

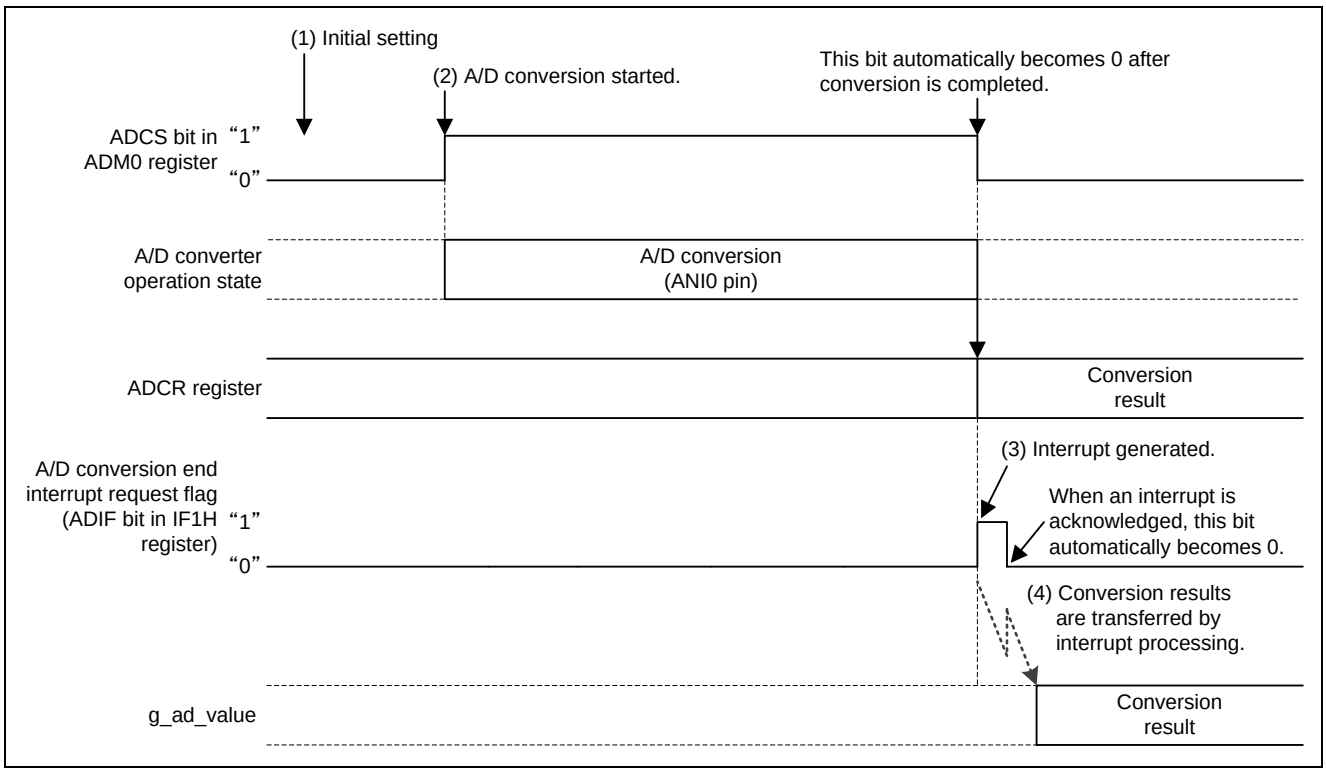


Figure 4.3 A/D Conversion Timing (example of migration from one-shot mode)

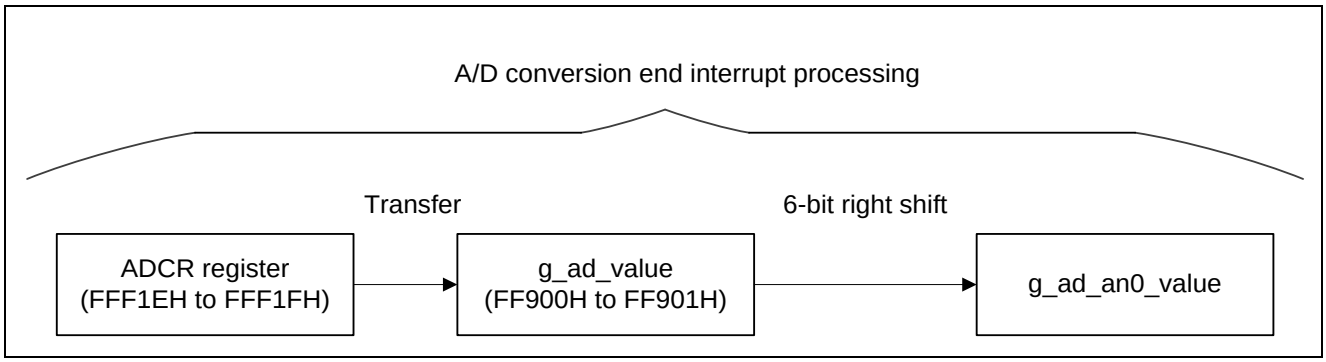


Figure 4.4 Relationship between ADCR Register and RAM (example of migration from one-shot mode)

4.4.2 List of Option Byte Settings

Table 4.5 lists option byte settings.

Table 4.5 Option Byte Settings (example of migration from one-shot mode)

Address	Setting	Contents
000C0H/010C0H	01101110B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H/010C1H	00110011B	LVD reset mode Detection voltage: rise 3.13 V/fall 3.06 V
000C2H/010C2H	11100000B	HS mode High-speed on-chip oscillator clock frequency: 24 MHz
000C3H/010C3H	10000100B	On-chip debugging is enabled.

4.4.3 List of Constants

Table 4.6 lists the constant used in the sample code.

Table 4.6 Constant Used in Sample Code (example of migration from one-shot mode)

Constant Name	Setting	Contents
AD_RESULT_ADDR	0FF900H	Transfer destination address of A/D conversion result

4.4.4 List of Variables

Table 4.7 lists the global variables.

Table 4.7 Global Variables (example of migration from one-shot mode)

Type	Variable Name	Contents	Function Used
uint16_t __near	g_ad_value	Buffer for storing A/D conversion results	r_adc_interrupt
uint16_t	g_ad_an0_value	Buffer for storing A/D conversion result of ANI0	r_adc_interrupt

4.4.5 Functions

Table 4.8 lists the Functions.

Table 4.8 Functions (example of migration from one-shot mode)

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	CPU initial setting
R_ADC_Create	Initial setting of A/D converter
main	Main processing
R_ADC_Start	A/D conversion start
r_adc_interrupt	A/D conversion interrupt

4.4.6 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	CPU initial setting
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_ADC_Create	
Outline	Initial setting of A/D converter
Header	None
Declaration	void R_ADC_Create(void)
Description	Perform the initial setting to use the A/D converter in software trigger mode, select mode, and one-shot conversion mode.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_ADC_Start	
Outline	A/D conversion start
Header	None
Declaration	void R_ADC_Start(void)
Description	Perform A/D conversion.
Argument	None
Return Value	None

r_adc_interrupt	
Outline	A/D conversion interrupt
Header	None
Declaration	static void __near r_adc_interrupt(void)
Description	Perform an A/D conversion end interrupt service routine.
Argument	None
Return Value	None

4.4.7 Flowcharts

(1) Overall Flowchart

Figure 4.5 shows the Overall Flowchart.

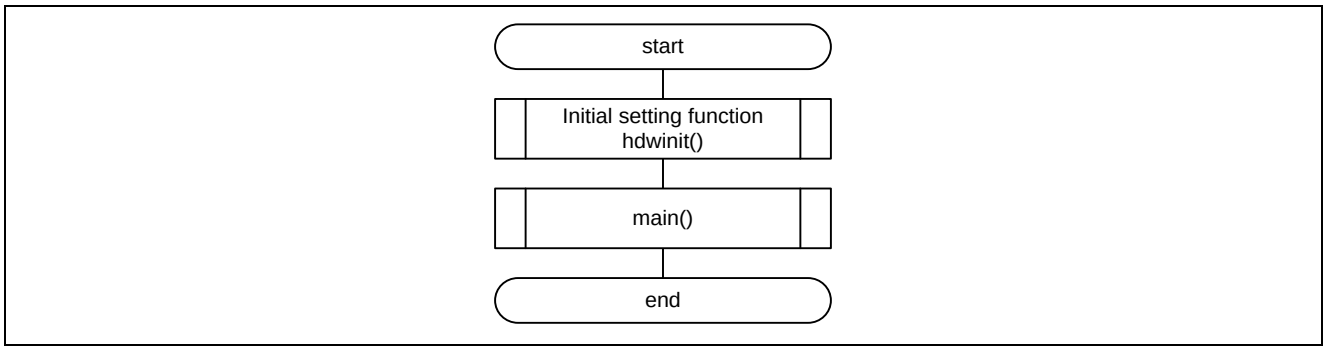


Figure 4.5 Overall Flowchart (example of migration from one-shot mode)

(2) Initial Setting

Figure 4.6 shows the Initial Setting.

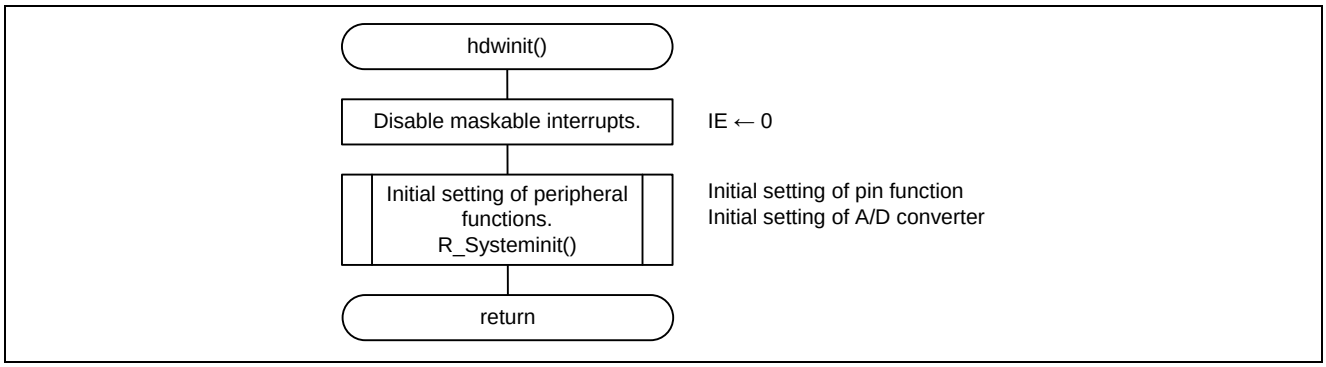


Figure 4.6 Initial Setting (example of migration from one-shot mode)

(3) Initial Setting of Peripheral Functions

Figure 4.7 shows the initial setting of peripheral functions.

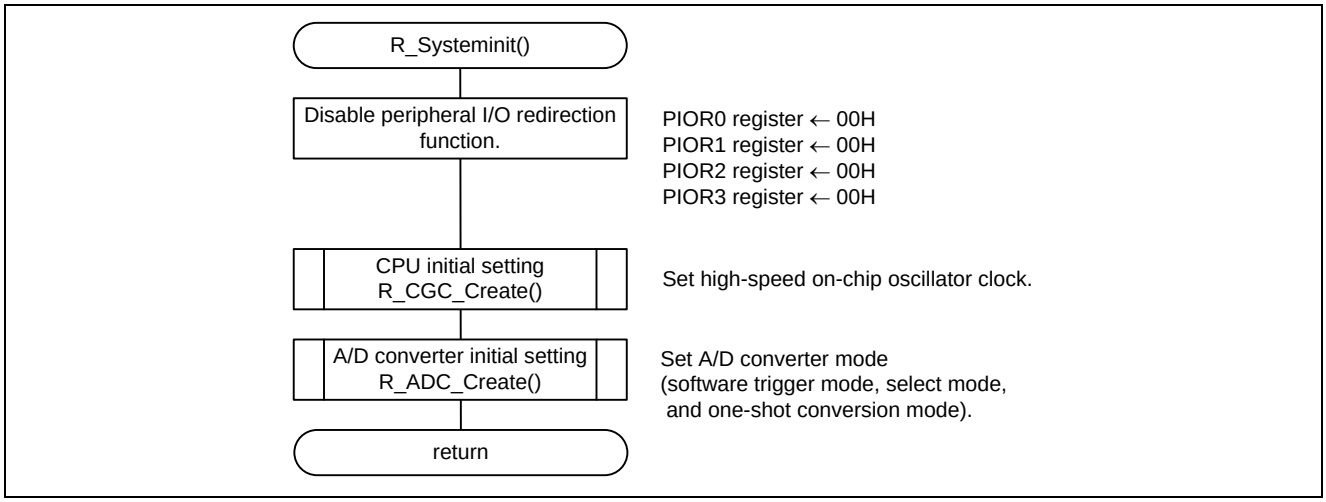


Figure 4.7 Initial Setting of Peripheral Functions (example of migration from one-shot mode)

(4) Initial Setting of CPU

Figure 4.8 shows the initial setting of the CPU.

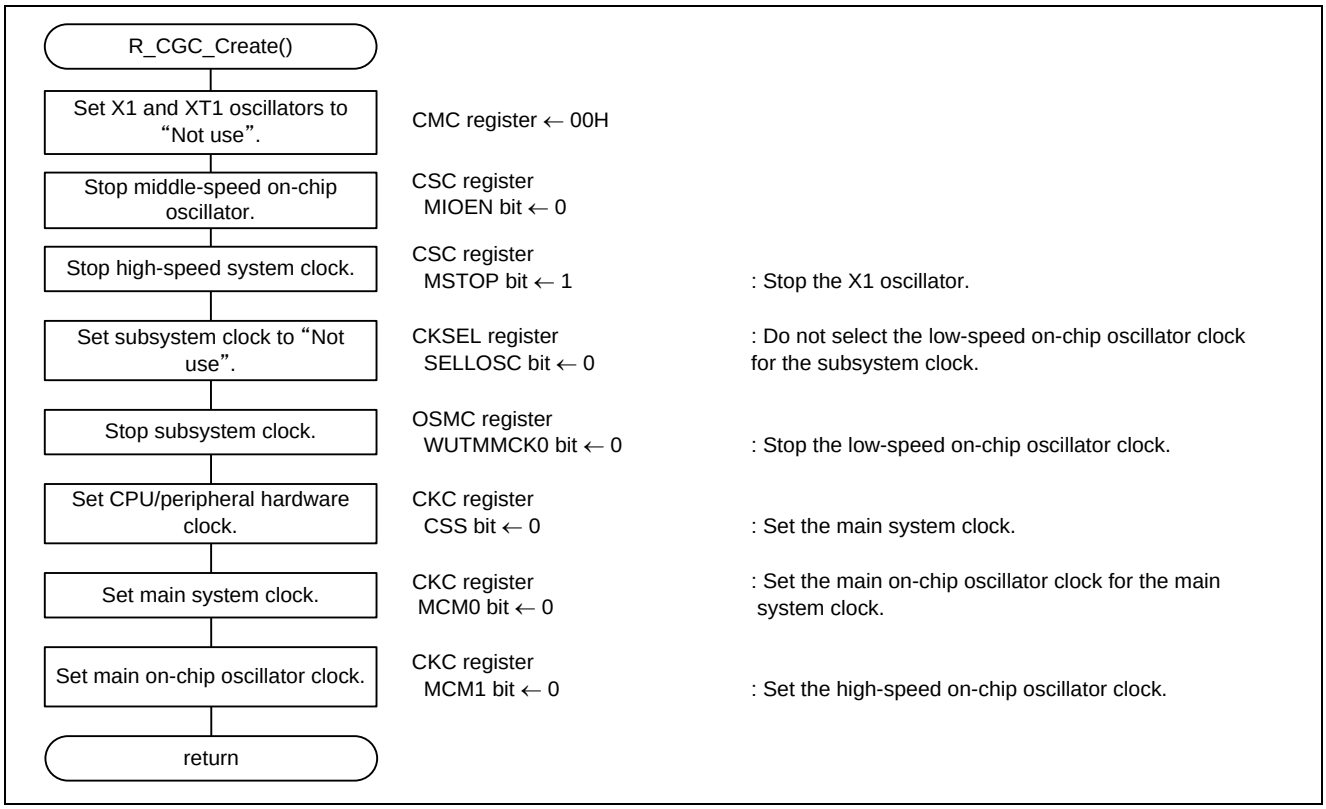


Figure 4.8 Initial Setting of CPU (example of migration from one-shot mode)

(5) Initial Setting of A/D Converter

Figure 4.9 shows the initial setting of the A/D converter.

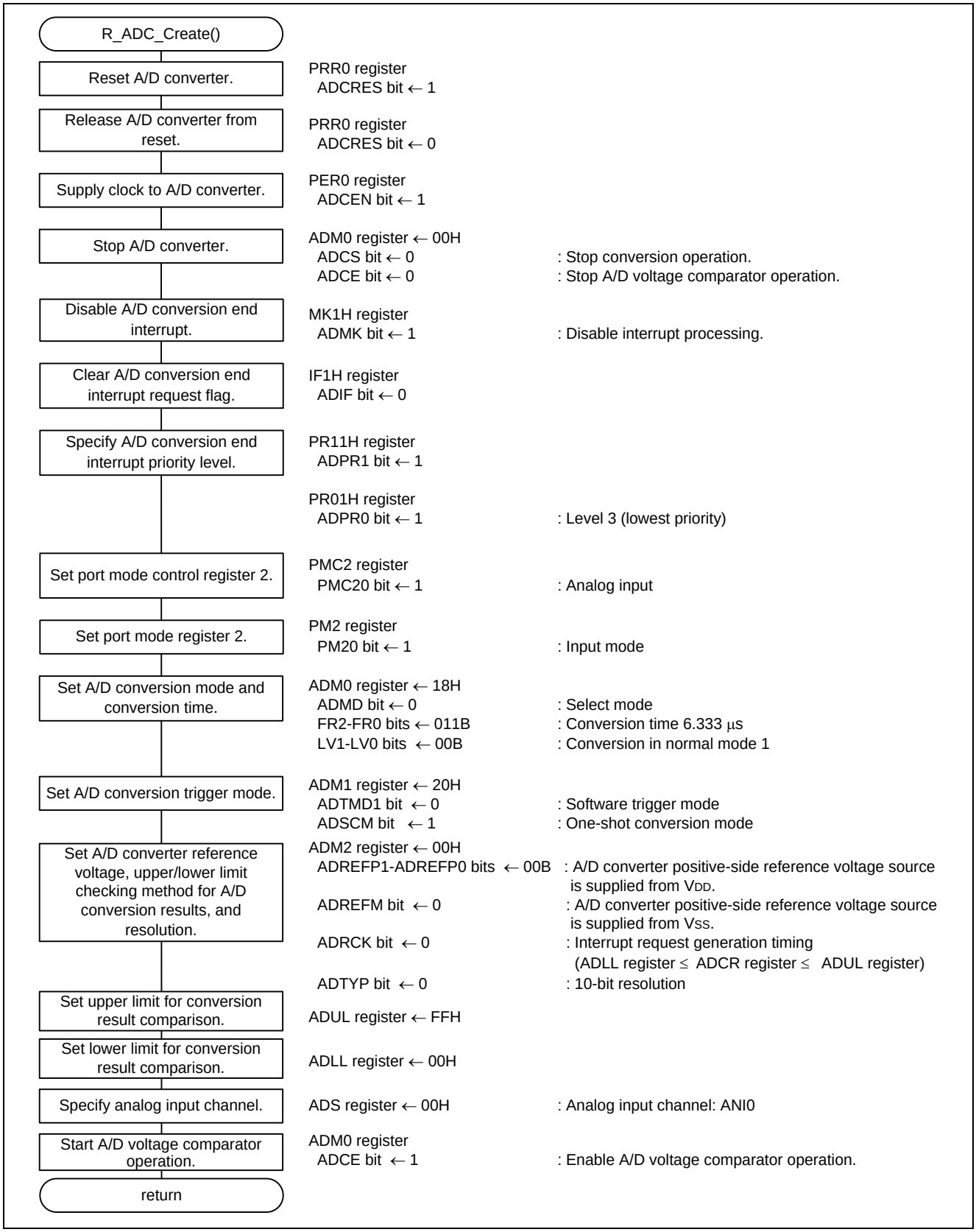


Figure 4.9 Initial Setting of A/D Converter (example of migration from one-shot mode)

Controlling reset of A/D converter

- Peripheral reset control register 0 (PRR0)
  Resets or releases the A/D converter from the reset state.

Symbol	7	6	5	4	3	2	1	0
PRR0	**0**	**IICA1RES**	**ADCRES**	**IICA0RES**	**0**	**SAU0RES**	**0**	**TAU0RES**
Set value	0	×	**0/1**	×	0	×	0	×

Bit 5

ADCRES	Reset control of A/D converter
0	**A/D converter reset release**
1	**A/D converter reset state**

Starting clock supply to A/D converter

- Peripheral enable register 0 (PER0)
  Starts supplying clock to the A/D converter.

Symbol	7	6	5	4	3	2	1	0
PER0	**0**	**IICA1EN**	**ADCEN**	**IICA0EN**	**0**	**SAU0EN**	**0**	**TAU0EN**
Set value	0	×	**1**	×	0	×	0	×

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.Stops input clock supply. • SFR used by the A/D converter cannot be written.
1	**Enables input clock supply.** • SFR used by the A/D converter can be read and written.

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Stopping A/D converter operation

- A/D converter mode register 0 (ADM0)
  Stops the A/D converter.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**0**	×	×	×	×	×	×	**0**

Bit 7

ADCS	A/D conversion operation control
0	**Stops conversion operation.** **[When read]** **Conversion stopped/standby status**
1	Enables conversion operation. [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status

Bit 0

ADCE	A/D voltage comparator operation control
0	**Stops A/D voltage comparator operation.**
1	Enables A/D voltage comparator operation.

Disabling A/D conversion end interrupt

- Interrupt mask flag register 1 (MK1H)
  Disables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Specifying A/D conversion end interrupt priority level

- Priority specification flag register (PR11H, PR01H)
  Specifies level 3 (lowest priority level).

Symbol	7	6	5	4	3	2	1	0
PR11H	**PPR111**	**PPR110**	**PPR19**	**PPR18**	**PPR17**	**KRPR1**	**TMKAPR1**	**ADPR1**
Set value	×	×	×	×	×	×	×	**1**

Symbol	7	6	5	4	3	2	1	0
PR01H	**PPR011**	**PPR010**	**PPR09**	**PPR08**	**PPR07**	**KRPR0**	**TMKAPR0**	**ADPR0**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADPR1	ADPR0	Priority level selection
0	0	Specifies level 0 (high priority level).
0	1	Specifies level 1.
1	0	Specifies level 2.
1	**1**	**Specifes level 3 (low priority level).**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting port mode control register 2

- Port mode control register 2 (PMC2)
  Sets the port mode control register 2 to analog input.

Symbol	7	6	5	4	3	2	1	0
PMC2	**1**	**1**	**1**	**1**	**PMC23**	**PMC22**	**PMC21**	**PMC20**
Set value	1	1	1	1	×	×	×	**1**

Bit 0

PMC20	P20 pin digital I/O/analog input selection
0	Digital I/O (alternate function other than analog input)
1	**Analog input**

Setting port mode register 2

- Port mode register 2 (PM2)
  Sets the port mode register 2 to input mode.

Symbol	7	6	5	4	3	2	1	0
PM2	**1**	**1**	**1**	**1**	**PM23**	**PM22**	**PM21**	**PM20**
Set value	1	1	1	1	×	×	×	**1**

Bit 0

PM20	P20 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion mode and conversion time

- A/D converter mode register 0 (ADM0)
  Sets the A/D conversion mode and conversion time.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	**0**	**0**	**1**	**1**	**0**	**0**	×

Bit 6

ADMD	Specification of A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

Bits 5-1

A/D converter mode register 0 (ADM0)					Mode	Conversion time selection					Conv. clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz	
0	0	0	**0**	**0**	**Normal 1**	Setting prohibited	Setting prohibited	Setting prohibited	76 µs	50.667 µs	$f_{CLK}/64$
0	0	1						76 µs	38 µs	25.333 µs	$f_{CLK}/32$
0	1	0					76 µs	38 µs	19 µs	12.667 µs	$f_{CLK}/16$
0	**1**	**1**					38 µs	19 µs	9.5 µs	**6.333 µs**	**$f_{CLK}/8$**
1	0	0					28.5 µs	14.25 µs	7.125 µs	4.75 µs	$f_{CLK}/6$
1	0	1				95 µs	23.75 µs	11.875 µs	5.938 µs	3.958 µs	$f_{CLK}/5$
1	1	0				76 µs	19 µs	9.5 µs	4.75 µs	3.167 µs	$f_{CLK}/4$
1	1	1				38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited	$f_{CLK}/2$
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	68 µs	45.333 µs	$f_{CLK}/64$
0	0	1						68 µs	34 µs	22.667 µs	$f_{CLK}/32$
0	1	0					68 µs	34 µs	17 µs	11.333 µs	$f_{CLK}/16$
0	1	1					34 µs	17 µs	8.5 µs	5.667 µs	$f_{CLK}/8$
1	0	0					25.5 µs	12.75 µs	6.375 µs	4.25 µs	$f_{CLK}/6$
1	0	1				85 µs	21.25 µs	10.625 µs	5.3125µs	3.542 µs	$f_{CLK}/5$
1	1	0				68 µs	17 µs	8.5 µs	4.25 µs	2.833 µs	$f_{CLK}/4$
1	1	1				34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited	$f_{CLK}/2$

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.

Symbol	7	6	5	4	3	2	1	0
ADM1	**ADTMD1**	**ADTMD0**	**ADSCM**	**0**	**0**	**0**	**ADTRS1**	**ADTRS0**
Set value	**0**	×	**1**	0	0	0	×	×

Bits 7-6

ADTMD1	ADTMD0	Selection of A/D conversion trigger mode
0	**-**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 2 (ADM2)
  Selects the A/D converter reference voltage source, checks the conversion result against the upper-limit/lower-limit value, and selects A/D conversion resolution.

Symbol	7	6	5	4	3	2	1	0
ADM2	**ADREFP1**	**ADREFP0**	**ADREFM**	**0**	**ADRCK**	**AWC**	**0**	**ADTYP**
Set value	**0**	**0**	**0**	0	**0**	×	0	**0**

Bits 7-6

ADREFP1	ADREFP0	Selection of + side reference voltage source of A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from internal reference voltage (1.45 V)
1	1	Setting prohibited
Before rewriting ADREFP1 or ADREFP0 bit, set ADREFP1 and ADREFP0 to 0 and 0. When setting ADREFP1 and ADREFP0 bits to 1 and 0, respectively, this must be configured in accordance with the following procedure: (1) Set ADCE = 0 (2) Set ADREFP1 and ADREFP0 to 1 and 0, respectively. (3) Set ADCE = 1 A wait time (T.B.D) is necessary after (2) and (3). When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output. Be sure to perform A/D conversion while ADISS = 0.		

Bit 5

ADREFM	Selection of – side reference voltage source of A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADRCK	Checking upper limit and lower limit conversion result values
0	**Interrupt signal (INTAD) is generated when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	Interrupt signal (INTAD) is generated when ADCR register < ADLL register, ADUL register < ADCR register.

Bit 0

ADTYP	Selection of A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting upper limit value for conversion result comparison

- Conversion result comparison upper limit setting register (ADUL)
  Sets the upper limit conversion result compare value to FFH.

Symbol	7	6	5	4	3	2	1	0
ADUL	**ADUL7**	**ADUL6**	**ADUL5**	**ADUL4**	**ADUL3**	**ADUL2**	**ADUL1**	**ADUL0**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Setting lower limit values for conversion result comparison

- Conversion result comparison lower limit setting register (ADLL)
  Sets the lower limit conversion result compare value to 00H.

Symbol	7	6	5	4	3	2	1	0
ADLL	**ADLL7**	**ADLL6**	**ADLL5**	**ADLL4**	**ADLL3**	**ADLL2**	**ADLL1**	**ADLL0**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting analog input channel

- Analog input channel specification register (ADS)
  Sets the analog input channel to ANI0.

Symbol	7	6	5	4	3	2	1	0
ADS	**ADISS**	**0**	**0**	**ADS4**	**ADS3**	**ADS2**	**ADS1**	**ADS0**
Set value	**0**	0	0	**0**	**0**	**0**	**0**	**0**

- Select mode (ADMD = 0)

Bits 7, 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**P20/ANI0/AV_{REFP} pin**
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	1	0	0	0	0	ANI16	P01/ANI16 pin
0	1	0	0	0	1	ANI17	P00/ANI17 pin
0	1	0	0	1	0	ANI18	P33/ANI18 pin
0	1	0	0	1	1	ANI19	P32/ANI19 pin
0	1	0	1	0	0	ANI20	P31/ANI20 pin
0	1	0	1	0	1	ANI21	P30/ANI21 pin
0	1	0	1	1	0	ANI22	P56/ANA22 pin
0	1	0	1	1	1	—	PGAOUT(PGA output))
1	0	0	0	0	0	—	Temperature sensor output voltage
1	0	0	0	0	1	—	Internal reference voltage (1.45V)
Other than above						Setting prohibited	

Setting A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  Starts A/D voltage comparator operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation.
1	**Enables A/D voltage comparator operation.**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(6) Main Processing

Figure 4.10 shows the flowchart for the main processing.

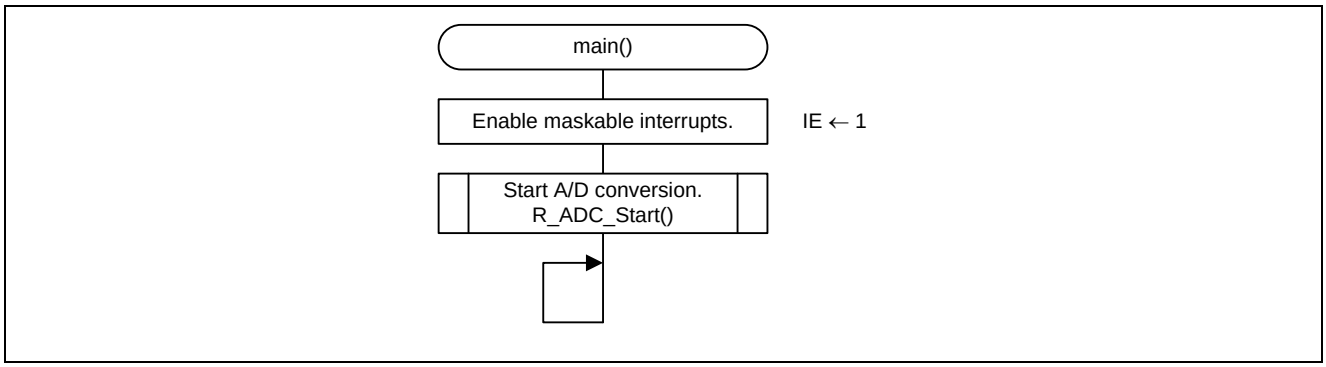


Figure 4.10 Main Processing (example of migration from one-shot mode)

(7) Staring A/D Conversion

Figure 4.11 shows the flowchart for starting A/D conversion.

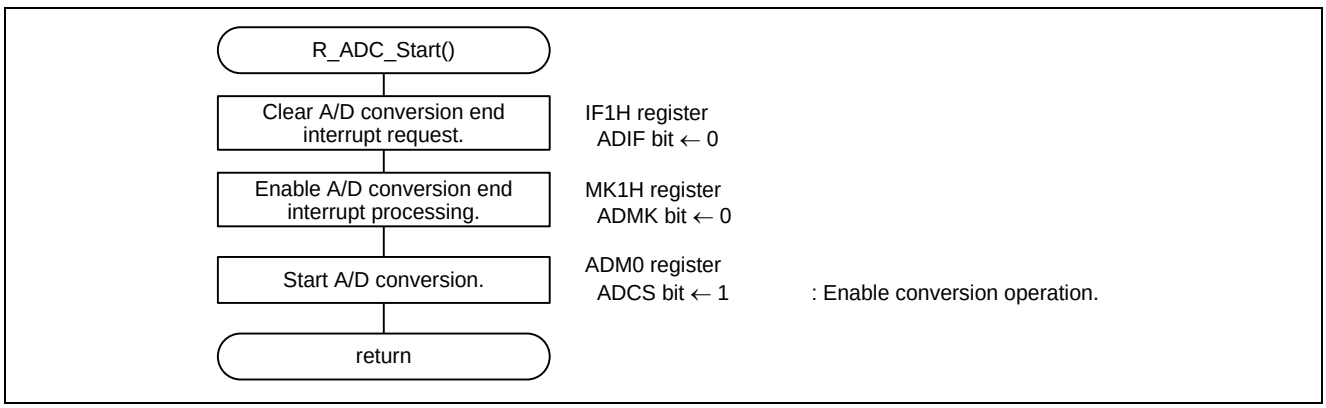


Figure 4.11 Starting A/D Conversion (example of migration from one-shot mode)

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	**Interrupt request flag**
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Enabling A/D conversion end interrupt

- Interrupt mask flag register (MK1H)
  Enables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADMK	**Interrupt servicing control**
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Starting A/D converter

- A/D converter mode register 0 (ADM0)
  Starts A/D conversion operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**1**	×	×	×	×	×	×	×

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	**Enables conversion operation** **[When read]** **While in the software trigger mode: Conversion operation status** **While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(8) A/D conversion end interrupt

Figure 4.12 shows the flowchart for A/D conversion end interrupt processing.

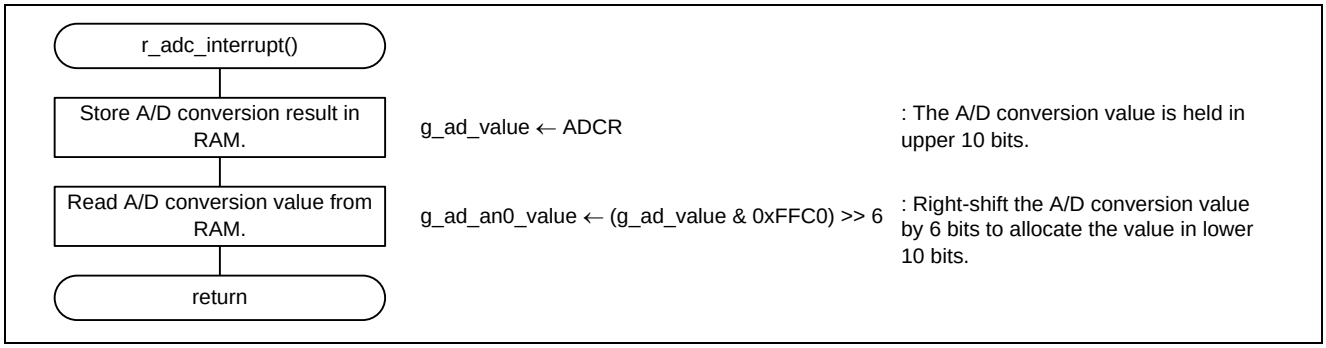


Figure 4.12 A/D Conversion End Interrupt (example of migration from one-shot mode)

4.5 Sample Code

Sample code can be downloaded from the Renesas Electronics website.

4.6 Reference Application Note

- RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: A/D Converter CC-RL (R01AN3059)

4.7 Reference Documents

User's Manual

- RL78/G11 User's Manual: Hardware
  (The latest versions can be downloaded from the Renesas Electronics website.)

- R8C/32C Group Hardware Manual
  (The latest versions can be downloaded from the Renesas Electronics website.)

- Technical Update/Technical News
  (The latest information can be downloaded from the Renesas Electronics website.)

Migration Guide

- Migration to CubeSuite+ Integrated Development Environment for RL78 Family
  (On-chip Debug) - Migration from R8C, M16C to RL78 (R20UT2150)

5. Example of Migration from Repeat Mode 0

5.1 Specifications

To implement R8C/32C repeat mode 0 in the RL78/G11, the AD converter (software trigger, select, sequential conversion mode) is used. The A/D conversion results are stored in the RAM by interrupt processing.

The analog input voltage of one pin selected from the ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, temperature sensor output, and PGAOUT pins is A/D-converted in select mode and sequential conversion mode, and the A/D conversion result values are stored in the RAM assigned by software processing. Specifically, A/D conversion on the selected one pin is sequentially performed; each time A/D conversion ends, the conversion result is stored in the 10-bit A/D conversion result register (ADCR), and an A/D conversion end interrupt request is generated. Finally, the A/D conversion result is transferred from the ADCR register to the RAM by interrupt processing.

Table 5.1 shows the peripheral function used and the purpose of use, and Figure 5.1 shows the operation summary.

Table 5.1 Peripheral Function Used and Purpose of Use (example of migration from repeat mode 0)

Peripheral Function	Purpose of Use
A/D converter	Performs A/D conversion on the analog input voltage.

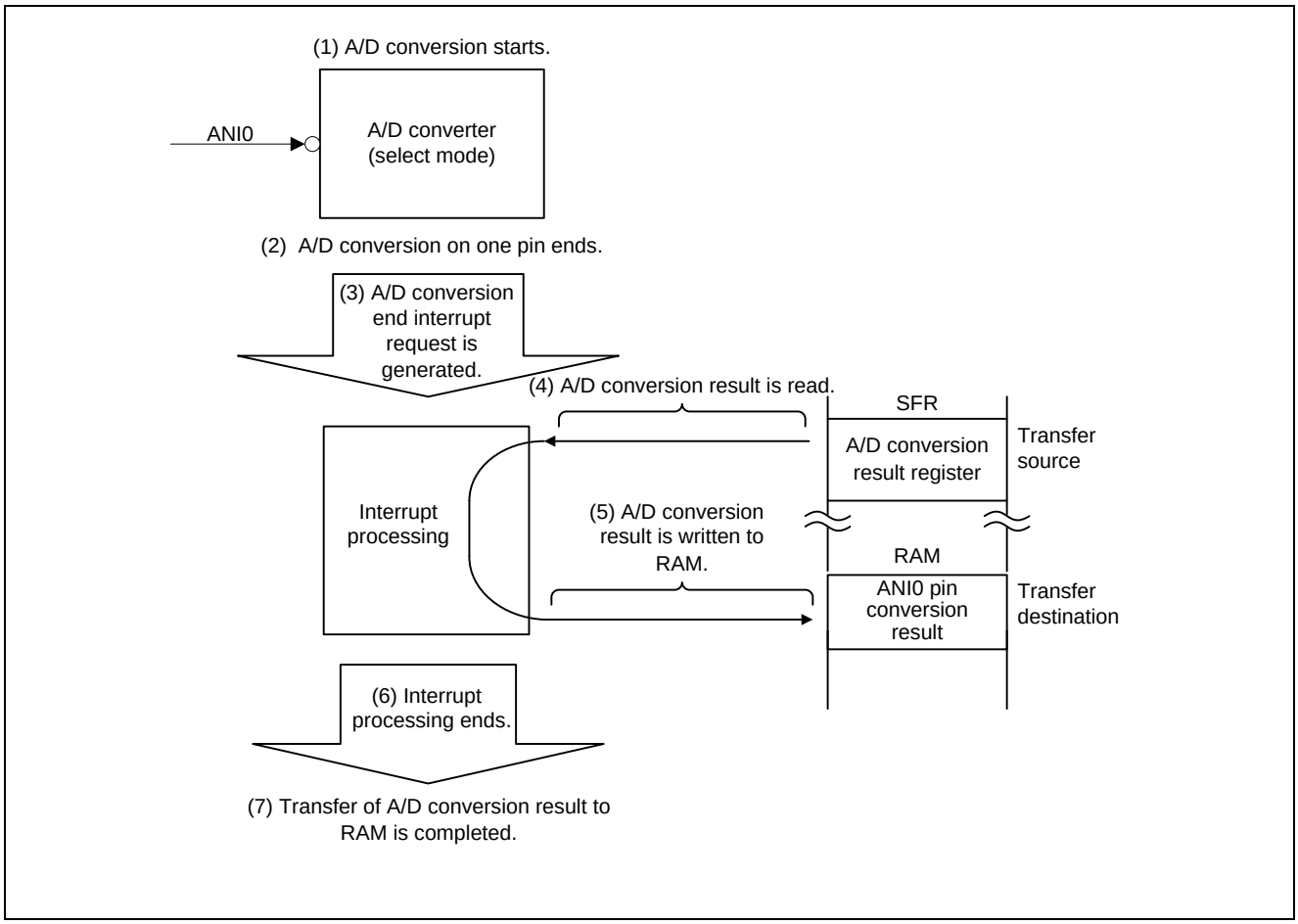


Figure 5.1 Operation Summary (example of migration from repeat mode 0)

5.2 Conditions for Confirming Operations

The sample code operations described in this application note are confirmed under the following conditions.

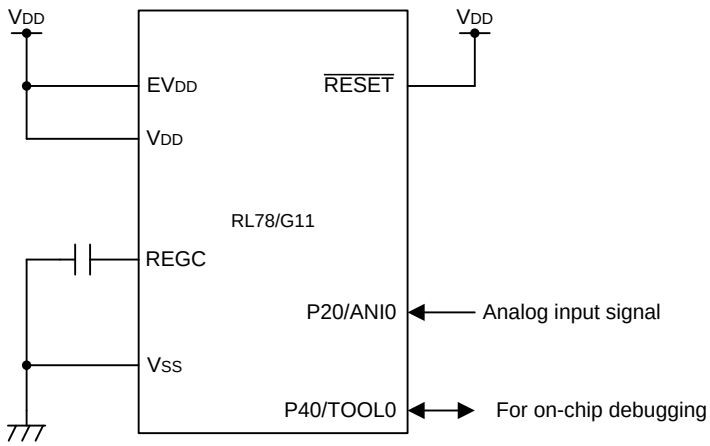
Table 5.2 Conditions for Confirming Operations (example of migration from repeat mode 0)

Item	Description
Microcontroller used	RL78/G11 (R5F1056A)
Operating frequency	• High-speed on-chip oscillator clock (f_{IH}): 24 MHz • CPU/peripheral hardware clock (f_{CLK}): 24 MHz
Operating voltage	5.0 V (can be operated from 3.6 V to 5.5 V) LVD operation (V_{LVD}): Reset mode; rise 3.13 V/fall 3.06 V
Integrated development environment (CS+)	CS+ for CC V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.4.0.015 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.

5.3 Hardware Descriptions

5.3.1 Hardware Configuration Example

Figure 5.2 shows an example of the hardware configuration used for this application.



Note 1: The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied. Input-only ports should be each connected to V_{DD} or V_{SS} via a resistor.

Note 2: Any pin whose name begins with EV_{DD} should be connected to V_{DD}.

Note 3: V_{DD} should be equal to or greater than the reset-release voltage (V_{LVD}) specified for the LVD.

Figure 5.2 Hardware Configuration (example of migration from repeat mode 0)

5.3.2 List of Pins Used

Table 5.3 lists the pin used and its function.

Table 5.3 Pin Used and Its Function (example of migration from repeat mode 0)

Pin Name	I/O	Function
P20/ANI0	Input	A/D converter input (ANI0)

5.4 Software Descriptions

5.4.1 Operation Summary

With this sample program, the A/D conversion on one pin is performed in select mode, and the conversion result is stored in the RAM by A/D conversion end interrupt processing. By setting sequential conversion mode, A/D conversion is repeated.

Upon completion of the A/D conversion on the ANI0 pin, an A/D conversion end interrupt is generated. In interrupt processing, the A/D conversion result is transferred from the transfer source addresses (ADCR register (FFF1EH, FFF1FH)) to the transfer destination addresses (variable g_ad_value (FF900H to FF901H)). In addition, the A/D conversion result transferred is relocated in the lower 10 bits before being stored in the buffer for storing the A/D conversion results of ANI0 (variable g_ad_an0_value).

Table 5.4 shows the A/D converter settings.

Table 5.4 A/D Converter Settings (example of migration from repeat mode 0)

Item to be Set	Settings
Conversion clock frequency (f_{AD})	f_{CLK}/8
A/D conversion mode	• A/D conversion trigger mode: Software trigger • A/D conversion channel selection mode: Select mode • A/D conversion operation mode: Sequential conversion mode
Resolution	10 bits
Analog input channel	ANI0
A/D conversion result comparison upper limit (ADUL register)	FFH
A/D conversion result comparison lower limit (ADLL register)	00H
Upper and lower limit conversion result checking	INTAD generated when ADLL register ≤ ADCR register ≤ ADUL register

(1) The initial setting is made for the A/D converter.
(2) The ADCS bit in the ADM0 register is set to 1 (conversion enabled) to start A/D conversion.
(3) Upon completion of the A/D conversion on the ANI0 pin, an A/D conversion end interrupt is generated.
(4) In interrupt processing, the A/D conversion result is read from the ADCR register and transferred to the RAM (variable g_ad_value).
Also, the A/D conversion result (variable g_ad_value) is shifted to the right by 6 bits (relocated in the lower 10 bits) and stored in the variable g_ad_an0_value.
(5) After this, A/D conversion is sequentially performed, where steps (3) and (4) are repeated.

Figure 5.3 shows the A/D conversion timing and Figure 5.4 shows the relationship between the ADCR register and RAM.

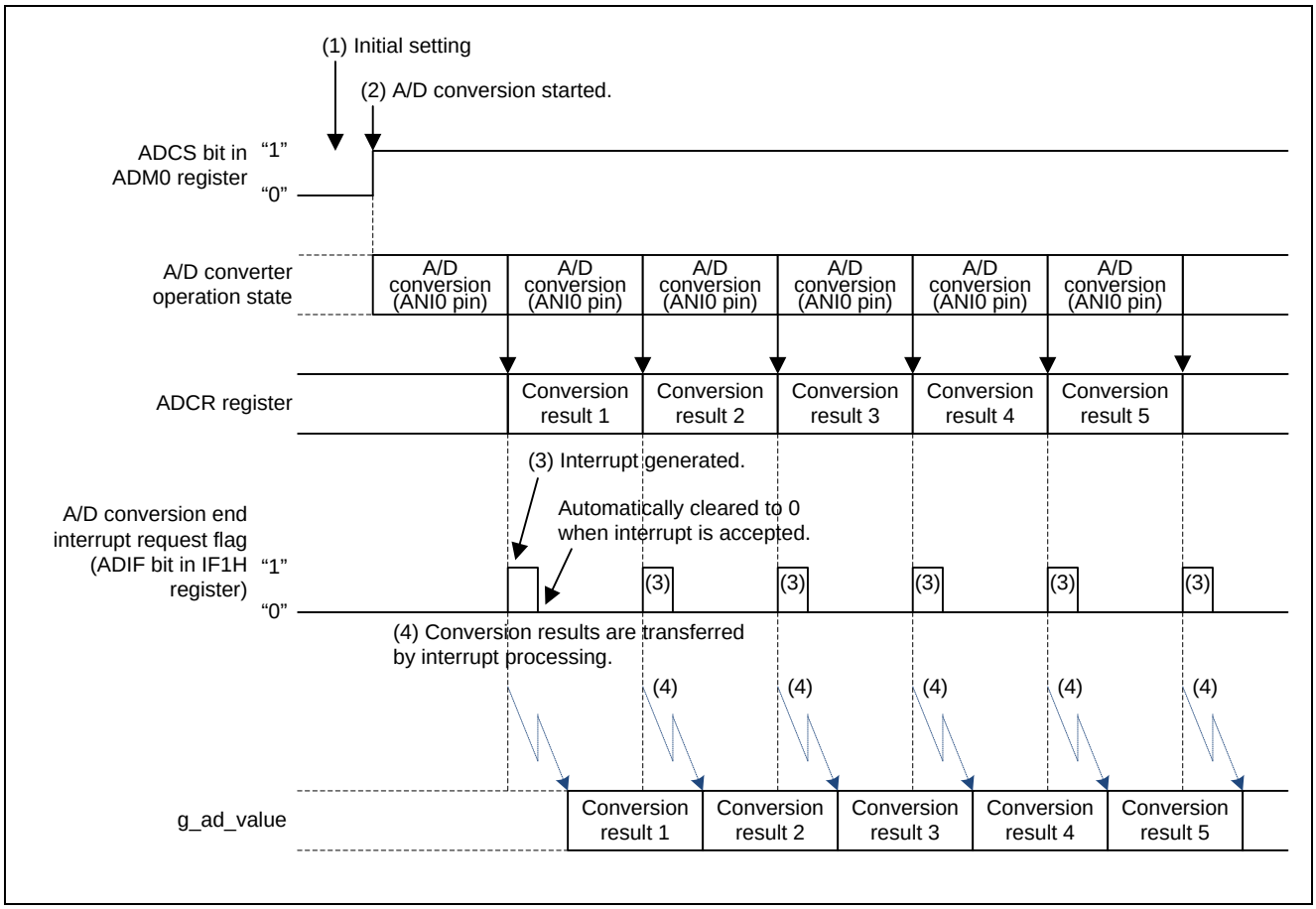


Figure 5.3 A/D Conversion Timing (example of migration from repeat mode 0)

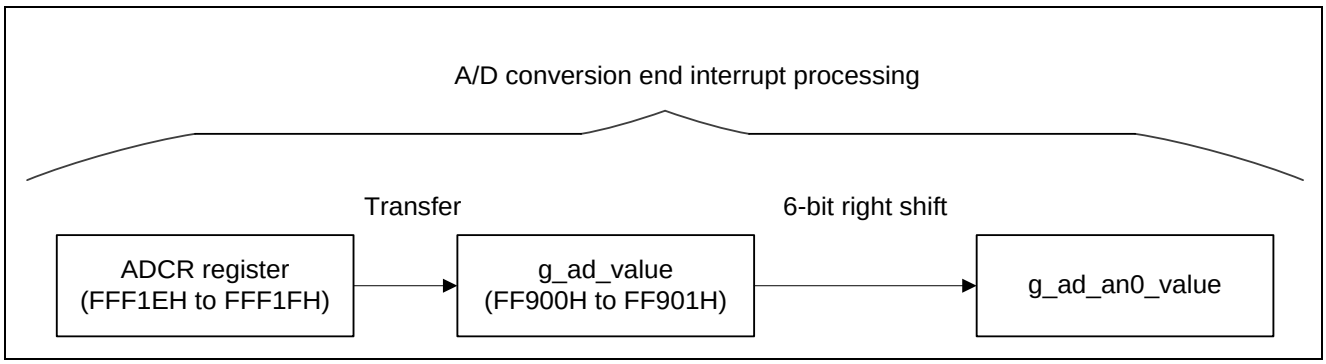


Figure 5.4 Relationship between ADCR Register and RAM (example of migration from repeat mode 0)

5.4.2 List of Option Byte Settings

Table 5.5 lists option byte settings.

Table 5.5 Option Byte Settings (example of migration from repeat mode 0)

Address	Setting	Contents
000C0H/010C0H	01101110B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H/010C1H	00110011B	LVD reset mode Detection voltage: rise 3.13 V/fall 3.06 V
000C2H/010C2H	11100000B	HS mode High-speed on-chip oscillator clock frequency: 24 MHz
000C3H/010C3H	10000100B	On-chip debugging is enabled.

5.4.3 List of Constants

Table 5.6 lists the constant used in the sample code.

Table 5.6 Constant Used in Sample Code (example of migration from repeat mode 0)

Constant Name	Setting	Contents
AD_RESULT_ADDR	0FF900H	Transfer destination address of A/D conversion result

5.4.4 List of Variables

Table 5.7 lists the global variables.

Table 5.7 Global Variables (example of migration from repeat mode 0)

Type	Variable Name	Contents	Function Used
uint16_t __near	g_ad_value	Buffer for storing A/D conversion results	r_adc_interrupt
uint16_t	g_ad_an0_value	Buffer for storing A/D conversion result of ANI0	r_adc_interrupt

5.4.5 Functions

Table 5.8 lists the Functions.

Table 5.8 Functions (example of migration from repeat mode 0)

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	CPU initial setting
R_ADC_Create	Initial setting of A/D converter
main	Main processing
R_ADC_Start	A/D conversion start
r_adc_interrupt	A/D conversion interrupt

5.4.6 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	CPU initial setting
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_ADC_Create	
Outline	Initial setting of A/D converter
Header	None
Declaration	void R_ADC_Create(void)
Description	Perform the initial setting to use the A/D converter in software trigger mode, select mode, and sequential conversion mode.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_ADC_Start	
Outline	A/D conversion start
Header	None
Declaration	void R_ADC_Start(void)
Description	Perform A/D conversion.
Argument	None
Return Value	None

r_adc_interrupt	
Outline	A/D conversion interrupt
Header	None
Declaration	static void __near r_adc_interrupt(void)
Description	Perform an A/D conversion end interrupt service routine.
Argument	None
Return Value	None

5.4.7 Flowcharts

(1) Overall Flowchart

Figure 5.5 shows the Overall Flowchart.

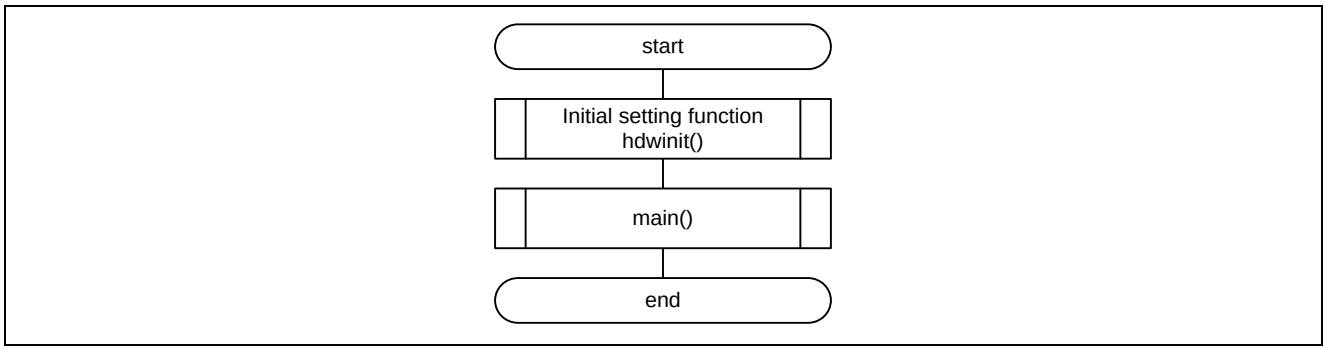


Figure 5.5 Overall Flowchart (example of migration from repeat mode 0)

(2) Initial Setting

Figure 5.6 shows the Initial Setting.

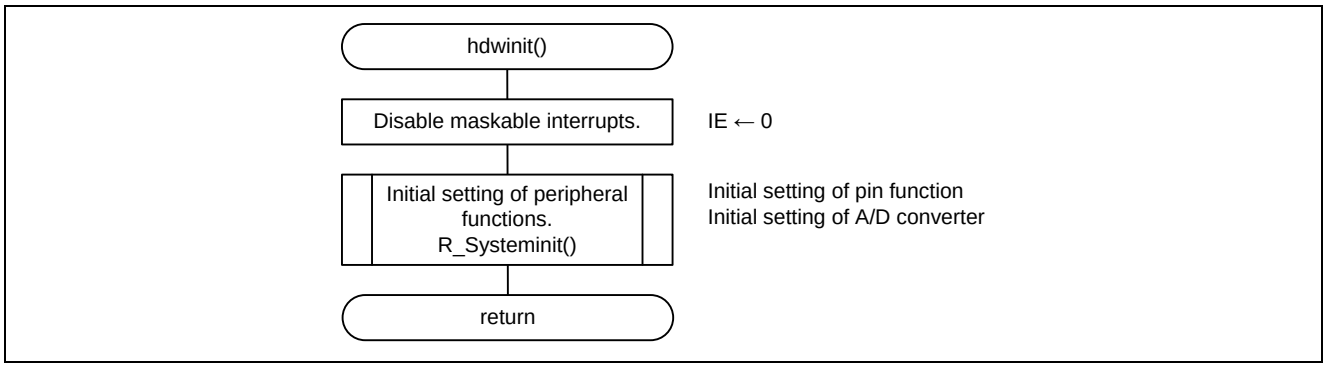


Figure 5.6 Initial Setting (example of migration from repeat mode 0)

(3) Initial Setting of Peripheral Functions

Figure 5.7 shows the initial setting of peripheral functions.

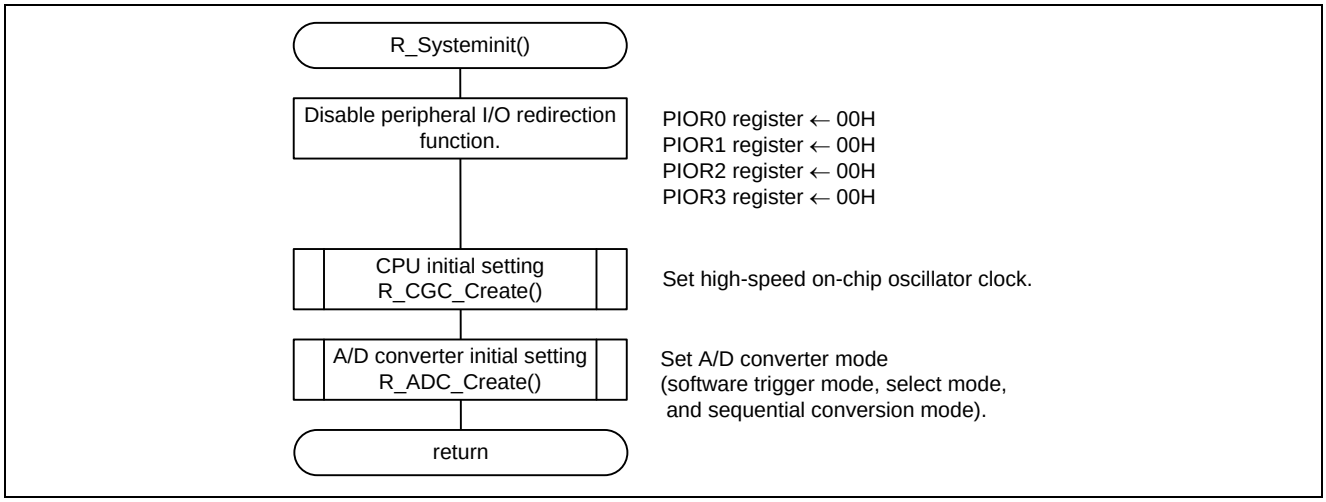


Figure 5.7 Initial Setting of Peripheral Functions (example of migration from repeat mode 0)

(4) Initial Setting of CPU

Figure 5.8 shows the initial setting of the CPU.

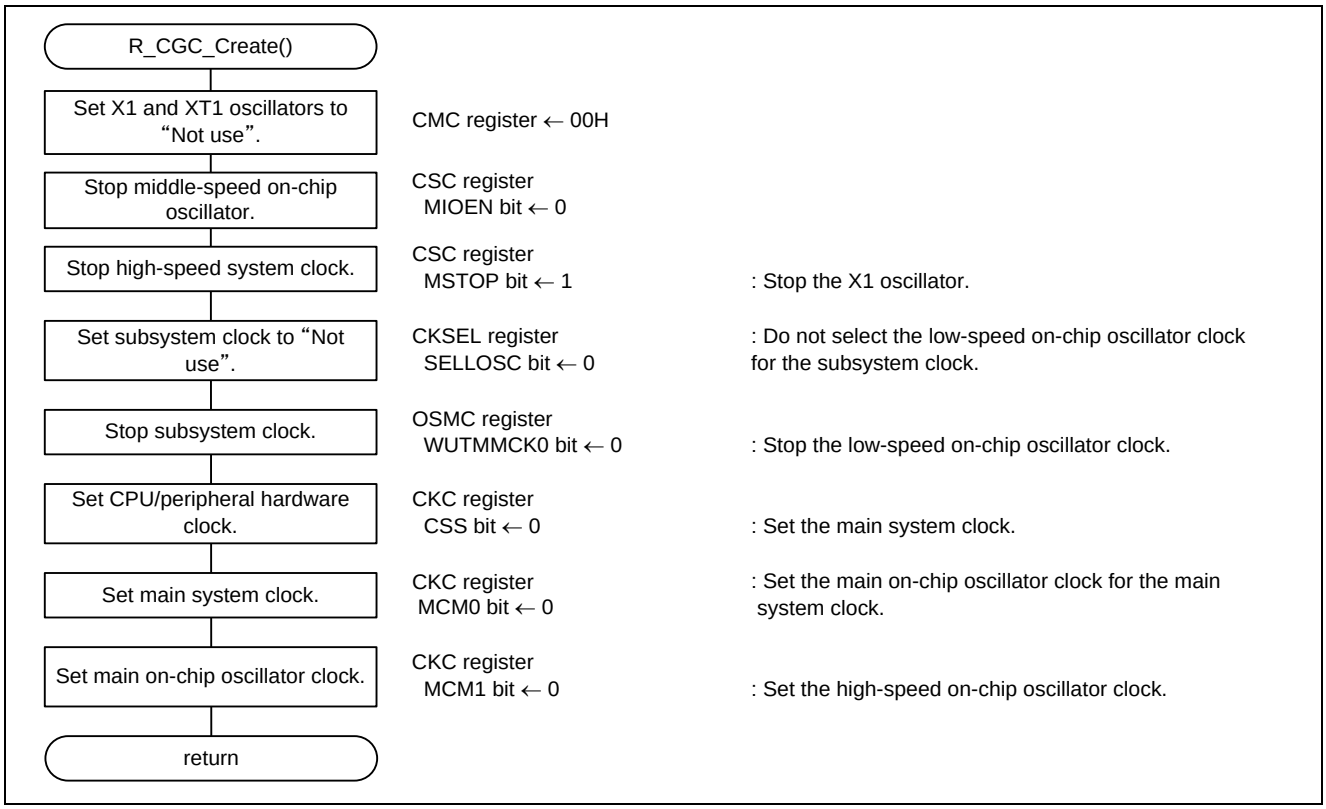


Figure 5.8 Initial Setting of CPU (example of migration from repeat mode 0)

(5) Initial Setting of A/D Converter

Figure 5.9 shows the initial setting of the A/D converter.

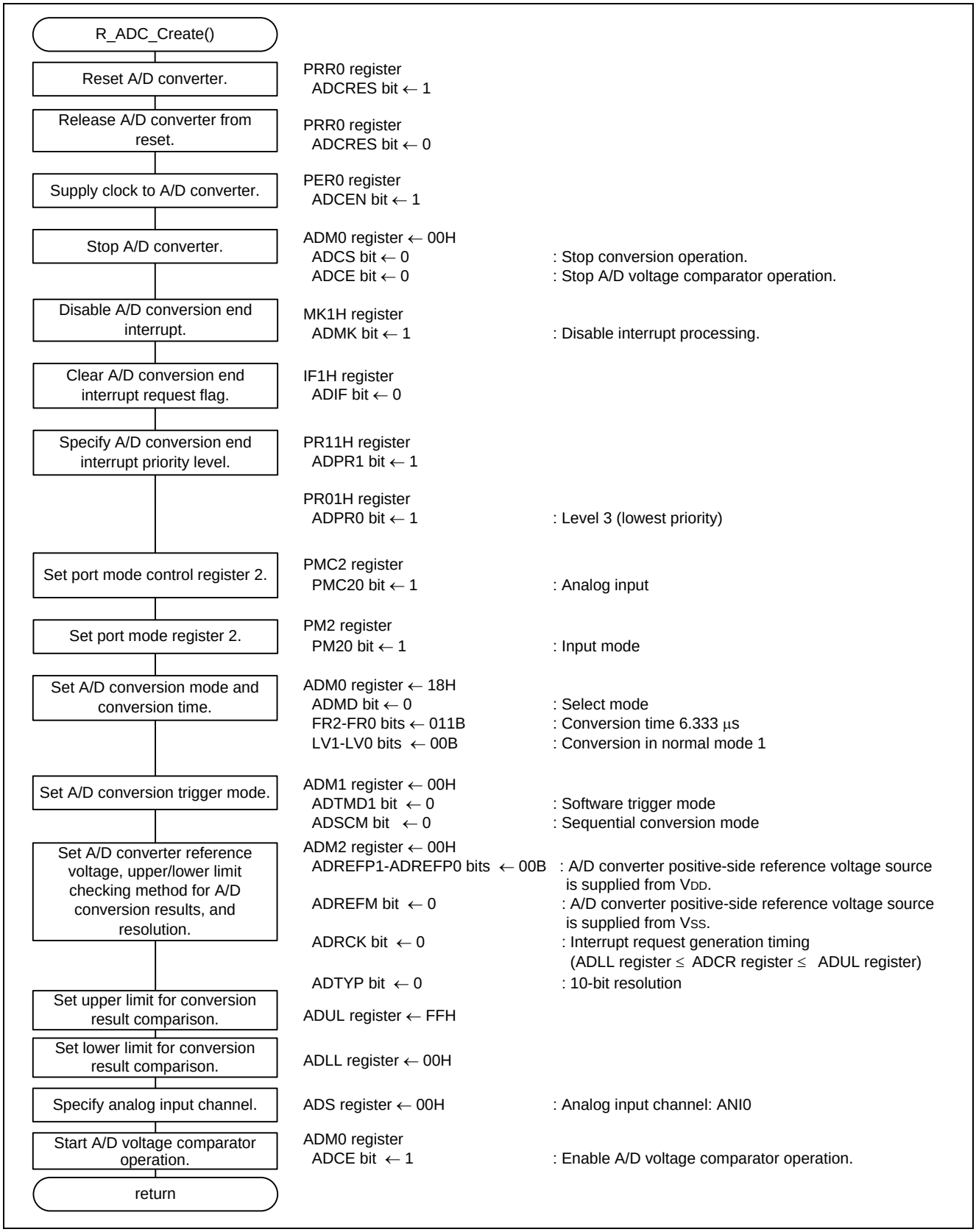


Figure 5.9 Initial Setting of A/D Converter (example of migration from repeat mode 0)

Controlling reset of A/D converter

- Peripheral reset control register 0 (PRR0)
  Resets or releases the A/D converter from the reset state.

Symbol	7	6	5	4	3	2	1	0
PRR0	**0**	**IICA1RES**	**ADCRES**	**IICA0RES**	**0**	**SAU0RES**	**0**	**TAU0RES**
Set value	0	×	**0/1**	×	0	×	0	×

Bit 5

ADCRES	Reset control of A/D converter
0	**A/D converter reset release**
1	**A/D converter reset state**

Starting clock supply to A/D converter

- Peripheral enable register 0 (PER0)
  Starts supplying clock to the A/D converter.

Symbol	7	6	5	4	3	2	1	0
PER0	**0**	**IICA1EN**	**ADCEN**	**IICA0EN**	**0**	**SAU0EN**	**0**	**TAU0EN**
Set value	0	×	**1**	×	0	×	0	×

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.Stops input clock supply. • SFR used by the A/D converter cannot be written.
1	**Enables input clock supply.** • SFR used by the A/D converter can be read and written.

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Stopping A/D converter operation

- A/D converter mode register 0 (ADM0)
  Stops the A/D converter.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**0**	×	×	×	×	×	×	**0**

Bit 7

ADCS	A/D conversion operation control
0	**Stops conversion operation.** **[When read]** **Conversion stopped/standby status**
1	Enables conversion operation. [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status

Bit 0

ADCE	A/D voltage comparator operation control
0	**Stops A/D voltage comparator operation.**
1	Enables A/D voltage comparator operation.

Disabling A/D conversion end interrupt

- Interrupt mask flag register 1 (MK1H)
  Disables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Specifying A/D conversion end interrupt priority level

- Priority specification flag register (PR11H, PR01H)
  Specifies level 3 (lowest priority level).

Symbol	7	6	5	4	3	2	1	0
PR11H	**PPR111**	**PPR110**	**PPR19**	**PPR18**	**PPR17**	**KRPR1**	**TMKAPR1**	**ADPR1**
Set value	×	×	×	×	×	×	×	**1**

Symbol	7	6	5	4	3	2	1	0
PR01H	**PPR011**	**PPR010**	**PPR09**	**PPR08**	**PPR07**	**KRPR0**	**TMKAPR0**	**ADPR0**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADPR1	ADPR0	Priority level selection
0	0	Specifies level 0 (high priority level).
0	1	Specifies level 1.
1	0	Specifies level 2.
1	**1**	**Specifes level 3 (low priority level).**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting port mode control register 2

- Port mode control register 2 (PMC2)
  Sets the port mode control register 2 to analog input.

Symbol	7	6	5	4	3	2	1	0
PMC2	**1**	**1**	**1**	**1**	**PMC23**	**PMC22**	**PMC21**	**PMC20**
Set value	1	1	1	1	×	×	×	**1**

Bit 0

PMC20	P20 pin digital I/O/analog input selection
0	Digital I/O (alternate function other than analog input)
1	**Analog input**

Setting port mode register 2

- Port mode register 2 (PM2)
  Sets the port mode register 2 to input mode.

Symbol	7	6	5	4	3	2	1	0
PM2	**1**	**1**	**1**	**1**	**PM23**	**PM22**	**PM21**	**PM20**
Set value	1	1	1	1	×	×	×	**1**

Bit 0

PM20	P20 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion mode and conversion time

- A/D converter mode register 0 (ADM0)
  Sets the A/D conversion mode and conversion time.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	**0**	**0**	**1**	**1**	**0**	**0**	×

Bit 6

ADMD	Specification of A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

Bits 5-1

A/D converter mode register 0 (ADM0)					Mode	Conversion time selection					Conv. clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz	
0	0	0	**0**	**0**	**Normal 1**	Setting prohibited	Setting prohibited	Setting prohibited	76 µs	50.667 µs	f_{CLK}/64
0	0	1						76 µs	38 µs	25.333 µs	f_{CLK}/32
0	1	0					76 µs	38 µs	19 µs	12.667 µs	f_{CLK}/16
0	**1**	**1**					38 µs	19 µs	9.5 µs	**6.333 µs**	**f_{CLK}/8**
1	0	0					28.5 µs	14.25 µs	7.125 µs	4.75 µs	f_{CLK}/6
1	0	1				95 µs	23.75 µs	11.875 µs	5.938 µs	3.958 µs	f_{CLK}/5
1	1	0				76 µs	19 µs	9.5 µs	4.75 µs	3.167 µs	f_{CLK}/4
1	1	1				38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	68 µs	45.333 µs	f_{CLK}/64
0	0	1						68 µs	34 µs	22.667 µs	f_{CLK}/32
0	1	0					68 µs	34 µs	17 µs	11.333 µs	f_{CLK}/16
0	1	1					34 µs	17 µs	8.5 µs	5.667 µs	f_{CLK}/8
1	0	0					25.5 µs	12.75 µs	6.375 µs	4.25 µs	f_{CLK}/6
1	0	1				85 µs	21.25 µs	10.625 µs	5.3125µs	3.542 µs	f_{CLK}/5
1	1	0				68 µs	17 µs	8.5 µs	4.25 µs	2.833 µs	f_{CLK}/4
1	1	1				34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited	f_{CLK}/2

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.

Symbol	7	6	5	4	3	2	1	0
ADM1	**ADTMD1**	**ADTMD0**	**ADSCM**	**0**	**0**	**0**	**ADTRS1**	**ADTRS0**
Set value	**0**	×	**0**	0	0	0	×	×

Bits 7-6

ADTMD1	ADTMD0	Selection of A/D conversion trigger mode
0	**-**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of A/D conversion mode
0	**Sequential conversion mode**
1	One-shot conversion mode

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 2 (ADM2)
  Selects the A/D converter reference voltage source, checks the conversion result against the upper-limit/lower-limit value, and selects A/D conversion resolution.

Symbol	7	6	5	4	3	2	1	0
ADM2	**ADREFP1**	**ADREFP0**	**ADREFM**	**0**	**ADRCK**	**AWC**	**0**	**ADTYP**
Set value	**0**	**0**	**0**	0	**0**	×	0	**0**

Bits 7-6

ADREFP1	ADREFP0	Selection of + side reference voltage source of A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from internal reference voltage (1.45 V)
1	1	Setting prohibited
Before rewriting ADREFP1 or ADREFP0 bit, set ADREFP1 and ADREFP0 to 0 and 0. When setting ADREFP1 and ADREFP0 bits to 1 and 0, respectively, this must be configured in accordance with the following procedure: (1) Set ADCE = 0 (2) Set ADREFP1 and ADREFP0 to 1 and 0, respectively. (3) Set ADCE = 1 A wait time (T.B.D) is necessary after (2) and (3). When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output. Be sure to perform A/D conversion while ADISS = 0.		

Bit 5

ADREFM	Selection of – side reference voltage source of A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADRCK	Checking upper limit and lower limit conversion result values
0	**Interrupt signal (INTAD) is generated when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	Interrupt signal (INTAD) is generated when ADCR register < ADLL register, ADUL register < ADCR register.

Bit 0

ADTYP	Selection of A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting upper limit value for conversion result comparison

- Conversion result comparison upper limit setting register (ADUL)
  Sets the upper limit conversion result compare value to FFH.

Symbol	7	6	5	4	3	2	1	0
ADUL	**ADUL7**	**ADUL6**	**ADUL5**	**ADUL4**	**ADUL3**	**ADUL2**	**ADUL1**	**ADUL0**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Setting lower limit values for conversion result comparison

- Conversion result comparison lower limit setting register (ADLL)
  Sets the lower limit conversion result compare value to 00H.

Symbol	7	6	5	4	3	2	1	0
ADLL	**ADLL7**	**ADLL6**	**ADLL5**	**ADLL4**	**ADLL3**	**ADLL2**	**ADLL1**	**ADLL0**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting analog input channel

- Analog input channel specification register (ADS)
  Sets the analog input channel to ANI0.

Symbol	7	6	5	4	3	2	1	0
ADS	**ADISS**	**0**	**0**	**ADS4**	**ADS3**	**ADS2**	**ADS1**	**ADS0**
Set value	**0**	0	0	**0**	**0**	**0**	**0**	**0**

- Select mode (ADMD = 0)

Bits 7, 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**P20/ANI0/AV_{REFP} pin**
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	1	0	0	0	0	ANI16	P01/ANI16 pin
0	1	0	0	0	1	ANI17	P00/ANI17 pin
0	1	0	0	1	0	ANI18	P33/ANI18 pin
0	1	0	0	1	1	ANI19	P32/ANI19 pin
0	1	0	1	0	0	ANI20	P31/ANI20 pin
0	1	0	1	0	1	ANI21	P30/ANI21 pin
0	1	0	1	1	0	ANI22	P56/ANA22 pin
0	1	0	1	1	1	—	PGAOUT(PGA output))
1	0	0	0	0	0	—	Temperature sensor output voltage
1	0	0	0	0	1	—	Internal reference voltage (1.45V)
Other than above						Setting prohibited	

Setting A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  Starts A/D voltage comparator operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation.
1	**Enables A/D voltage comparator operation.**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(6) Main Processing

Figure 5.10 shows the flowchart for the main processing.

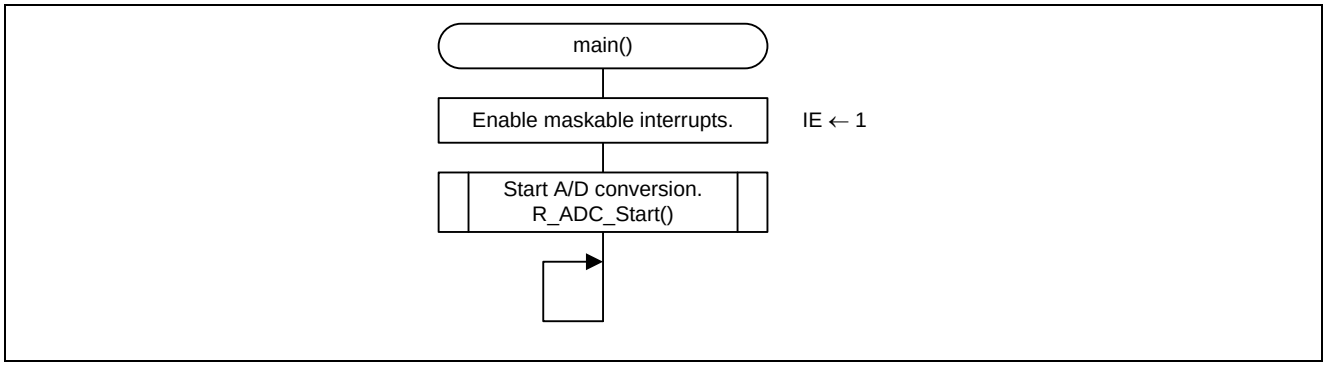


Figure 5.10 Main Processing (example of migration from repeat mode 0)

(7) Staring A/D Conversion

Figure 5.11 shows the flowchart for starting A/D conversion.

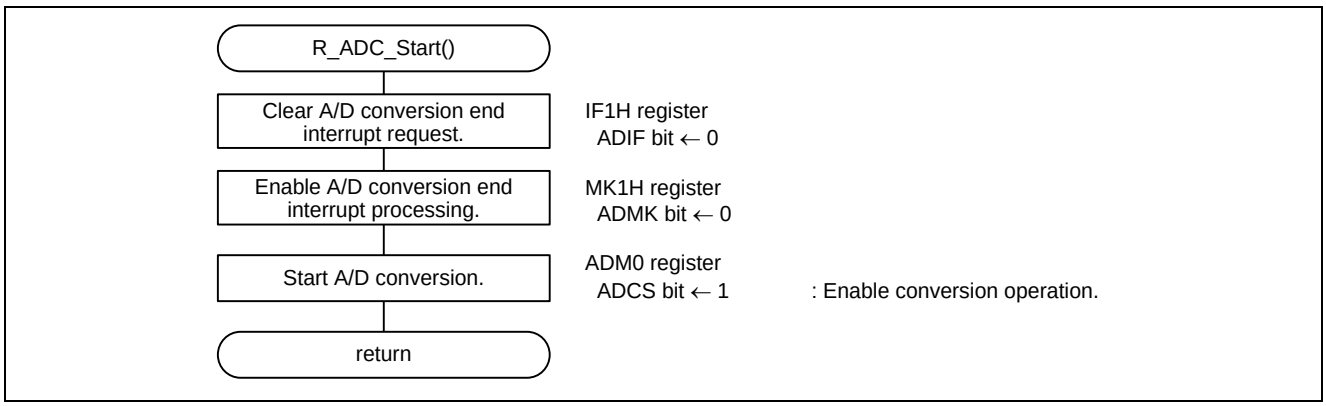


Figure 5.11 Starting A/D Conversion (example of migration from repeat mode 0)

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	**Interrupt request flag**
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Enabling A/D conversion end interrupt

- Interrupt mask flag register (MK1H)
  Enables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADMK	**Interrupt servicing control**
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Starting A/D converter

- A/D converter mode register 0 (ADM0)
  Starts A/D conversion operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**1**	×	×	×	×	×	×	×

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	**Enables conversion operation** **[When read]** **While in the software trigger mode: Conversion operation status** **While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(8) A/D conversion end interrupt

Figure 5.12 shows the flowchart for A/D conversion end interrupt processing.

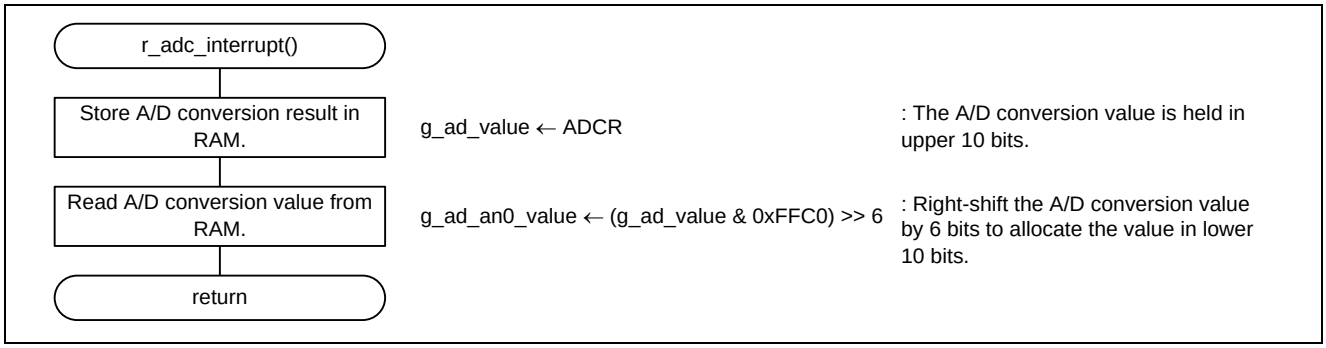


Figure 5.12 A/D Conversion End Interrupt (example of migration from repeat mode 0)

5.5 Sample Code

Sample code can be downloaded from the Renesas Electronics website.

5.6 Reference Application Note

- RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: A/D Converter CC-RL (R01AN3059)

- RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) CC-RL (R01AN2581)

5.7 Reference Documents

User's Manual

- RL78/G11 User's Manual: Hardware
  (The latest versions can be downloaded from the Renesas Electronics website.)

- R8C/32C Group Hardware Manual
  (The latest versions can be downloaded from the Renesas Electronics website.)

- Technical Update/Technical News
  (The latest information can be downloaded from the Renesas Electronics website.)

Migration Guide

- Migration to CubeSuite+ Integrated Development Environment for RL78 Family
  (On-chip Debug) - Migration from R8C, M16C to RL78 (R20UT2150)

6. Example of Migration from Repeat Mode 1

6.1 Specifications

To implement R8C/32C repeat mode 1 in the RL78/G11, the AD converter (software trigger, select, sequential conversion mode) and DTC transfer (repeat mode) are used.

The analog input voltage of one pin selected from ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, temperature sensor output, and PGAOUT pins is A/D-converted in select mode and sequential conversion mode, and the A/D conversion result values are stored in the RAM corresponding to the number of A/D conversions (one to eight) by DTC transfer. Specifically, A/D conversion on the selected one pin is sequentially performed; each time A/D conversion ends, the conversion result is stored in the 10-bit A/D conversion result register (ADCR), and an A/D conversion end interrupt signal is generated. In response to the interrupt signal, the DTC is activated, and the A/D conversion result is transferred from the ADCR register to the RAM. When A/D conversion and DTC transfer are performed eight times, an A/D conversion end interrupt request is generated.

Table 6.1 shows the peripheral functions used and the purpose of use, and Figure 6.1 shows the operation summary.

Table 6.1 Peripheral Functions Used and Purpose of Use (example of migration from repeat mode 1)

Peripheral Function	Purpose of Use
A/D converter	Performs A/D conversion on the analog input voltage.
DTC	Transfers A/D conversion results to RAM.

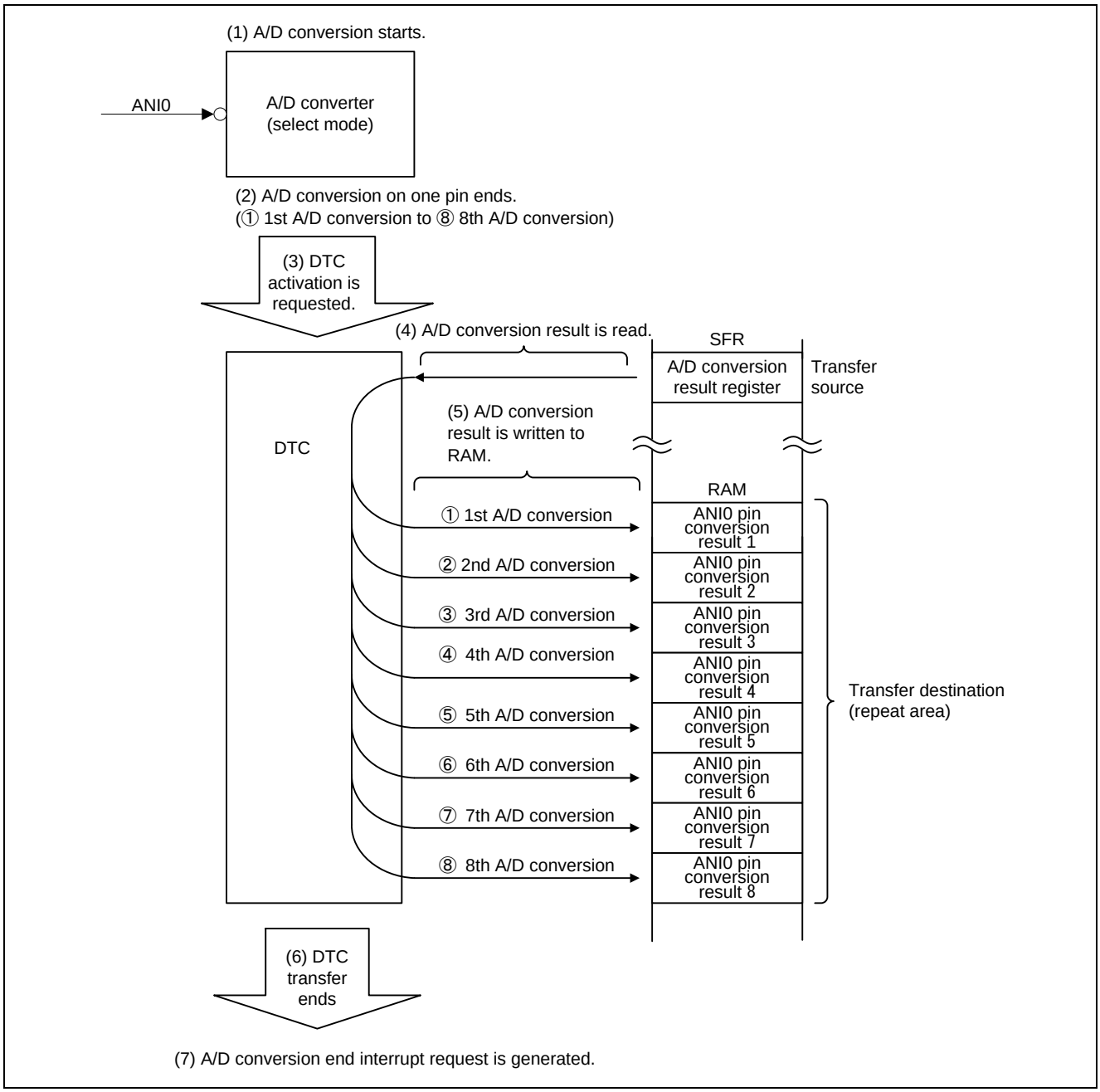


Figure 6.1 Operation Summary (example of migration from repeat mode 1)

6.2 Conditions for Confirming Operations

The sample code operations described in this application note are confirmed under the following conditions.

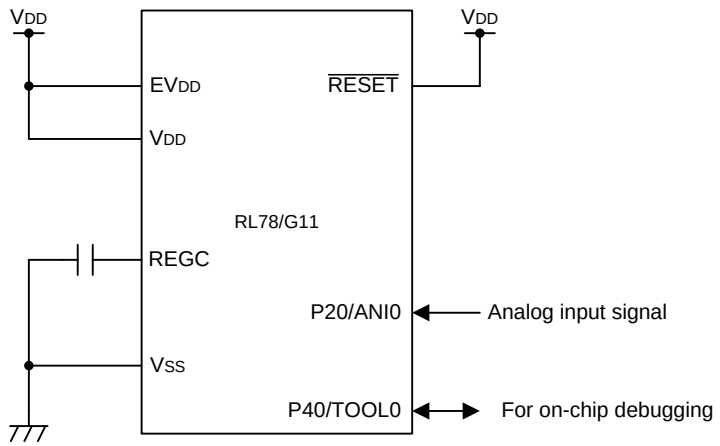
Table 6.2 Conditions for Confirming Operations (example of migration from repeat mode 1)

Item	Description
Microcontroller used	RL78/G11 (R5F1056A)
Operating frequency	• High-speed on-chip oscillator clock (f_{IH}): 24 MHz • CPU/peripheral hardware clock (f_{CLK}): 24 MHz
Operating voltage	5.0 V (can be operated from 3.6 V to 5.5 V) LVD operation (V_{LVD}): Reset mode; rise 3.13 V/fall 3.06 V
Integrated development environment (CS+)	CS+ for CC V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.4.0.015 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.

6.3 Hardware Descriptions

6.3.1 Hardware Configuration Example

Figure 6.2 shows an example of the hardware configuration used for this application.



Note 1: The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied. Input-only ports should be each connected to V_{DD} or V_{SS} via a resistor.

Note 2: Any pin whose name begins with EV_{DD} should be connected to V_{DD}.

Note 3: V_{DD} should be equal to or greater than the reset-release voltage (V_{LVD}) specified for the LVD.

Figure 6.2 Hardware Configuration (example of migration from repeat mode 1)

6.3.2 List of Pins Used

Table 6.3 lists the pin used and its function.

Table 6.3 Pin Used and Its Function (example of migration from repeat mode 1)

Pin Name	I/O	Function
P20/ANI0	Input	A/D converter input (ANI0)

6.4 Software Descriptions

6.4.1 Operation Summary

With this sample program, the A/D conversion on one pin is performed in select mode, and the conversion results are stored in the RAM by DTC transfer. By setting sequential conversion mode, A/D conversion is repeated.

Upon completion of the first A/D conversion on the ANI0 pin, the first DTC transfer is performed from the transfer source addresses (ADCR register (FFF1EH, FFF1FH)) to the transfer destination addresses (g_ad_value[0] (FF900H to FF901H)). Upon completion of the second A/D conversion on the ANI0 pin, the second DTC transfer is performed to g_ad_value[1] (FF902H to FF903H) since the transfer destination is set as the repeat area. Similarly, the third to eighth A/D conversion results are DTC-transferred. Upon completion of the eighth transfer, an A/D conversion end interrupt is generated.

In interrupt processing, the A/D conversion results corresponding to the number of A/D conversion times (1 to 8) stored in the array g_ad_value[] (FF900H to FF915H) are relocated in the lower 10 bits before being stored in the buffer for storing the A/D conversion results (variable g_ad _an0_value1 to g_ad_an0_value8).

After this, the above sequence is repeated to update the acquired A/D conversion results.

Table 6.4 shows the A/D converter settings and Table 6.5 shows the DTC settings.

Table 6.4 A/D Converter Settings (example of migration from repeat mode 1)

Item to be Set	Settings
Conversion clock frequency (f_{AD})	$f_{CLK}/8$
A/D conversion mode	• A/D conversion trigger mode: Software trigger • A/D conversion channel selection mode: Select mode • A/D conversion operation mode: Sequential conversion mode
Resolution	10 bits
Analog input channel	ANI0
A/D conversion result comparison upper limit (ADUL register)	FFH
A/D conversion result comparison lower limit (ADLL register)	00H
Upper and lower limit conversion result checking	INTAD generated when ADLL register ≤ ADCR register ≤ ADUL register

Table 6.5 DTC Settings (example of migration from repeat mode 1)

Item to be Set	Settings
	Control Data 0
Transfer mode	Repeat mode
Repeat mode interrupt	Enabled
Source address control	Fixed
Destination address control	Repeat area
Chain transfer control	Disabled
Trasnfer block size	2 bytes (16-bit transfer)
DTC transfer count	8
Trasnfer source address	ADCR (FFF1EH to FFF1FH)
Trasnfer destination address	g_ad_value[0] (FF900H to FF901H), g_ad_value[1] (FF902H to FF903H), g_ad_value[2] (FF904H to FF905H), g_ad_value[3] (FF906H to FF907H), g_ad_value[4] (FF908H to FF909H), g_ad_value[5] (FF910H to FF911H), g_ad_value[6] (FF912H to FF913H), g_ad_value[7] (FF914H to FF915H)

(1) The initial setting is made for the A/D converter and DTC.
(2) The ADCS bit in the ADM0 register is set to 1 (conversion enabled) to start A/D conversion.
(3) Upon completion of the A/D conversion on the ANI0 pin, the DTC is activated.
(4) The DTC reads the A/D conversion result from the ADCR register and transfers it to the RAM (g_ad_value[0] to g_ad_value[7]) corresponding to the number of A/D conversion times (1 to 8).
(5) Upon completion of the eighth DTC transfer, an A/D conversion end interrupt is generated.
(6) In interrupt processing, DTC activation is again enabled. Also, the A/D conversion results g_ad_value[0] to g_ad_value[7] are shifted to the right by 6 bits (relocated in the lower 10 bits) and stored in the variables g_ad_an0_value1 to g_ad_an0_value8.
(7) After this, steps (2) to (6) are repeated.

Figure 6.3 shows the A/D conversion and DTC transfer timing and Figure 6.4 shows the relationship between the ADCR register and RAM.

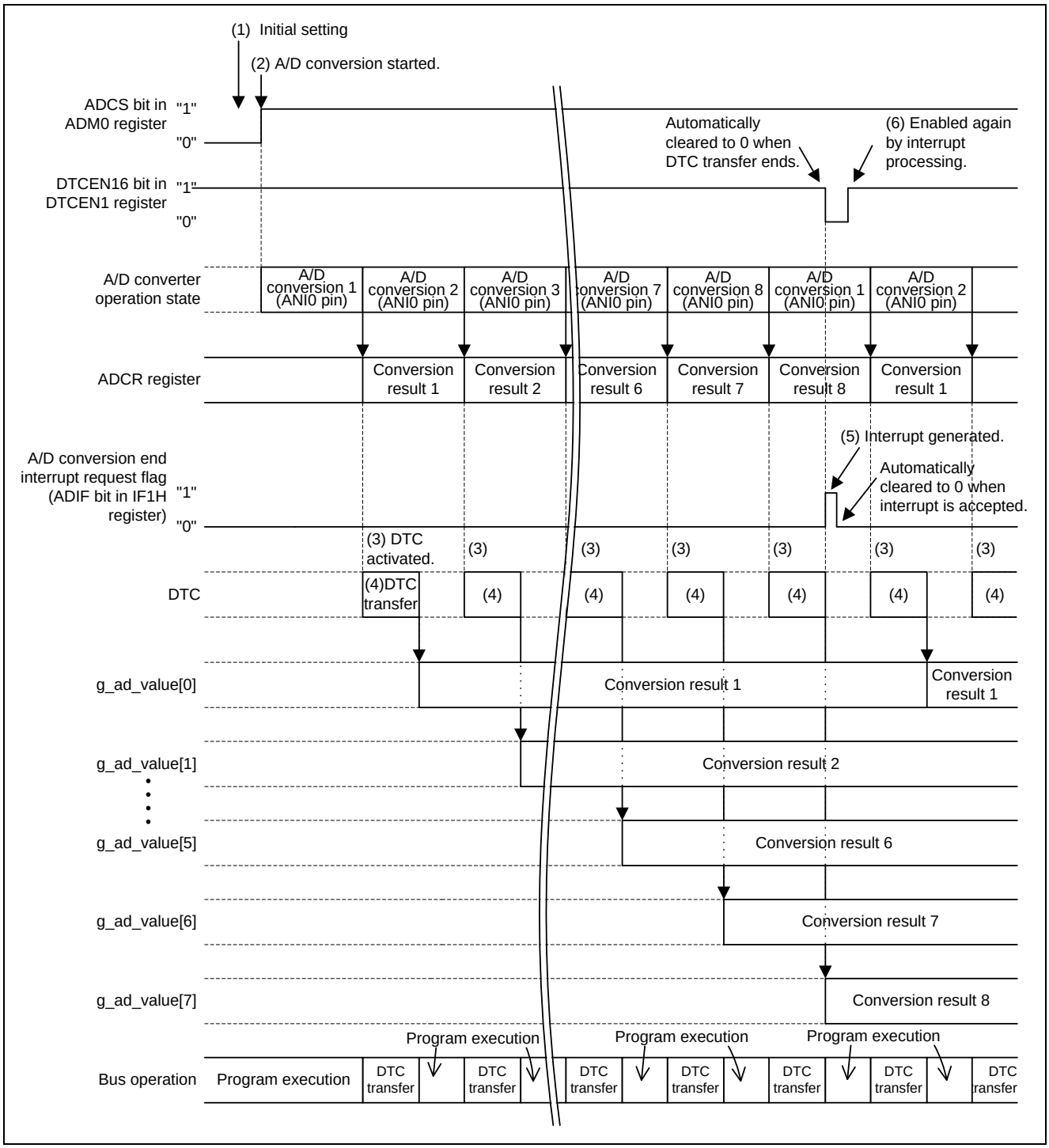


Figure 6.3 A/D Conversion and DTC TransferTiming (example of migration from repeat mode 1)

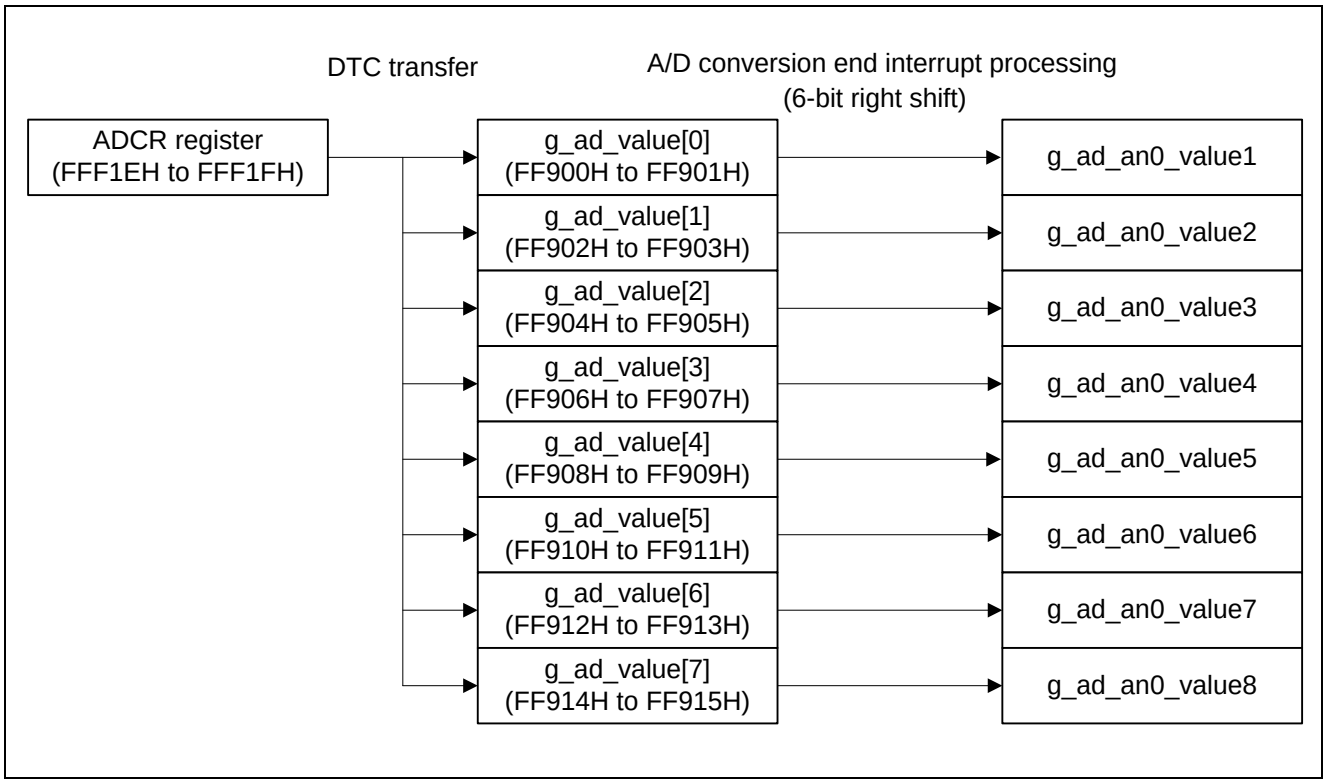


Figure 6.4 Relationship between ADCR Register and RAM (example of migration from repeat mode 1)

6.4.2 List of Option Byte Settings

Table 6.6 lists option byte settings.

Table 6.6 Option Byte Settings (example of migration from repeat mode 1)

Address	Setting	Contents
000C0H/010C0H	01101110B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H/010C1H	00110011B	LVD reset mode Detection voltage: rise 3.13 V/fall 3.06 V
000C2H/010C2H	11100000B	HS mode High-speed on-chip oscillator clock frequency: 24 MHz
000C3H/010C3H	10000100B	On-chip debugging is enabled.

6.4.3 List of Constants

Table 6.7 lists the constant used in the sample code.

Table 6.7 Constant Used in Sample Code (example of migration from repeat mode 1)

Constant Name	Setting	Contents
AD_RESULT_ADDR	0FF900H	Transfer destination address of A/D conversion result

6.4.4 List of Variables

Table 6.8 lists the global variables.

Table 6.8 Global Variables (example of migration from repeat mode 1)

Type	Variable Name	Contents	Function Used
uint16_t __near	g_ad_value[8]	Buffer for storing A/D conversion results	r_adc_interrupt
uint16_t	g_ad_an0_value1	Buffer 1 for storing A/D conversion result of ANI0	r_adc_interrupt
uint16_t	g_ad_an0_value2	Buffer 2 for storing A/D conversion result of ANI0	r_adc_interrupt
uint16_t	g_ad_an0_value3	Buffer 3 for storing A/D conversion result of ANI0	r_adc_interrupt
uint16_t	g_ad_an0_value4	Buffer 4 for storing A/D conversion result of ANI0	r_adc_interrupt
uint16_t	g_ad_an0_value5	Buffer 5 for storing A/D conversion result of ANI0	r_adc_interrupt
uint16_t	g_ad_an0_value6	Buffer 6 for storing A/D conversion result of ANI0	r_adc_interrupt
uint16_t	g_ad_an0_value7	Buffer 7 for storing A/D conversion result of ANI0	r_adc_interrupt
uint16_t	g_ad_an0_value8	Buffer 8 for storing A/D conversion result of ANI0	r_adc_interrupt

6.4.5 Functions

Table 6.9 lists the Functions.

Table 6.9 Functions (example of migration from repeat mode 1)

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	CPU initial setting
R_ADC_Create	Initial setting of A/D converter
R_DTC_Create	Initial setting of DTC
main	Main processing
R_DTCD0_Start	DTC activation
R_ADC_Start	A/D conversion start
r_adc_interrupt	A/D conversion interrupt

6.4.6 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	CPU initial setting
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_ADC_Create	
Outline	Initial setting of A/D converter
Header	None
Declaration	void R_ADC_Create(void)
Description	Perform the initial setting to use the A/D converter in software trigger mode, select mode, and sequential conversion mode.
Argument	None
Return Value	None

R_DTC_Create	
Outline	Initial setting of DTC
Header	None
Declaration	void R_DTC_Create(void)
Description	Perform the initial setting to use the DTC in repeat mode.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_DTCD0_Start	
Outline	DTC activation
Header	None
Declaration	void R_DTCD0_Start(void)
Description	Enable DTC activation.
Argument	None
Return Value	None

R_ADC_Start	
Outline	A/D conversion start
Header	None
Declaration	void R_ADC_Start(void)
Description	Perform A/D conversion.
Argument	None
Return Value	None

r_adc_interrupt	
Outline	A/D conversion interrupt
Header	None
Declaration	static void __near r_adc_interrupt(void)
Description	Perform an A/D conversion end interrupt service routine.
Argument	None
Return Value	None

6.4.7 Flowcharts

(1) Overall Flowchart

Figure 6.5 shows the Overall Flowchart.

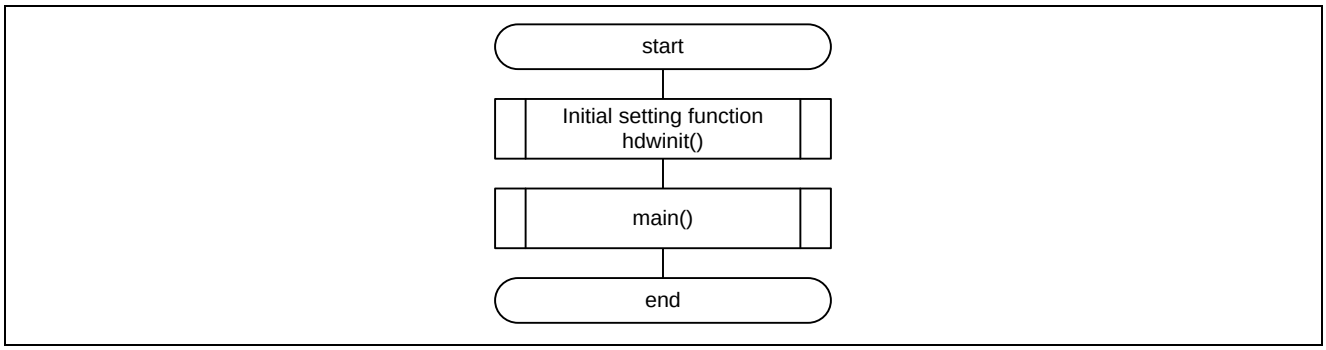


Figure 6.5 Overall Flowchart (example of migration from repeat mode 1)

(2) Initial Setting

Figure 6.6 shows the Initial Setting.

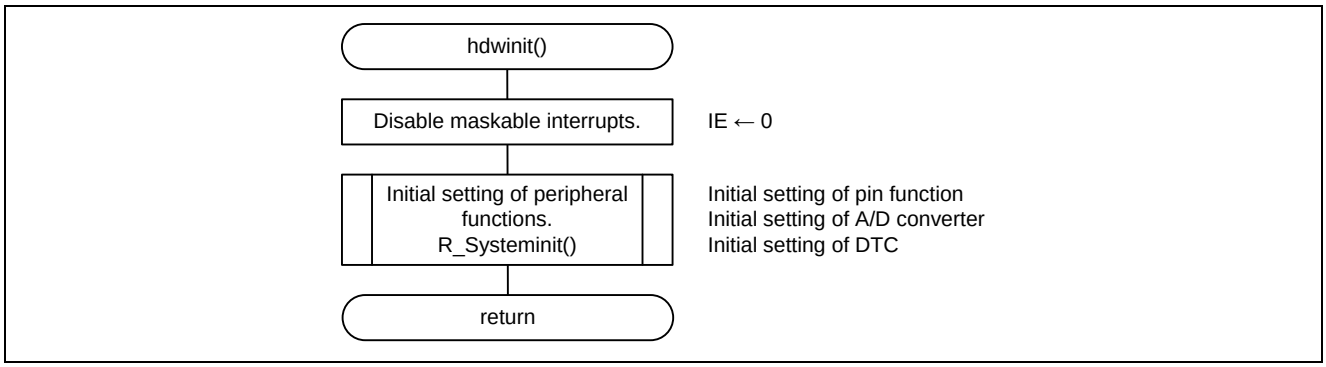


Figure 6.6 Initial Setting (example of migration from repeat mode 1)

(3) Initial Setting of Peripheral Functions

Figure 6.7 shows the initial setting of peripheral functions.

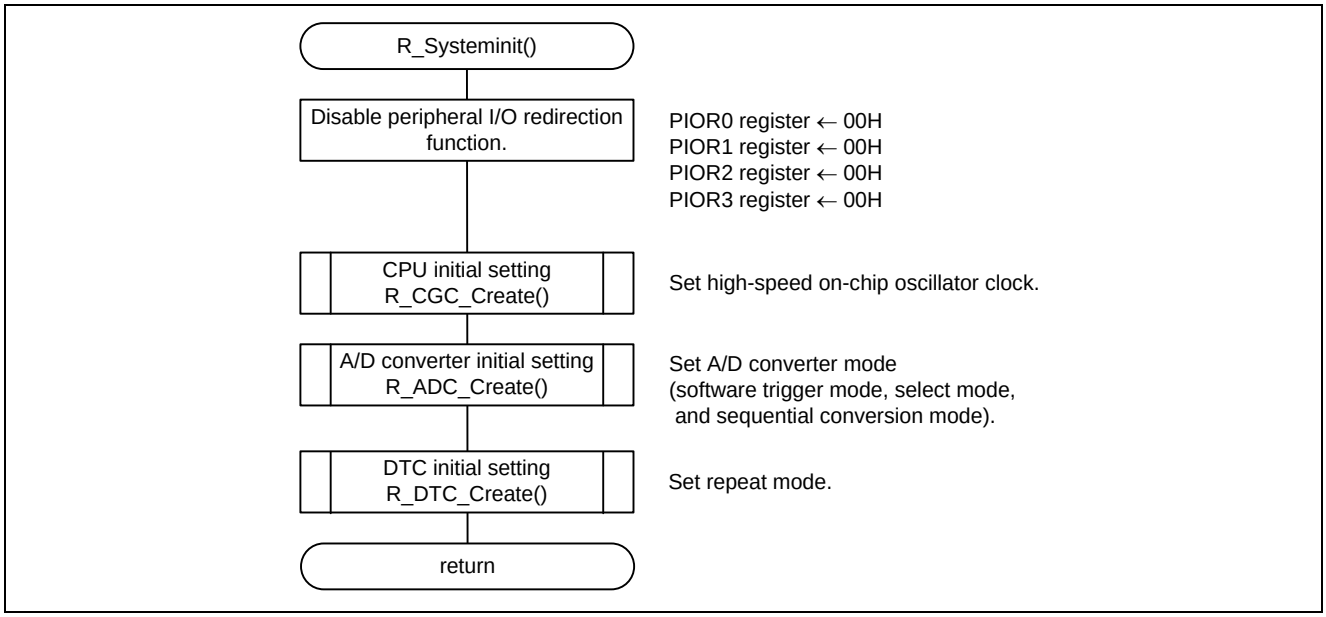


Figure 6.7 Initial Setting of Peripheral Functions (example of migration from repeat mode 1)

(4) Initial Setting of CPU

Figure 6.8 shows the initial setting of the CPU.

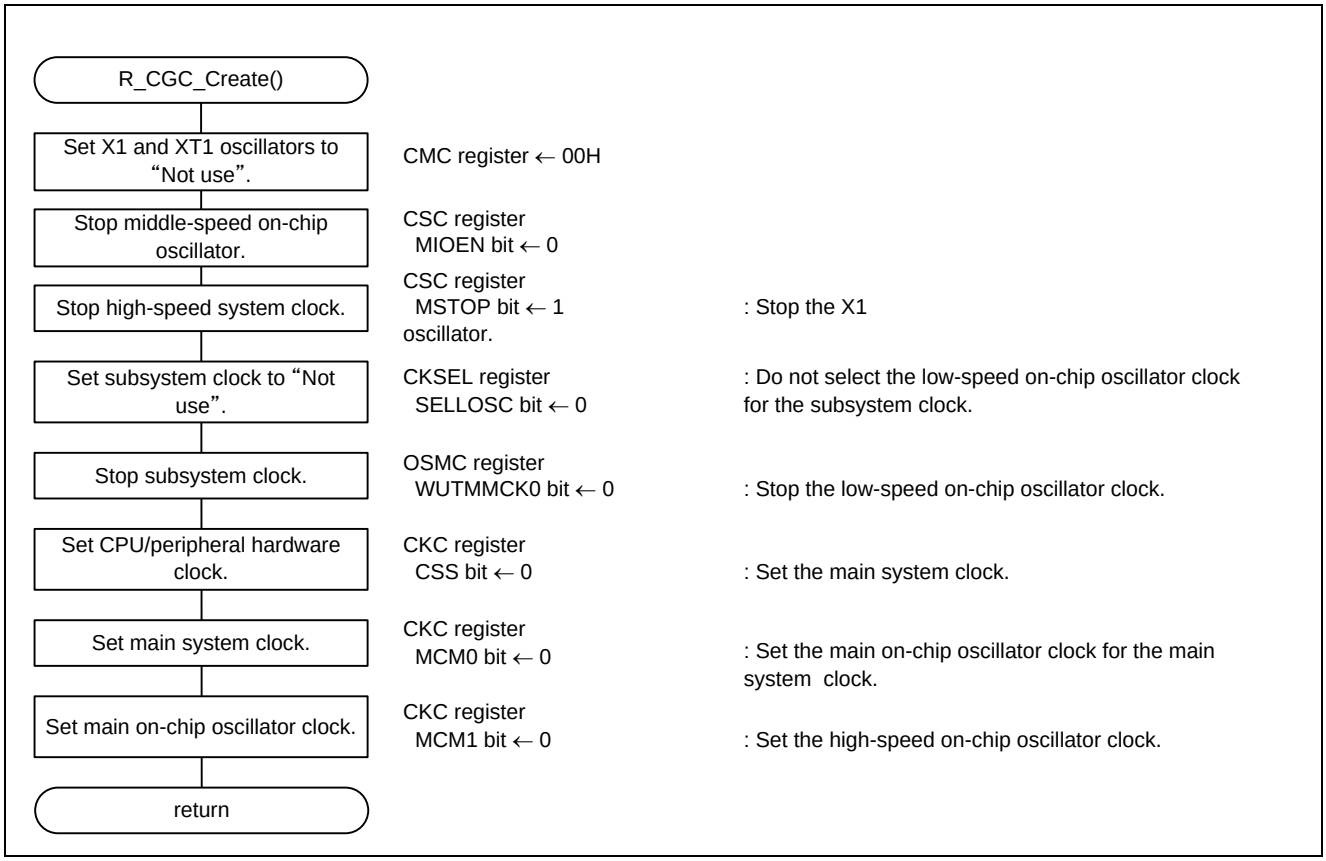


Figure 6.8 Initial Setting of CPU (example of migration from repeat mode 1)

(5) Initial Setting of A/D Converter

Figure 6.9 shows the initial setting of the A/D converter.

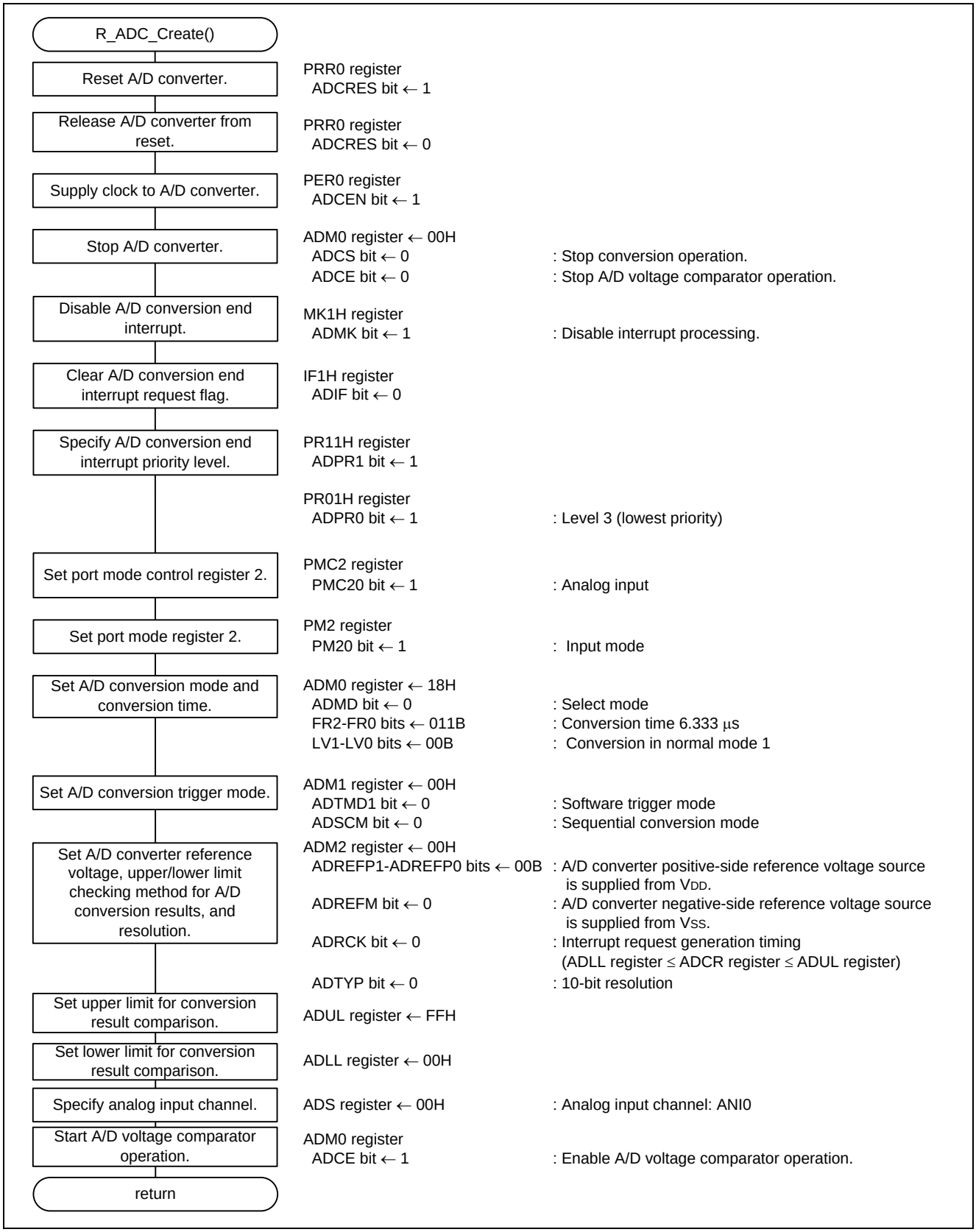


Figure 6.9 Initial Setting of A/D Converter (example of migration from repeat mode 1)

Controlling reset of A/D converter

- Peripheral reset control register 0 (PRR0)
  Resets or releases the A/D converter from the reset state.

Symbol	7	6	5	4	3	2	1	0
PRR0	**0**	**IICA1RES**	**ADCRES**	**IICA0RES**	**0**	**SAU0RES**	**0**	**TAU0RES**
Set value	0	×	**0/1**	×	0	×	0	×

Bit 5

ADCRES	Reset control of A/D converter
0	**A/D converter reset release**
1	**A/D converter reset state**

Starting clock supply to A/D converter

- Peripheral enable register 0 (PER0)
  Starts supplying clock to the A/D converter.

Symbol	7	6	5	4	3	2	1	0
PER0	**0**	**IICA1EN**	**ADCEN**	**IICA0EN**	**0**	**SAU0EN**	**0**	**TAU0EN**
Set value	0	×	**1**	×	0	×	0	×

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.Stops input clock supply. • SFR used by the A/D converter cannot be written.
1	**Enables input clock supply.** • SFR used by the A/D converter can be read and written.

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Stopping A/D converter operation

- A/D converter mode register 0 (ADM0)
  Stops A/D converter.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**0**	×	×	×	×	×	×	**0**

Bit 7

ADCS	A/D conversion operation control
0	**Stops conversion operation.** **[When read]** **Conversion stopped/standby status**
1	Enables conversion operation. [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status

Bit 0

ADCE	A/D voltage comparator operation control
0	**Stops A/D voltage comparator operation.**
1	Enables A/D voltage comparator operation.

Disabling A/D conversion end interrupt

- Interrupt mask flag register 1 (MK1H)
  Disables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Specifying A/D conversion end interrupt priority level

- Priority specification flag register (PR11H, PR01H)
  Specifies level 3 (lowest priority level).

Symbol	7	6	5	4	3	2	1	0
PR11H	**PPR111**	**PPR110**	**PPR19**	**PPR18**	**PPR17**	**KRPR1**	**TMKAPR1**	**ADPR1**
Set value	×	×	×	×	×	×	×	**1**

Symbol	7	6	5	4	3	2	1	0
PR01H	**PPR011**	**PPR010**	**PPR09**	**PPR08**	**PPR07**	**KRPR0**	**TMKAPR0**	**ADPR0**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADPR1	ADPR0	Priority level selection
0	0	Specifies level 0 (high priority level).
0	1	Specifies level 1.
1	0	Specifies level 2.
1	**1**	**Specifes level 3 (low priority level).**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting port mode control register 2

- Port mode control register 2 (PMC2)
  Sets the port mode control register 2 to analog input.

Symbol	7	6	5	4	3	2	1	0
PMC2	**1**	**1**	**1**	**1**	**PMC23**	**PMC22**	**PMC21**	**PMC20**
Set value	1	1	1	1	×	×	×	**1**

Bit 0

PMC20	P20 pin digital I/O/analog input selection
0	Digital I/O (alternate function other than analog input)
1	**Analog input**

Setting port mode register 2

- Port mode register 2 (PM2)
  Sets the port mode register 2 to input mode.

Symbol	7	6	5	4	3	2	1	0
PM2	**1**	**1**	**1**	**1**	**PM23**	**PM22**	**PM21**	**PM20**
Set value	1	1	1	1	×	×	×	**1**

Bit 0

PM20	P20 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion mode and conversion time

- A/D converter mode register 0 (ADM0)
  Sets the A/D conversion mode and conversion time.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	**0**	**0**	**1**	**1**	**0**	**0**	×

Bit 6

ADMD	Specification of A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

Bits 5-1

A/D converter mode register 0 (ADM0)					Mode	Conversion time selection					Conv. clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz	
0	0	0	**0**	**0**	**Normal 1**	Setting prohibited	Setting prohibited	Setting prohibited	76 µs	50.667 µs	f_{CLK}/64
0	0	1						76 µs	38 µs	25.333 µs	f_{CLK}/32
0	1	0					76 µs	38 µs	19 µs	12.667 µs	f_{CLK}/16
0	**1**	**1**					38 µs	19 µs	9.5 µs	**6.333 µs**	**f_{CLK}/8**
1	0	0					28.5 µs	14.25 µs	7.125 µs	4.75 µs	f_{CLK}/6
1	0	1				95 µs	23.75 µs	11.875 µs	5.938 µs	3.958 µs	f_{CLK}/5
1	1	0				76 µs	19 µs	9.5 µs	4.75 µs	3.167 µs	f_{CLK}/4
1	1	1				38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	68 µs	45.333 µs	f_{CLK}/64
0	0	1						68 µs	34 µs	22.667 µs	f_{CLK}/32
0	1	0					68 µs	34 µs	17 µs	11.333 µs	f_{CLK}/16
0	1	1					34 µs	17 µs	8.5 µs	5.667 µs	f_{CLK}/8
1	0	0					25.5 µs	12.75 µs	6.375 µs	4.25 µs	f_{CLK}/6
1	0	1				85 µs	21.25 µs	10.625 µs	5.3125µs	3.542 µs	f_{CLK}/5
1	1	0				68 µs	17 µs	8.5 µs	4.25 µs	2.833 µs	f_{CLK}/4
1	1	1				34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited	f_{CLK}/2

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.

Symbol	7	6	5	4	3	2	1	0
ADM1	**ADTMD1**	**ADTMD0**	**ADSCM**	**0**	**0**	**0**	**ADTRS1**	**ADTRS0**
Set value	**0**	×	**0**	0	0	0	×	×

Bits 7-6

ADTMD1	ADTMD0	Selection of A/D conversion trigger mode
0	**-**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of A/D conversion mode
0	**Sequential conversion mode**
1	One-shot conversion mode

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 2 (ADM2)
  Selects the A/D converter reference voltage source, checks the conversion result against upper-limit/lower-limit value, and selects A/D conversion resolution.

Symbol	7	6	5	4	3	2	1	0
ADM2	**ADREFP1**	**ADREFP0**	**ADREFM**	**0**	**ADRCK**	**AWC**	**0**	**ADTYP**
Set value	**0**	**0**	**0**	0	**0**	×	0	**0**

Bits 7-6

ADREFP1	ADREFP0	Selection of + side reference voltage source of A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from internal reference voltage (1.45 V)
1	1	Setting prohibited
Before rewriting ADREFP1 or ADREFP0 bit, set ADREFP1 and ADREFP0 to 0 and 0. When setting ADREFP1 and ADREFP0 bits to 1 and 0, respectively, this must be configured in accordance with the following procedures. (1) Set ADCE = 0 (2) Set ADREFP1 and ADREFP0 to 1 and 0, respectively. (3) Set ADCE = 1 A wait time (T.B.D) is necessary after (2) and (3). When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output. Be sure to perform A/D conversion while ADISS = 0.		

Bit 5

ADREFM	Selection of – side reference voltage source of A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADRCK	Checking upper limit and lower limit conversion result values
0	**Interrupt signal (INTAD) is generated when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	Interrupt signal (INTAD) is generated when ADCR register < ADLL register, ADUL register < ADCR register.

Bit 0

ADTYP	Selection of A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting upper limit value for conversion result comparison

- Conversion result comparison upper limit setting register (ADUL)
  Sets the upper limit conversion result compare value to FFH.

Symbol	7	6	5	4	3	2	1	0
ADUL	**ADUL7**	**ADUL6**	**ADUL5**	**ADUL4**	**ADUL3**	**ADUL2**	**ADUL1**	**ADUL0**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Setting lower limit values for conversion result comparison

- Conversion result comparison lower limit setting register (ADLL)
  Sets the lower limit conversion result compare value to 00H.

Symbol	7	6	5	4	3	2	1	0
ADLL	**ADLL7**	**ADLL6**	**ADLL5**	**ADLL4**	**ADLL3**	**ADLL2**	**ADLL1**	**ADLL0**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting analog input channel

- Analog input channel specification register (ADS)
  Sets the analog input channel to ANI0.

Symbol	7	6	5	4	3	2	1	0
ADS	**ADISS**	**0**	**0**	**ADS4**	**ADS3**	**ADS2**	**ADS1**	**ADS0**
Set value	**0**	0	0	**0**	**0**	**0**	**0**	**0**

- Select mode (ADMD = 0)

Bits 7, 4-0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**P20/ANI0/AV_{REFP} pin**
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	1	0	0	0	0	ANI16	P01/ANI16 pin
0	1	0	0	0	1	ANI17	P00/ANI17 pin
0	1	0	0	1	0	ANI18	P33/ANI18 pin
0	1	0	0	1	1	ANI19	P32/ANI19 pin
0	1	0	1	0	0	ANI20	P31/ANI20 pin
0	1	0	1	0	1	ANI21	P30/ANI21 pin
0	1	0	1	1	0	ANI22	P56/ANA22 pin
0	1	0	1	1	1	—	PGAOUT(PGA output)）
1	0	0	0	0	0	—	Temperature sensor output voltage
1	0	0	0	0	1	—	Internal reference voltage (1.45V)
Other than above						Setting prohibited	

Setting A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  Starts A/D voltage comparator operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation.
1	**Enables A/D voltage comparator operation.**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(6) Initial Setting of DTC

Figure 6.10 shows the initial setting of the DTC.

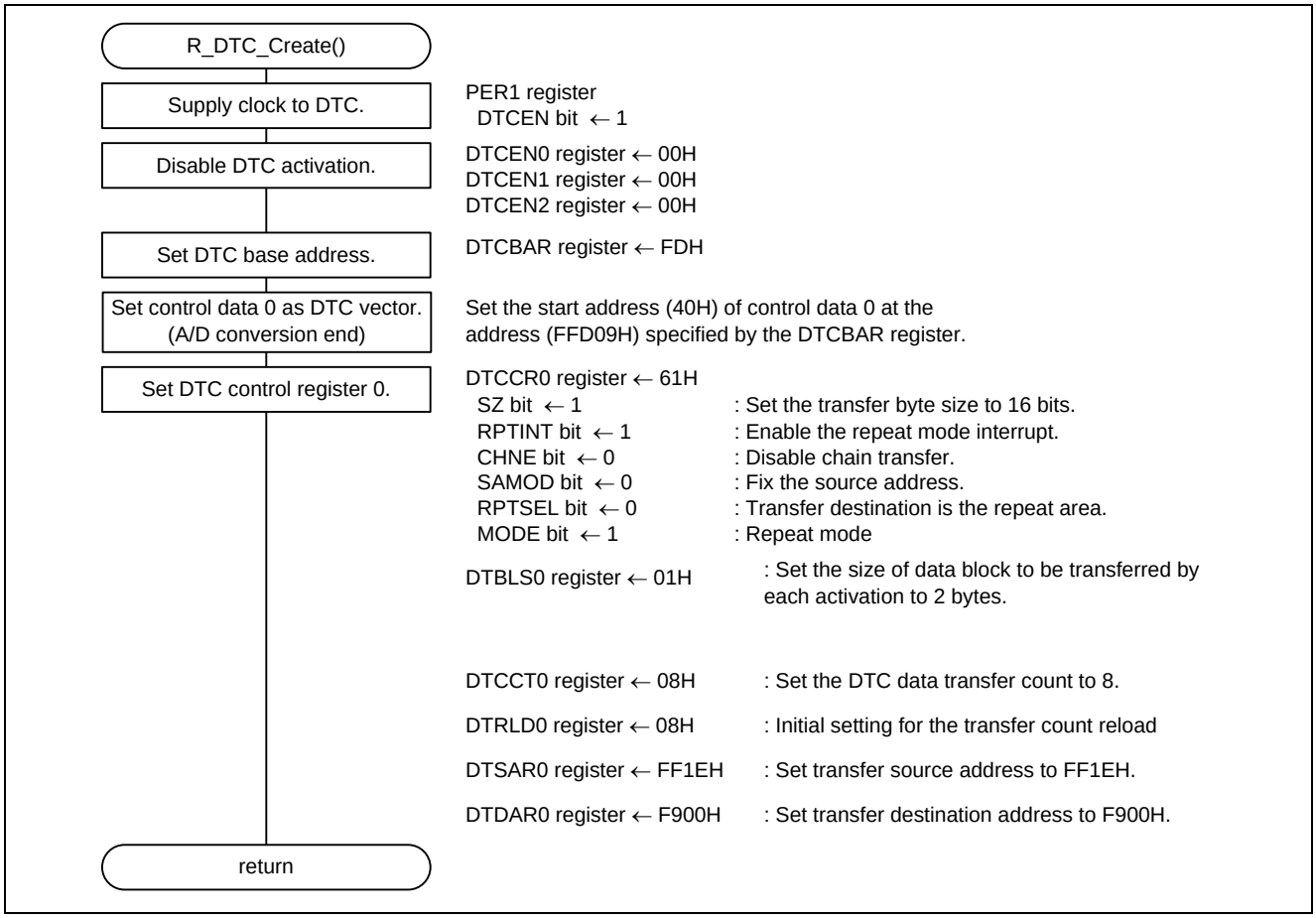


Figure 6.10 Initial Setting of DTC (example of migration from repeat mode 1)

Starting clock supply to DTC

- Peripheral enable register 1 (PER1)
  Starts supplying clock to the DTC.

Symbol	7	6	5	4	3	2	1	0
PER1	**DACEN**	**0**	**CMPEN**	**0**	**DTCEN**	**PGA0EN**	**0**	**0**
Set value	×	0	×	0	**1**	×	0	0

Bit 3

DTCEN	Control of DTC input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Disabling DTC activation

- DTC activation enable register i (DTCENi) (i = 0 to 2)
  Disables DTC activation.

Symbol	7	6	5	4	3	2	1	0
DTCENi	**DTCENi7**	**DTCENi6**	**DTCENi5**	**DTCENi4**	**DTCENi3**	**DTCENi2**	**DTCENi1**	**DTCENi0**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7

DTCENi7	DTC activation enable i7
0	**Activation disabled**
1	Activation enabled
The DTCENi7 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 6

DTCENi6	DTC activation enable i6
0	**Activation disabled**
1	Activation enabled
The DTCENi6 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 5

DTCENi5	DTC activation enable i5
0	**Activation disabled**
1	Activation enabled
The DTCENi5 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Bit 4

DTCENi4	DTC activation enable i4
0	**Activation disabled**
1	Activation enabled
The DTCENi4 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 3

DTCENi3	DTC activation enable i3
0	**Activation disabled**
1	Activation enabled
The DTCENi3 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 2

DTCENi2	DTC activation enable i2
0	**Activation disabled**
1	Activation enabled
The DTCENi2 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 1

DTCENi1	DTC activation enable i1
0	**Activation disabled**
1	Activation enabled
The DTCENi1 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 0

DTCENi0	DTC activation enable i0
0	**Activation disabled**
1	Activation enabled
The DTCENi0 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Setting DTC base address

- DTC base address register (DTCBAR)
  Sets FDH for the DTC base address.

Symbol	7	6	5	4	3	2	1	0
DTCBAR	**DTCBAR 7**	**DTCBAR 6**	**DTCBAR 5**	**DTCBAR 4**	**DTCBAR 3**	**DTCBAR 2**	**DTCBAR 1**	**DTCBAR 0**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting DTC control register

- DTC control register 0 (DTCCR0)
  Sets the DTC control register 0.

Symbol	7	6	5	4	3	2	1	0
DTCCR0	**0**	**SZ**	**RPTINT**	**CHNE**	**DAMOD**	**SAMOD**	**RPTSEL**	**MODE**
Set value	0	**1**	**1**	**0**	×	**0**	**0**	**1**

Bit 6

SZ	Transfer data size selection
0	8 bits
1	**16 bits**

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	Interrupt generation disabled
1	**Interrupt generation enabled**
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	**Chain transfers disabled**
1	Chain transfers enabled
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 2

SAMOD	Transfer source address control
0	**Fixed**
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

RPTSEL	Repeat area selection
0	**Transfer destination is the repeat area**
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	Normal mode
1	**Repeat mode**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting DTC block size register 0

- DTC block size register 0 (DTBLS0)
  Sets the DTC block size register 0 to 01H (2 bytes).

Symbol	7	6	5	4	3	2	1	0
DTBLS0	**DTBLS07**	**DTBLS06**	**DTBLS05**	**DTBLS04**	**DTBLS03**	**DTBLS02**	**DTBLS01**	**DTBLS00**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

DTBLS0	**Transfer block size**	
	8-bit transfer	**16-bit transfer**
00H	256 bytes	512 bytes
01H	1 byte	**2 bytes**
02H	**2 bytes**	**4 bytes**
03H	3 bytes	6 bytes
.	.	.
.	.	.
.	.	.
FDH	253 bytes	506 bytes
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Setting DTC transfer count register 0

- DTC transfer count register 0 (DTCCT0)
  Sets the DTC transfer count register 0 to 08H (8 times).

Symbol	7	6	5	4	3	2	1	0
DTCCT0	**DTCCT07**	**DTCCT06**	**DTCCT05**	**DTCCT04**	**DTCCT03**	**DTCCT02**	**DTCCT01**	**DTCCT00**
Set value	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**

DTCCT0	**Number of transfers**
00H	256 times
01H	Once
02H	2 times
03H	3 times
:	:
08H	**8 times**
:	:
:	:
FDH	253 times
FEH	254 times
FFH	255 times

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting DTC transfer count reload register 0

- DTC transfer count reload register 0 (DTRLD0)
  Sets the DTC transfer count reload register 0 to 08H (8 times).

Symbol	7	6	5	4	3	2	1	0
DTRLD0	**DTRLD07**	**DTRLD06**	**DTRLD05**	**DTRLD04**	**DTRLD03**	**DTRLD02**	**DTRLD01**	**DTRLD00**
Set value	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**

Setting DTC source address register 0

- DTC source address register 0 (DTSAR0)
  Set the DTC source address register 0 to the transfer source address FF1EH.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR0	**DTSAR015**	**DTSAR014**	**DTSAR013**	**DTSAR012**	**DTSAR011**	**DTSAR010**	**DTSAR09**	**DTSAR08**	**DTSAR07**	**DTSAR06**	**DTSAR05**	**DTSAR04**	**DTSAR03**	**DTSAR02**	**DTSAR01**	**DTSAR00**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**

Setting DTC destination address register 0

- DTC destination address register 0 (DTDAR0)
  Set the DTC destination address register 0 to the transfer destination address F900H.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR0	**DTDAR015**	**DTDAR014**	**DTDAR013**	**DTDAR012**	**DTDAR011**	**DTDAR010**	**DTDAR09**	**DTDAR08**	**DTDAR07**	**DTDAR06**	**DTDAR05**	**DTDAR04**	**DTDAR03**	**DTDAR02**	**DTDAR01**	**DTDAR00**
Set value	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(7) Main Processing

Figure 6.11 shows the flowchart for the main processing.

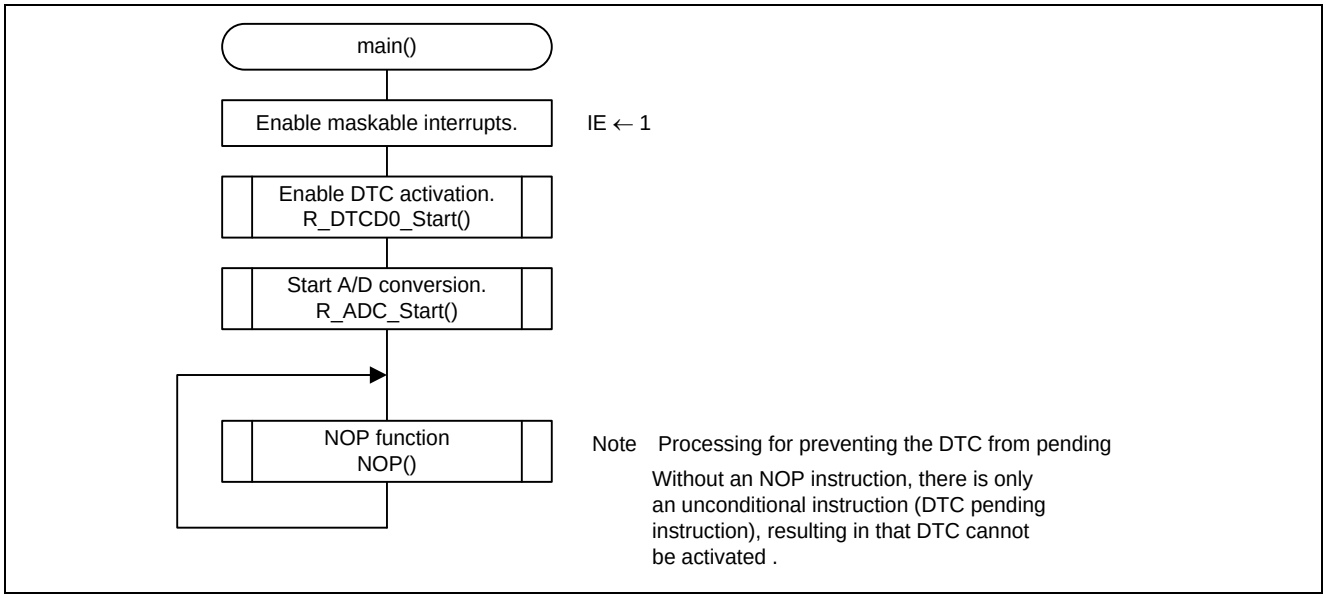


Figure 6.11 Main Processing (example of migration from repeat mode 1)

(8) Enabling DTC Activation

Figure 6.12 shows the flowchart for enabling DTC activation.

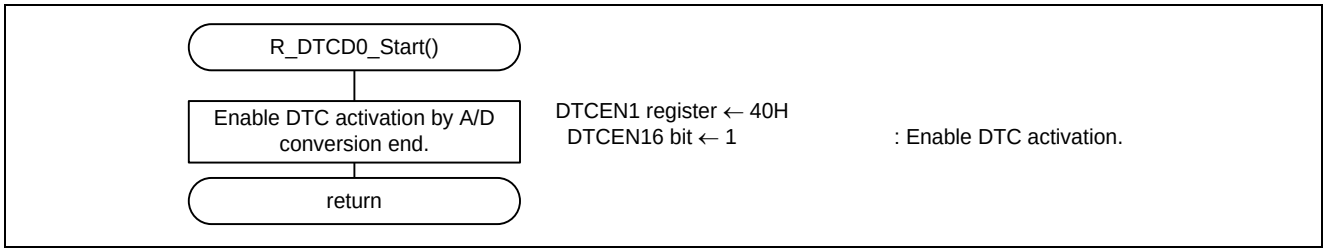


Figure 6.12 Enabling DTC Activation (example of migration from repeat mode 1)

Enabling DTC activation

- DTC activation enable register 1 (DTCEN1)
  Enables DTC activation by the A/D conversion end.

Symbol	7	6	5	4	3	2	1	0
DTCEN1	**DTCEN17**	**DTCEN16**	**DTCEN15**	**DTCEN14**	**DTCEN13**	**DTCEN12**	**DTCEN11**	**DTCEN10**
Set value	×	**1**	×	×	×	×	×	×

Bit 6

DTCEN16	DTC activation enable 16 (DTC activation source: A/D conversion end)
0	Activation disabled
1	**Activation enabled**
The DTCEN16 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(9) Staring A/D Conversion

Figure 6.13 shows the flowchart for starting A/D conversion.

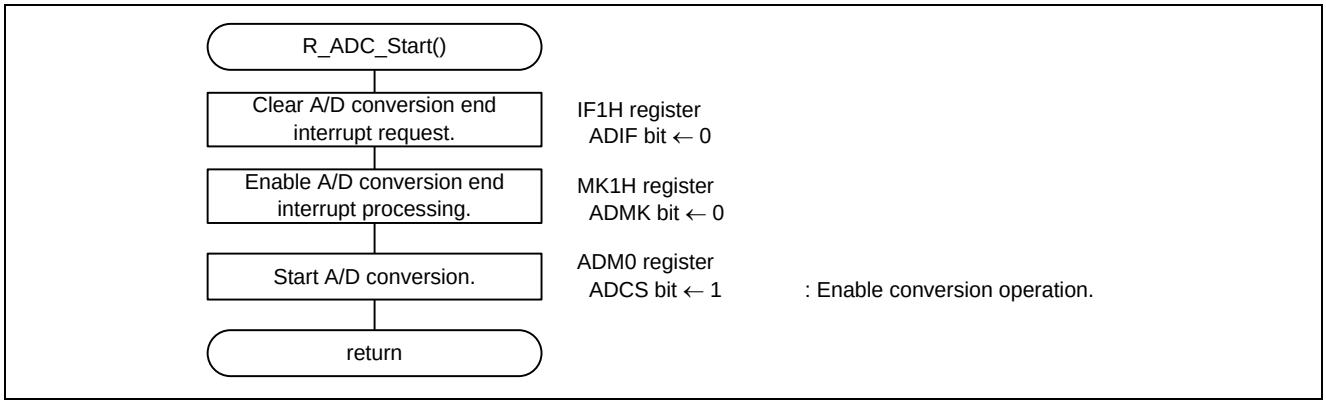


Figure 6.13 Starting A/D Conversion (example of migration from repeat mode 1)

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	**Interrupt request flag**
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Enabling A/D conversion end interrupt

- Interrupt mask flag register (MK1H)
  Enables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Starting A/D converter

- A/D converter mode register 0 (ADM0)
  Starts A/D conversion operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**1**	×	×	×	×	×	×	×

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	**Enables conversion operation** **[When read]** **While in the software trigger mode: Conversion operation status** **While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(10) A/D conversion end interrupt

Figure 6.14 shows the flowchart for A/D conversion end interrupt processing.

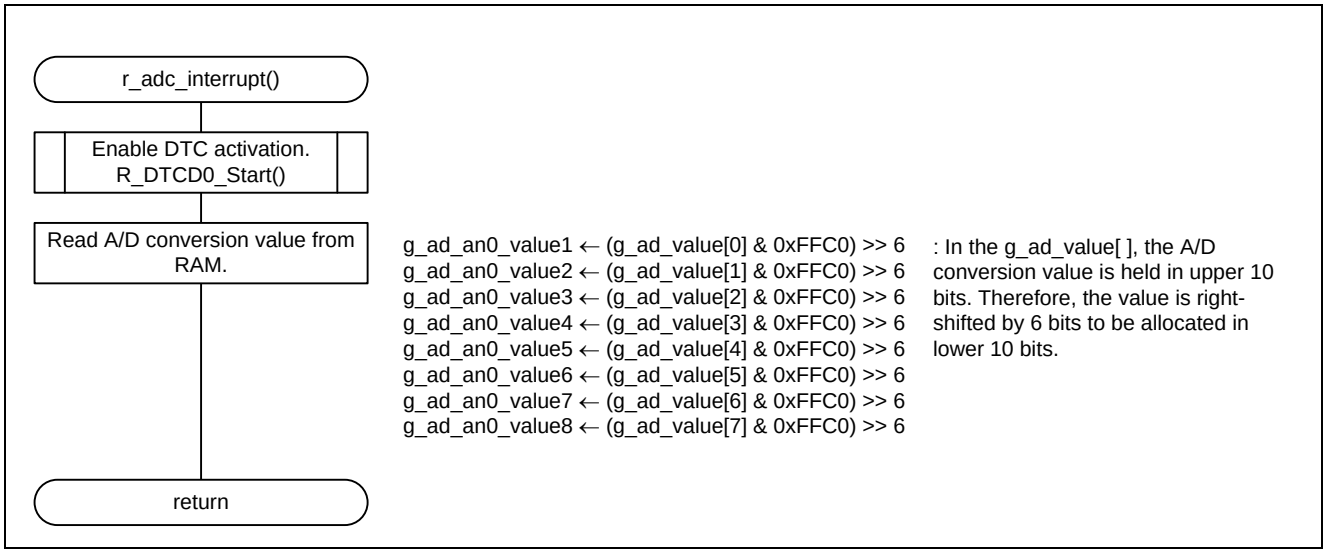


Figure 6.14 A/D Conversion End Interrupt (example of migration from repeat mode 1)

6.5 Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6.6 Reference Application Note

- RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: A/D Converter CC-RL (R01AN3059)

- RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) CC-RL (R01AN2581)

6.7 Reference Documents

User's Manual

- RL78/G11 User's Manual: Hardware
  (The latest versions can be downloaded from the Renesas Electronics website.)

- R8C/32C Group Hardware Manual
  (The latest versions can be downloaded from the Renesas Electronics website.)

- Technical Update/Technical News
  (The latest information can be downloaded from the Renesas Electronics website.)

Migration Guide

- Migration to CubeSuite+ Integrated Development Environment for RL78 Family
  (On-chip Debug) - Migration from R8C, M16C to RL78 (R20UT2150)

7. Example of Migration from Single Sweep Mode

7.1 Specifications

To implement R8C/32C single sweep mode in the RL78/G11, the AD converter (software trigger, scan, one-shot conversion mode) and DTC transfer (repeat mode) are used.

The analog input voltage of the ANI0 to ANI3 pins is A/D-converted in scan mode and one-shot conversion mode, and the A/D conversion result values are stored in the RAM assigned to each pin by DTC transfer. Specifically, A/D conversion on the pins is sequentially performed; each time A/D conversion on one pin ends, the conversion result is stored in the 10-bit A/D conversion result register (ADCR), and an A/D conversion end interrupt signal is generated. In response to the interrupt signal, the DTC is activated, and the A/D conversion result is transferred from the ADCR register to the RAM. When A/D conversion and DTC transfer on all the pins are completed, an A/D conversion end interrupt request is generated.

Table 7.1 shows the peripheral functions used and the purpose of use, and Figure 7.1 shows the operation summary.

Table 7.1 Peripheral Functions Used and Purpose of Use (example of migration from single sweep mode)

Peripheral Function	Purpose of Use
A/D converter	Performs A/D conversion on the analog input voltage.
DTC	Transfers A/D conversion result to RAM.

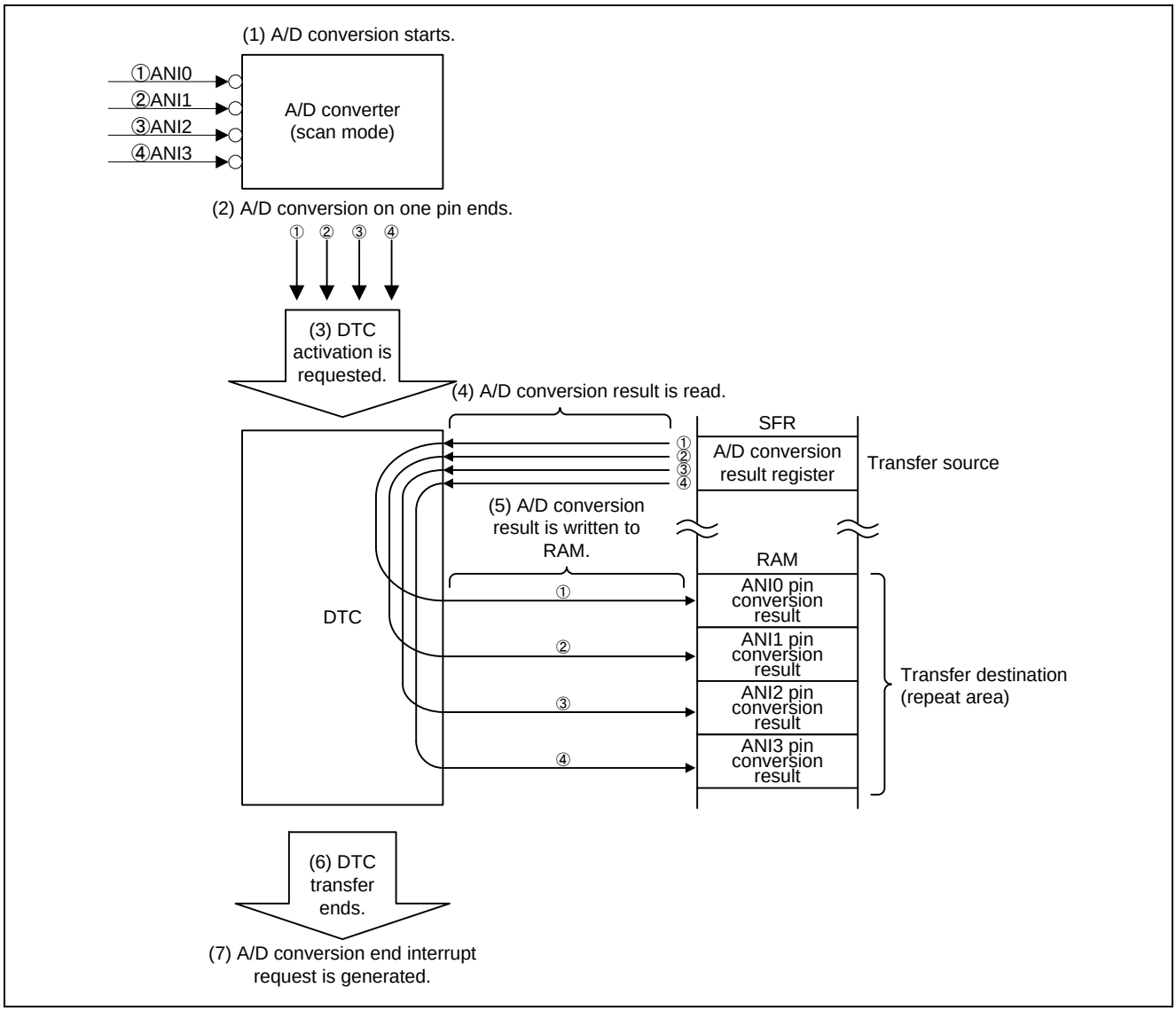


Figure 7.1 Operation Summary (example of migration from single sweep mode)

7.2 Conditions for Confirming Operations

The sample code operations described in this application note are confirmed under the following conditions.

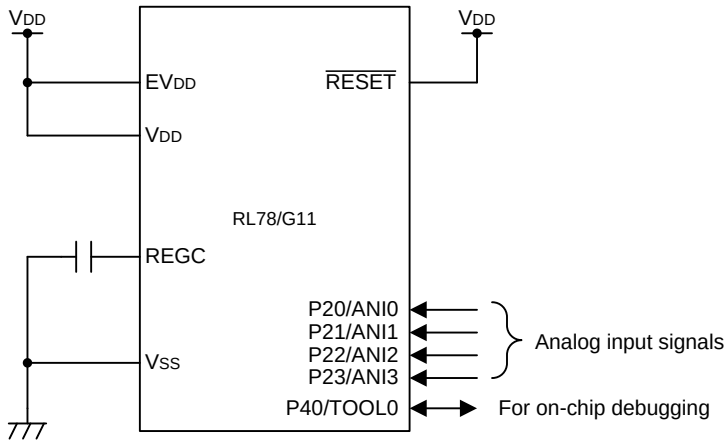
Table 7.2 Conditions for Confirming Operations (example of migration from single sweep mode)

Item	Description
Microcontroller used	RL78/G11 (R5F1056A)
Operating frequency	• High-speed on-chip oscillator clock (f_{IH}): 24 MHz • CPU/peripheral hardware clock (f_{CLK}): 24 MHz
Operating voltage	5.0 V (can be operated from 3.6 V to 5.5 V) LVD operation (V_{LVD}): Reset mode; rise 3.13 V/fall 3.06 V
Integrated development environment (CS+)	CS+ for CC V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.4.0.015 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.

7.3 Hardware Descriptions

7.3.1 Hardware Configuration Example

Figure 7.2 shows an example of the hardware configuration used for this application.



Note 1: The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied. Input-only ports should be each connected to V_{DD} or V_{SS} via a resistor.

Note 2: Any pin whose name begins with EV_{DD} should be connected to V_{DD}.

Note 3: V_{DD} should be equal to or greater than the reset-release voltage (V_{LVD}) specified for the LVD.

Figure 7.2 Hardware Configuration (example of migration from single sweep mode)

7.3.2 List of Pins Used

Table 7.3 lists the pins used and their functions.

Table 7.3 Pins Used and Their Functions (example of migration from single sweep mode)

Pin Name	I/O	Function
P20/ANI0	Input	A/D converter input (ANI0)
P21/ANI1	Input	A/D converter input (ANI1)
P22/ANI2	Input	A/D converter input (ANI2)
P23/ANI3	Input	A/D converter input (ANI3)

7.4 Software Descriptions

7.4.1 Operation Summary

With this sample program, the A/D conversion on four pins is performed in scan mode, and the conversion results are stored in the RAM by DTC transfer. The DTC is used in repeat mode with the transfer destination set as repeat area, and the conversion results on the four pins are sequentially stored in the RAM.

Upon completion of the A/D conversion on the ANI0 pin, the first DTC transfer is performed from the transfer source addresses (ADCR register (FFF1EH, FFF1FH)) to the transfer destination addresses (g_ad_value[0] (FF900H to FF901H)). Upon completion of the A/D conversion on the ANI1 pin, the second DTC transfer is performed to g_ad_value[1] (FF902H to FF903H) since the transfer destination is set as the repeat area. Similarly, the A/D conversion results of the ANI3 and ANI4 pins are DTC-transferred. Upon completion of the fourth transfer, an A/D conversion end interrupt is generated.

In interrupt processing, the A/D conversion results stored in the array g_ad_value[] (FF900H to FF907H) are relocated in the lower 10 bits before being stored in the buffers for storing the A/D conversion results (variable g_ad _an0_value to g_ad_an3_value).

Table 7.4 shows the A/D converter settings and Table 7.5 shows the DTC settings.

Table 7.4 A/D Converter Settings (example of migration from single sweep mode)

Item to be Set	Settings
Conversion clock frequency (f_{AD})	f_{CLK}/8
A/D conversion mode	• A/D conversion trigger mode: Software trigger • A/D conversion channel selection mode: Scan mode • A/D conversion operation mode: One-shot conversion mode
Resolution	10 bits
Analog input channel	• Scan 0: ANI0 • Scan 1: ANI1 • Scan 2: ANI2 • Scan 3: ANI3
A/D conversion result comparison upper limit (ADUL register)	FFH
A/D conversion result comparison lower limit (ADLL register)	00H
Upper and lower limit conversion result checking	INTAD generated when ADLL register ≤ ADCR register ≤ ADUL register

Table 7.5 DTC Settings (example of migration from repeat sweep ode)

Item to be Set	Settings
	Control Data 0
Transfer mode	Repeat mode
Repeat mode interrupt	Enabled
Source address control	Fixed
Destination address control	Repeat area
Chain transfer control	Disabled
Transfer block size	2 bytes (16-bit transfer)
DTC transfer count	4
Transfer source address	ADCR (FFF1EH to FFF1FH)
Transfer destination address	g_ad_value[0] (FF900H to FF901H), g_ad_value[1] (FF902H to FF903H), g_ad_value[2] (FF904H to FF905H), g_ad_value[3] (FF906H to FF907H)

(1) The initial setting is made for the A/D converter and DTC.
(2) The ADCS bit in the ADM0 register is set to 1 (conversion enabled) to start A/D conversion.
(3) Upon completion of the A/D conversion on each of the pins (ANI0, ANI1, ANI2, and ANI3 pins), the DTC is activated.
(4) The DTC reads the A/D conversion result from the ADCR register and transfers it to the RAM (g_ad_value[0] to g_ad_value[3]) corresponding to the pin.
(5) Upon completion of the fourth DTC transfer, an A/D conversion end interrupt is generated.In interrupt processing, the A/D conversion results g_ad_value[0] to g_ad_value[3] are shifted to the right by 6 bits (relocated in the lower 10 bits) and stored in the variables g_ad_an0_value to g_ad_an3_value.
(6) Determine if DTC activation is disabled by a program, enable DTC activation again, and start A/D conversion.
(7) After this, steps (2) to (6) are repeated.

Figure 7.3 shows the A/D conversion and DTC transfer timing and Figure 7.4 shows the relationship between the ADCR register and RAM.

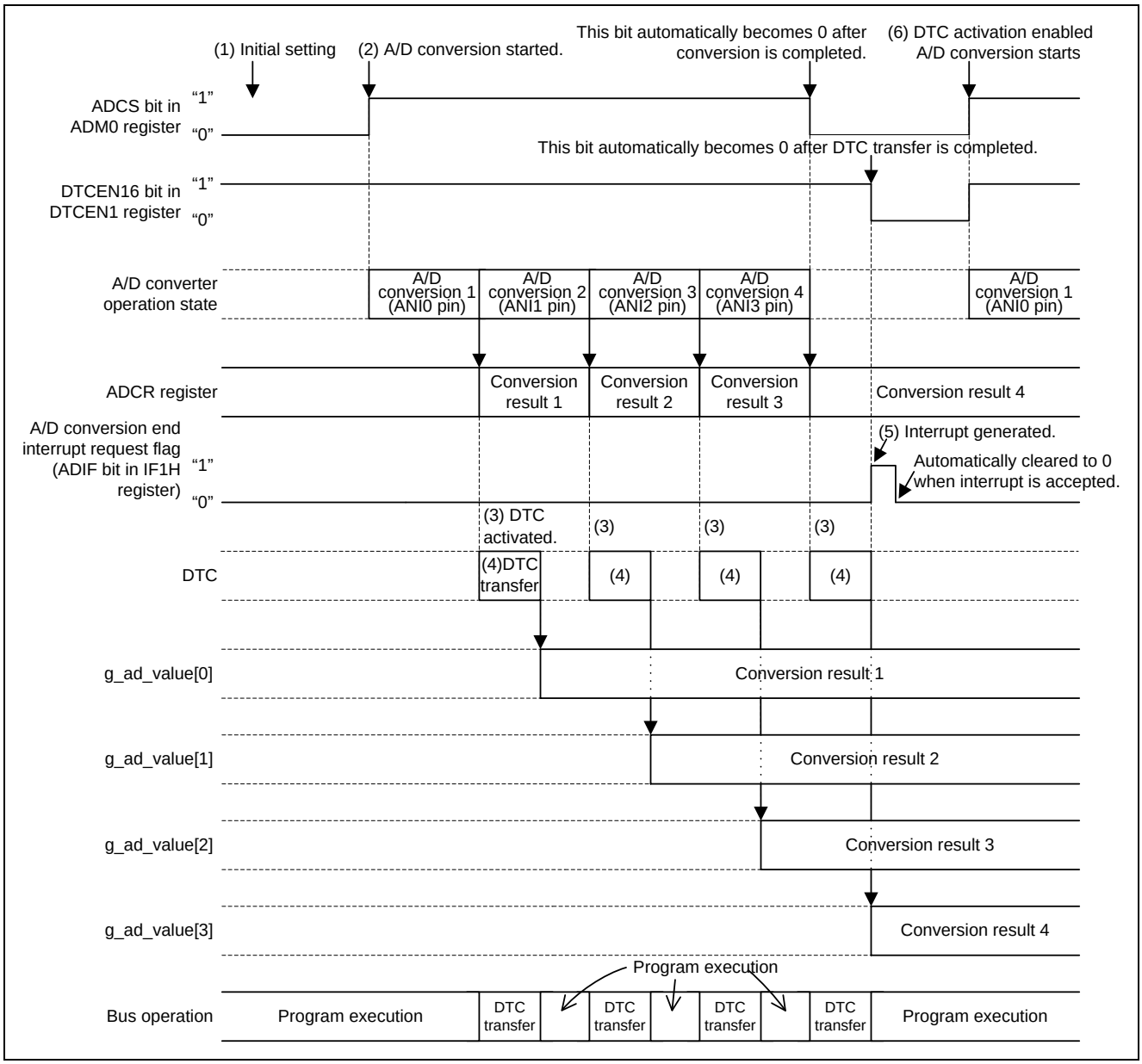


Figure 7.3 A/D Conversion and DTC Transfer Timing (example of migration from single sweep mode)

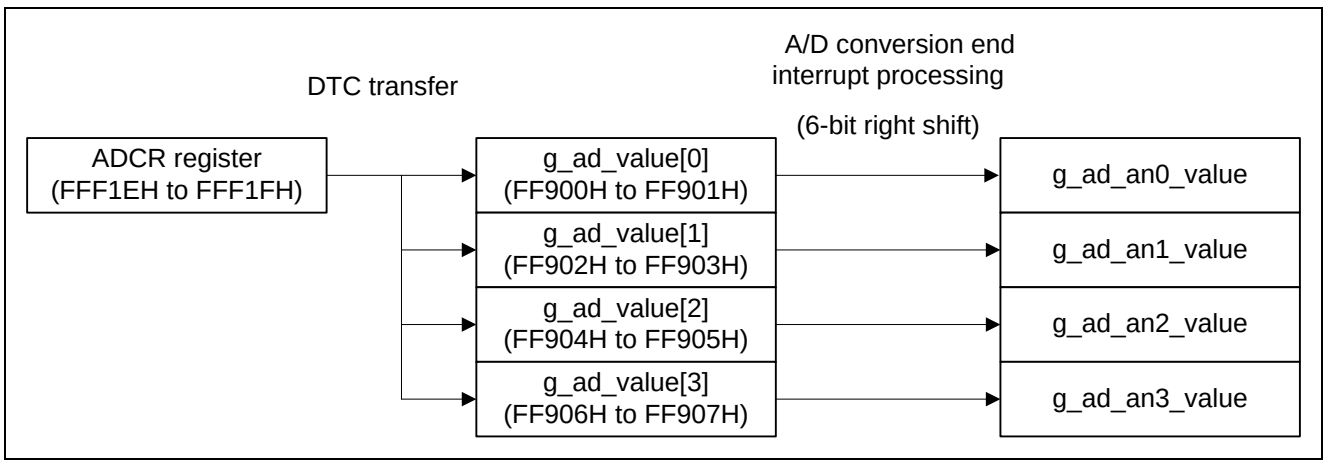


Figure 7.4 Relationship between ADCR Register and RAM

(example of migration from single sweep mode)

7.4.2 List of Option Byte Settings

Table 7.6 lists option byte settings.

Table 7.6 Option Byte Settings (example of migration from single sweep mode)

Address	Setting	Contents
000C0H/010C0H	01101110B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H/010C1H	00110011B	LVD reset mode Detection voltage: rise 3.13 V/fall 3.06 V
000C2H/010C2H	11100000B	HS mode High-speed on-chip oscillator clock frequency: 24 MHz
000C3H/010C3H	10000100B	On-chip debugging is enabled.

7.4.3 List of Constants

Table 7.7 lists the constant used in the sample code.

Table 7.7 Constant Used in Sample Code (example of migration from single sweep mode)

Constant Name	Setting	Contents
AD_RESULT_ADDR	0FF900H	Transfer destination address of A/D conversion result

7.4.4 List of Variables

Table 7.8 lists the global variables.

Table 7.8 Global Variables (example of migration from single sweep mode)

Type	Variable Name	Contents	Function Used
uint16_t __near	g_ad_value[4]	Buffer for storing A/D conversion results of ANI0 to ANI3	r_adc_interrupt
uint16_t	g_ad_an0_value	Buffer for storing A/D conversion result of ANI0	r_adc_interrupt
uint16_t	g_ad_an1_value	Buffer for storing A/D conversion result of ANI1	r_adc_interrupt
uint16_t	g_ad_an2_value	Buffer for storing A/D conversion result of ANI2	r_adc_interrupt
uint16_t	g_ad_an3_value	Buffer for storing A/D conversion result of ANI3	r_adc_interrupt

7.4.5 Functions

Table 7.9 lists the Functions.

Table 7.9 Functions (example of migration from single sweep mode)

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	CPU initial setting
R_ADC_Create	Initial setting of A/D converter
R_DTC_Create	Initial setting of DTC
main	Main processing
R_DTCD0_Start	DTC activation
R_ADC_Start	A/D conversion start
r_adc_interrupt	A/D conversion interrupt

7.4.6 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	CPU initial setting
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_ADC_Create	
Outline	Initial setting of A/D converter
Header	None
Declaration	void R_ADC_Create(void)
Description	Perform the initial setting to use the A/D converter in software trigger mode, scan mode, and one-shot conversion mode.
Argument	None
Return Value	None

R_DTC_Create	
Outline	Initial setting of DTC
Header	None
Declaration	void R_DTC_Create(void)
Description	Perform the initial setting to use the DTC in repeat mode.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_DTCD0_Start	
Outline	DTC activation
Header	None
Declaration	void R_DTCD0_Start(void)
Description	Enable DTC activation.
Argument	None
Return Value	None

R_ADC_Start	
Outline	A/D conversion start
Header	None
Declaration	void R_ADC_Start(void)
Description	Perform A/D conversion.
Argument	None
Return Value	None

r_adc_interrupt	
Outline	A/D conversion interrupt
Header	None
Declaration	static void __near r_adc_interrupt(void)
Description	Perform an A/D conversion end interrupt service routine.
Argument	None
Return Value	None

7.4.7 Flowcharts

(1) Overall Flowchart

Figure 7.5 shows the Overall Flowchart.

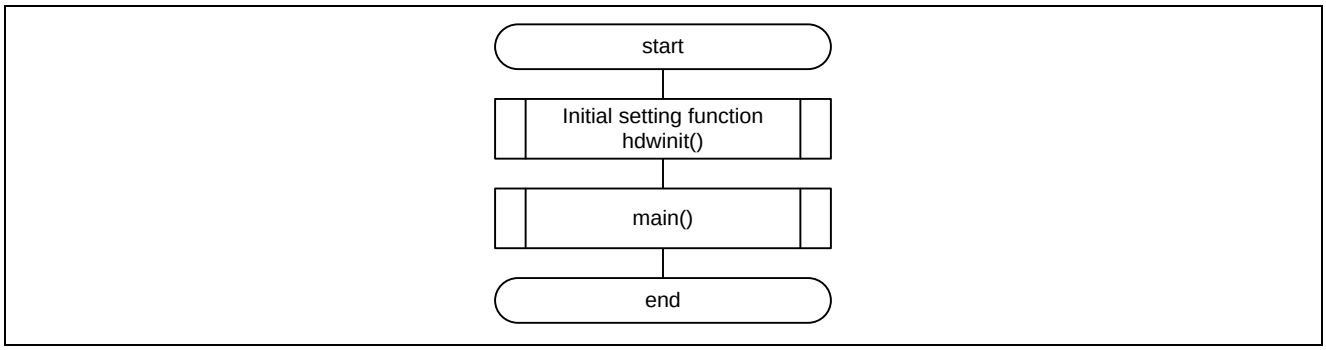


Figure 7.5 Overall Flowchart (example of migration from single sweep mode)

(2) Initial Setting

Figure 7.6 shows the Initial Setting.

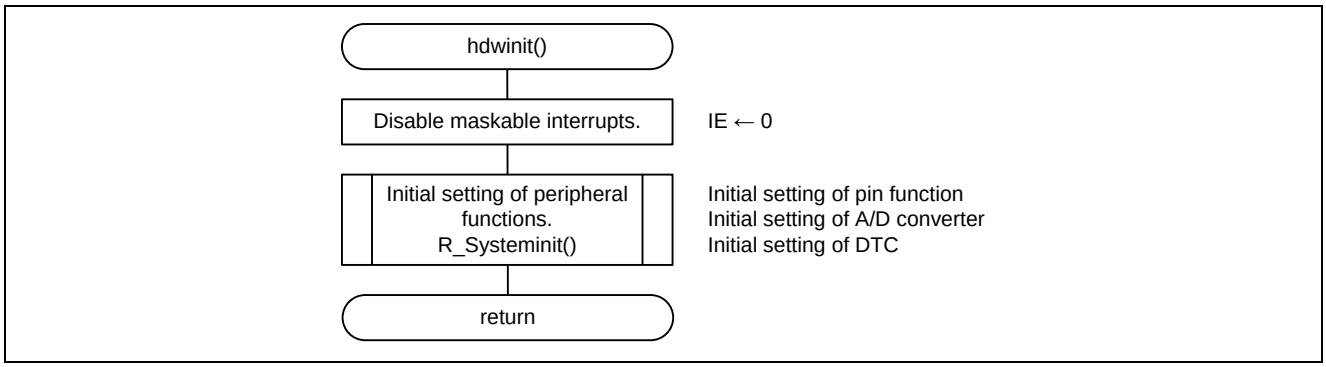


Figure 7.6 Initial Setting (example of migration from single sweep mode)

(3) Initial Setting of Peripheral Functions

Figure 7.7 shows the initial setting of peripheral functions.

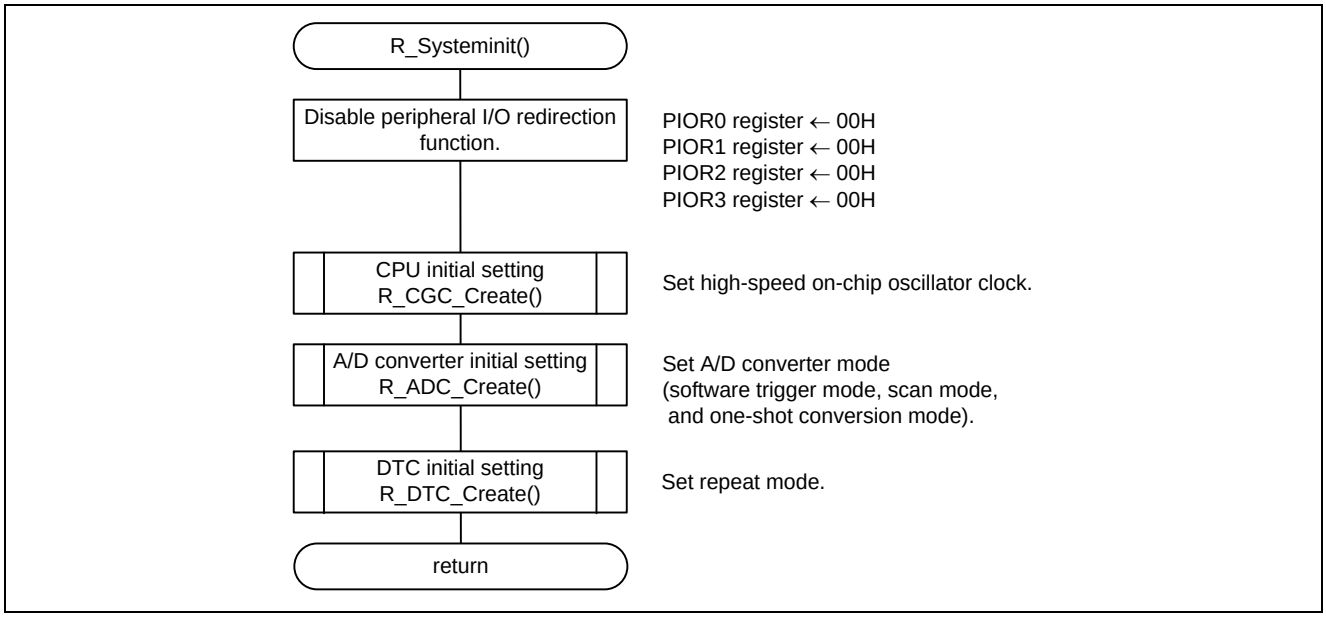


Figure 7.7 Initial Setting of Peripheral Functions (example of migration from single sweep mode)

(4) Initial Setting of CPU

Figure 7.8 shows the initial setting of the CPU.

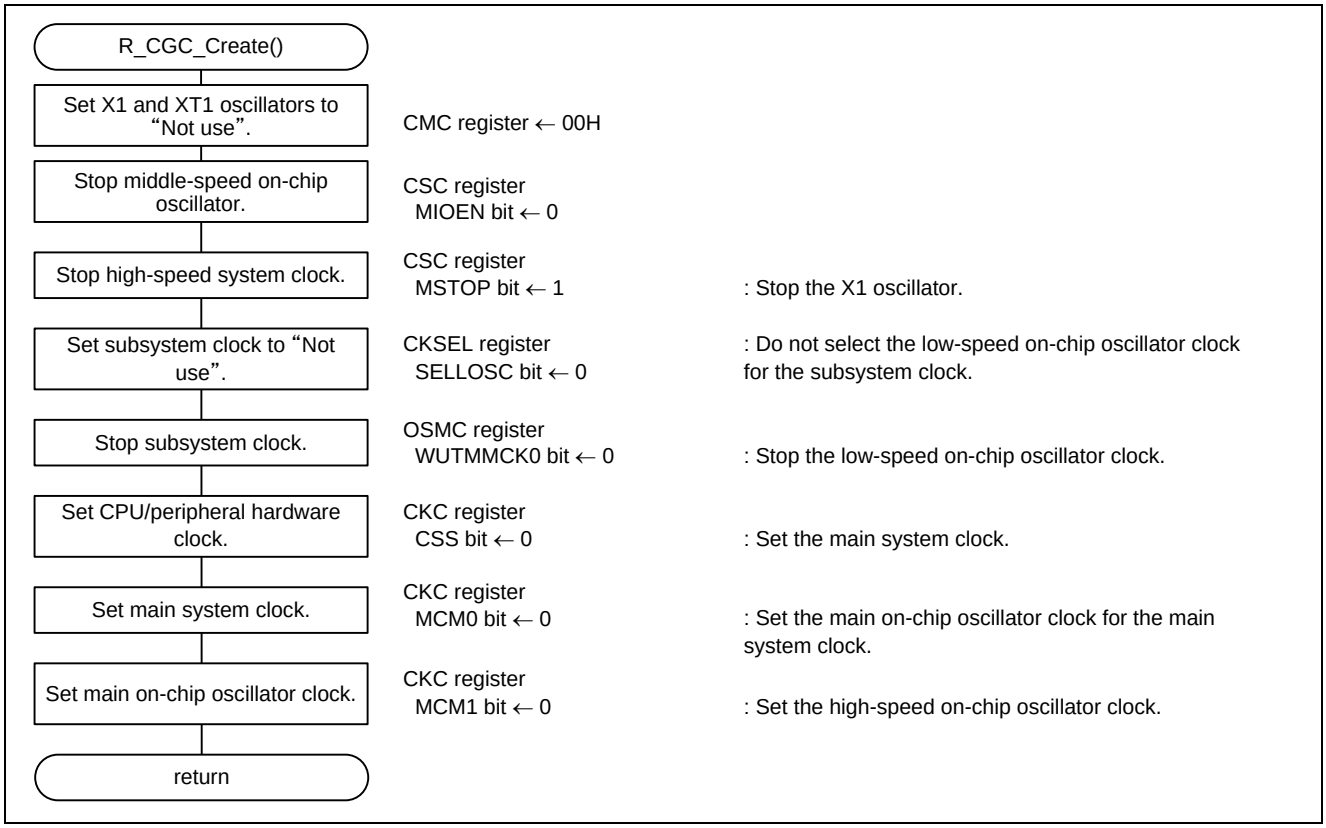


Figure 7.8 Initial Setting of CPU (example of migration from single sweep mode)

(5) Initial Setting of A/D Converter

Figure 7.9 shows the initial setting of the A/D converter.

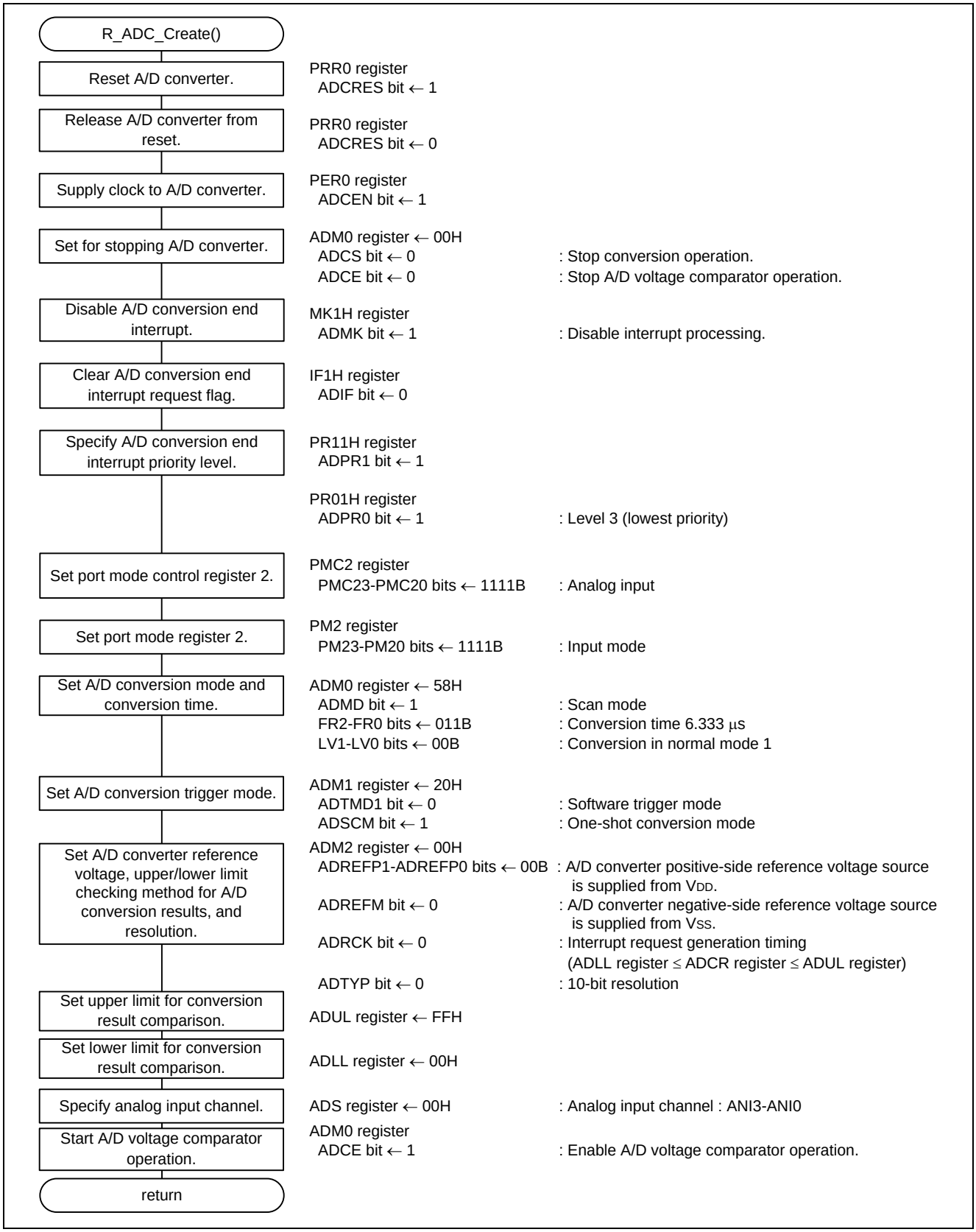


Figure 7.9 Initial Setting of A/D Converter (example of migration from single sweep mode)

Controlling reset of A/D converter

- Peripheral reset control register 0 (PRR0)
  Resets or releases the A/D converter from the reset state.

Symbol	7	6	5	4	3	2	1	0
PRR0	**0**	**IICA1RES**	**ADCRES**	**IICA0RES**	**0**	**SAU0RES**	**0**	**TAU0RES**
Set value	0	×	**0/1**	×	0	×	0	×

Bit 5

ADCRES	Reset control of A/D converter
0	**A/D converter reset release**
1	**A/D converter reset state**

Starting clock supply to A/D converter

- Peripheral enable register 0 (PER0)
  Starts supplying clock to the A/D converter.

Symbol	7	6	5	4	3	2	1	0
PER0	**0**	**IICA1EN**	**ADCEN**	**IICA0EN**	**0**	**SAU0EN**	**0**	**TAU0EN**
Set value	0	×	**1**	×	0	×	0	×

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.Stops input clock supply. • SFR used by the A/D converter cannot be written.
1	**Enables input clock supply.** • SFR used by the A/D converter can be read and written.

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Stopping A/D converter operation

- A/D converter mode register 0 (ADM0)
  Stops A/D converter.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**0**	×	×	×	×	×	×	**0**

Bit 7

ADCS	A/D conversion operation control
0	**Stops conversion operation.** **[When read]** **Conversion stopped/standby status**
1	Enables conversion operation. [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status

Bit 0

ADCE	A/D voltage comparator operation control
0	**Stops A/D voltage comparator operation.**
1	Enables A/D voltage comparator operation.

Disabling A/D conversion end interrupt

- Interrupt mask flag register 1 (MK1H)
  Disables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Specifying A/D conversion end interrupt priority level

- Priority specification flag register (PR11H, PR01H)
  Specifies level 3 (lowest priority level).

Symbol	7	6	5	4	3	2	1	0
PR11H	**PPR111**	**PPR110**	**PPR19**	**PPR18**	**PPR17**	**KRPR1**	**TMKAPR1**	**ADPR1**
Set value	×	×	×	×	×	×	×	**1**

Symbol	7	6	5	4	3	2	1	0
PR01H	**PPR011**	**PPR010**	**PPR09**	**PPR08**	**PPR07**	**KRPR0**	**TMKAPR0**	**ADPR0**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADPR1	ADPR0	Priority level selection
0	0	Specifies level 0 (high priority level).
0	1	Specifies level 1.
1	0	Specifies level 2.
1	**1**	**Specifes level 3 (low priority level).**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting port mode control register 2

- Port mode control register 2 (PMC2)
  Sets the port mode control register 2 to analog input.

Symbol	7	6	5	4	3	2	1	0
PMC2	**1**	**1**	**1**	**1**	**PMC23**	**PMC22**	**PMC21**	**PMC20**
Set value	1	1	1	1	**1**	**1**	**1**	**1**

Bits 3-0

PMC2n	P2n pin digital I/O/analog input selection
0	Digital I/O (alternate function other than analog input)
1	**Analog input**

Remark n: Channel number (n = 0 to 3)

Setting port mode register 2

- Port mode register 2 (PM2)
  Sets the port mode register 2 to input mode.

Symbol	7	6	5	4	3	2	1	0
PM2	**1**	**1**	**1**	**1**	**PM23**	**PM22**	**PM21**	**PM20**
Set value	1	1	1	1	**1**	**1**	**1**	**1**

Bits 3-0

PM2n	P2n pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Remark n: Channel number (n = 0 to 3)

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion mode and conversion time

- A/D converter mode register 0 (ADM0)
  Sets the A/D conversion mode and conversion time.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	**1**	**0**	**1**	**1**	**0**	**0**	×

Bit 6

ADMD	Specification of A/D conversion channel selection mode
0	Select mode
1	**Scan mode**

Bits 5-1

A/D converter mode register 0 (ADM0)					Mode	Conversion time selection					Conv. clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz	
0	0	0	**0**	**0**	**Normal 1**	Setting prohibited	Setting prohibited	Setting prohibited	76 µs	50.667 µs	$f_{CLK}/64$
0	0	1						76 µs	38 µs	25.333 µs	$f_{CLK}/32$
0	1	0					76 µs	38 µs	19 µs	12.667 µs	$f_{CLK}/16$
0	**1**	**1**					38 µs	19 µs	9.5 µs	**6.333 µs**	**$f_{CLK}/8$**
1	0	0					28.5 µs	14.25 µs	7.125 µs	4.75 µs	$f_{CLK}/6$
1	0	1				95 µs	23.75 µs	11.875 µs	5.938 µs	3.958 µs	$f_{CLK}/5$
1	1	0				76 µs	19 µs	9.5 µs	4.75 µs	3.167 µs	$f_{CLK}/4$
1	1	1				38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited	$f_{CLK}/2$
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	68 µs	45.333 µs	$f_{CLK}/64$
0	0	1						68 µs	34 µs	22.667 µs	$f_{CLK}/32$
0	1	0					68 µs	34 µs	17 µs	11.333 µs	$f_{CLK}/16$
0	1	1					34 µs	17 µs	8.5 µs	5.667 µs	$f_{CLK}/8$
1	0	0					25.5 µs	12.75 µs	6.375 µs	4.25 µs	$f_{CLK}/6$
1	0	1				85 µs	21.25 µs	10.625 µs	5.3125µs	3.542 µs	$f_{CLK}/5$
1	1	0				68 µs	17 µs	8.5 µs	4.25 µs	2.833 µs	$f_{CLK}/4$
1	1	1				34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited	$f_{CLK}/2$

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.

Symbol	7	6	5	4	3	2	1	0
ADM1	**ADTMD1**	**ADTMD0**	**ADSCM**	**0**	**0**	**0**	**ADTRS1**	**ADTRS0**
Set value	**0**	×	**1**	0	0	0	×	×

Bits 7-6

ADTMD1	ADTMD0	Selection of A/D conversion trigger mode
0	**-**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 2 (ADM2)
  Selects the A/D converter reference voltage source, checks the conversion result against upper-limit/lower-limit value, and selects A/D conversion resolution.

Symbol	7	6	5	4	3	2	1	0
ADM2	**ADREFP1**	**ADREFP0**	**ADREFM**	**0**	**ADRCK**	**AWC**	**0**	**ADTYP**
Set value	**0**	**0**	**0**	0	**0**	×	0	**0**

Bits 7-6

ADREFP1	ADREFP0	Selection of + side reference voltage source of A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from internal reference voltage (1.45 V)
1	1	Setting prohibited
Before rewriting ADREFP1 or ADREFP0 bit, set ADREFP1 and ADREFP0 bits to 0 and 0. When setting ADREFP1 and ADREFP0 bits to 1 and 0, respectively, this must be configured in accordance with the following procedures. (1) Set ADCE = 0 (2) Set ADREFP1 and ADREFP0 to 1 and 0, respectively. (3) Set ADCE = 1 A wait time (T.B.D) is necessary after (2) and (3). When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output. Be sure to perform A/D conversion while ADISS = 0.		

Bit 5

ADREFM	Selection of – side reference voltage source of A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADRCK	Checking upper limit and lower limit conversion result values
0	**Interrupt signal (INTAD) is generated when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	Interrupt signal (INTAD) is generated when ADCR register < ADLL register, ADUL register < ADCR register.

Bit 0

ADTYP	Selection of A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting upper limit value for conversion result comparison

- Conversion result comparison upper limit setting register (ADUL)
  Sets the upper limit conversion result compare value to FFH.

Symbol	7	6	5	4	3	2	1	0
ADUL	**ADUL7**	**ADUL6**	**ADUL5**	**ADUL4**	**ADUL3**	**ADUL2**	**ADUL1**	**ADUL0**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Setting lower limit values for conversion result comparison

- Conversion result comparison lower limit setting register (ADLL)
  Sets the lower limit conversion result compare value to 00H.

Symbol	7	6	5	4	3	2	1	0
ADLL	**ADLL7**	**ADLL6**	**ADLL5**	**ADLL4**	**ADLL3**	**ADLL2**	**ADLL1**	**ADLL0**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Setting analog input channels

- Analog input channel specification register (ADS)
  Set analog input channels to ANI0 to ANI3.

Symbol	7	6	5	4	3	2	1	0
ADS	**ADISS**	**0**	**0**	**ADS4**	**ADS3**	**ADS2**	**ADS1**	**ADS0**
Set value	**0**	0	0	**0**	**0**	**0**	**0**	**0**

- Scan mode (ADMD = 1)

Bits 7, 4-0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel			
						Scan 0	Scan 1	Scan 2	Scan 3
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**ANI1**	**ANI2**	**ANI3**
Other than the above						Setting prohibited			

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  Starts A/D voltage comparator operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation.
1	**Enables A/D voltage comparator operation.**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(6) Initial Setting of DTC

Figure 7.10 shows the initial setting of the DTC.

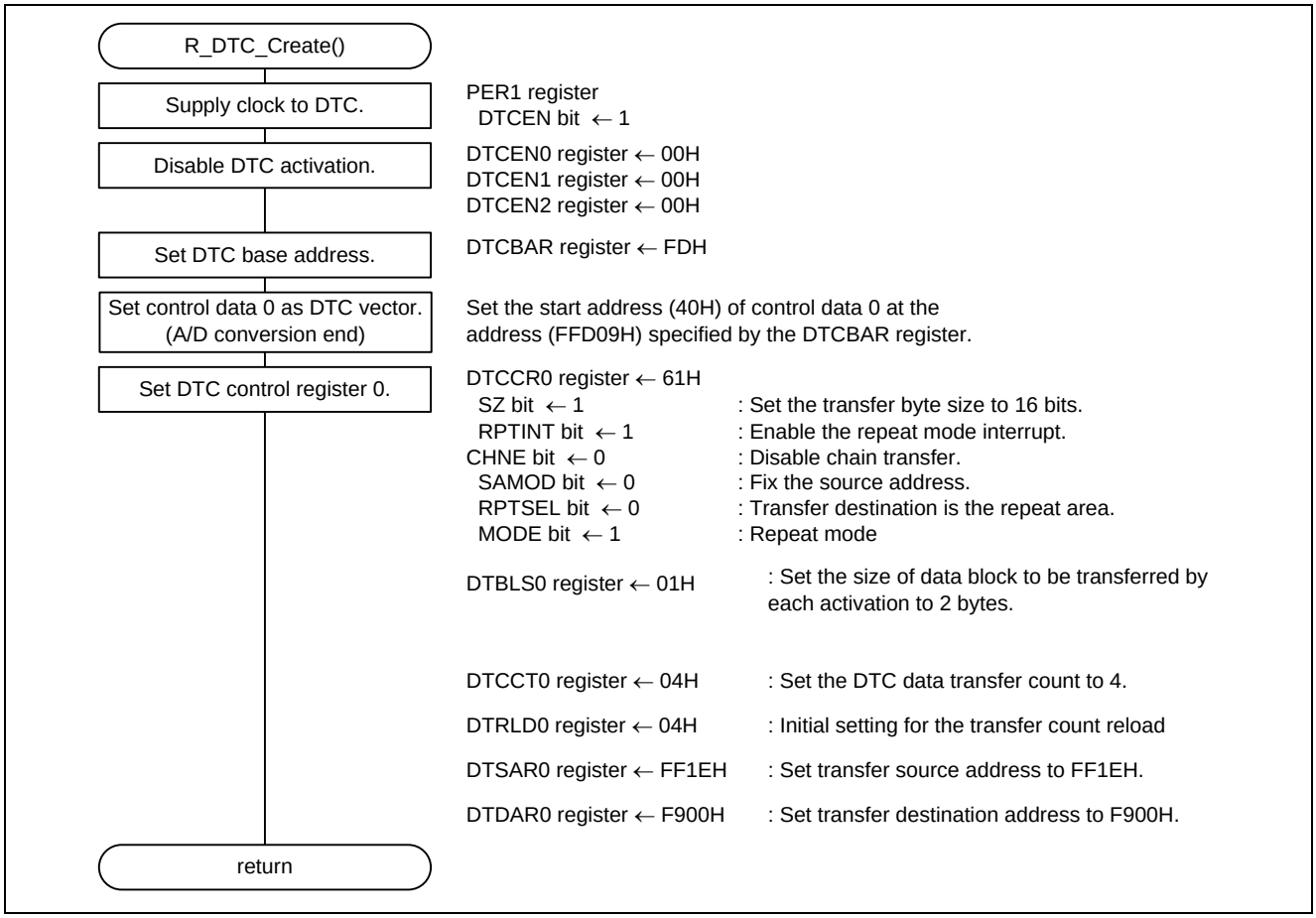


Figure 7.10 Initial Setting of DTC (example of migration from single sweep mode)

Starting clock supply to DTC

- Peripheral enable register 1 (PER1)
  Starts supplying clock to the DTC.

Symbol	7	6	5	4	3	2	1	0
PER1	**DACEN**	**0**	**CMPEN**	**0**	**DTCEN**	**PGA0EN**	**0**	**0**
Set value	×	0	×	0	**1**	×	0	0

Bit 3

DTCEN	Control of DTC input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Disabling DTC activation

- DTC activation enable register i (DTCENi) (i = 0 to 2)
  Disables DTC activation.

Symbol	7	6	5	4	3	2	1	0
DTCENi	**DTCENi7**	**DTCENi6**	**DTCENi5**	**DTCENi4**	**DTCENi3**	**DTCENi2**	**DTCENi1**	**DTCENi0**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7

DTCENi7	DTC activation enable i7
0	**Activation disabled**
1	Activation enabled
The DTCENi7 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 6

DTCENi6	DTC activation enable i6
0	**Activation disabled**
1	Activation enabled
The DTCENi6 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 5

DTCENi5	DTC activation enable i5
0	**Activation disabled**
1	Activation enabled
The DTCENi5 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Bit 4

DTCENi4	DTC activation enable i4
0	**Activation disabled**
1	Activation enabled
The DTCENi4 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 3

DTCENi3	DTC activation enable i3
0	**Activation disabled**
1	Activation enabled
The DTCENi3 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 2

DTCENi2	DTC activation enable i2
0	**Activation disabled**
1	Activation enabled
The DTCENi2 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 1

DTCENi1	DTC activation enable i1
0	**Activation disabled**
1	Activation enabled
The DTCENi1 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 0

DTCENi0	DTC activation enable i0
0	**Activation disabled**
1	Activation enabled
The DTCENi0 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Setting DTC base address

- DTC base address register (DTCBAR)
  Sets FDH for the DTC base address.

Symbol	7	6	5	4	3	2	1	0
DTCBAR	**DTCBAR 7**	**DTCBAR 6**	**DTCBAR 5**	**DTCBAR 4**	**DTCBAR 3**	**DTCBAR 2**	**DTCBAR 1**	**DTCBAR 0**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting DTC control register

- DTC control register 0 (DTCCR0)
  Sets the DTC control register 0.

Symbol	7	6	5	4	3	2	1	0
DTCCR0	**0**	**SZ**	**RPTINT**	**CHNE**	**DAMOD**	**SAMOD**	**RPTSEL**	**MODE**
Set value	0	**1**	**1**	**0**	×	**0**	**0**	**1**

Bit 6

SZ	Transfer data size selection
0	8 bits
1	**16 bits**

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	Interrupt generation disabled
1	**Interrupt generation enabled**
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	**Chain transfers disabled**
1	Chain transfers enabled
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 2

SAMOD	Transfer source address control
0	**Fixed**
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

RPTSEL	Repeat area selection
0	**Transfer destination is the repeat area**
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	Normal mode
1	**Repeat mode**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting DTC block size register 0

- DTC block size register 0 (DTBLS0)
  Sets the DTC block size register 0 to 01H (2 bytes).

Symbol	7	6	5	4	3	2	1	0
DTBLS0	**DTBLS07**	**DTBLS06**	**DTBLS05**	**DTBLS04**	**DTBLS03**	**DTBLS02**	**DTBLS01**	**DTBLS00**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

DTBLS0	**Transfer block size**	
	8-bit transfer	**16-bit transfer**
00H	256 bytes	512 bytes
01H	1 byte	**2 bytes**
02H	**2 bytes**	**4 bytes**
03H	3 bytes	6 bytes
.	.	.
.	.	.
.	.	.
FDH	253 bytes	506 bytes
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Setting DTC transfer count register 0

- DTC transfer count register 0 (DTCCT0)
  Sets the DTC transfer count register 0 to 04H (4 times).

Symbol	7	6	5	4	3	2	1	0
DTCCT0	**DTCCT07**	**DTCCT06**	**DTCCT05**	**DTCCT04**	**DTCCT03**	**DTCCT02**	**DTCCT01**	**DTCCT00**
Set value	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**

DTCCT0	**Number of transfers**
00H	256 times
01H	Once
02H	2 times
03H	3 times
04H	**4 times**
:	:
:	:
:	:
FDH	253 times
FEH	254 times
FFH	255 times

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting DTC transfer count reload register 0

- DTC transfer count reload register 0 (DTRLD0)
  Sets the DTC transfer count reload register 0 to 04H (4 times).

Symbol	7	6	5	4	3	2	1	0
DTRLD0	**DTRLD07**	**DTRLD06**	**DTRLD05**	**DTRLD04**	**DTRLD03**	**DTRLD02**	**DTRLD01**	**DTRLD00**
Set value	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**

Setting DTC source address register 0

- DTC source address register 0 (DTSAR0)
  Set the DTC source address register 0 to the transfer source address FF1EH.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR0	**DTSAR015**	**DTSAR014**	**DTSAR013**	**DTSAR012**	**DTSAR011**	**DTSAR010**	**DTSAR09**	**DTSAR08**	**DTSAR07**	**DTSAR06**	**DTSAR05**	**DTSAR04**	**DTSAR03**	**DTSAR02**	**DTSAR01**	**DTSAR00**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**

Setting DTC destination address register 0

- DTC destination address register 0 (DTDAR0)
  Set the DTC destination address register 0 to the transfer destination address F900H.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR0	**DTDAR015**	**DTDAR014**	**DTDAR013**	**DTDAR012**	**DTDAR011**	**DTDAR010**	**DTDAR09**	**DTDAR08**	**DTDAR07**	**DTDAR06**	**DTDAR05**	**DTDAR04**	**DTDAR03**	**DTDAR02**	**DTDAR01**	**DTDAR00**
Set value	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(7) Main Processing

Figure 7.11 shows the flowchart for the main processing.

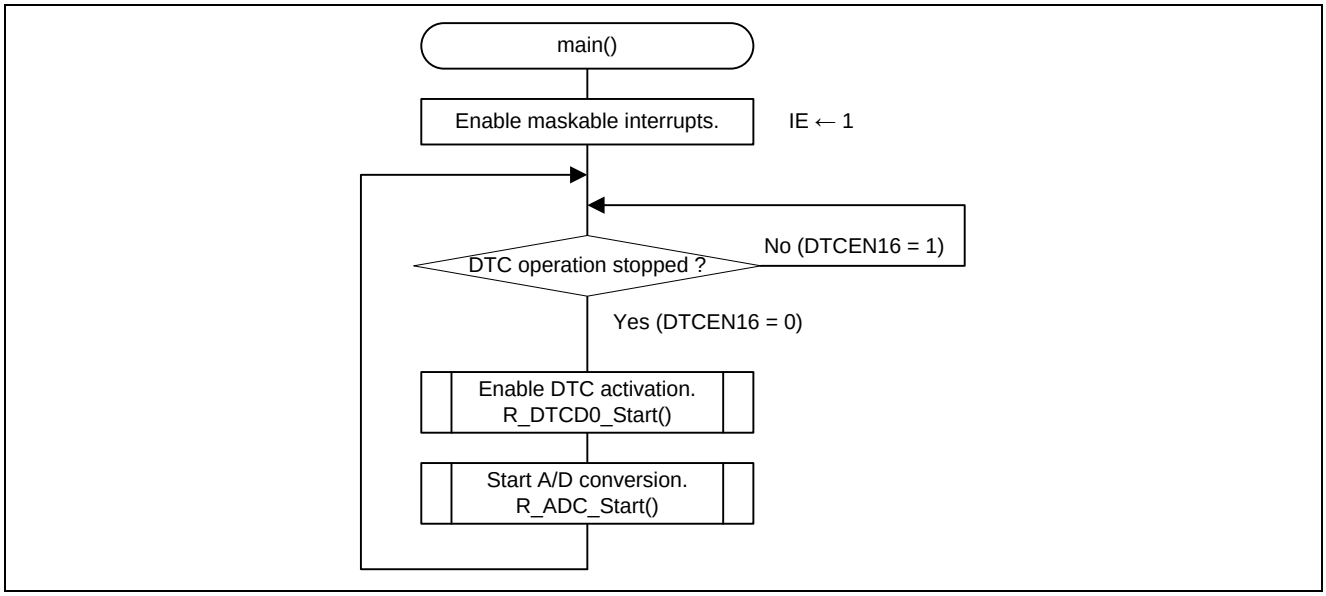


Figure 7.11 Main Processing (example of migration from single sweep mode)

(8) Enabling DTC Activation

Figure 7.12 shows the flowchart for enabling DTC activation.

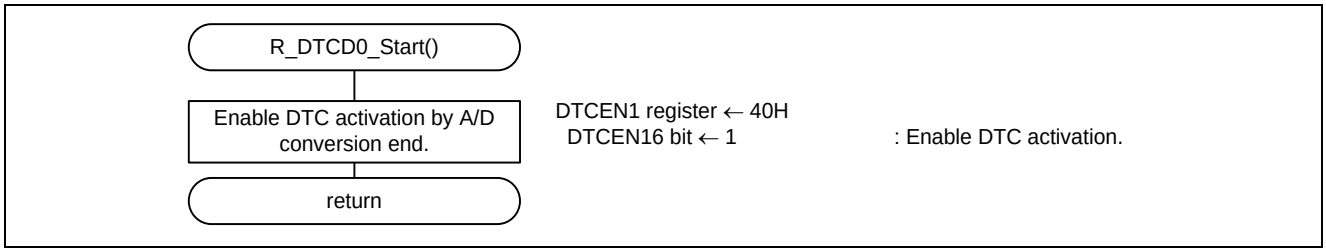


Figure 7.12 Enabling DTC Activation (example of migration from single sweep mode)

Enabling DTC activation

- DTC activation enable register 1 (DTCEN1)
  Enables DTC activation by the A/D conversion end.

Symbol	7	6	5	4	3	2	1	0
DTCEN1	**DTCEN17**	**DTCEN16**	**DTCEN15**	**DTCEN14**	**DTCEN13**	**DTCEN12**	**DTCEN11**	**DTCEN10**
Set value	×	**1**	×	×	×	×	×	×

Bit 6

DTCEN16	DTC activation enable 16 (DTC activation source: A/D conversion end)
0	Activation disabled
1	**Activation enabled**
The DTCEN16 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(9) Staring A/D Conversion

Figure 7.13 shows the flowchart for starting A/D conversion.

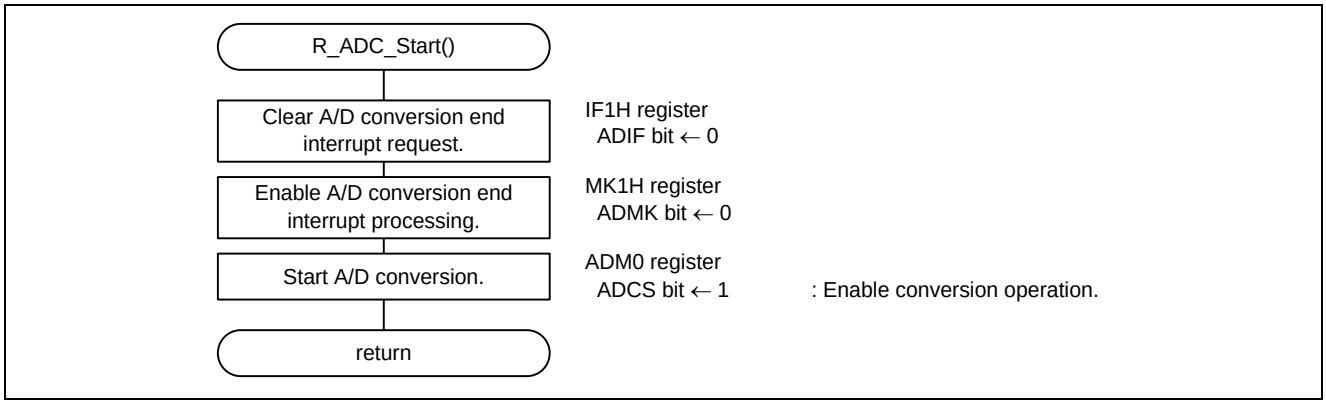


Figure 7.13 Starting A/D Conversion (example of migration from single sweep mode)

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	**Interrupt request flag**
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Enabling A/D conversion end interrupt

- Interrupt mask flag register (MK1H)
  Enables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Starting A/D converter

- A/D converter mode register 0 (ADM0)
  Starts A/D conversion operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**1**	×	×	×	×	×	×	×

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	**Enables conversion operation** **[When read]** **While in the software trigger mode: Conversion operation status** **While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(10) A/D conversion end interrup

Figure 7.14 shows the flowchart for A/D conversion end interrupt processing.

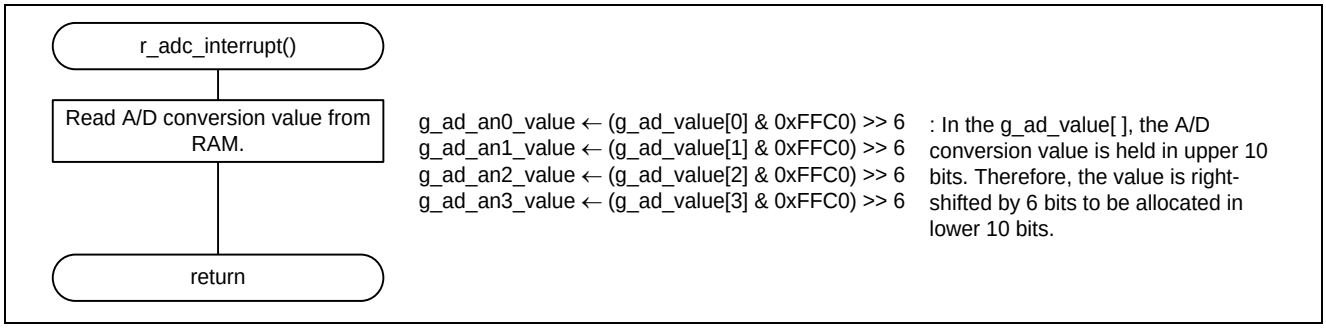


Figure 7.14 A/D Conversion End Interrupt (example of migration from single sweep mode)

7.5 Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7.6 Reference Application Note

- RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: A/D Converter CC-RL (R01AN3059)

- RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: Data Transfer Controller (R01AN1503)

- RL78/G14 How to Use the DTC for the RL78/G14 (R01AN0861)

- RL78/G14 Transferring A/D Conversion Result Using the DTC CC-RL (R01AN2574)

7.7 Reference Documents

User's Manual

- RL78/G11 User's Manual: Hardware
  (The latest versions can be downloaded from the Renesas Electronics website.)

- R8C/32C Group Hardware Manual
  (The latest versions can be downloaded from the Renesas Electronics website.)

- Technical Update/Technical News
  (The latest information can be downloaded from the Renesas Electronics website.)

Migration Guide

- Migration to CubeSuite+ Integrated Development Environment for RL78 Family
  (On-chip Debug) - Migration from R8C, M16C to RL78 (R20UT2150)

8. Example of Migration from Repeat Sweep Mode

8.1 Specifications

To implement R8C/32C repeat sweep mode in the RL78/G11, the AD converter (software trigger, scan, sequential conversion mode) and DTC transfer (repeat mode) are used.

The analog input voltage of the ANI0 to ANI3 pins is A/D-converted in scan mode and sequential conversion mode, and the A/D conversion result values are stored in the RAM assigned to each pin by DTC transfer. Specifically, A/D conversion on the pins is sequentially performed; each time A/D conversion on one pin ends, the conversion result is stored in the 10-bit A/D conversion result register (ADCR), and an A/D conversion end interrupt signal is generated. In response to the interrupt signal, the DTC is activated, and the A/D conversion result is transferred from the ADCR register to the RAM. When A/D conversion and DTC transfer on all the pins are completed, an A/D conversion end interrupt request is generated.

Table 8.1 shows the peripheral functions used and the purpose of use, and Figure 8.1 shows the operation summary.

Table 8.1 Peripheral Functions Used and Purpose of Use (example of migration from repeat sweep mode)

Peripheral Function	Purpose of Use
A/D converter	Performs A/D conversion on the analog input voltage.
DTC	Transfers A/D conversion result to RAM.

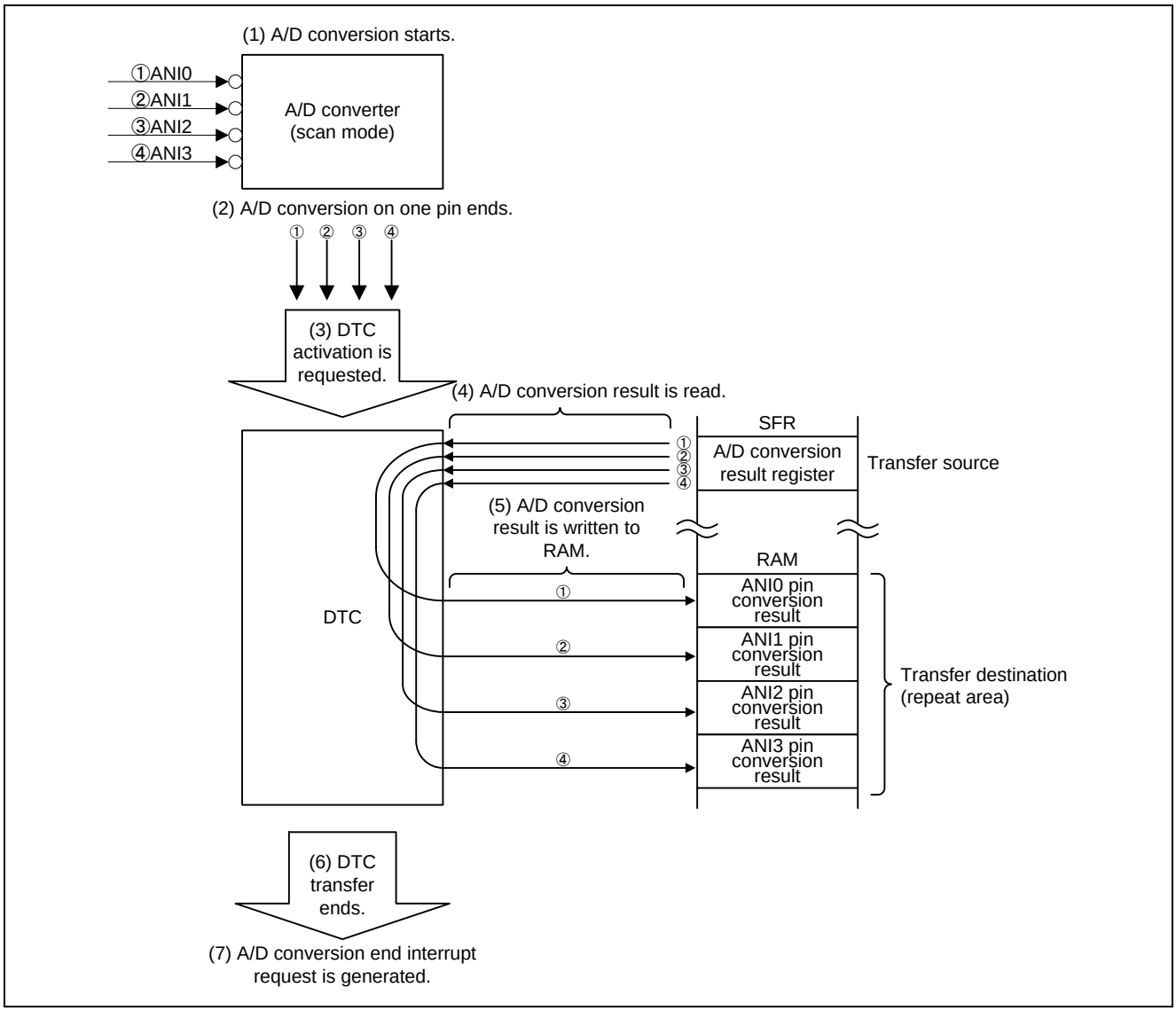


Figure 8.1 Operation Summary (example of migration from repeat sweep mode)

8.2 Conditions for Confirming Operations

The sample code operations described in this application note are confirmed under the following conditions.

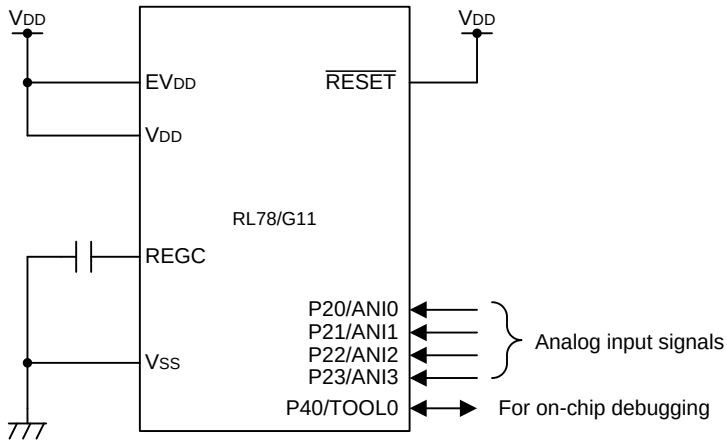
Table 8.2 Conditions for Confirming Operations (example of migration from repeat sweep mode)

Item	Description
Microcontroller used	RL78/G11 (R5F1056A)
Operating frequency	• High-speed on-chip oscillator clock (f_{IH}): 24 MHz • CPU/peripheral hardware clock (f_{CLK}): 24 MHz
Operating voltage	5.0 V (can be operated from 3.6 V to 5.5 V) LVD operation (V_{LVD}): Reset mode; rise 3.13 V/fall 3.06 V
Integrated development environment (CS+)	CS+ for CC V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.4.0.015 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.

8.3 Hardware Descriptions

8.3.1 Hardware Configuration Example

Figure 8.2 shows an example of the hardware configuration used for this application.



Note 1: The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied. Input-only ports should be each connected to V_{DD} or V_{SS} via a resistor.

Note 2: Any pin whose name begins with EV_{DD} should be connected to V_{DD}.

Note 3: V_{DD} should be equal to or greater than the reset-release voltage (V_{LVD}) specified for the LVD.

Figure 8.2 Hardware Configuration (example of migration from repeat sweep mode)

8.3.2 List of Pins Used

Table 8.3 lists the pins used and their functions.

Table 8.3 Pins Used and Their Functions (example of migration from repeat sweep mode)

Pin Name	I/O	Function
P20/ANI0	Input	A/D converter input (ANI0)
P21/ANI1	Input	A/D converter input (ANI1)
P22/ANI2	Input	A/D converter input (ANI2)
P23/ANI3	Input	A/D converter input (ANI3)

8.4 Software Descriptions

8.4.1 Operation Summary

With this sample program, the A/D conversion on four pins is performed in scan mode, and the conversion results are stored in the RAM by DTC transfer. The DTC is used in repeat mode with the transfer destination set as repeat area, and the conversion results on the four pins are sequentially stored in the RAM. By setting sequential conversion mode, A/D conversion on the four pins is repeated.

Upon completion of the A/D conversion on the ANI0 pin, the first DTC transfer is performed from the transfer source addresses (ADCR register (FFF1EH, FFF1FH)) to the transfer destination addresses (g_ad_value[0] (FF900H to FF901H)). Upon completion of the A/D conversion on the ANI1 pin, the second DTC transfer is performed to g_ad_value[1] (FF902H to FF903H) since the transfer destination is set as the repeat area. Similarly, the A/D conversion results of the ANI3 and ANI4 pins are DTC-transferred. Upon completion of the fourth transfer, an A/D conversion end interrupt is generated.

In interrupt processing, the A/D conversion results stored in the array g_ad_value[] (FF900H to FF907H) are relocated in the lower 10 bits before being stored in the buffers for storing the A/D conversion results (variable g_ad _an0_value to g_ad_an3_value).

After this, the above sequence is repeated to update the acquired A/D conversion results.

Table 8.4 shows the A/D converter settings and Table 8.5 shows the DTC settings.

Table 8.4 A/D Converter Settings (example of migration from repeat sweep mode)

Item to be Set	Settings
Conversion clock frequency (f_{AD})	f_{CLK}/8
A/D conversion mode	• A/D conversion trigger mode: Software trigger • A/D conversion channel selection mode: Scan mode • A/D conversion operation mode: Sequential conversion mode
Resolution	10 bits
Analog input channel	• Scan 0: ANI0 • Scan 1: ANI1 • Scan 2: ANI2 • Scan 3: ANI3
A/D conversion result comparison upper limit (ADUL register)	FFH
A/D conversion result comparison lower limit(ADLL register)	00H
Upper and lower limit conversion result checking	INTAD generated when ADLL register ≤ ADCR register ≤ ADUL register

Table 8.5 DTC Settings (example of migration from repeat sweep ode)

Item to be Set	Settings
	Control Data 0
Transfer mode	Repeat mode
Repeat mode interrupt	Enabled
Source address control	Fixed
Destination address control	Repeat area
Chain transfer control	Disabled
Transfer block size	2 bytes (16-bit transfer)
DTC transfer count	4
Transfer source address	ADCR (FFF1EH to FFF1FH)
Transfer destination address	g_ad_value[0] (FF900H to FF901H), g_ad_value[1] (FF902H to FF903H), g_ad_value[2] (FF904H to FF905H), g_ad_value[3] (FF906H to FF907H)

(1) The initial setting is made for the A/D converter and DTC.
(2) The ADCS bit in the ADM0 register is set to 1 (conversion enabled) to start A/D conversion.
(3) Upon completion of the A/D conversion on each of the pins (ANI0, ANI1, ANI2, and ANI3 pins), the DTC is activated.
(4) The DTC reads the A/D conversion result from the ADCR register and transfers it to the RAM (g_ad_value[0] to g_ad_value[3]) corresponding to the pin.
(5) Upon completion of the fourth DTC transfer, an A/D conversion end interrupt is generated.
(6) In interrupt processing, DTC activation is again enabled. Also, the A/D conversion results g_ad_value[0] to g_ad_value[3] are shifted to the right by 6 bits (relocated in the lower 10 bits) and stored in the variables g_ad_an0_value to g_ad_an3_value.
(7) After this, steps (2) to (6) are repeated

Figure 8.3 shows the A/D conversion and DTC transfer timing and Figure 8.4 shows the relationship between the ADCR register and RAM.

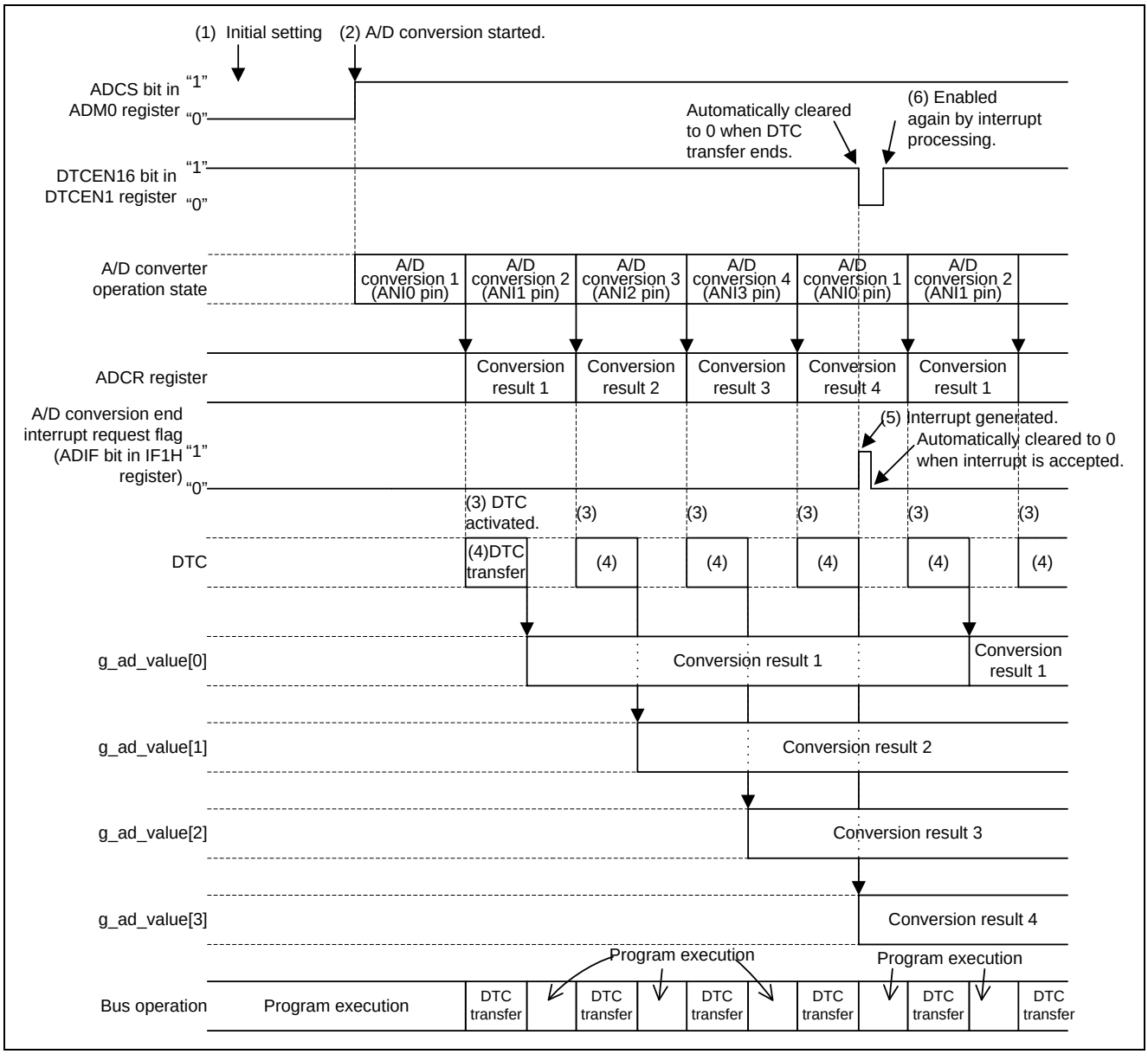


Figure 8.3 A/D Conversion and DTC Transfer Timing (example of migration from repeat sweep mode)

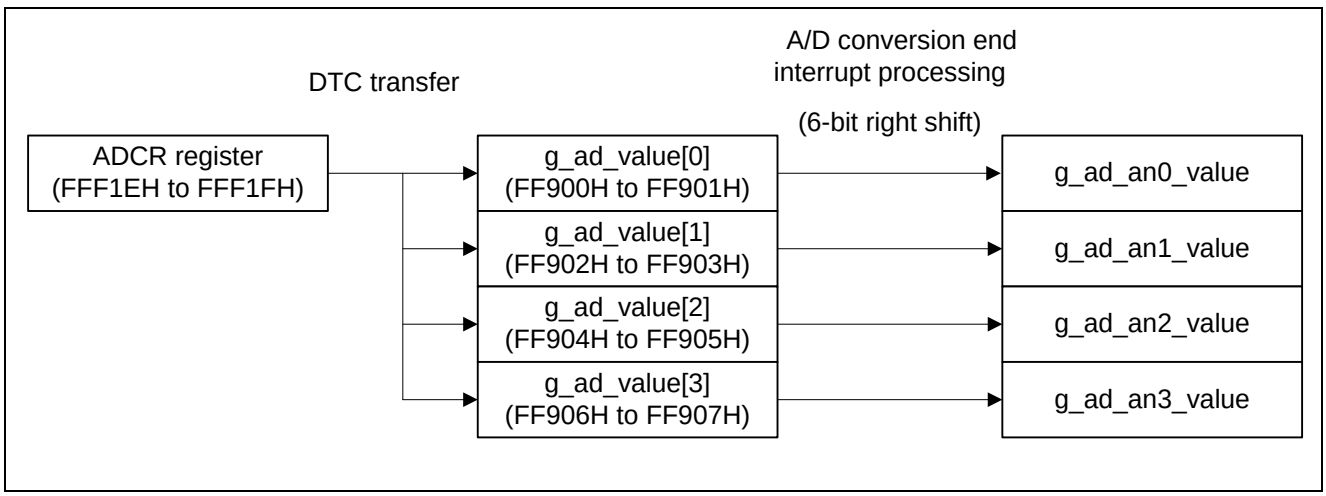


Figure 8.4 Relationship between ADCR Register and RAM
(example of migration from repeat sweep mode)

8.4.2 List of Option Byte Settings

Table 8.6 lists option byte settings.

Table 8.6 Option Byte Settings (example of migration from repeat sweep mode)

Address	Setting	Contents
000C0H/010C0H	01101110B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H/010C1H	00110011B	LVD reset mode Detection voltage: rise 3.13 V/fall 3.06 V
000C2H/010C2H	11100000B	HS mode High-speed on-chip oscillator clock frequency: 24 MHz
000C3H/010C3H	10000100B	On-chip debugging is enabled.

8.4.3 List of Constants

Table 8.7 lists the constant used in the sample code.

Table 8.7 Constant Used in Sample Code (example of migration from repeat sweep mode)

Constant Name	Setting	Contents
AD_RESULT_ADDR	0FF900H	Transfer destination address of A/D conversion result

8.4.4 List of Variables

Table 8.8 lists the global variables.

Table 8.8 Global Variables (example of migration from repeat sweep mode)

Type	Variable Name	Contents	Function Used
uint16_t __near	g_ad_value[4]	Buffer for storing A/D conversion results of ANI0 to ANI3	r_adc_interrupt
uint16_t	g_ad_an0_value	Buffer for storing A/D conversion result of ANI0	r_adc_interrupt
uint16_t	g_ad_an1_value	Buffer for storing A/D conversion result of ANI1	r_adc_interrupt
uint16_t	g_ad_an2_value	Buffer for storing A/D conversion result of ANI2	r_adc_interrupt
uint16_t	g_ad_an3_value	Buffer for storing A/D conversion result of ANI3	r_adc_interrupt

8.4.5 Functions

Table 8.9 lists the Functions.

Table 8.9 Functions (example of migration from repeat sweep mode)

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	CPU initial setting
R_ADC_Create	Initial setting of A/D converter
R_DTC_Create	Initial setting of DTC
main	Main processing
R_DTCD0_Start	DTC activation
R_ADC_Start	A/D conversion start
r_adc_interrupt	A/D conversion interrupt

8.4.6 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	CPU initial setting
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_ADC_Create	
Outline	Initial setting of A/D converter
Header	None
Declaration	void R_ADC_Create(void)
Description	Perform the initial setting to use the A/D converter in software trigger mode, scan mode, and sequential conversion mode.
Argument	None
Return Value	None

R_DTC_Create	
Outline	Initial setting of DTC
Header	None
Declaration	void R_DTC_Create(void)
Description	Perform the initial setting to use the DTC in repeat mode.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_DTCD0_Start	
Outline	DTC activation
Header	None
Declaration	void R_DTCD0_Start(void)
Description	Enable DTC activation.
Argument	None
Return Value	None

R_ADC_Start	
Outline	A/D conversion start
Header	None
Declaration	void R_ADC_Start(void)
Description	Perform A/D conversion.
Argument	None
Return Value	None

r_adc_interrupt	
Outline	A/D conversion interrupt
Header	None
Declaration	static void __near r_adc_interrupt(void)
Description	Perform an A/D conversion end interrupt service routine.
Argument	None
Return Value	None

8.4.7 Flowcharts

(1) Overall Flowchart

Figure 8.5 shows the Overall Flowchart.

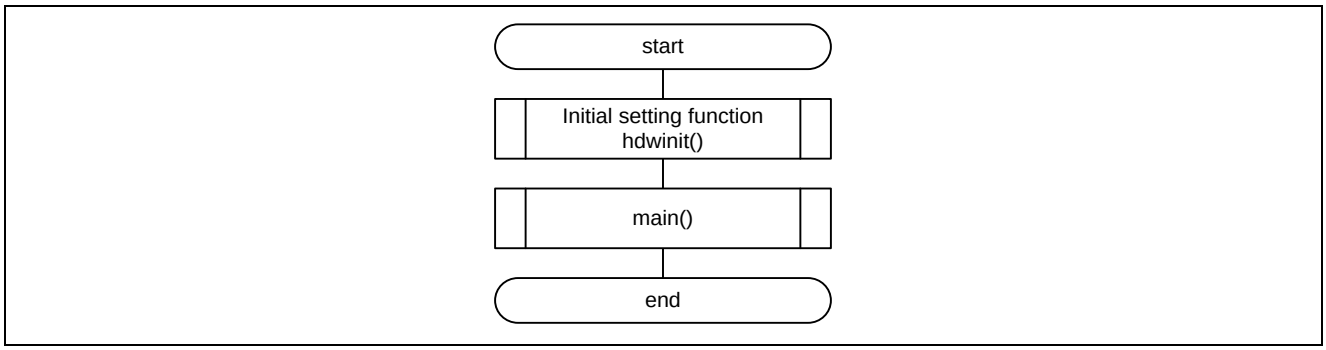


Figure 8.5 Overall Flowchart (example of migration from repeat sweep mode)

(2) Initial Setting

Figure 8.6 shows the Initial Setting.

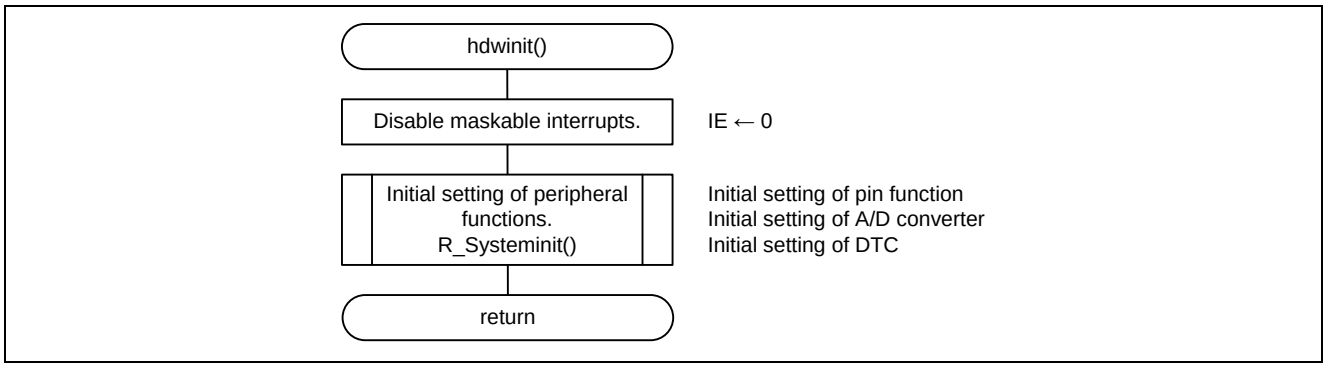


Figure 8.6 Initial Setting (example of migration from repeat sweep mode)

(3) Initial Setting of Peripheral Functions

Figure 8.7 shows the initial setting of peripheral functions.

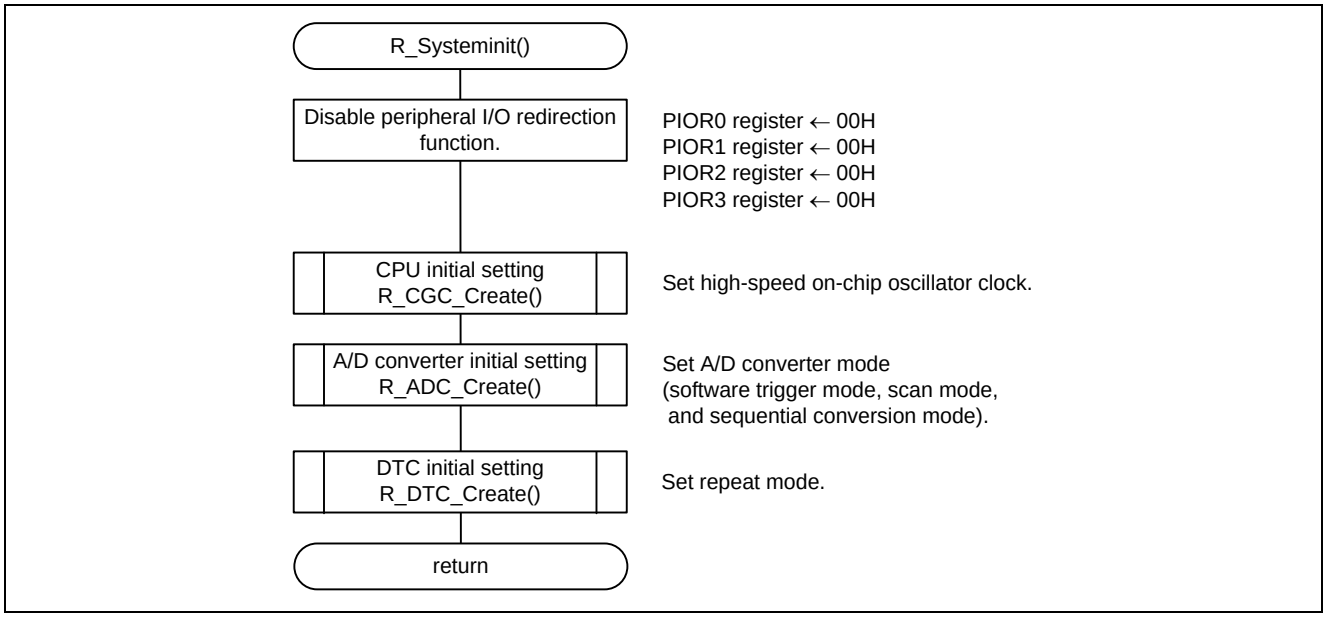


Figure 8.7 Initial Setting of Peripheral Functions (example of migration from repeat sweep mode)

(4) Initial Setting of CPU

Figure 8.8 shows the initial setting of the CPU.

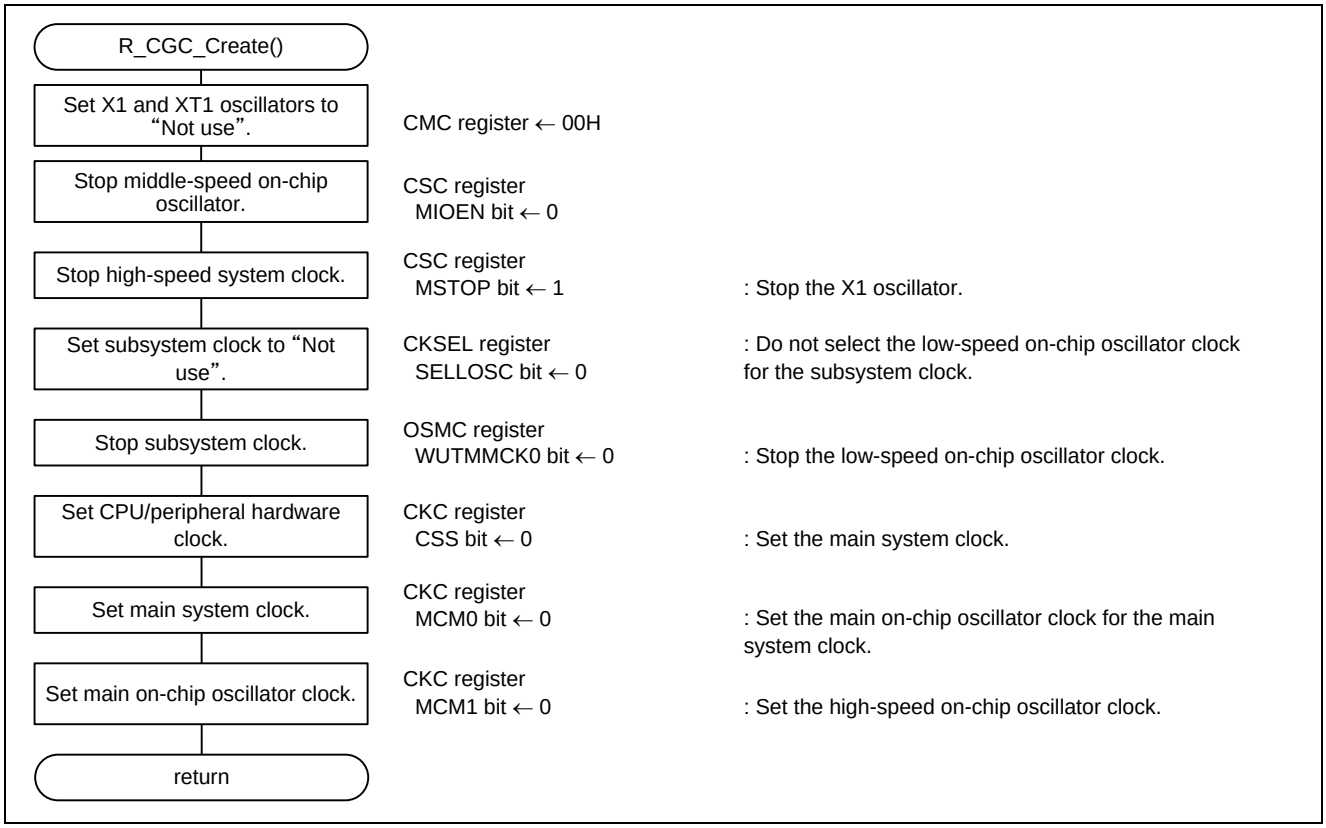


Figure 8.8 Initial Setting of CPU (example of migration from repeat sweep mode)

(5) Initial Setting of A/D Converter

Figure 8.9 shows the initial setting of the A/D converter.

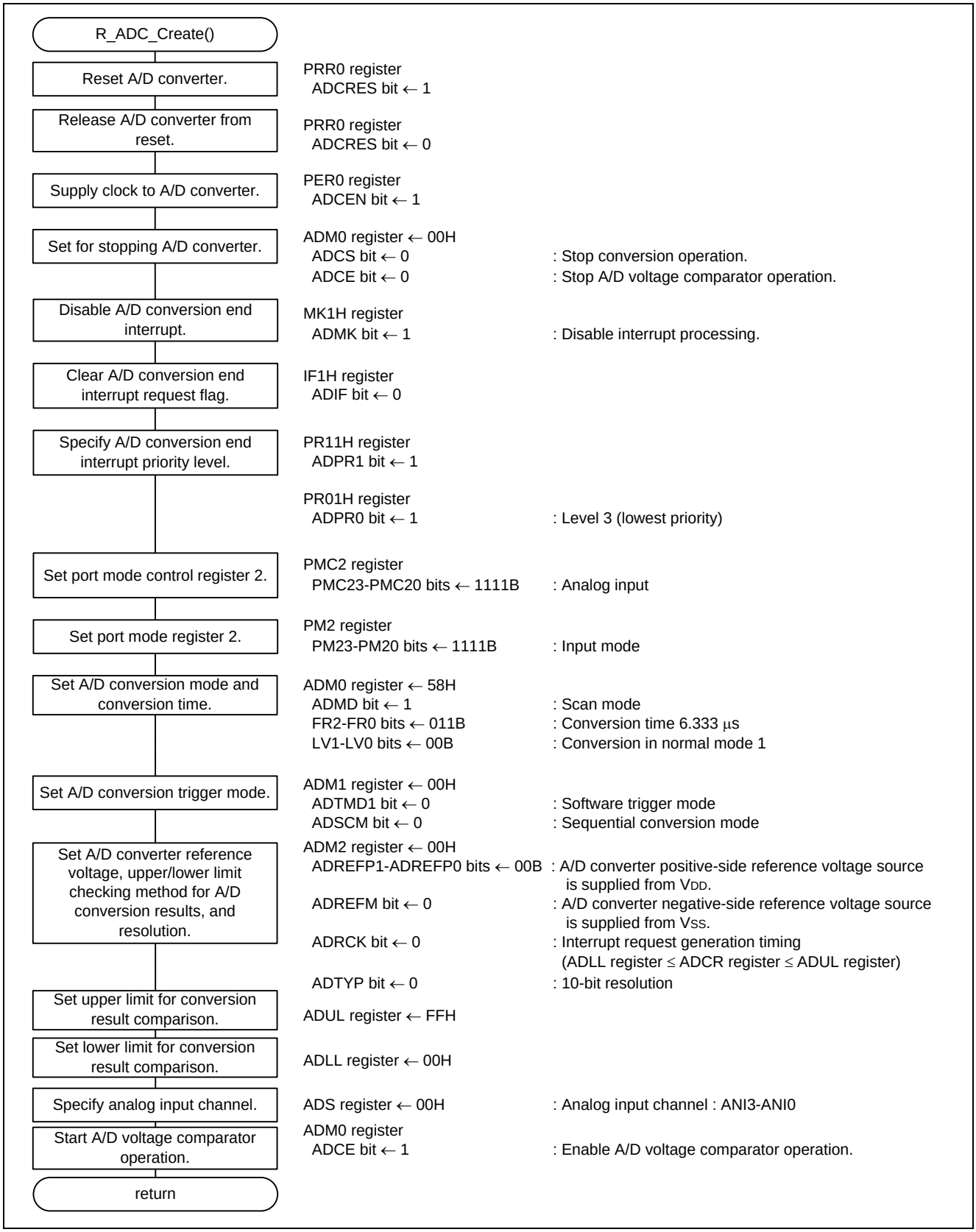


Figure 8.9 Initial Setting of A/D Converter (example of migration from repeat sweep mode)

Controlling reset of A/D converter

- Peripheral reset control register 0 (PRR0)
  Resets or releases the A/D converter from the reset state.

Symbol	7	6	5	4	3	2	1	0
PRR0	**0**	**IICA1RES**	**ADCRES**	**IICA0RES**	**0**	**SAU0RES**	**0**	**TAU0RES**
Set value	0	×	**0/1**	×	0	×	0	×

Bit 5

ADCRES	Reset control of A/D converter
0	**A/D converter reset release**
1	**A/D converter reset state**

Starting clock supply to A/D converter

- Peripheral enable register 0 (PER0)
  Starts supplying clock to the A/D converter.

Symbol	7	6	5	4	3	2	1	0
PER0	**0**	**IICA1EN**	**ADCEN**	**IICA0EN**	**0**	**SAU0EN**	**0**	**TAU0EN**
Set value	0	×	**1**	×	0	×	0	×

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.Stops input clock supply. • SFR used by the A/D converter cannot be written.
1	**Enables input clock supply.** • SFR used by the A/D converter can be read and written.

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Stopping A/D converter operation

- A/D converter mode register 0 (ADM0)
  Stops A/D converter.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**0**	×	×	×	×	×	×	**0**

Bit 7

ADCS	A/D conversion operation control
0	**Stops conversion operation.** **[When read]** **Conversion stopped/standby status**
1	Enables conversion operation. [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status

Bit 0

ADCE	A/D voltage comparator operation control
0	**Stops A/D voltage comparator operation.**
1	Enables A/D voltage comparator operation.

Disabling A/D conversion end interrupt

- Interrupt mask flag register 1 (MK1H)
  Disables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Specifying A/D conversion end interrupt priority level

- Priority specification flag register (PR11H, PR01H)
  Specifies level 3 (lowest priority level).

Symbol	7	6	5	4	3	2	1	0
PR11H	**PPR111**	**PPR110**	**PPR19**	**PPR18**	**PPR17**	**KRPR1**	**TMKAPR1**	**ADPR1**
Set value	×	×	×	×	×	×	×	**1**

Symbol	7	6	5	4	3	2	1	0
PR01H	**PPR011**	**PPR010**	**PPR09**	**PPR08**	**PPR07**	**KRPR0**	**TMKAPR0**	**ADPR0**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADPR1	ADPR0	Priority level selection
0	0	Specifies level 0 (high priority level).
0	1	Specifies level 1.
1	0	Specifies level 2.
1	**1**	**Specifes level 3 (low priority level).**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting port mode control register 2

- Port mode control register 2 (PMC2)
  Sets the port mode control register 2 to analog input.

Symbol	7	6	5	4	3	2	1	0
PMC2	**1**	**1**	**1**	**1**	**PMC23**	**PMC22**	**PMC21**	**PMC20**
Set value	1	1	1	1	**1**	**1**	**1**	**1**

Bits 3-0

PMC2n	P2n pin digital I/O/analog input selection
0	Digital I/O (alternate function other than analog input)
1	**Analog input**

Remark n: Channel number (n = 0 to 3)

Setting port mode register 2

- Port mode register 2 (PM2)
  Sets the port mode register 2 to input mode.

Symbol	7	6	5	4	3	2	1	0
PM2	**1**	**1**	**1**	**1**	**PM23**	**PM22**	**PM21**	**PM20**
Set value	1	1	1	1	**1**	**1**	**1**	**1**

Bits 3-0

PM2n	P2n pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Remark n: Channel number (n = 0 to 3)

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion mode and conversion time

- A/D converter mode register 0 (ADM0)
  Sets the A/D conversion mode and conversion time.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	**1**	**0**	**1**	**1**	**0**	**0**	×

Bit 6

ADMD	Specification of A/D conversion channel selection mode
0	Select mode
1	**Scan mode**

Bits 5-1

A/D converter mode register 0 (ADM0)					Mode	Conversion time selection					Conv. clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 24 MHz	
0	0	0	**0**	**0**	**Normal 1**	Setting prohibited	Setting prohibited	Setting prohibited	76 µs	50.667 µs	$f_{CLK}/64$
0	0	1						76 µs	38 µs	25.333 µs	$f_{CLK}/32$
0	1	0					76 µs	38 µs	19 µs	12.667 µs	$f_{CLK}/16$
0	**1**	**1**					38 µs	19 µs	9.5 µs	**6.333 µs**	**$f_{CLK}/8$**
1	0	0					28.5 µs	14.25 µs	7.125 µs	4.75 µs	$f_{CLK}/6$
1	0	1				95 µs	23.75 µs	11.875 µs	5.938 µs	3.958 µs	$f_{CLK}/5$
1	1	0				76 µs	19 µs	9.5 µs	4.75 µs	3.167 µs	$f_{CLK}/4$
1	1	1				38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited	$f_{CLK}/2$
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	68 µs	45.333 µs	$f_{CLK}/64$
0	0	1						68 µs	34 µs	22.667 µs	$f_{CLK}/32$
0	1	0					68 µs	34 µs	17 µs	11.333 µs	$f_{CLK}/16$
0	1	1					34 µs	17 µs	8.5 µs	5.667 µs	$f_{CLK}/8$
1	0	0					25.5 µs	12.75 µs	6.375 µs	4.25 µs	$f_{CLK}/6$
1	0	1				85 µs	21.25 µs	10.625 µs	5.3125µs	3.542 µs	$f_{CLK}/5$
1	1	0				68 µs	17 µs	8.5 µs	4.25 µs	2.833 µs	$f_{CLK}/4$
1	1	1				34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited	$f_{CLK}/2$

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.

Symbol	7	6	5	4	3	2	1	0
ADM1	**ADTMD1**	**ADTMD0**	**ADSCM**	**0**	**0**	**0**	**ADTRS1**	**ADTRS0**
Set value	**0**	×	**0**	0	0	0	×	×

Bits 7-6

ADTMD1	ADTMD0	Selection of A/D conversion trigger mode
0	**-**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of A/D conversion mode
0	**Sequential conversion mode**
1	One-shot conversion mode

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 2 (ADM2)
  Selects the A/D converter reference voltage source, checks the conversion result against upper-limit/lower-limit value, and selects A/D conversion resolution.

Symbol	7	6	5	4	3	2	1	0
ADM2	**ADREFP1**	**ADREFP0**	**ADREFM**	**0**	**ADRCK**	**AWC**	**0**	**ADTYP**
Set value	**0**	**0**	**0**	0	**0**	×	0	**0**

Bits 7-6

ADREFP1	ADREFP0	Selection of + side reference voltage source of A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from internal reference voltage (1.45 V)
1	1	Setting prohibited
Before rewriting ADREFP1 or ADREFP0 bit, set ADREFP1 and ADREFP0 bits to 0 and 0. When setting ADREFP1 and ADREFP0 bits to 1 and 0, respectively, this must be configured in accordance with the following procedures. (1) Set ADCE = 0 (2) Set ADREFP1 and ADREFP0 to 1 and 0, respectively. (3) Set ADCE = 1 A wait time (T.B.D) is necessary after (2) and (3). When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output. Be sure to perform A/D conversion while ADISS = 0.		

Bit 5

ADREFM	Selection of – side reference voltage source of A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADRCK	Checking upper limit and lower limit conversion result values
0	**Interrupt signal (INTAD) is generated when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	Interrupt signal (INTAD) is generated when ADCR register < ADLL register, ADUL register < ADCR register.

Bit 0

ADTYP	Selection of A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting upper limit value for conversion result comparison

- Conversion result comparison upper limit setting register (ADUL)
  Sets the upper limit conversion result compare value to FFH.

Symbol	7	6	5	4	3	2	1	0
ADUL	**ADUL7**	**ADUL6**	**ADUL5**	**ADUL4**	**ADUL3**	**ADUL2**	**ADUL1**	**ADUL0**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Setting lower limit values for conversion result comparison

- Conversion result comparison lower limit setting register (ADLL)
  Sets the lower limit conversion result compare value to 00H.

Symbol	7	6	5	4	3	2	1	0
ADLL	**ADLL7**	**ADLL6**	**ADLL5**	**ADLL4**	**ADLL3**	**ADLL2**	**ADLL1**	**ADLL0**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Setting analog input channels

- Analog input channel specification register (ADS)
  Set analog input channels to ANI0 to ANI3.

Symbol	7	6	5	4	3	2	1	0
ADS	**ADISS**	**0**	**0**	**ADS4**	**ADS3**	**ADS2**	**ADS1**	**ADS0**
Set value	**0**	0	0	**0**	**0**	**0**	**0**	**0**

- Scan mode (ADMD = 1)

Bits 7, 4-0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel			
						Scan 0	Scan 1	Scan 2	Scan 3
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**ANI1**	**ANI2**	**ANI3**
Other than the above						Setting prohibited			

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  Starts A/D voltage comparator operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	×	×	×	×	×	×	×	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation.
1	**Enables A/D voltage comparator operation.**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(6) Initial Setting of DTC

Figure 8.10 shows the initial setting of the DTC.

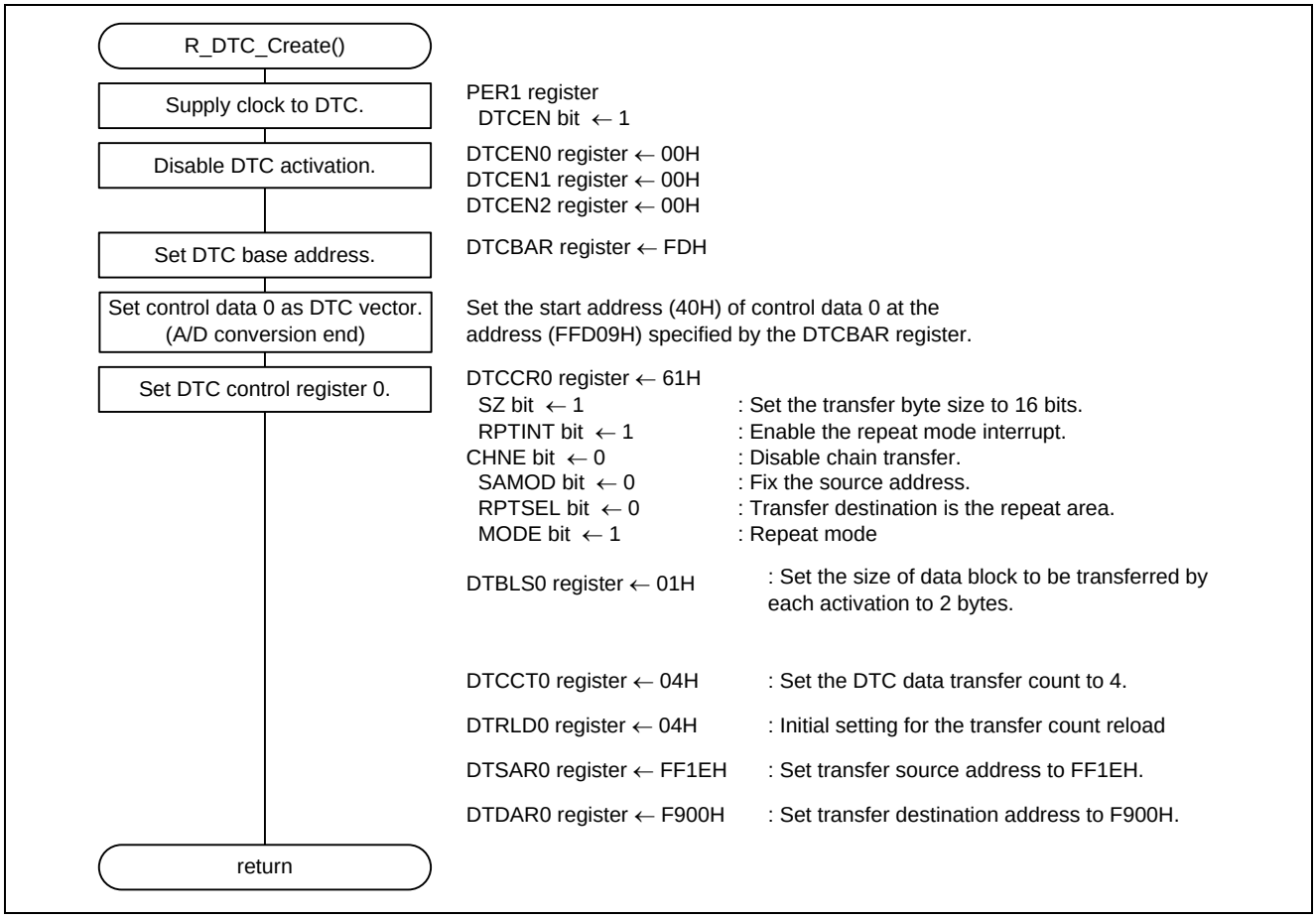


Figure 8.10 Initial Setting of DTC (example of migration from repeat sweep mode)

Starting clock supply to DTC

- Peripheral enable register 1 (PER1)
  Starts supplying clock to the DTC.

Symbol	7	6	5	4	3	2	1	0
PER1	**DACEN**	**0**	**CMPEN**	**0**	**DTCEN**	**PGA0EN**	**0**	**0**
Set value	×	0	×	0	**1**	×	0	0

Bit 3

DTCEN	Control of DTC input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Disabling DTC activation

- DTC activation enable register i (DTCENi) (i = 0 to 2)
  Disables DTC activation.

Symbol	7	6	5	4	3	2	1	0
DTCENi	**DTCENi7**	**DTCENi6**	**DTCENi5**	**DTCENi4**	**DTCENi3**	**DTCENi2**	**DTCENi1**	**DTCENi0**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7

DTCENi7	DTC activation enable i7
0	**Activation disabled**
1	Activation enabled
The DTCENi7 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 6

DTCENi6	DTC activation enable i6
0	**Activation disabled**
1	Activation enabled
The DTCENi6 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 5

DTCENi5	DTC activation enable i5
0	**Activation disabled**
1	Activation enabled
The DTCENi5 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Bit 4

DTCENi4	DTC activation enable i4
0	**Activation disabled**
1	Activation enabled
The DTCENi4 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 3

DTCENi3	DTC activation enable i3
0	**Activation disabled**
1	Activation enabled
The DTCENi3 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 2

DTCENi2	DTC activation enable i2
0	**Activation disabled**
1	Activation enabled
The DTCENi2 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 1

DTCENi1	DTC activation enable i1
0	**Activation disabled**
1	Activation enabled
The DTCENi1 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Bit 0

DTCENi0	DTC activation enable i0
0	**Activation disabled**
1	Activation enabled
The DTCENi0 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

Setting DTC base address

- DTC base address register (DTCBAR)
  Sets FDH for the DTC base address.

Symbol	7	6	5	4	3	2	1	0
DTCBAR	**DTCBAR 7**	**DTCBAR 6**	**DTCBAR 5**	**DTCBAR 4**	**DTCBAR 3**	**DTCBAR 2**	**DTCBAR 1**	**DTCBAR 0**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting DTC control register

- DTC control register 0 (DTCCR0)
  Sets the DTC control register 0.

Symbol	7	6	5	4	3	2	1	0
DTCCR0	**0**	**SZ**	**RPTINT**	**CHNE**	**DAMOD**	**SAMOD**	**RPTSEL**	**MODE**
Set value	0	**1**	**1**	**0**	×	**0**	**0**	**1**

Bit 6

SZ	Transfer data size selection
0	8 bits
1	**16 bits**

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	Interrupt generation disabled
1	**Interrupt generation enabled**
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	**Chain transfers disabled**
1	Chain transfers enabled
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 2

SAMOD	Transfer source address control
0	**Fixed**
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

RPTSEL	Repeat area selection
0	**Transfer destination is the repeat area**
1	Transfer source is the repeat area
The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).	

Bit 0

MODE	Transfer mode selection
0	Normal mode
1	**Repeat mode**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Setting DTC block size register 0

- DTC block size register 0 (DTBLS0)
  Sets the DTC block size register 0 to 01H (2 bytes).

Symbol	7	6	5	4	3	2	1	0
DTBLS0	**DTBLS07**	**DTBLS06**	**DTBLS05**	**DTBLS04**	**DTBLS03**	**DTBLS02**	**DTBLS01**	**DTBLS00**
Set value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

DTBLS0	**Transfer block size**	
	8-bit transfer	**16-bit transfer**
00H	256 bytes	512 bytes
01H	1 byte	**2 bytes**
02H	**2 bytes**	**4 bytes**
03H	3 bytes	6 bytes
.	.	.
.	.	.
.	.	.
FDH	253 bytes	506 bytes
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

Setting DTC transfer count register 0

- DTC transfer count register 0 (DTCCT0)
  Sets the DTC transfer count register 0 to 04H (4 times).

Symbol	7	6	5	4	3	2	1	0
DTCCT0	**DTCCT07**	**DTCCT06**	**DTCCT05**	**DTCCT04**	**DTCCT03**	**DTCCT02**	**DTCCT01**	**DTCCT00**
Set value	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**

DTCCT0	**Number of transfers**
00H	256 times
01H	Once
02H	2 times
03H	3 times
04H	**4 times**
:	:
:	:
:	:
FDH	253 times
FEH	254 times
FFH	255 times

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting DTC transfer count reload register 0

- DTC transfer count reload register 0 (DTRLD0)
  Sets the DTC transfer count reload register 0 to 04H (4 times).

Symbol	7	6	5	4	3	2	1	0
DTRLD0	**DTRLD07**	**DTRLD06**	**DTRLD05**	**DTRLD04**	**DTRLD03**	**DTRLD02**	**DTRLD01**	**DTRLD00**
Set value	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**

Setting DTC source address register 0

- DTC source address register 0 (DTSAR0)
  Set the DTC source address register 0 to the transfer source address FF1EH.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR0	**DTSAR015**	**DTSAR014**	**DTSAR013**	**DTSAR012**	**DTSAR011**	**DTSAR010**	**DTSAR09**	**DTSAR08**	**DTSAR07**	**DTSAR06**	**DTSAR05**	**DTSAR04**	**DTSAR03**	**DTSAR02**	**DTSAR01**	**DTSAR00**
Set value	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**

Setting DTC destination address register 0

- DTC destination address register 0 (DTDAR0)
  Set the DTC destination address register 0 to the transfer destination address F900H.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR0	**DTDAR015**	**DTDAR014**	**DTDAR013**	**DTDAR012**	**DTDAR011**	**DTDAR010**	**DTDAR09**	**DTDAR08**	**DTDAR07**	**DTDAR06**	**DTDAR05**	**DTDAR04**	**DTDAR03**	**DTDAR02**	**DTDAR01**	**DTDAR00**
Set value	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(7) Main Processing

Figure 8.11 shows the flowchart for the main processing.

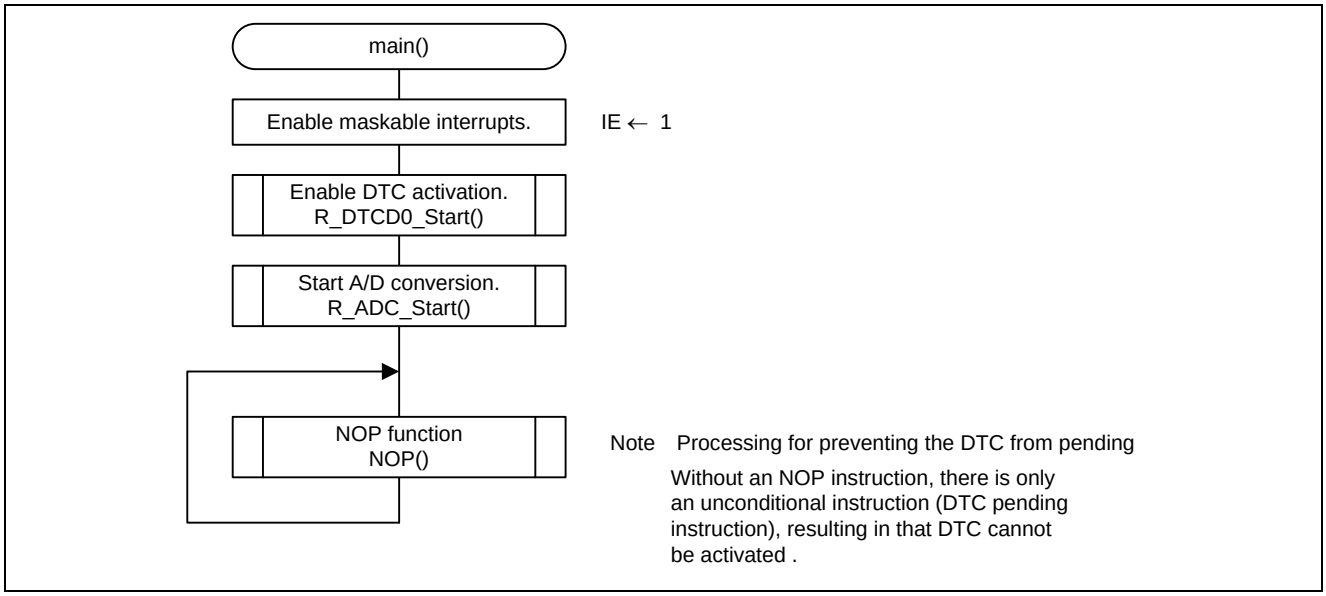


Figure 8.11 Main Processing (example of migration from repeat sweep mode)

(8) Enabling DTC Activation

Figure 8.12 shows the flowchart for enabling DTC activation.

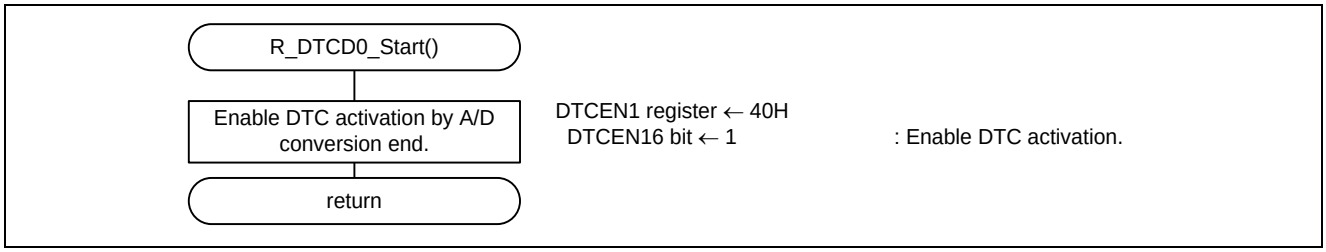


Figure 8.12 Enabling DTC Activation (example of migration from repeat sweep mode)

Enabling DTC activation

- DTC activation enable register 1 (DTCEN1)
  Enables DTC activation by the A/D conversion end.

Symbol	7	6	5	4	3	2	1	0
DTCEN1	**DTCEN17**	**DTCEN16**	**DTCEN15**	**DTCEN14**	**DTCEN13**	**DTCEN12**	**DTCEN11**	**DTCEN10**
Set value	×	**1**	×	×	×	×	×	×

Bit 6

DTCEN16	DTC activation enable 16 (DTC activation source: A/D conversion end)
0	Activation disabled
1	**Activation enabled**
The DTCEN16 bit is set to 0 (activation disabled) by a condition for generating a transfer end interrupt.	

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(9) Staring A/D Conversion

Figure 8.13 shows the flowchart for starting A/D conversion.

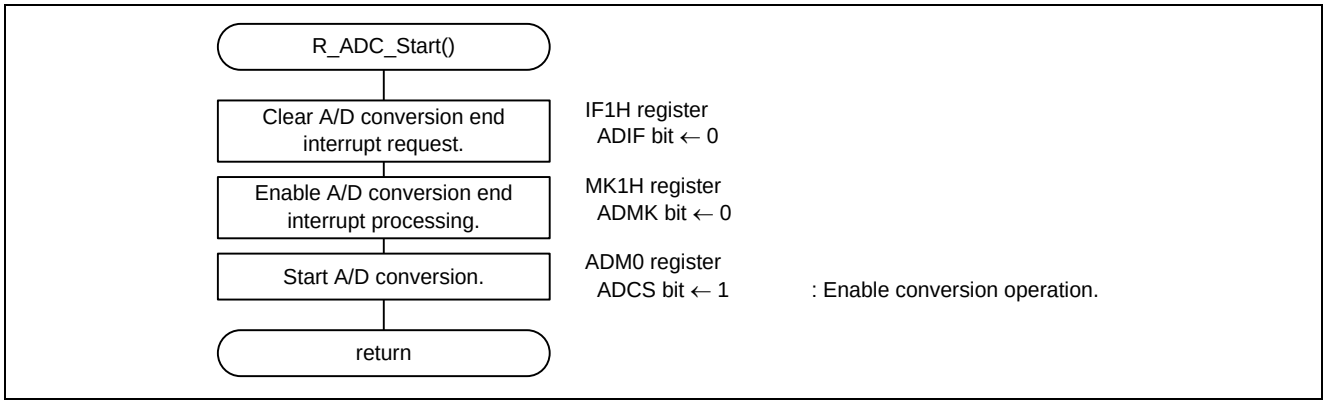


Figure 8.13 Starting A/D Conversion (example of migration from repeat sweep mode)

Setting A/D conversion end interrupt request flag

- Interrupt request flag register (IF1H)
  Clears the A/D conversion end interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	**PIF11**	**PIF10**	**PIF9**	**PIF8**	**PIF7**	**KRIF**	**TMKAIF**	**ADIF**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADIF	**Interrupt request flag**
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Enabling A/D conversion end interrupt

- Interrupt mask flag register (MK1H)
  Enables the A/D conversion end interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	**PMK11**	**PMK10**	**PMK9**	**PMK8**	**PMK7**	**KRMK**	**TMKAMK**	**ADMK**
Set value	×	×	×	×	×	×	×	**0**

Bit 0

ADMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Starting A/D converter

- A/D converter mode register 0 (ADM0)
  Starts A/D conversion operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	**ADCS**	**ADMD**	**FR2**	**FR1**	**FR0**	**LV1**	**LV0**	**ADCE**
Set value	**1**	×	×	×	×	×	×	×

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	**Enables conversion operation** **[When read]** **While in the software trigger mode: Conversion operation status** **While in the hardware trigger wait mode: A/D power supply stabilization wait status + conversion operation status**

x in “Set value” of the above table indicates that the pertinent bit is not used in this function.

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

(10) A/D conversion end interrup

Figure 8.14 shows the flowchart for A/D conversion end interrupt processing.

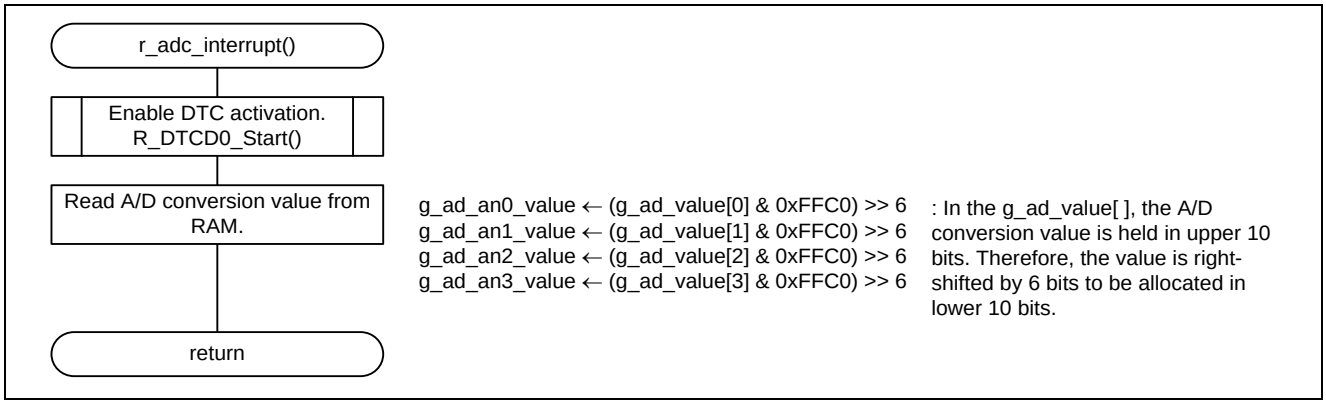


Figure 8.14 A/D Conversion End Interrupt (example of migration from repeat sweep mode)

8.5 Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8.6 Reference Application Note

- RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: A/D Converter CC-RL (R01AN3059)

- RL78/G14, R8C/36M Group
  Migration Guide from R8C to RL78: Data Transfer Controller (R01AN1503)

- RL78/G14 How to Use the DTC for the RL78/G14 (R01AN0861)

8.7 Reference Documents

User's Manual

- RL78/G11 User's Manual: Hardware
  (The latest versions can be downloaded from the Renesas Electronics website.)

- R8C/32C Group Hardware Manual
  (The latest versions can be downloaded from the Renesas Electronics website.)

- Technical Update/Technical News
  (The latest information can be downloaded from the Renesas Electronics website.)

Migration Guide

- Migration to CubeSuite+ Integrated Development Environment for RL78 Family
  (On-chip Debug) - Migration from R8C, M16C to RL78 (R20UT2150)

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Apr 13, 2018	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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