RL78/G11

IH Control using Timer KB0 CC-RL

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Introduction

This application note describes IH control using the 16-bit timer KB0 of RL78/G11.

Target Device

RL78/G11

When applying this application note to other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Specifications

Applying a current to the IH coil generates eddy current in metal pots and pans. By utilizing the Joule heat produced by the eddy current, the IH cooker achieves cooking.

This application note describes an example in which a half-bridge resonant circuit used for thermal control of an IH cooker by using the timer KB function incorporated in the RL78/G11.

Figure 1.1 shows an equivalent circuit of the half-bridge LC resonant circuit.

With this circuit, IGBTH and IGBTL are alternately turned on to generate LC resonance, which applies a current to the IH coil. As a PWM cycle becomes closer to the oscillation frequency of the circuit, firepower becomes larger, and as a PWM cycle becomes farther from the oscillation frequency, firepower becomes smaller. Therefore, IGBTH and IGBTL are controlled using the PWM output function of the timer KB so that the cycle should change according to the firepower that the user wants.

Here, the firepower can be stabilized by monitoring the output from the current detection circuit of the IH part.

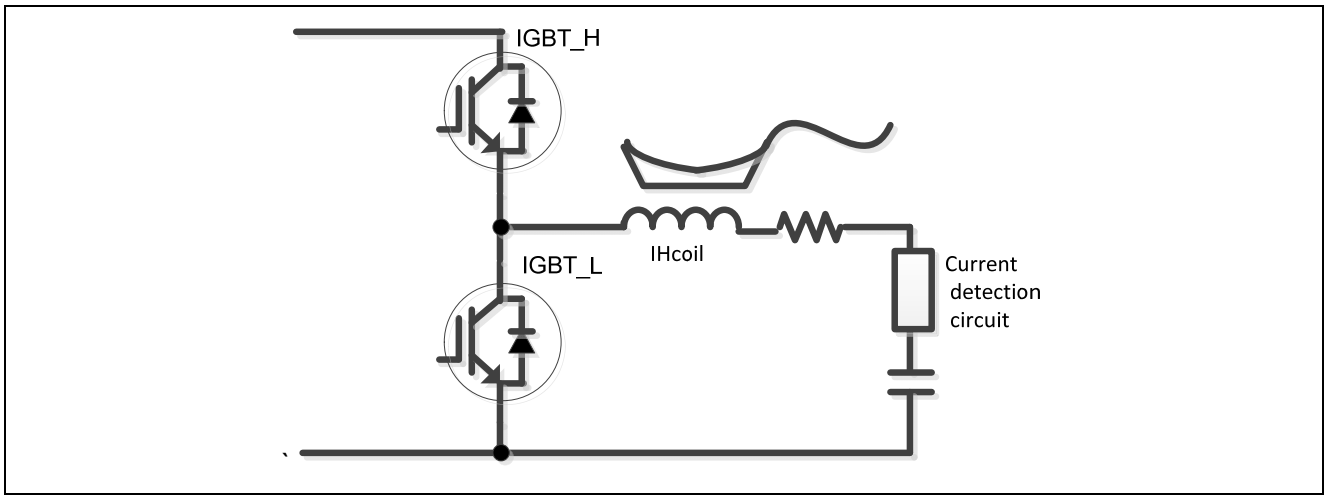

Figure 1.1 Equivalent Circuit of Half-Bridge LC Resonant Circuit

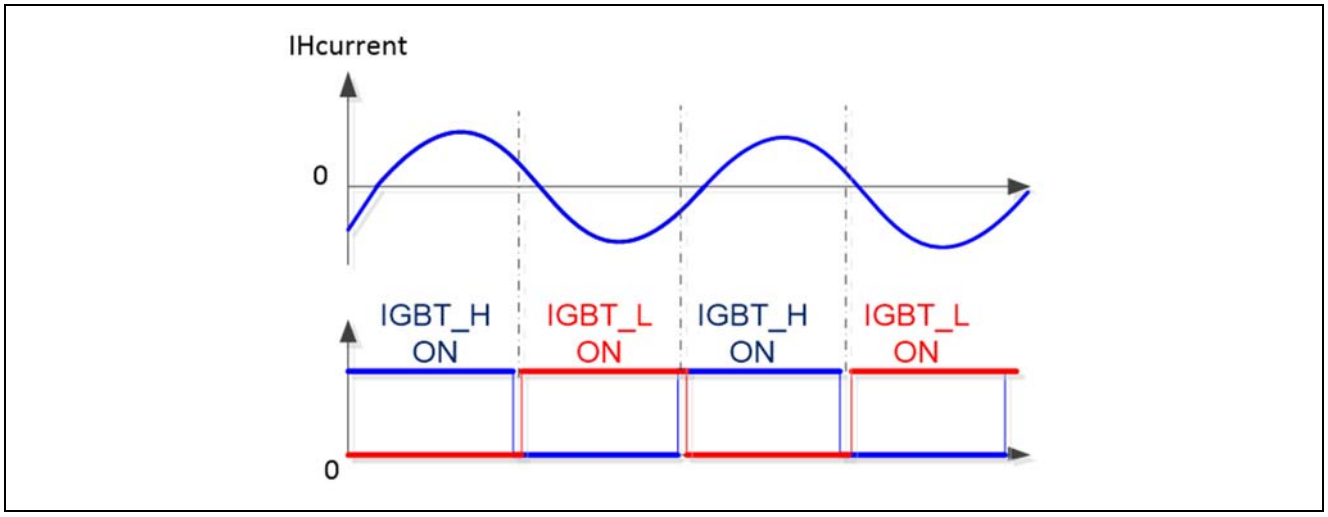

Figure 1.2 IH Inverter Control Timing

Table 1.1 shows the peripheral functions used and their usage.

Table 1.1 Peripheral Functions Used and their Usage

Peripheral Function	Usage
16-bit timer KB0	Turns on or off IGBT.
Internal comparator	Detects over-voltage or over-current and forcibly cuts off PWM output.
Interrupt	Detects zero cross of supply voltage (AC).
A/D converter	Measures output voltage from the current detection circuit. Measures IH coil temperature. Measures voltage of IH firepower control signal.

1.1 Timer KB Basic Operation

The timer KB basic operation is shown in Figure 1.3, Timer KB Basic Operation. The timer KB provides PWM output to alternately turn on and off TKBO0 (IGBTH) and TKBO1 (IGBTL). In this application note, the PWM frequency is 20 kHz to 50 kHz depending on the input level of the A/D converter (ANI16) and the duty cycle is approximately 50%. The dead time, in which neither TKBO0 nor TKBO1 is output, is approximately 1 μs. The duty cycle is updated according to the level of ANI16 measured in an AC voltage cycle.

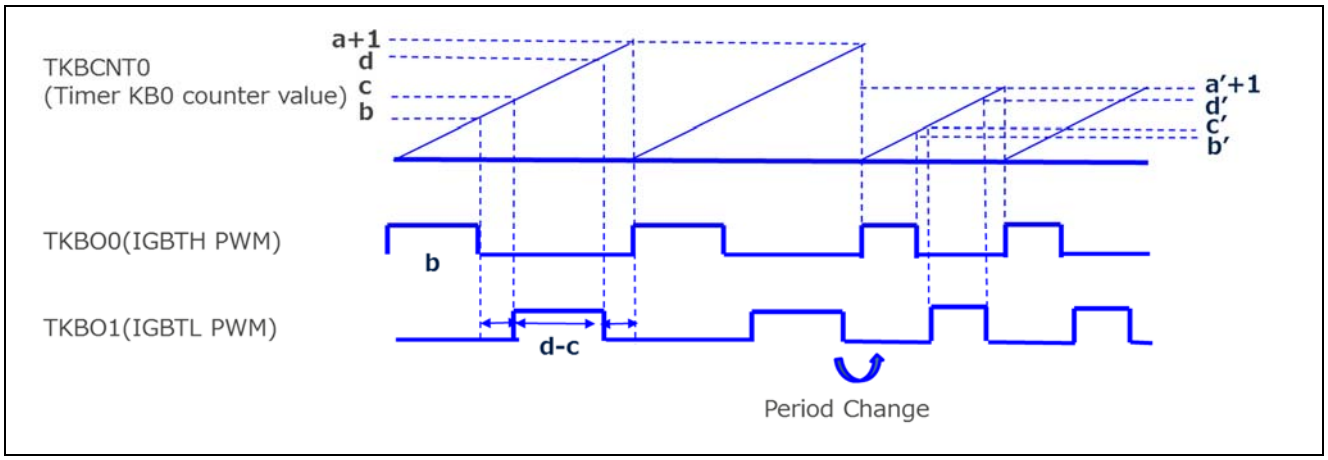

Figure 1.3 Timer KB Basic Operation

Setting example for 20 kHz
Period: a + 1 = 50 μs
Duty period: b = d - c = 24 μs
Dead time: d – c – b = a + 1 – d = 1 μs

Setting example for 50 kHz
Period: a' + 1 = 20 μs
Duty period: b' = d' - c' = 9 μs
Dead time: d' - c' - b = a' + 1 - d = 1 μs

1.2 Forced output stop of Timer KB0

Forced output stop function 1 of timer KB0 is used. IVCMP0 and IVCMP1 pins are used for measuring over-voltage and over-current of the system. IVCMP0 is compared to the output of the internal D/A channel 0 and IVCMP1 to the internal reference voltage (1.45 V). The timer KB0 output is fixed to the low level at the rising edge of CMP0/CMP1. The forced output stop function can be cancelled by manipulating the software bit TKBPAHTSnp. However, cancellation of the forced output stop function is not used in this application note.

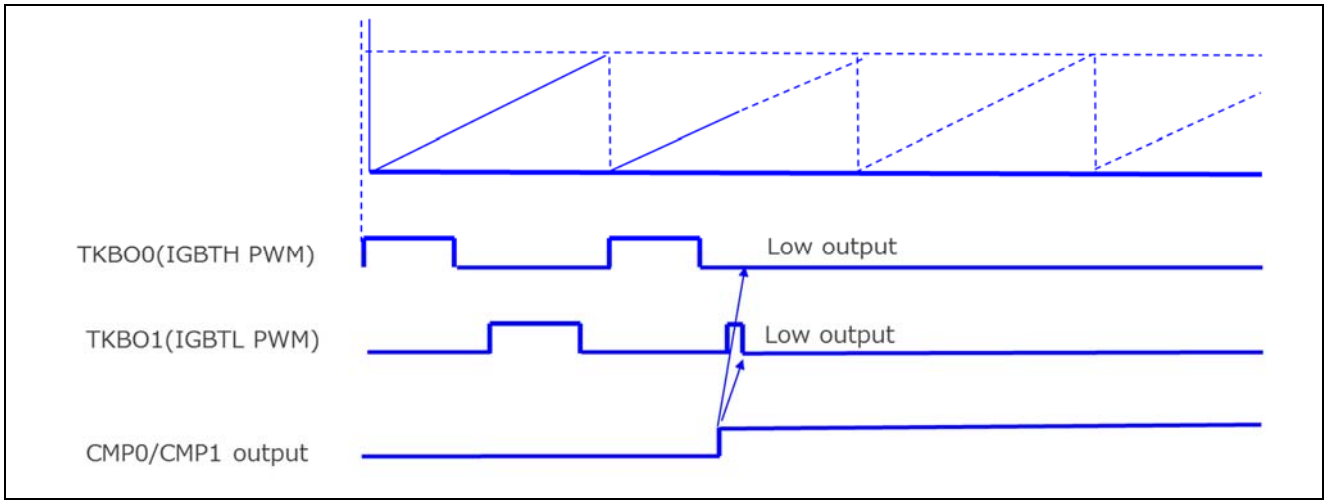

Figure 1.4 Forced Output Stop of Timer KB0

2. Conditions for Confirming Operation

The sample code operations described in this application note are confirmed under the following conditions.

Table 2.1 Conditions for Confirming Operations

Item	Description
Microcontroller used	RL78/G11 (R5F1056A)
Operating frequency	● High-speed on-chip oscillator (HOCO) clock: 24 MHz ● CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (can be operated from 2.9 V to 5.5 V) LVD operation (V_{LVD}): Reset mode 2.65 V (2.65 V to 2.71 V)
Integrated development environment (CS+)	CS+ for CC V4.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.03.00 from Renesas Electronics Corp.

3. Related Application Notes

- RL78/G11 Forced Stop of PWM Output through Comparator and External Interrupt CC-RL(R1AN3477E)

4. Hardware Descriptions

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration described in this application note.

To the IH driver IC, TKBO0 and TKBO1 output from TMKB are connected. For detection of the IH part discharge, INTP11 is used, which can be set for restarting TMKB. Besides, over-current and over-voltage are detected for stable control of the IH inverter. For over-current detection, the A/D converter is used to monitor the current flowing through the IH coil. For over-voltage detection, the external interrupt request signal INTP10 is used. In this application note, the A/D converter is used to determine the firepower level (high, middle, or low) of the IH cooker.

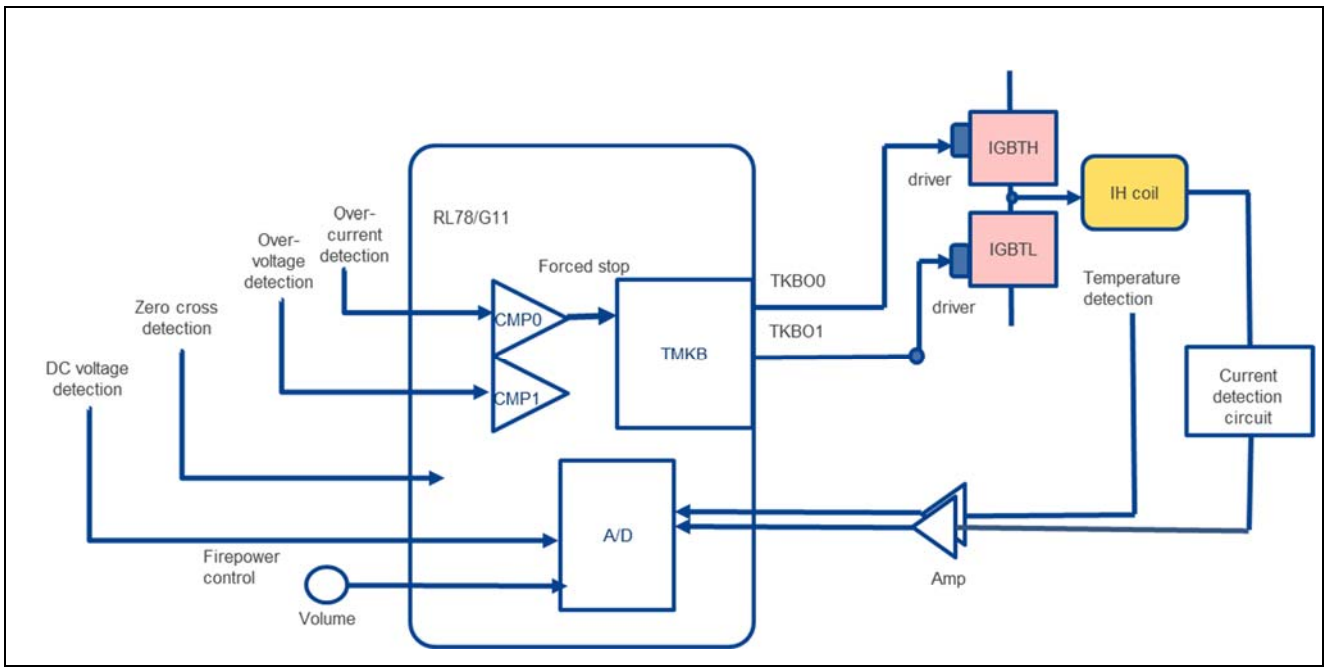

Figure 4.1 Hardware Configuration

Caution 1 The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied (input-only ports should be each connected to V_{DD} or V_{SS} via a resistor).

4.2 List of Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P30/ANI21/KR1/TI00/TO01/INTP3/SCK11/SCL11/(TxD0)/ PCLBUZ0/TKBO1/SDAA0	Output	IGBTL driver control
P31/ANI20/KR0/TI01/TO00/INTP4/TKBO0/(RxD0)/ SI11/SDA11/SCLA0	Output	IGBTH driver control
P122/X2/EXCLK/(SI10/RxD1)/(TI02)/INTP1	Input	AC voltage zero cross detection
P56/ANI22/KR2/SCK00/SCL00/SO11/INTP10/ (TO03)/(INTFO)/SCLA1	Input	DC voltage detection
P22/ANI2/PGAI/IVCMP0	Input	Over-current detection
P33/ANI18/IVCMP1/(INTP11)	Input	Over-voltage detection
P23/ANI3/ANO1/PGAGND	Input	Temperature detection
P00/ANI17/PCLBUZ1/TI03/(VCOUT1)/SI10/RxD1/ SDA10/(SDAA1)	Input	IH current detection
P01/ANI16/INTP5/SO10/TxD1	Input	Volume input for firepower control
P20/ANI0/AVREFP/IVREF1/(SO10/TXD1)	—	A/D_power supply
P21/ANI1/AVREFM/IVREF0	—	A/D_GND

5. Software Descriptions

5.1 Operation Summary

This application note describes the software for controlling IH by using the timer KB0, external interrupt, A/D converter, and TAU.

The timer KB0 provides PWM output for IGBT control via TKBO0 and TKBO1.

The timer KB0 also provides three-step periodic PWM output according to the value of Volume input for firepower control (ANI16).

The forced stop function is implemented using forced output stop function 1.

Forced output stop function 1 is triggered by the CMP0 and CMP1 rising edges caused by the over-current detection (IVCMP0) input and over-voltage detection (IVCMP1) input and fixes TKBO0 and TKBO1 output to the low level.

Measurement using the A/D converter (DC voltage detection, temperature detection, IH current detection, and Volume for firepower control) is started when 10 ms elapses by the interval timer after the rising edge of the AC voltage zero cross signal (INTP1).

(1) Make the initial settings for the ports.

(2) Make the initial settings for the A/D converter.

(3) Make the initial settings for the timer KB0.

(4) Make the initial settings for the timer array unit.

(5) Make the initial settings for the comparators.

(6) Start detection of the INTP1 rising edge.

(7) Start the timer KB.

5.2 List of Option Byte Settings

Table 5.1 lists option byte settings.

Table 5.1 Option Byte Settings

Address	Setting	Contents
000C0H	11101111B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H	01111111B	LVD reset mode: 2.75 V (2.75 V to 2.81 V)
000C2H	11100000B	HS mode; HOCO: 24MHz
000C3H	10000100B	On-chip debugging is enabled.

5.3 List of Constants

Table 5.2 lists the constants used in the sample code.

Table 5.2 Constants Used in Sample Code

Constant Name	Setting	Contents
CHNUM	4	Number of analog input channels used

5.4 List of Variables

Table 5.3 lists the global variables.

Table 5.3 Global Variables

Type	Variable Name	Contents	Function Used
uint16_t	adc_buffer[4]	Buffer for storing A/D conversion results	main()

5.5 List of Functions

Table 5.4 lists the functions.

Table 5.4 Functions

Function Name	Summary
R_COMP0_Start	Starts comparator 0 for over-current detection.
R_COMP1_Start	Starts comparator 1 for over-voltage detection.
R_INTC1_Start	Starts external interrupt INTP10 for AC zero cross detection.
R_TMR_KB0_Start	Starts 16-bit timer KB0 for IGBT control.
R_ADC_Set_OperationOn	Enables A/D converter operation.
R_ADC_Start	Starts A/D conversion.
R_ADC_Get_Result	Stops A/D conversion.
R_TAU0_Channel1_Lower8bit_Start	Starts TAU for determination of various measurement timings.
r_tau0_channel1_interrupt	TAU operation end interrupt

5.6 Function Specifications

The following gives the specifications of the functions used in the sample code.

[Function name] R_ COMP0_Start

Summary	Process of starting comparator 0 operation
Header	r_cg_comp.h, r_cg_userdefine.h
Declaration	void R_ COMP0_Start(void)
Description	Starts comparator 0 operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_COMP1_Start

Summary	Process of starting comparator 1 operation
Header	r_cg_comp.h, r_cg_userdefine.h
Declaration	void R_ COMP1_Start(void)
Description	Starts comparator 1 operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_INTC1_Start

Summary	Process of starting external interrupt operation
Header	r_cg_intp.h, r_cg_userdefine.h
Declaration	void R_ INTC1_Stop(void)
Description	Starts external interrupt operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_TMR_KB0_Start

Summary	Process of starting 16-bit timer KB operation
Header	r_cg_tmkb.h, r_cg_userdefine.h
Declaration	void R_TMR_KB0_Start (void)
Description	Starts 16-bit timer KB operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_ADC_Set_OperationOn

Summary	Process of starting A/D converter operation
Header	r_cg_adc.h, r_cg_userdefine.h
Declaration	void R_ADC_Set_OperationOn (void)
Description	Enables A/D converter operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_ADC_Start

Summary	Start of A/D conversion
Header	r_cg_adc.h, r_cg_userdefine.h
Declaration	void R_ADC_Start (void)
Description	Starts A/D conversion.
Arguments	None
Return values	None
Remarks	None

[Function name] R_ADC_Get_Result

Summary	Acquisition of A/D conversion results	
Header	r_cg_adc.h, r_cg_userdefine.h	
Declaration	void R_ADC_Get_Result (uint16_t * const buffer)	
Description	Acquires A/D conversion results.	
Arguments	buffer	Address of RAM area for acquiring conversion results
Return values	None	
Remarks	None	

[Function name] R_TAU0_Channel1_Lower8bit_Start

Summary	Process of starting TAU operation
Header	r_cg_tau.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel1_Lower8bit_Start (void)
Description	Starts TAU operation.
Arguments	None
Return values	None
Remarks	None

[Function name] r_tau0_channel1_interrupt

Summary	Process of TAU0 operation end interrupt
Header	r_cg_tau.h, r_cg_userdefine.h
Declaration	static void __near r_tau0_channel1_interrupt (void)
Description	Processes TAU0 operation end interrupt.
Arguments	None
Return values	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the processes described in this application note.

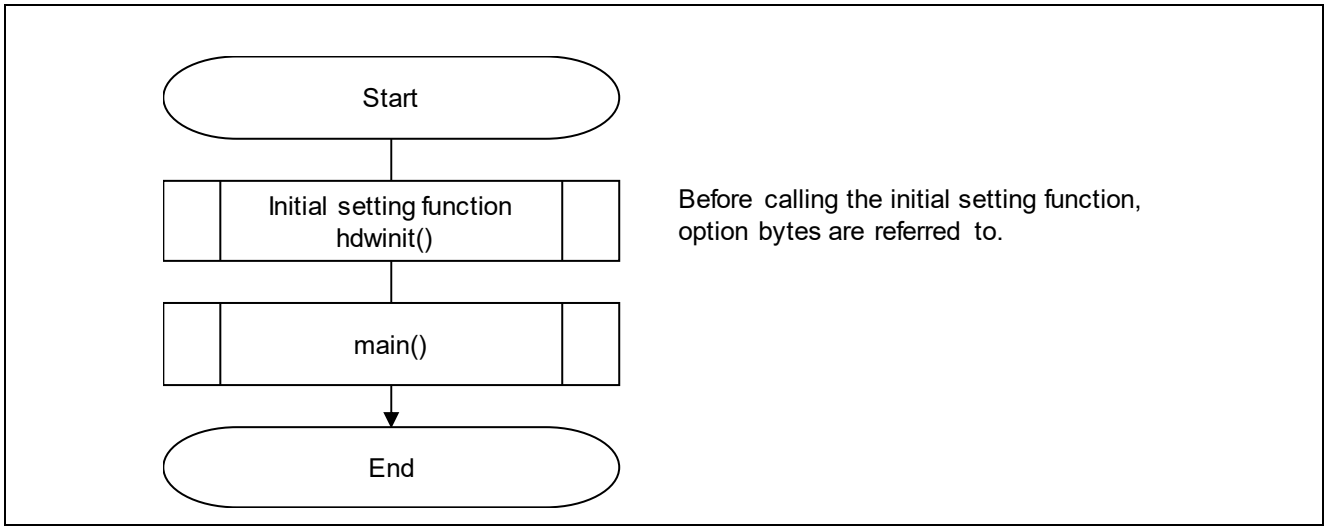

Figure 5.1 Overall Flow

Note: The start-up routine is executed before and after the initial setting function.

5.7.1 Initial Setting Function

Figure 5.2 shows the flowchart of the initial setting function.

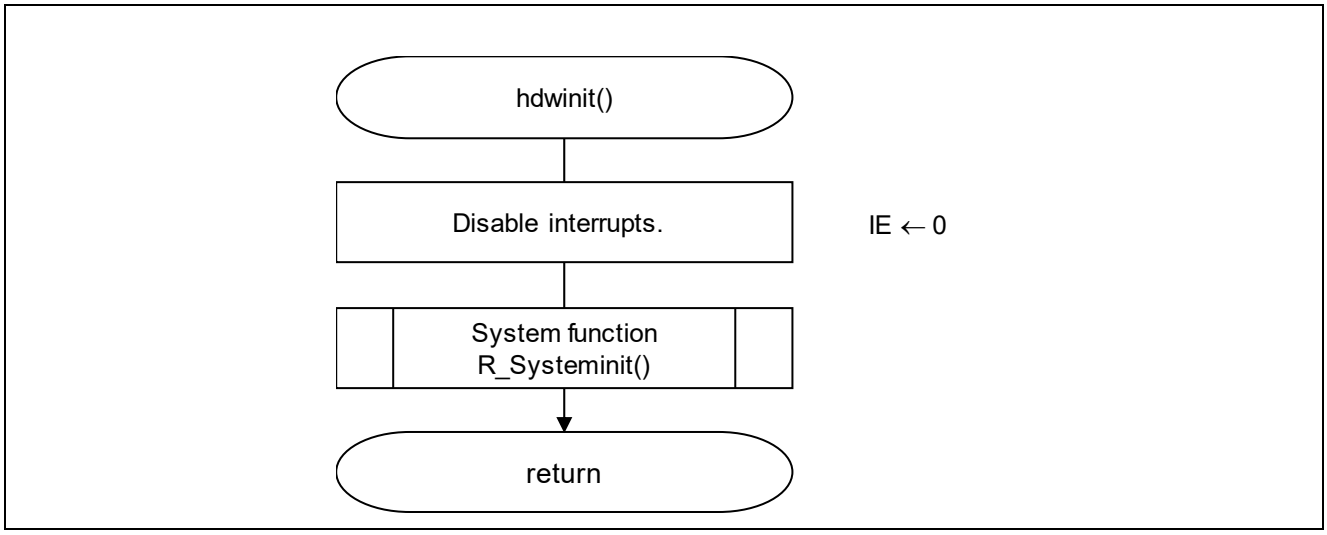

Figure 5.2 Initial Setting Function

5.7.2 System Function

Figure 5.3 shows the flowchart of the system function.

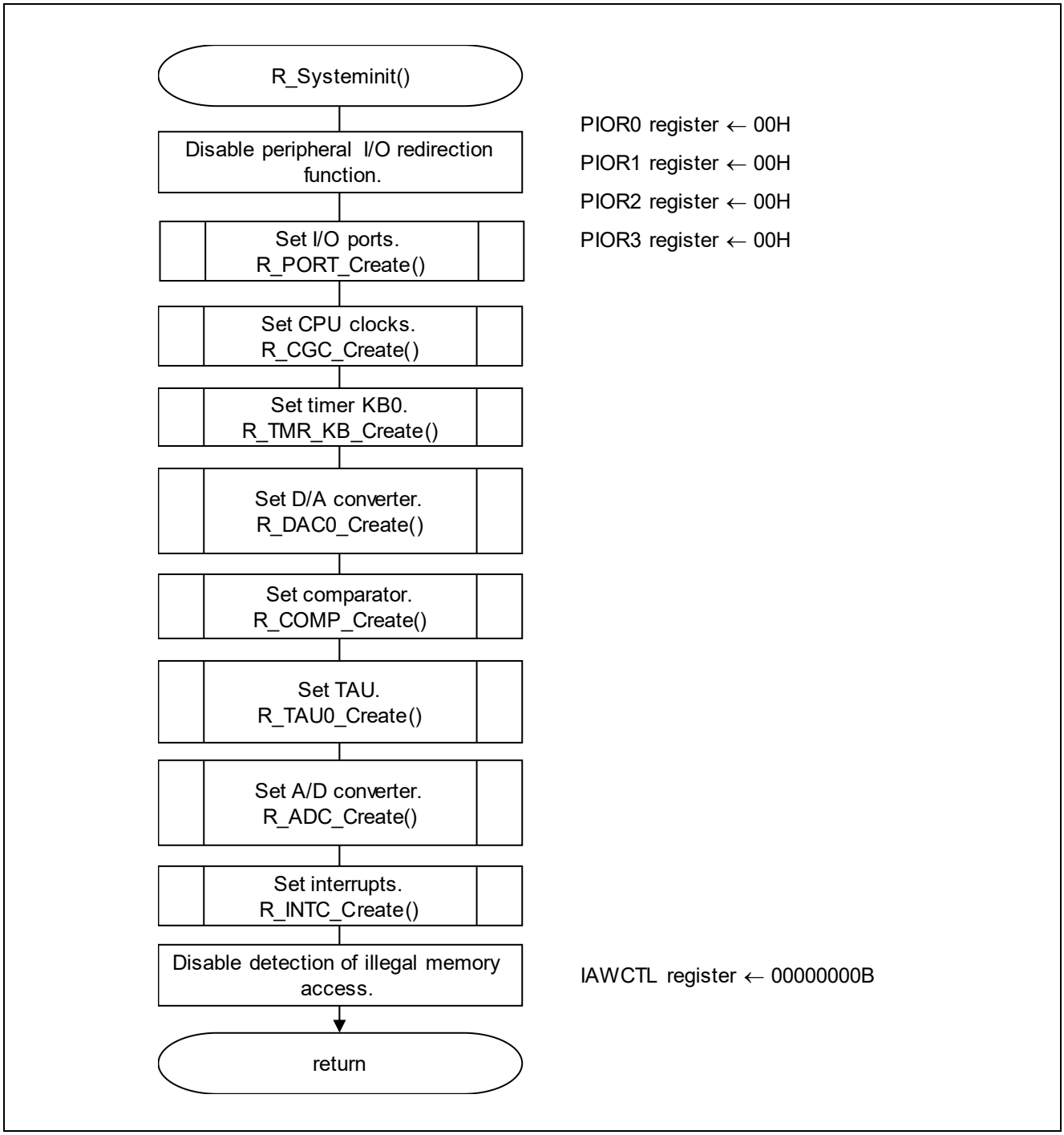

Figure 5.3 System Function

5.7.3 Setting I/O Ports

Figure 5.4 shows the flowchart for setting the I/O ports.

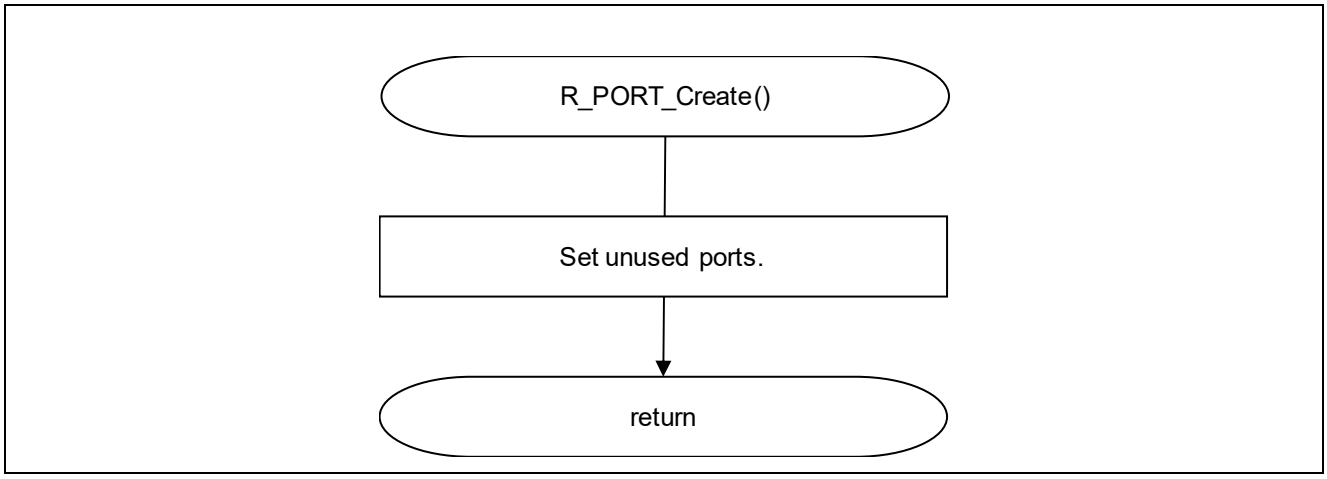

Figure 5.4 Setting I/O Ports

Note: For unused port settings, refer to the RL78/G11 User's Manual: Hardware.

Caution: Design unused ports so that the electrical characteristics are satisfied by appropriately treating the pertinent pins. Separately connect unused input-only ports to V_{DD} or V_{SS} via a resistor.

5.7.4 Setting CPU Clocks

Figure 5.5 shows the flowchart for setting the CPU clocks.

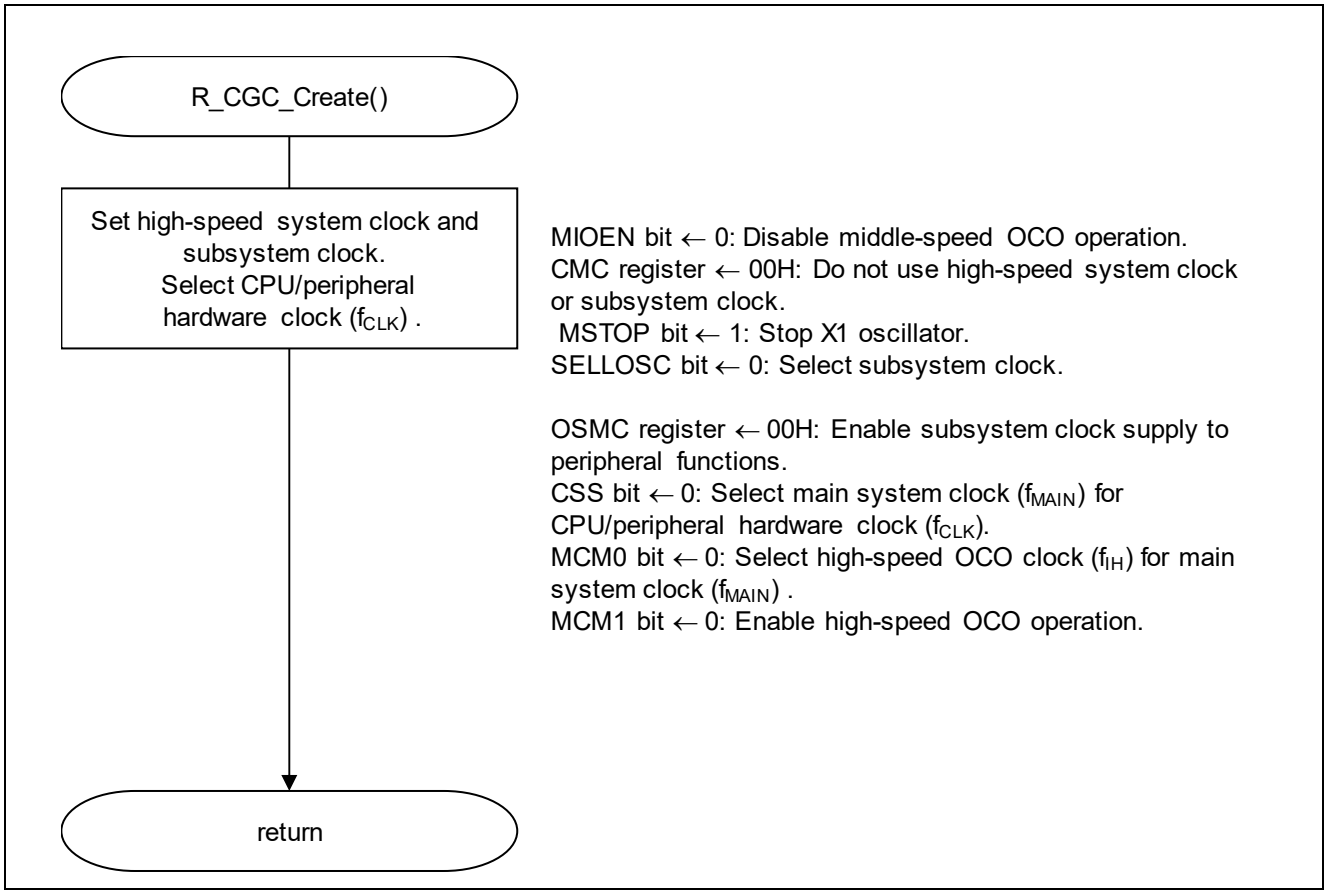

Figure 5.5 Setting CPU Clocks

5.7.5 Setting Timer KB0

Figure 5.6 shows the flowchart for setting the timer KB0.

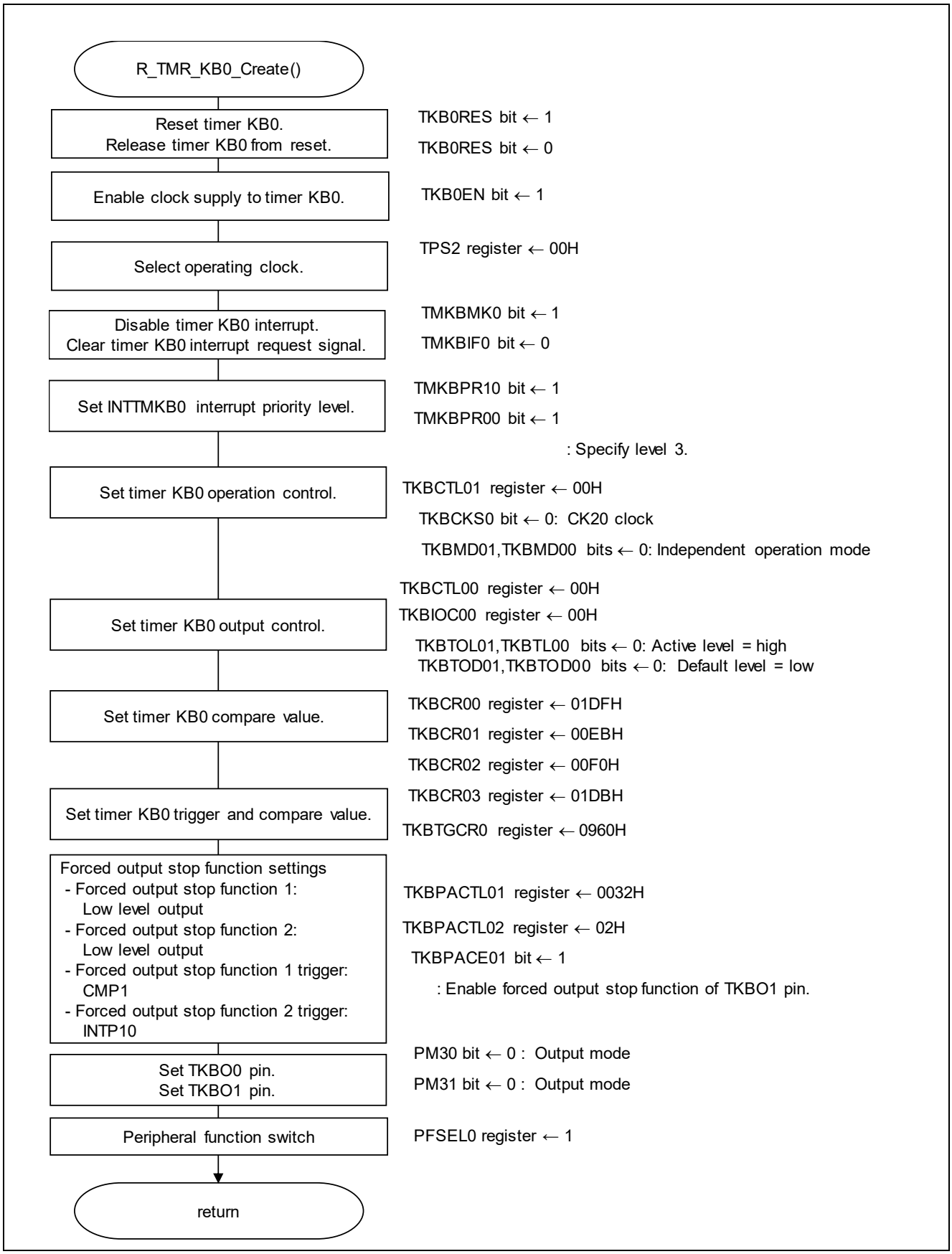

Figure 5.6 Setting Timer KB0

Controlling reset of timer KB0

- Peripheral reset control register 2 (PRR2)
  Controls reset of the timer KB0.

Symbol: PRR2

7	6	5	4	3	2	1	0
TMKARES	0	DOCRES	0	0	0	0	TKB0RES
x	0	x	0	0	0	0	**1/0**

Bit 0

TKB0RES	Reset control of timer KB0
0	**Timer KB0 reset release**
1	**Timer KB0 reset state**

Starting clock supply to timer KB0

- Peripheral enable register 2 (PER2)
  Starts supplying clock to the timer KB0.

Symbol: PER2

7	6	5	4	3	2	1	0
TMKAEN	0	DOCEN	0	0	0	0	TKB0EN
x	0	x	0	0	0	0	**1**

Bit 0

TKB0EN	Control of timer KB0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB0 operation clock

- Timer clock select register 2 (TPS2)
  Selects the timer KB operation clock.

Symbol: TPS2

7	6	5	4	3	2	1	0
0	TPS212	TPS211	TPS210	0	TPS202	TPS201	TPS200
0	**0**	**0**	**0**	0	**0**	**0**	**0**

Bits 2 to 0

TPS202	TPS201	TPS200	Selection of operation clock (CK20)					
				f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 24 MHz
0	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	**24 MHz**
0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	750 kHz
Other than the above			Setting prohibited					

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB0 interrupt

- Interrupt request flag register (IF2L)
  Clears interrupt request flags.
- Interrupt mask flag register (MK2L)
  Disables interrupt servicing.

Symbol: IF2L

7	6	5	4	3	2	1	0
FLIF	IICAIF1	TMKBIF0	ITIF01	ITIF00	DOCIF	CMPIF1	CMPIF0
x	x	**0**	x	x	x	x	x

Bit 5

TMKBIF0	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Symbol: MK2L

7	6	5	4	3	2	1	0
FLMK	IICAMK1	TMKBMK0	ITMK01	ITMK00	DOCMK	CMPMK1	CMPMK0
X	x	**1**	x	x	x	x	x

Bit 5

TMKBMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB operation control

- 16-bit timer KB operation control register 01 (TKBCTL01)
  Controls timer KB0 operation.
  Selects timer KB0 clock.
  Selects timer KB0 operation mode.

Symbol: TKBCTL01

7	6	5	4	3	2	1	0
TKBCE0	0	0	TKBCKS0	0	0	TKBMD01	TKBMD00
0	0	0	**0**	0	0	**0**	**0**

Bit 7

TKBCE0	Timer KB0 operation control
0	**Stops timer operation (counter is set to FFFF).**
1	Enables timer count operation.

Bit 4

TKBCKS0	Timer KB0 clock selection
0	**CK20 clock selected by TPS202 to TPS200 bits**
1	CK21 clock selected by TPS212 to TPS210 bits

Bits 1 and 0

TKBMD01	TKBMD00	Timer KB0 operation mode selection
0	**0**	**Standalone mode (uses master)**
1	1	Interleave PFC output mode
Other than the above		Setting prohibited

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB0 output control

- 16-bit timer KB output control register 00 (TKBIOC00)
  Sets the active level in timer output TKBO0.
  Sets the default level in timer output TKBO2.

Symbol: TKBIOC00

7	6	5	4	3	2	1	0
0	0	0	0	TKBTOL01	TKBTOL00	TKBTOD01	TKBTOD00
0	0	0	0	**0**	**0**	**0**	**0**

Bits 3 and 2

TKBTOL0n	Active level setting of timer output TKBOn (n = 1,0)
0	**High level**
1	Low level

Bits 1 and 0

TKBTOD0n	Default level setting of timer output TKBOn (n = 1,0)
0	**Low level**
1	High level

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer KB0 forced output stop function

- Forced output stop function control register 00 (TKBPACTL00)
  Selects the external interrupt trigger, comparator trigger, and operation mode for forced output stop function 2.
  Selects the comparator trigger, output status, and clear condition for forced output stop function 1.

- Forced output stop function control register 02 (TKBPACTL02)
  Controls trigger signal input.

Symbol: TKBPACTL00

15	14	13	12	11	10	9	8
TKBPAFXS013	TKBPAFXS012	TKBPAFXS011	TKBPAFXS010	0	0	0	TKBPAFCM01
0	**0**	**0**	**0**	0	0	0	**0**

7	6	5	4	3	2	1	0
0	0	TKBPAHZS011	TKBPAHZS010	KBPAHCM011	KBPAHCM010	TKBPAMD011	TKBPAMD010
0	0	**1**	**1**	**0**	**1**	**1**	**0**

Bit 15

TKBPAFXS013	External interruption trigger selection for forced output stop function 2
0	**INTP11 cannot be used as a trigger.**
1	INTP11 can be used as a trigger.

Bit 14

TKBPAFXS012	External interruption trigger selection for forced output stop function 2
0	**INTP10 cannot be used as a trigger.**
1	INTP10 can be used as a trigger.

Bit 13

TKBPAFXS011	Comparator trigger selection for forced output stop function 2
0	**CMP1 cannot be used as a trigger.**
1	CMP1 can be used as a trigger.

Bit 12

TKBPAFXS010	Comparator trigger selection for forced output stop function 2
0	**CMP0 cannot be used as a trigger.**
1	CMP0 can be used as a trigger.

Bit 8

TKBPAFCM01	Operation mode selection for forced output stop function 2
0	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.**
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: TKBPACTL00

15	14	13	12	11	10	9	8
TKBPAFXS013	TKBPAFXS012	TKBPAFXS011	TKBPAFXS010	0	0	0	TKBPAFCM01
0	**0**	**0**	**0**	0	0	0	**0**

7	6	5	4	3	2	1	0
0	0	TKBPAHZS011	TKBPAHZS010	KBPAHCM011	KBPAHCM010	TKBPAMD011	TKBPAMD010
0	0	**1**	**1**	**0**	**0**	**1**	**0**

Bit 5

TKBPAHZS011	Comparator trigger selection for forced output stop function 1
0	CMP1 cannot be used as a trigger.
1	**CMP1 can be used as a trigger.**

Bit 4

TKBPAHZS010	Comparator trigger selection for forced output stop function 1
0	CMP0 cannot be used as a trigger.
1	**COM0 can be used as a trigger.**

Bits 3 and 2

TKBPAHCM011	TKBPAHCM010	Clear condition selection for forced output stop function 1
0	**0**	**Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT01) = 1 is written, regardless of the trigger signal level.**
0	**1**	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing “forced output stop function release trigger (TKBPAHTT01) = 1” is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT01) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT01) = 1 is written, regardless of the trigger signal level. Note
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing “forced output stop function release trigger (TKBPAHTT01) = 1” is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT01) = 1 is written when the trigger signal is in its inactive period. Note

Note: When timer KB is stopped (TKBCE0 = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCE0 = 1).

Note: For details of register settings, refer to the RL78/G11 User’s Manual: Hardware.

Symbol: TKBPACTL00

15	14	13	12	11	10	9	8
TKBPAFXS013	TKBPAFXS012	TKBPAFXS011	TKBPAFXS010	0	0	0	TKBPAFCM01
0	**0**	**0**	**0**	0	0	0	**0**

7	6	5	4	3	2	1	0
0	0	TKBPAHZS011	TKBPAHZS010	KBPAHCM011	KBPAHCM010	TKBPAMD011	TKBPAMD010
0	0	**1**	**1**	**0**	**0**	**1**	**0**

Bits 1 and 0

TKBPAMD011	TKBPAMD010	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	**Hi-Z output**	**Output fixed at low level**
0	1	Hi-Z output	Output fixed at high level
1	**0**	**Output fixed at low level**	**Output fixed at low level**
1	1	Output fixed at high level	Output fixed at high level

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: TKBPACTL02

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TKBPACE01	TTKBPACE00
0	0	0	0	0	0	**0**	**1**

Bits 1 and 0

TKBPACE0n	Input control of trigger signal used for forced output stop function of the TKBO0 pin
0	**Disable operation of forced output stop function**
1	**Enable operation of forced output stop function**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.7.6 Setting D/A Converter

Figure 5.7 shows the flowchart for setting the D/A converter.

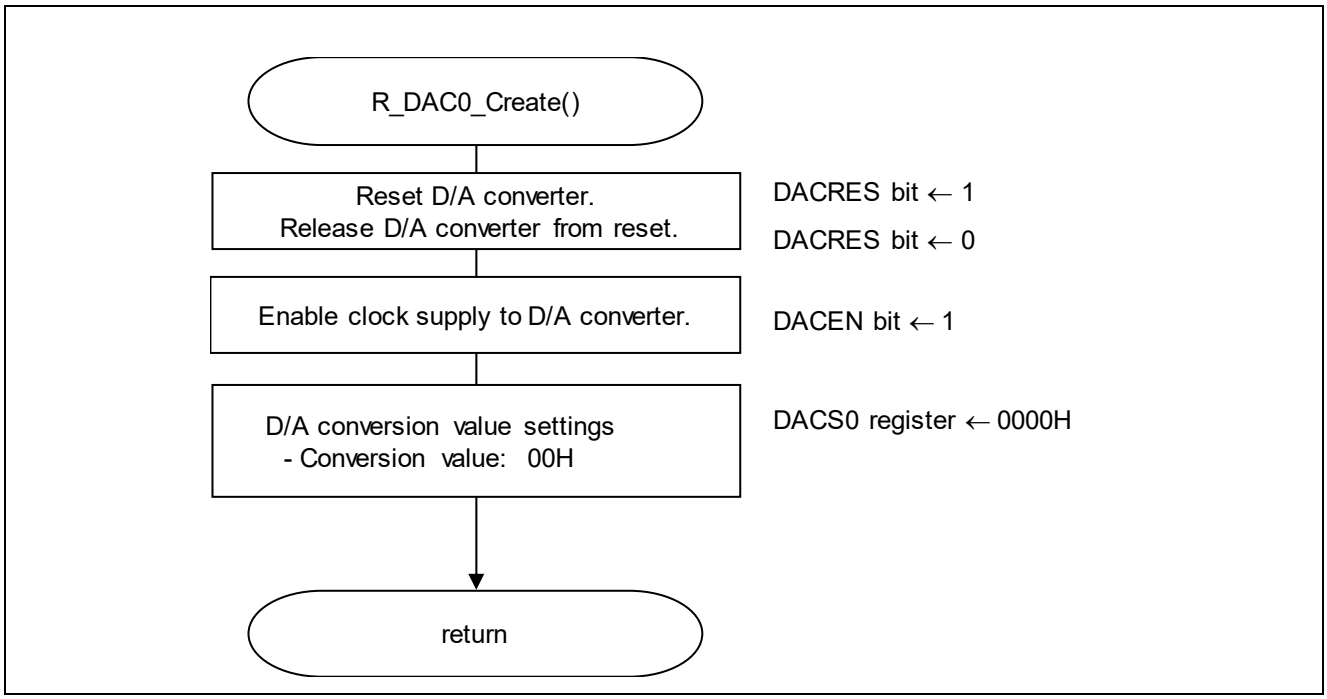

Figure 5.7 Setting D/A Converter

Setting peripheral reset of D/A converter

- Peripheral reset control register (PRR1)
  Controls reset of the D/A converter.

Symbol: PRR1

7	6	5	4	3	2	1	0
DACRES	0	CMPRES	0	0	PGA0RES	0	0
0/1	0	x	0	0	x	0	0

Bit 7

DACRES	Reset control of D/A converter
0	**D/A converter reset release**
1	**D/A converter reset state**

Starting clock supply to D/A converter

- Peripheral enable register 1 (PER1)
  Starts supplying clock to the D/A converter.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	0	CMPEN	0	DTCEN	PGA0EN	0	0
1	0	x	0	x	x	0	0

Bit 0

DACEN	Control of D/A converter input clock
0	Stops input clock supply.
1	**Supplies input clock.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting D/A conversion value

- D/A conversion value setting register 0 (DACS0)
  Sets the analog voltage value to be output to the D/A converter pins.

Symbol: DACS0

7	6	5	4	3	2	1	0
DACS07	DACS06	DACS05	DACS04	DACA03	DACS02	DACS01	DACS00
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.7.7 Setting A/D Converter

Figure 5.8 shows the flowchart for setting the A/D converter.

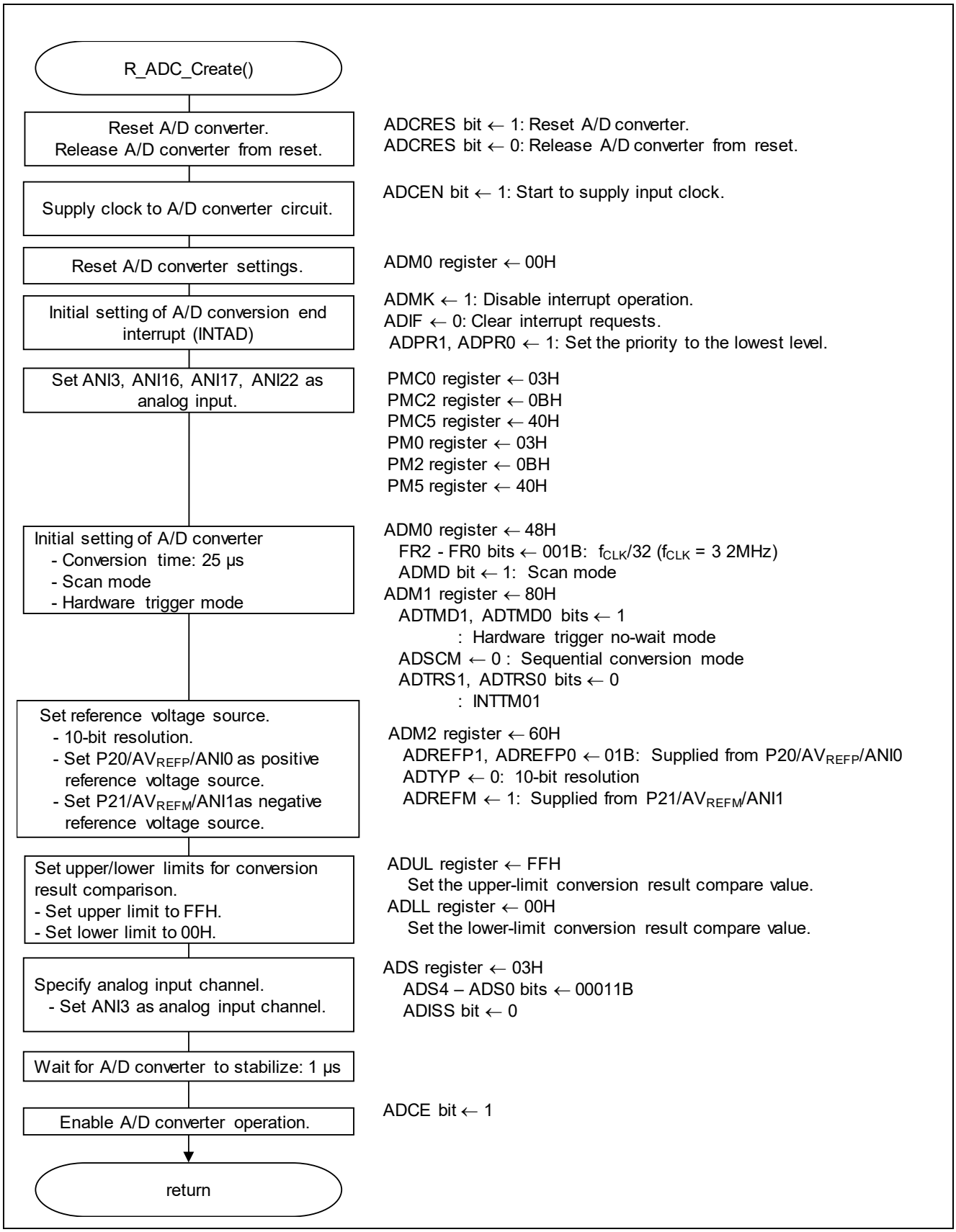

Figure 5.8 Setting A/D Converter

Starting clock supply to A/D converter

- Peripheral enable register 0 (PER0)
  Starts supplying clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
0	ICA1EN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
0	x	**1**	x	0	x	0	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Setting A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Sets the A/D conversion channel select mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**1**	**0**	**0**	**1**	**0**	**0**	x

Bit 6

ADMD	Specification of A/D conversion channel selection mode
0	Select mode
1	**Scan mode**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**0**	**0**	**0**	**1**	**1**	**0**	x

Bits 5 to 1

ADM0					Mode	Conv clock (f_{AD})	No. of conv clock (Sampling clock)	Conv time	Conversion time selection				
FR2	FR1	FR0	LV1	LV2					f_{CLK}= 1MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 16MHz	f_{CLK}= 24MHz
0	0	0	**0**	**0**	**Normal 1**	**f_{CLK}/64**	**19 f_{AD} (No. of Sampling clock: 7 f_{AD})**	1216/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	84µs	50.667µs
0	**0**	**1**				**f_{CLK}/32**		**608/f_{CLK}**			76µs	42µs	**25.333µs**
0	1	0				f_{CLK}/16		304/f_{CLK}		76µs	38µs	19µs	12.667µs
0	1	1				f_{CLK}/8		152/f_{CLK}		38µs	19µs	9.5µs	6.333µs
1	0	0				f_{CLK}/6		114/f_{CLK}		28.5	14.25µs	7.125µs	4.75µs
1	0	1				f_{CLK}/5		95/f_{CLK}	95µs	23.75µs	11.875µs	5.938µs	3.958µs
1	1	0				f_{CLK}/4		76/f_{CLK}	76µs	19µs	9.5µs	4.75µs	3.167µs
1	1	1				f_{CLK}/2		38/f_{CLK}	38µs	9.5µs	4.75µs	2.375µs	Setting prohibited
0	0	0	1	1	Normal 2	f_{CLK}/64	17 f_{AD} (No. of Sampling clock: 5 f_{AD})	1088/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	68µs	45.333µs
0	0	1				f_{CLK}/32		544/f_{CLK}			68µs	34µs	22.667µs
0	1	0				f_{CLK}/16		272/f_{CLK}		68µs	34µs	17µs	11.333µs
0	1	1				f_{CLK}/8		136/f_{CLK}		34µs	17µs	8.5µs	5.667µs
1	0	0				f_{CLK}/6		102/f_{CLK}		25.5µs	12.75µs	6.375µs	4.25µs
1	0	1				f_{CLK}/5		85/f_{CLK}	85µs	21,25µs	10.625µs	5.3125µs	3.542µs
1	1	0				f_{CLK}/4		68/f_{CLK}	68µs	17µs	8.5µs	4.25µs	2.833µs
1	1	1				f_{CLK}/2		34/f_{CLK}	34µs	8.5µs	4.25µs	2.125µs	Setting prohibited

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.
  Specifies the A/D conversion operation mode
  Selects the hardware trigger signal.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
1	**0**	**0**	0	0	0	**0**	**0**

Bits 7 and 6

ADTMD1	ADTMD0	Selection of A/D conversion trigger mode
0	x	Software trigger mode
1	**0**	**Hardware trigger no-wait mode**
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of A/D conversion mode
0	**Sequential conversion mode**
1	One-shot conversion mode

Bits 1 and 0

ADTRS1	ADTRS0	Selection of hardware trigger signal
0	**0**	**End of timer channel 01 count or capture interrupt signal (INTTM01)**
0	1	Event signal selected by ELC
1	0	Real-time clock 2 interrupt signal (INTRTC)
1	1	12-bit interval timer interrupt signal (INTIT)

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting reference voltage source

- A/D converter mode register 2 (ADM2)

Selects the A/D converter positive-side reference voltage source.
Selects the A/D converter negative-side reference voltage source.
Checks the conversion result upper-limit/lower-limit value
Sets SNOOZE mode.
Selects A/D conversion resolution.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP
0	**1**	**1**	0	**0**	**0**	0	**0**

Bits 7 and 6

ADREFP1	ADREFP0	Selection of + side reference voltage source of A/D converter
0	0	Supplied from V_{DD}
0	**1**	**Supplied from AV_{REFP}/ANI**
1	0	Supplied from internal reference voltage (1.45 V)
1	1	Setting prohibited

Bit 5

ADREFM	Selection of □ side reference voltage source of A/D converter
0	Supplied from V_{SS}
1	**Supplied from AV_{REFM}/ANI1**

Bit 3

ADRCK	Checking upper limit and lower limit conversion result values
0	**Interrupt signal (INTAD) is generated when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	Interrupt signal (INTAD) is generated when ADCR register < ADLL register, ADUL register < ADCR register.

Bit 2

AWC	Specification of SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting upper limit and lower limit values for conversion result comparison

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Sets the upper limit and lower limit conversion result compare values.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting input channel

- Analog input channel specification register (ADS)
  Specifies the input channel of analog voltage to be converted.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	0	0	**0**	**0**	**0**	**1**	**1**

Bits 7, 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV_{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV_{REFM} pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	**0**	**0**	**0**	**1**	**1**	**ANI3**	**P23/ANI3 pin**
0	1	0	0	0	0	ANI16	P01/ANI16 pin
0	1	0	0	0	1	ANI17	P00/ANI17 pin
0	1	0	0	1	0	ANI18	P33/ANI18 pin
0	1	0	0	1	1	ANI19	P32/ANI19 pin
0	1	0	1	0	0	ANI20	P31/ANI20 pin
0	1	0	1	0	1	ANI21	P30/ANI21 pin
0	1	0	1	1	0	ANI22	P56/ANI22 pin
0	1	0	1	1	1	—	PGAOUT(PGA output)
1	0	0	0	0	0	—	Temperature sensor output voltage note1
1	0	0	0	0	1	—	Internal reference voltage (1.45V) note1
Other than above						Setting prohibited	

Note1: Operation is possible only in HS (high-speed main) mode.

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting A/D conversion end interrupt

- Interrupt request flag register (IF1H)
  Clears interrupt request flags.
- Interrupt mask flag register (MK1H)
  Disables interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
PIF11	PIF10	PIF9	PIF8	PIF7	KRIF	TMKAIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
PMK11	PMK10	PMK9	PMK8	PMK7	KRMK	TMKAMK	ADMK
x	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.7.8 Setting Comparator

Figure 5.9 shows the flowchart for setting the comparator.

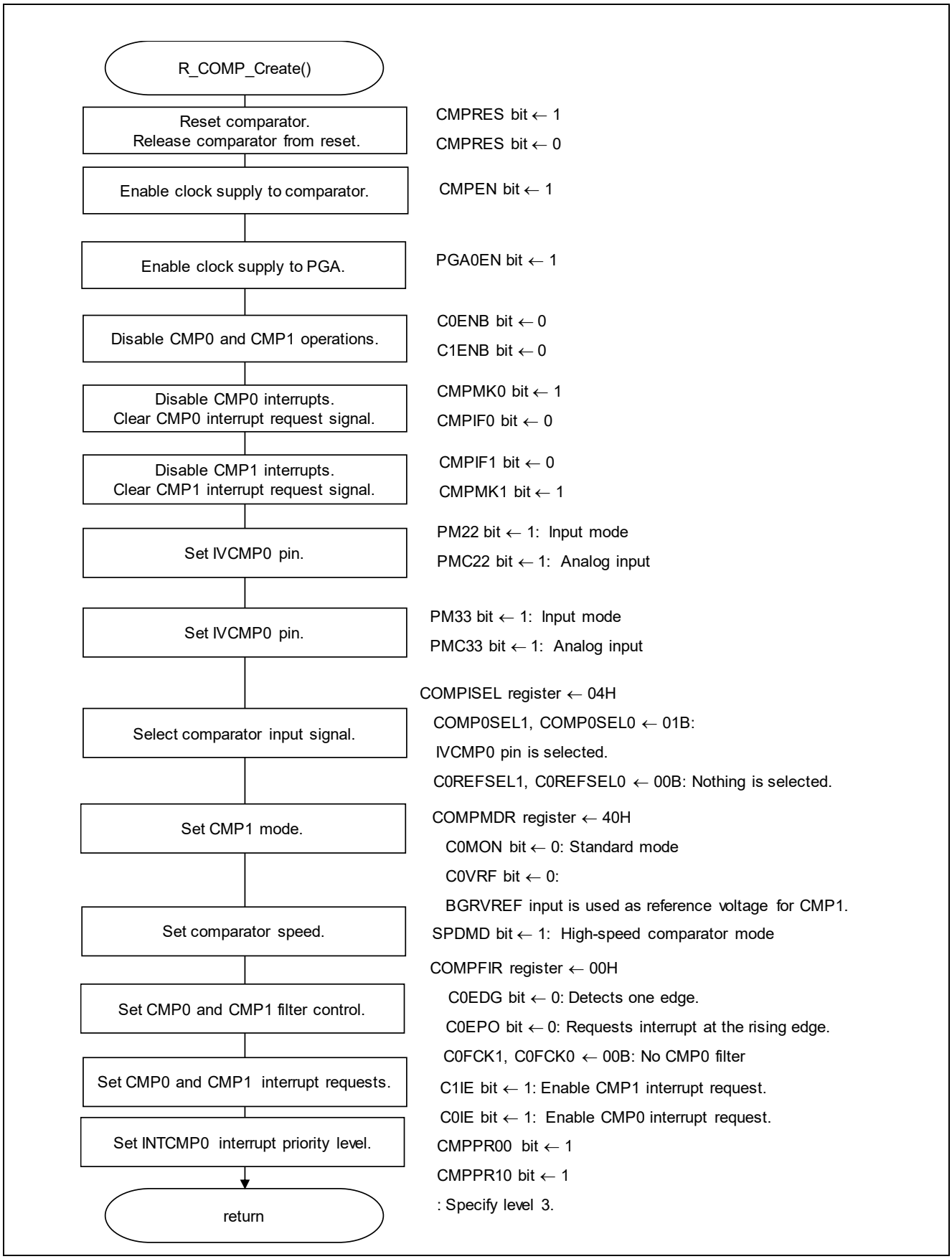

Figure 5.9 Setting Comparators

Starting clock supply to comparator

- Peripheral enable register 1 (PER1)

Starts supplying clock to the A/D converter.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	0	CMPEN	0	DTCEN	PGA0EN	0	0
x	0	**1**	0	x	x	0	0

Bit 5

CMPEN	Control of comparator input clock
0	Stops input clock supply.
1	**Enables input clock supply.**

Setting comparator operation

- Comparator mode setting register (COMPMDR)

Enables comparator operation.

Symbol: COMPMDR

7	6	5	4	3	2	1	0
C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	C0ENB
x	x	x	**0**	x	x	x	**0**

Bit 4

C1ENB	Comparator 1 operation enable
0	**Comparator 1 operation disabled**
1	Comparator 1 operation enabled

Bit 0

C0ENB	Comparator 0 operation enable
0	**Comparator 0 operation disabled**
1	Comparator 0 operation enabled

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting comparator interrupt

- Interrupt request flag register (IF2L)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK2L)
  Disables the interrupt processing.

Symbol: IF2L

7	6	5	4	3	2	1	0
FLIF	IICAIF1	TMKBIF0	ITIF01	ITIF00	DOCIF	CMPIF1	CMPIF0
x	x	x	x	x	x	**0**	**0**

Bits 0 and 1

CMPIF0,1	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK2L

7	6	5	4	3	2	1	0
FLMK	IICAMK1	TMKBMK0	ITMK01	ITMK00	DOCMK	CMPMK1	CMPMK0
x	x	x	x	x	x	**1**	**1**

Bits 4 and 5

CMPMK0,1	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Setting comparator peripheral reset

- Peripheral reset control register (PRR1)
  Controls comparator peripheral resets.

Symbol: PRR1

7	6	5	4	3	2	1	0
DACRES	0	CMPRES	0	0	PGA0RES	0	0
x	0	**0/1**	0	0	x	0	0

Bit 5

CMPRES	Peripheral reset control on each peripheral hardware
0	**Peripheral reset release**
1	**Peripheral reset state**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.7.9 Setting Timer Array Unit

Figure 5.10 shows the flowchart for setting the TAU.

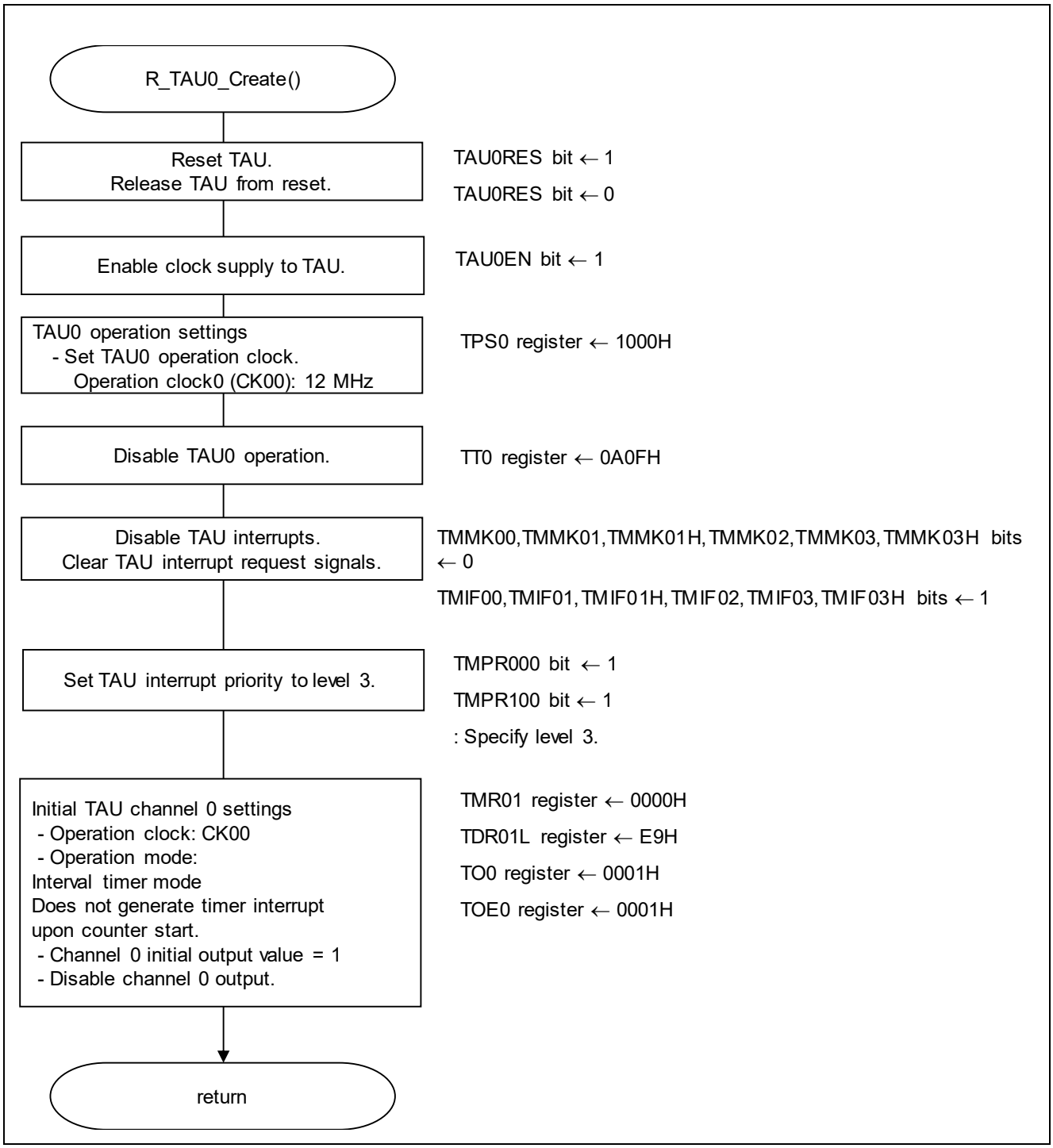

Figure 5.10 Setting Timer Array Unit

Starting clock supply to TAU0

- Peripheral enable register 0 (PER0)

Starts clock supply to TAU0.

Symbol: PER0

7	6	5	4	3	2	1	0
0	IICA1EN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
0	x	x	x	0	x	0	**1**

Bit 0

TAU0EN	Control of TAU0 input clock supply
0	Stops input clock supply.
1	**Supplies input clock.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting timer clock frequency

- Timer clock select register 0 (TPS0)
  Selects the operation clock for TAU0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS031	PRS030	0	0	PRS021	PRS020	PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
x	x	x	x	x	x	x	x	x	x	x	x	**0**	**1**	**1**	**0**

Bits 3 to 0

PRS003	PRS002	PRS001	PRS000	Operation clock (CK00) selection					
					f_{CLK}= 2MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz	f_{CLK}= 24MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	24 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	313kHz	625 kHz	750 kHz
0	**1**	**1**	**0**	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	**156 kHz**	313 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting channel 0 operation mode

- Timer mode register 01 (TMR01)
  Selects the operation clock (f_{MCK}).
  Selects the count clock.
  Sets software trigger start.
  Sets the operation mode.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	0	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 15 and 14

CKS011	CKS010	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by the timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS01	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS010 and CKS011 bits**
1	Valid edge of input signal input from the TI01 pin

Bit 11

SPLIT01	Selection of 8 or 16-bit timer operation for channel 1
0	**Operates as 16-bit timer.** **(Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)**
1	Operates as 8-bit timer.

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 011	CKS 010	0	CCS 01	0	STS 012	STS 011	STS 010	CIS 011	CIS 010	0	0	MD 013	MD 012	MD 011	MD 010
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 10 to 8

STS012	STS011	STS010	Setting of start trigger or capture trigger of channel1
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TI01 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI01 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 and 6

CIS011	CIS010	Selection of TI01 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 011	CKS 010	0	CCS 01	0	STS 012	STS 011	STS 010	CIS 011	CIS 010	0	0	MD 013	MD 012	MD 011	MD 010
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 3 to 0

MD 013	MD 012	MD 011	Operation mode of channel 1	Corresponding function	Count operation of TCR
0	**0**	**0**	**Interval timer mode**	**Interval timer / Square wave output / Divider function / PWM output (master)**	**Counting down**
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		
The operation of each mode varies depending on MD010 bit (see table below).					

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD010	Setting of starting counting and interrupt
- Interval timer mode (0, 0, 0) **- Capture mode (0, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
- Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
- One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation At that time, interrupt is generated.
- Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

Setting interval timer period

- Timer data register 01 (TDR01)
  Sets the interval timer compare value.

Symbol: TDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer interrupt (INTTM01) generation timing = (Set value of TDR01 + 1) x Count clock period

Enabling timer output

- Timer output enable register 0 (TOE0)
  Enables/disables timer output of each channel

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE 07	TOE 06	TOE 05	TOE 04	TOE 03	TOE 02	TOE 01	TOE 00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	**1**	x

Bit 1

TOE01	Timer output enable/disable of channel 0
0	Timer output is disabled. Timer operation is not applied to the TO01 bit and the output is fixed. Writing to the TO01 bit is enabled and the level set in the TO01 bit is output from the TO01 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO01 bit and an output waveform is generated.** **Writing to the TO01 bit is ignored.**

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.7.10 Setting Interrupts

Figure 5.11 shows the flowchart for initial setting of the interrupts.

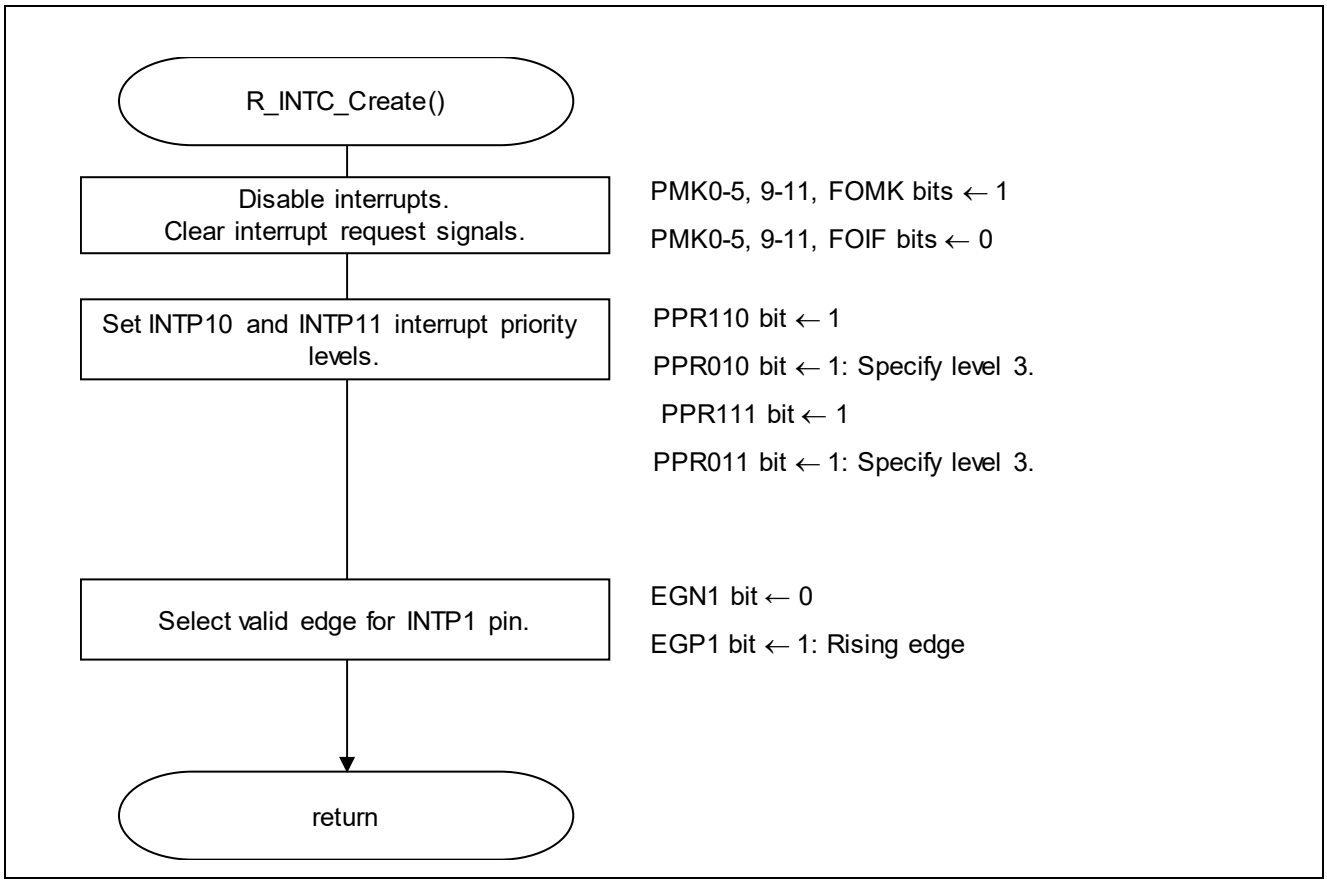

Figure 5.11 Setting Interrupts

Setting interrupt edge

- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
  Selects the valid edge.

Symbol: EGP0

7	6	5	4	3	2	1	0
EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0
0	0	0	0	0	0	**1**	0

Symbol: EGN0

7	6	5	4	3	2	1	0
EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
0	0	0	0	0	0	**0**	0

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 11)
0	0	Edge detection disabled
0	1	Falling edge
1	**0**	**Rising edge**
1	1	Both rising and falling edges

Note: For details of register settings, refer to the RL78/G11 User's Manual: Hardware.

5.7.11 Main Function

Figure 5.12 shows the flowchart for the main function.

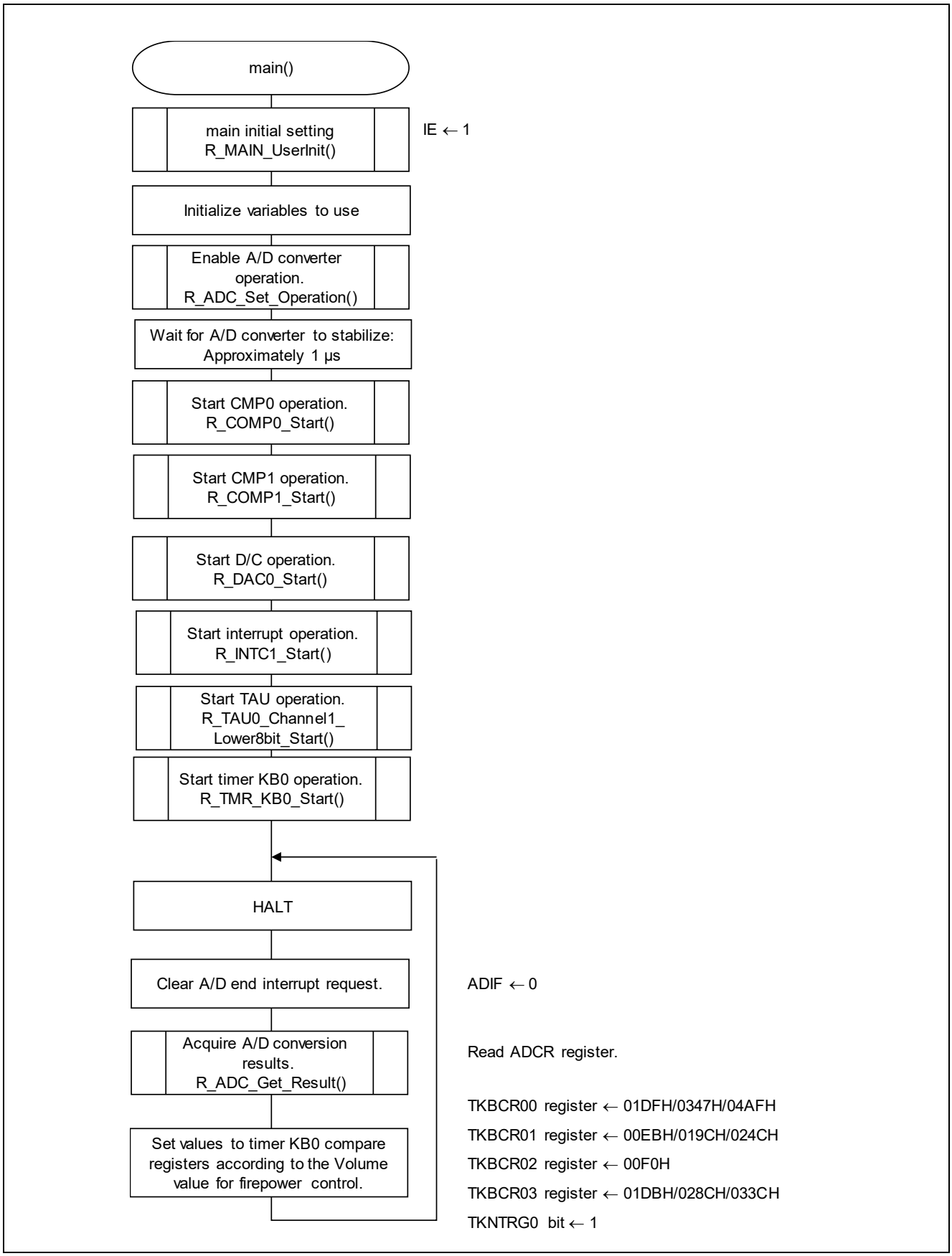

Figure 5.12 main Function

5.7.12 Initial Setting of main

Figure 5.13 shows the flowchart for initial setting of the main.

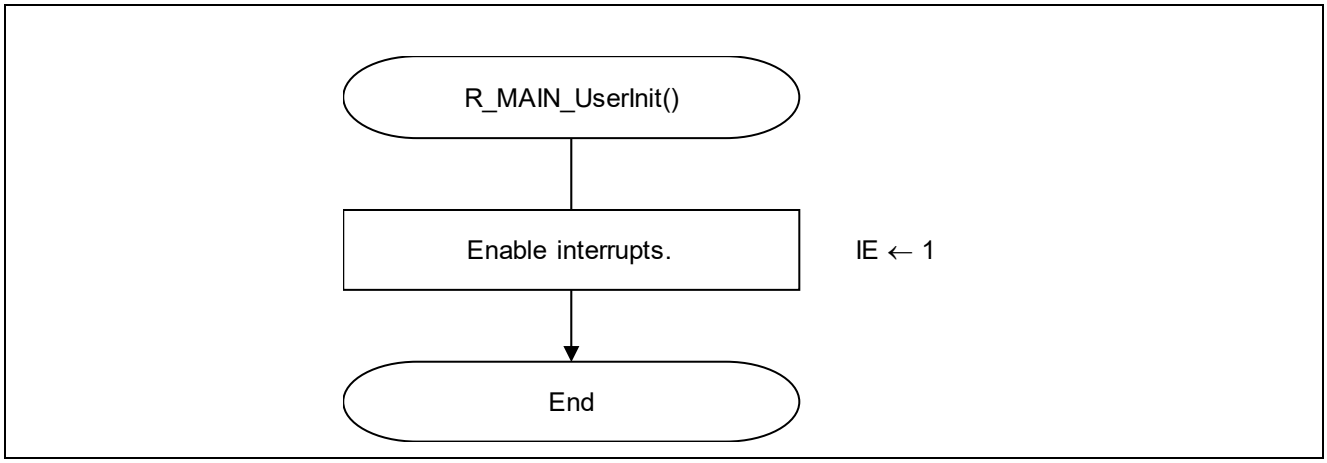

Figure 5.13 Initial Setting of main

5.7.13 Starting Comparator 0 Operation

Figure 5.14 shows the flowchart for starting comparator 0 operation.

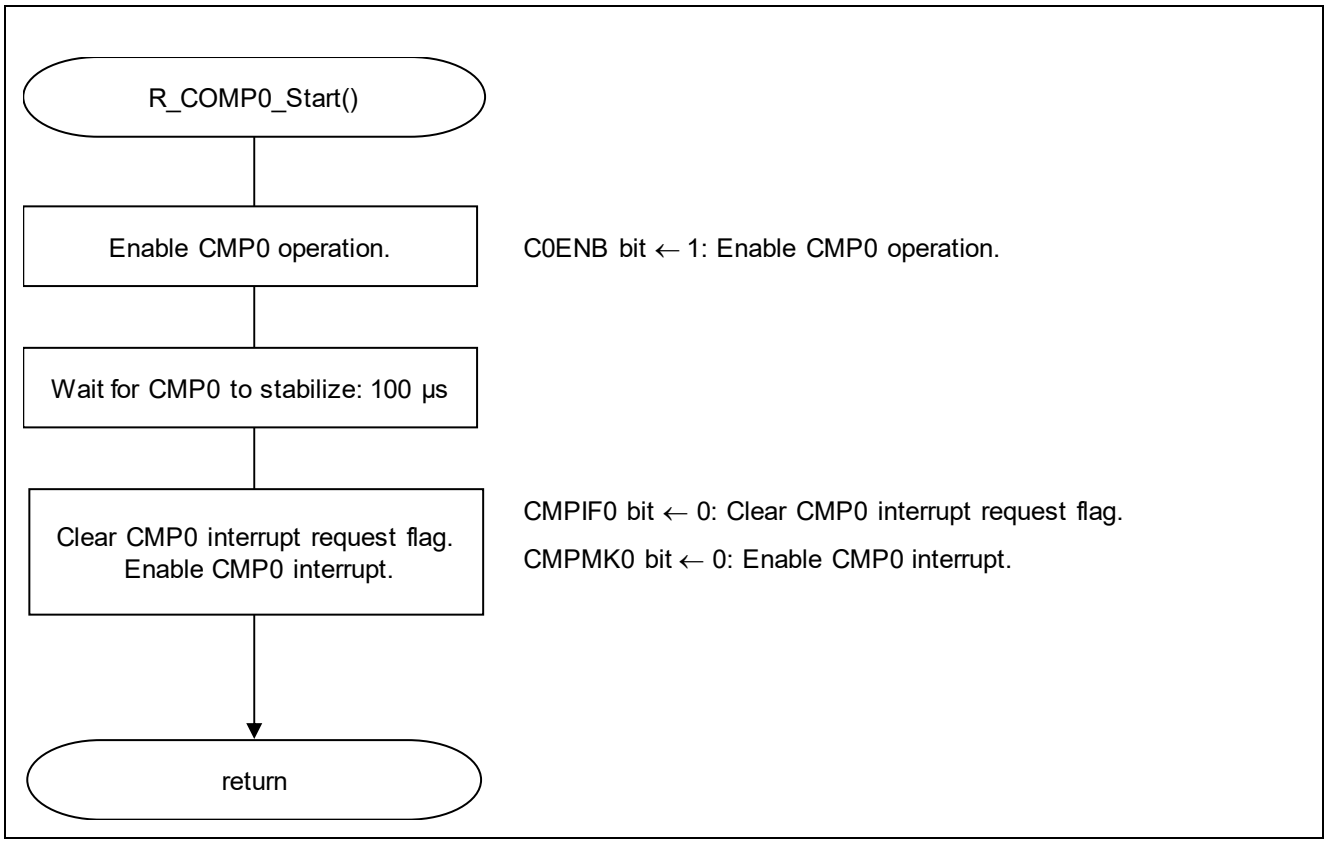

Figure 5.14 Starting Comparator 0 Operation

5.7.14 Starting Comparator 1 Operation

Figure 5.15 shows the flowchart for starting comparator 1 operation.

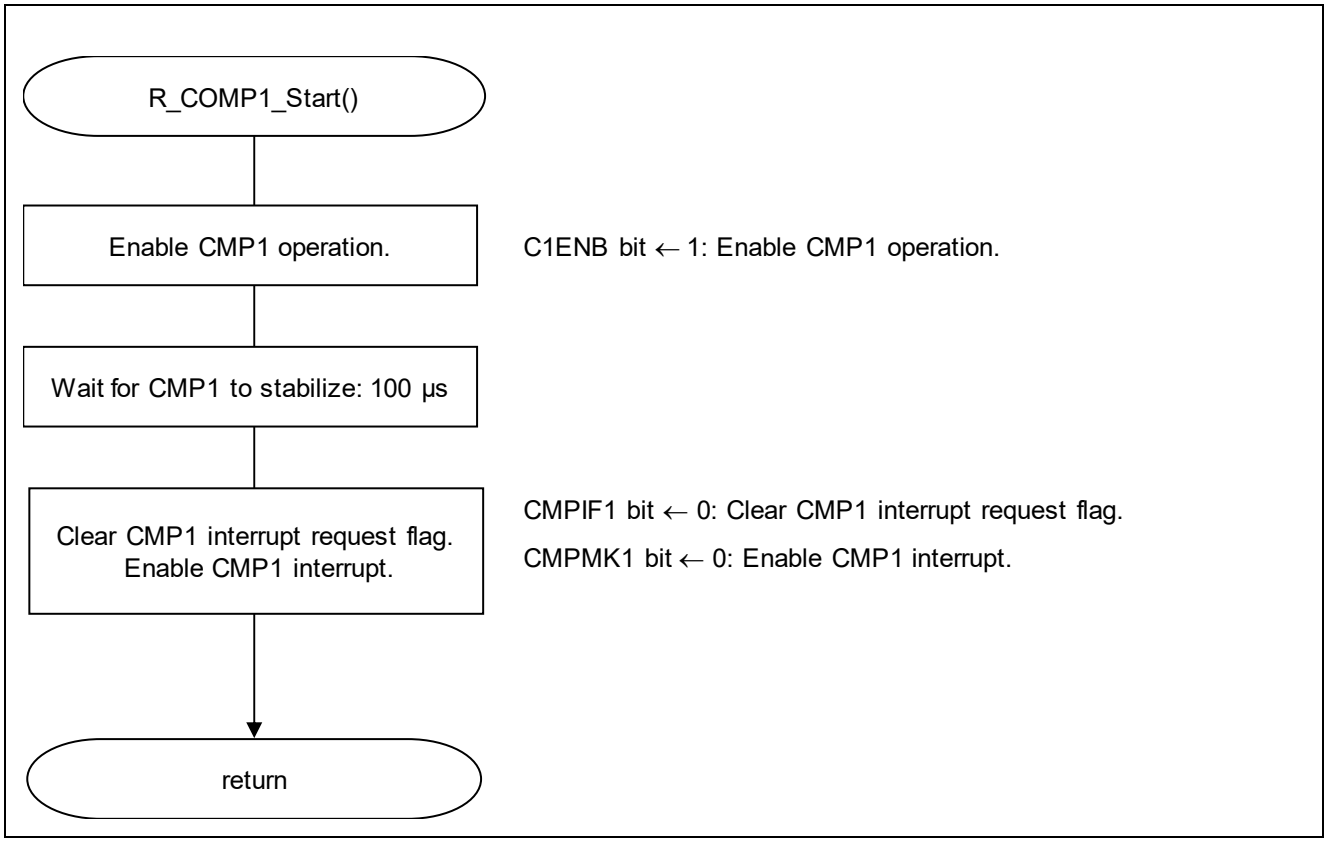

Figure 5.15 Starting Comparator 1 Operation

5.7.15 Starting D/A Converter Operation

Figure 5.16 shows the flowchart for starting D/A converter operation.

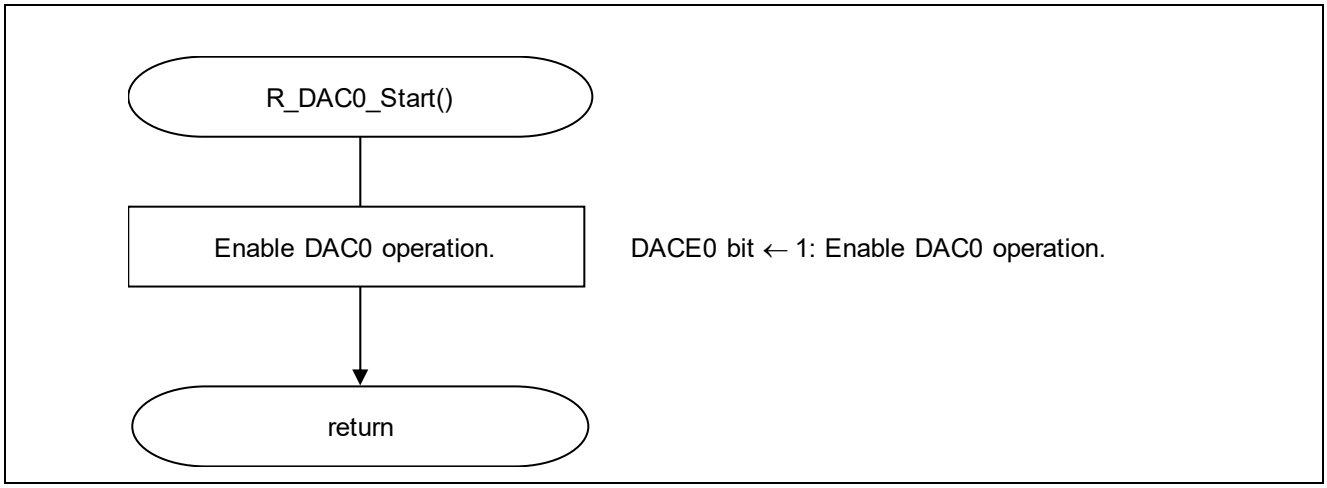

Figure 5.16 Starting D/A Converter Operation

5.7.16 Starting Interrupt Operation

Figure 5.17 shows the flowchart for starting interrupt operation.

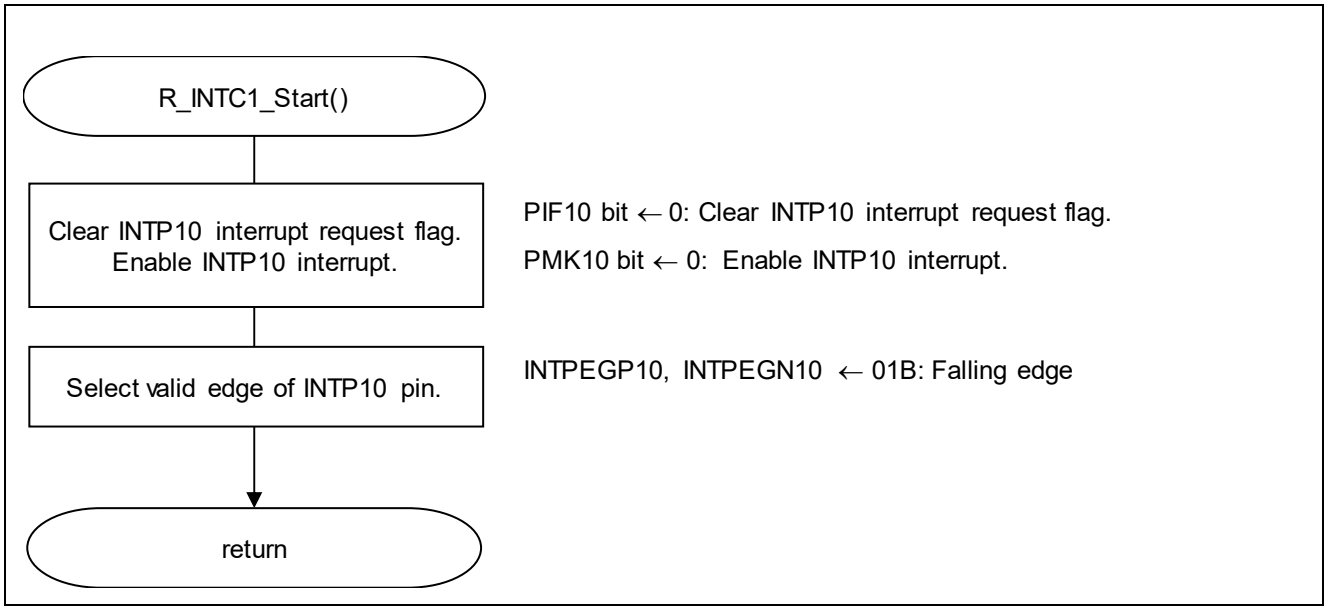

Figure 5.17 Starting Interrupt Operation

5.7.17 Starting TAU Operation

Figure 5.18 shows the flowchart for starting TAU operation.

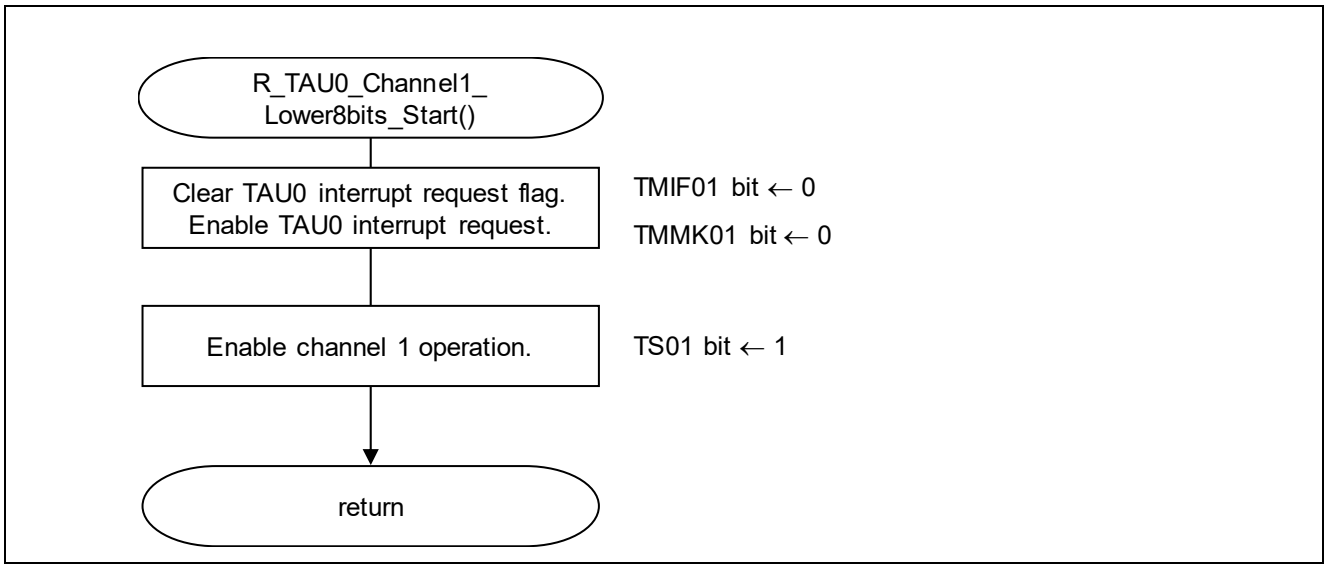

Figure 5.18 Starting TAU Operation

5.7.18 Starting Timer KB0 Operation

Figure 5.19 shows the flowchart for starting timer KB0 operation.

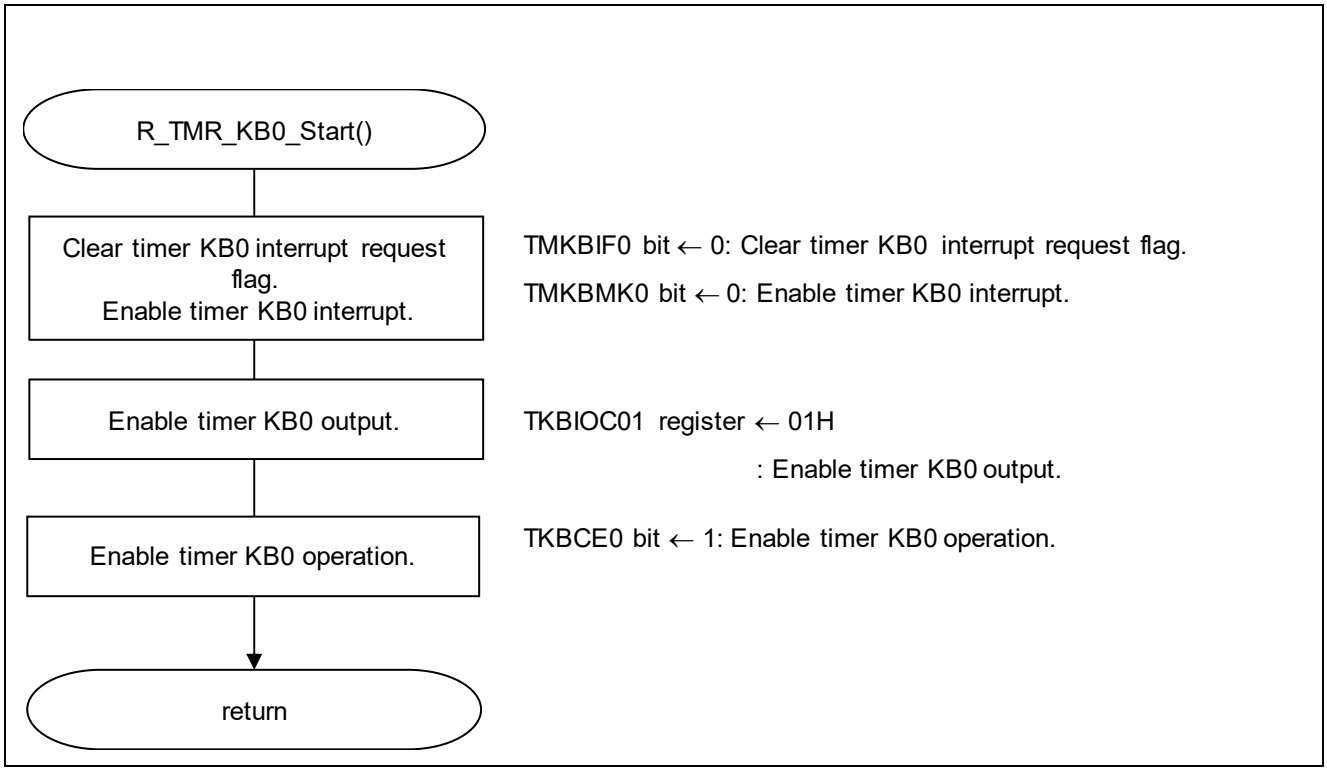

Figure 5.19 Starting Timer KB0 Operation

5.7.19 Enabling A/D Converter Operation

Figure 5.20 shows the flowchart for enabling A/D converter operation.

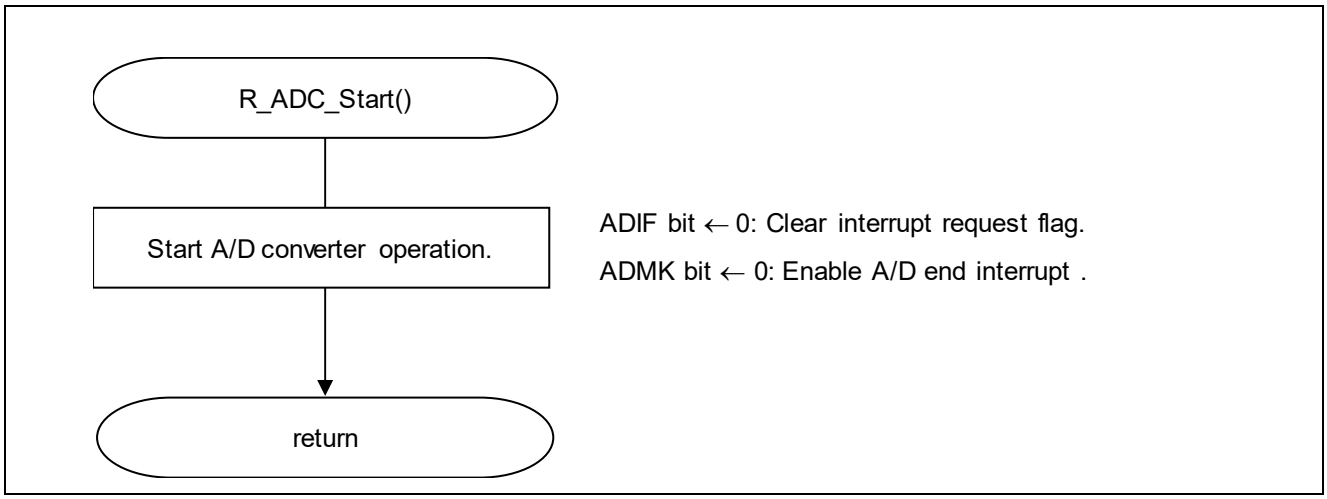

Figure 5.20 Enabling A/D Converter Operation

5.7.20 Starting A/D Conversion Trigger Wait

Figure 5.21 shows the flowchart for starting A/D conversion trigger wait.

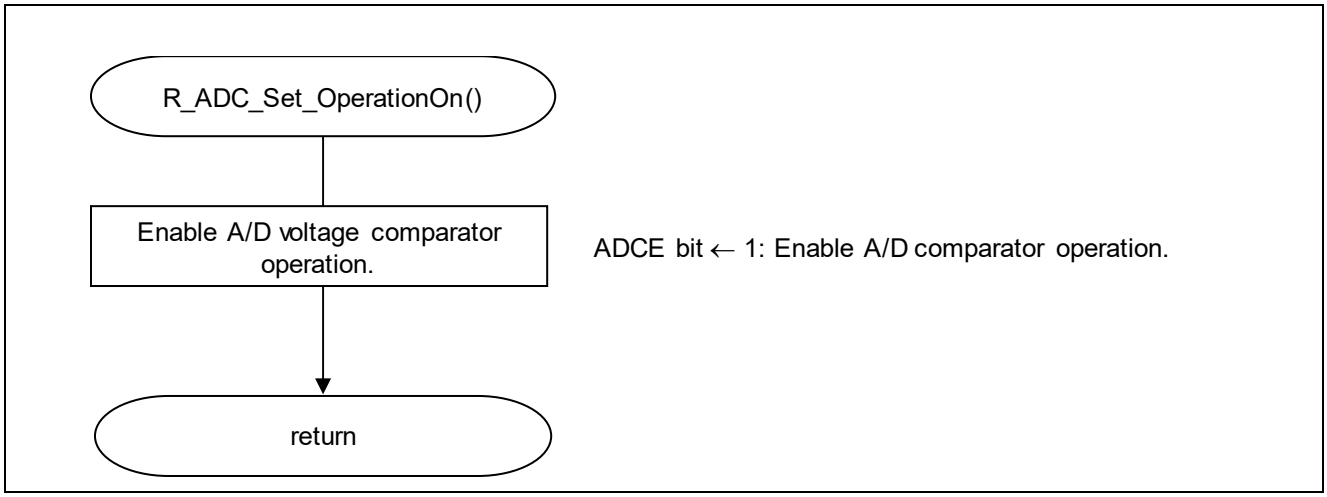

Figure 5.21 Starting A/D Conversion Trigger Wait

5.7.21 Processing TAU Operation End Interrupt

Figure 5.22 shows the flowchart for processing TAU operation end interrupt.

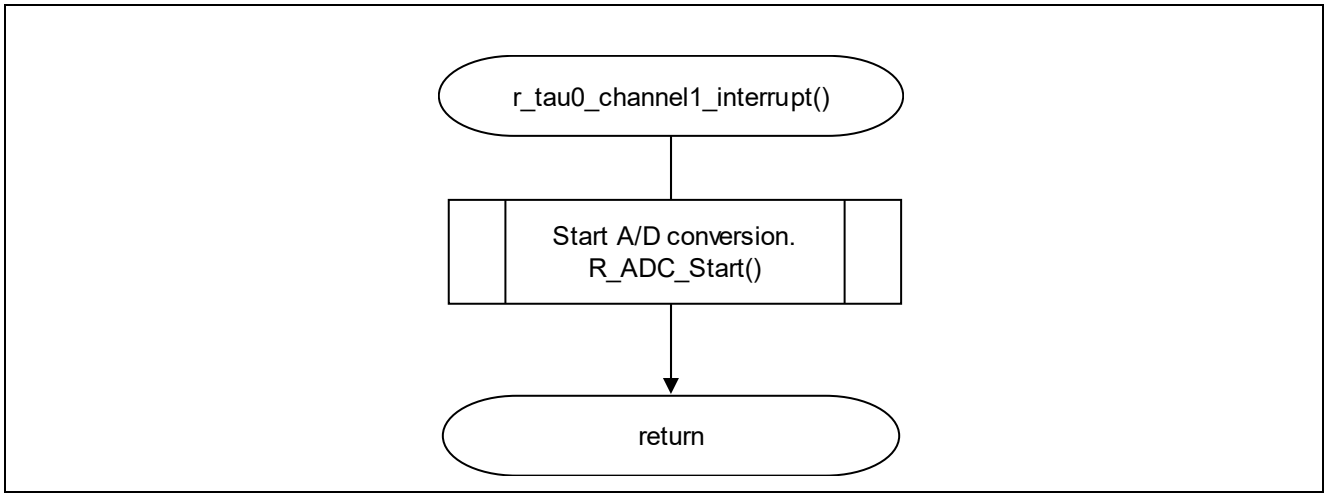

Figure 5.22 Processing TAU Operation End Interrupt

6. Sample Code

The user can get the sample code from the Renesas Electronics website.

7. Reference Documents

RL78/G11 User's Manual: Hardware (R01UH0637E)

RL78 Family User's Manual: Software (R01US0015E)

(Get the latest version from the Renesas Electronics website.)

Technical Updates/Technical News

(Get the latest information from the Renesas Electronics website.)

Website and Support

Renesas Electronics Website

https://www.renesas.com/en-us/

Inquiries

https://www.renesas.com/en-us/support/contact.html

REVISION HISTORY	RL78/G11 IH Control using Timer KB0 CC-RL

Rev.	Date	Revision Contents	
		Page	Description
1.00	Mar. 24, 2017	—	First edition issued.
1.10	Apr. 07, 2017	4, 7	Fixed typo.
1.20	Jan. 31, 2019	37	Fixed typo.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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