Introduction

This application note describes how to change the RL78/G11’s CPU clock and set it to standby (changing operation modes).

This application uses switch input to change the CPU clock and the operation mode, while controlling 5 LEDs to indicate the CPU clock status and the operation mode.

Target Device

RL78/G11

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.
Contents

1. Specifications .......................................................................................................................... 4
2. CPU Clock Changes ................................................................................................................. 7
   1.1 Changing from high-speed on-chip oscillator clock to middle-speed on-chip oscillator clock .... 8
   1.2 Changing from high-speed on-chip oscillator clock to low-speed on-chip oscillator clock ........ 9
   1.3 Changing from high-speed on-chip oscillator clock to high-speed system clock ................. 10
   1.4 Changing from middle-speed on-chip oscillator clock to high-speed on-chip oscillator clock .... 12
   1.5 Changing from middle-speed on-chip oscillator clock to low-speed on-chip oscillator clock ... 13
   1.6 Changing from high-speed on-chip oscillator clock to high-speed system clock ................. 14
   1.7 Changing from low-speed on-chip oscillator clock to high-speed on-chip oscillator clock ...... 16
   1.8 Changing from low-speed on-chip oscillator clock to middle-speed on-chip oscillator clock ... 17
   1.9 Changing from low-speed on-chip oscillator clock to high-speed system clock .................. 18
   1.10 Changing from high-speed system clock to high-speed on-chip oscillator clock ................. 20
   1.11 Changing from high-speed system clock to middle-speed on-chip oscillator clock .......... 21
   1.12 Changing from high-speed system clock to low-speed on-chip oscillator clock ................. 22

3. Operation Confirmation Conditions ......................................................................................... 23

4. Related Application Notes ..................................................................................................... 23

5. Hardware Explanation ............................................................................................................. 24
   4.1 Hardware Configuration Example ....................................................................................... 24
   4.2 Used Pin List ....................................................................................................................... 24

5. Software Explanation ............................................................................................................. 25
   5.1 Operation Outline ............................................................................................................... 25
   5.2 Option Byte Settings ......................................................................................................... 28
   5.3 Variables ........................................................................................................................... 28
   5.4 Functions (subroutines) ..................................................................................................... 29
   5.5 Function (subroutine) Specifications .................................................................................. 30
   5.6 Flowcharts ......................................................................................................................... 38
   5.6.1 Main Processing............................................................................................................. 39
   5.6.2 Initialization Function .................................................................................................... 43
   5.6.3 System Function ............................................................................................................ 44
   5.6.4 Input/Output Port Settings .............................................................................................. 45
   5.6.5 Clock Generator Setting ................................................................................................ 46
   5.6.6 External Interrupt Setting ............................................................................................... 51
   5.6.7 12-bit Interval Timer Setting .......................................................................................... 53
   5.6.8 Main initializes settings .................................................................................................. 56
   5.6.9 Status Transition AtoB .................................................................................................. 57
   5.6.10 CPU operation (NOP instruction execution) ................................................................. 57
   5.6.11 Status Transition BtoD ............................................................................................... 58
   5.6.12 Error Processing of Status Transition ......................................................................... 60
   5.6.13 Status Transition DtoL ................................................................................................ 60
   5.6.14 Status Transition LtoD ................................................................................................. 61
   5.6.15 Status Transition DtoM ............................................................................................... 61
   5.6.16 Status Transition MtoD ............................................................................................... 62
   5.6.17 Status Transition DtoB ................................................................................................ 63
   5.6.18 Status Transition BtoF ................................................................................................ 65
   5.6.19 Status Transition FtoB ................................................................................................ 65
   5.6.20 Status Transition BtoG ................................................................................................ 66
   5.6.21 Status Transition GtoB ................................................................................................ 66
   5.6.22 Status Transition BtoH ................................................................................................ 67
   5.6.23 A/D Converter Setting ................................................................................................. 68
   5.6.24 A/D Converter Initial Setting ....................................................................................... 69
   5.6.25 Status Transition HtoB ............................................................................................... 74
   5.6.26 Status Transition BtoC ............................................................................................... 75
1. Specifications

This application describes how to switch the CPU clock and operation mode using switch input, as shown in Figure 1.1 Operating Mode Status Transition Diagram.

In addition, the application controls five LEDs to indicate the status of the CPU clock and the operation mode.

The Peripheral Functions and Applications used in this application note, Operating Mode Status Transition Diagram, and Operation Modes and Corresponding LED Status are show in Table 1.1, Figure 1.1, and Table 1.2, correspondingly.

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port output</td>
<td>Controls LEDs (LED1-LED5) connected to pins P00, P01, P54, P55, P56.</td>
</tr>
<tr>
<td>External interrupt</td>
<td>Interrupt (INTP0) that detects a pin input edge according to switch input (SW1).</td>
</tr>
<tr>
<td>12-bit interval timer</td>
<td>Interrupt (INTIT) that detects an interval signal from the 12-bit interval timer</td>
</tr>
<tr>
<td>A/D converter</td>
<td>Converts analog signal input level of the P20/ANI0 pin.</td>
</tr>
</tbody>
</table>
Figure 1.1 Operating Mode Status Transition Diagram
### Table 1.2 Operation Modes and Corresponding LED Status

<table>
<thead>
<tr>
<th>CPU/Peripheral Hardware Clock (fCLK)</th>
<th>Operation mode</th>
<th>LED Status</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Normal operation</td>
<td>LED1</td>
</tr>
<tr>
<td>High-speed on-chip oscillator clock (fIH)</td>
<td>mode</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>HALT mode</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>SNOOZE mode</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>STOP mode</td>
<td>OFF</td>
</tr>
<tr>
<td>Middle-speed on-chip oscillator clock (fIM)</td>
<td>Normal operation mode</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>HALT mode</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>SNOOZE mode</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>STOP mode</td>
<td>OFF</td>
</tr>
<tr>
<td>Low-speed on-chip oscillator clock (fIL)</td>
<td>Normal operation mode</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>HALT mode</td>
<td>OFF</td>
</tr>
<tr>
<td>High-speed system clock (fMX)</td>
<td>Normal operation</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>HALT mode</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>STOP mode</td>
<td>OFF</td>
</tr>
</tbody>
</table>
1.1 CPU Clock Changes

This section describes the special function register (SFR) settings required for changing the CPU clock.

- Changing from high-speed on-chip oscillator clock to middle-speed on-chip oscillator clock
- Changing from high-speed on-chip oscillator clock to low-speed on-chip oscillator clock
- Changing from high-speed on-chip oscillator clock to high-speed system clock
- Changing from middle-speed on-chip oscillator clock to high-speed on-chip oscillator clock
- Changing from middle-speed on-chip oscillator clock to low-speed on-chip oscillator clock
- Changing from middle-speed on-chip oscillator clock to high-speed system clock
- Changing from low-speed on-chip oscillator clock to high-speed on-chip oscillator clock
- Changing from low-speed on-chip oscillator clock to middle-speed on-chip oscillator clock
- Changing from low-speed on-chip oscillator clock to high-speed system clock
- Changing from high-speed system clock to high-speed on-chip oscillator clock
- Changing from high-speed system clock to middle-speed on-chip oscillator clock
- Changing from high-speed system clock to low-speed on-chip oscillator clock
1.1.1 Changing from high-speed on-chip oscillator clock to middle-speed on-chip oscillator clock

When changing the CPU clock from the high-speed on-chip oscillator clock to the middle-speed on-chip oscillator clock, start the oscillation using the clock operation status control register (CSC), then wait for the oscillation to stabilize using the timer function or another function. After the oscillation stabilization time has elapsed, set the middle-speed on-chip oscillator clock to \( f_{CLK} \) using the system clock control register (CKC). Confirm that the status of the main on-chip oscillator clock status has switched to the middle-speed on-chip oscillator clock, and then stop the high-speed on-chip oscillator.

① Set (1) the MIOEN bit of the CSC register, and then start oscillating the middle-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
<td>HIHOSTOP</td>
</tr>
<tr>
<td>x</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

② Use a software wait to wait for the oscillation of the middle-speed on-chip oscillator to stabilize. Count the wait time (oscillation stabilization time: 4µs) using the timer function or another function.

③ Set(1) the MCM1 bit of the CKC register to specify the middle-speed on-chip oscillator clock as the main on-chip oscillator clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CLS</td>
<td>CSS</td>
<td>MCS</td>
<td>MCM0</td>
<td>0</td>
<td>0</td>
<td>MCS1</td>
<td>MCM1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

④ Confirm that the MCS1 bit of the CKC register has changed to 1, set (1) the HIHOSTOP bit and stop the oscillating the high-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
<td>HIHOSTOP</td>
</tr>
<tr>
<td>x</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.2 Changing from high-speed on-chip oscillator clock to low-speed on-chip oscillator clock

When changing the CPU clock from the high-speed on-chip oscillator clock to the low-speed on-chip oscillator clock, start the oscillation using the subsystem clock select register (CKSEL), then wait for the oscillation to stabilize using the timer function or another function. After the oscillation stabilization time has elapsed, set the low-speed on-chip oscillator clock to $f_{CLK}$ using the system clock control register (CKC). Confirm that the status of the CPU/peripheral hardware clock status has switched to the subsystem clock, and then stop the high-speed on-chip oscillator.

① Set (1) the SELLOSC bit of the CKSEL register, and then start oscillating the low-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CKSEL</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

② Use a software wait to wait for the oscillation of the low-speed on-chip oscillator to stabilize. Count the wait time (oscillation stabilization time: 210µs) using the timer function or another function. In this application note is always to operate the low-speed on-chip oscillator. For this reason, it does not perform oscillation stabilization wait of the low-speed on-chip oscillator.

③ Set (1) the CSS bit of the CKC register to specify the subsystem clock as the CPU/peripheral hardware clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

④ Confirm that the CLS bit of the CKC register has changed to 1, set (1) the HIOSTOP bit and stop the oscillating the high-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.3 Changing from high-speed on-chip oscillator clock to high-speed system clock

When changing the CPU clock from the high-speed on-chip oscillator clock to the high-speed system clock, set the oscillator and start oscillation using the following registers: clock operation mode control register (CMC), oscillation stabilization time select register (OSTS), clock operation status control register (CSC). Next, wait for the oscillation to stabilize using the oscillation stabilization time counter status register (OSTC).

After the oscillation stabilizes, set the high-speed system clock to $f_{CLK}$ using the system clock control register (CKC).

Confirm that the status of the main system clock has changed to the high-speed system clock, and then stop the high-speed on-chip oscillator.

1. Set (1) the OSCSEL bit of the CMC register (when $f_x > 10MHz$, set (1) the AMPH bit) to operate the X1 oscillator. Set (1) the EXCLK bit and OSCSEL bit when using the external clock.

<table>
<thead>
<tr>
<th>CMC</th>
<th>EXCLK</th>
<th>OSCSEL</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>AMPH</th>
</tr>
</thead>
<tbody>
<tr>
<td>0/1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0/1</td>
</tr>
</tbody>
</table>

AMPH bit: clear to 0 when the X1 oscillation clock is 10 MHZ or lower.

2. Using the OSTS register, select the oscillation stabilization time of the X1 oscillation circuit. This setting does not have to exist at the time the external clock is used.

Example: Set the following values for a wait of at least 102μs based on a 10 MHz resonator.

<table>
<thead>
<tr>
<th>OSTS</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>OSTS2</td>
<td>OSTS1</td>
<td>OSTS0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

3. Clear (0) the MSTOP bit of the CSC register to start oscillating the X1 oscillator. After the external clock is input to the external clock signal, to clear (0) the MSTOP bit.

<table>
<thead>
<tr>
<th>CSC</th>
<th>MSTOP</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>MIOEN</th>
<th>HIOSTOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>0</td>
</tr>
</tbody>
</table>

4. Use the OSTC register to wait for oscillation of the X1 oscillator to stabilize. External clock is not required oscillation stabilization wait.

Example: Wait until the bits reach the following values for a wait of at least 102μs based on a 10 MHz resonator.

<table>
<thead>
<tr>
<th>OSTC</th>
<th>MOST8</th>
<th>MOST9</th>
<th>MOST10</th>
<th>MOST11</th>
<th>MOST13</th>
<th>MOST15</th>
<th>MOST17</th>
<th>MOST18</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
⑤ Set(1) the MCM0 bit of the CKC register to specify the high-speed system clock as the main system clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CLS</td>
<td>CSS</td>
<td>MCS</td>
<td>MCM0</td>
<td>0</td>
<td>0</td>
<td>MCS1</td>
<td>MCM1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

⑥ Confirm that the MCS bit of the CKC register has changed to 1, set (1) the HIOSTOP bit and stop the oscillating the high-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
<td>HIOSTOP</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>1</td>
</tr>
</tbody>
</table>

Register setting values:
- \(x\): unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.4 Changing from middle-speed on-chip oscillator clock to high-speed on-chip oscillator clock

When changing the CPU clock from the middle-speed on-chip oscillator clock to the high-speed on-chip oscillator clock, start the oscillation using the clock operation status control register (CSC), then wait for the oscillation to stabilize using the timer function or another function. After the oscillation stabilization time has elapsed, set the high-speed on-chip oscillator clock to \( f_{CLK} \) using the system clock control register (CKC). Confirm that the status of the main on-chip oscillator clock status has switched to the high-speed on-chip oscillator clock, and then stop the middle-speed on-chip oscillator.

① Clear (0) the HIOSTOP bit of the CSC register, and then start oscillating the high-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MIOEN</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>HIOSTOP</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

② Use a software wait to wait for the oscillation of the high-speed on-chip oscillator to stabilize. Count the wait time (oscillation stabilization time: 65µs) using the timer function or another function.

③ Clear (0) the MCM1 bit of the CKC register to specify the high-speed on-chip oscillator clock as the main on-chip oscillator clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLS</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CSS</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MCS</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MCM0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MCM1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

④ Confirm that the MCS1 bit of the CKC register has changed to 0, clear (0) the MIOEN bit and stop the oscillating the middle-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MIOEN</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>HIOSTOP</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.5 Changing from middle-speed on-chip oscillator clock to low-speed on-chip oscillator clock

When changing the CPU clock from the middle-speed on-chip oscillator clock to the low-speed on-chip oscillator clock, start the oscillation using the subsystem clock select register (CKSEL), then wait for the oscillation to stabilize using the timer function or another function. After the oscillation stabilization time has elapsed, set the low-speed on-chip oscillator clock to fCLK using the system clock control register (CKC). Confirm that the status of the CPU/peripheral hardware clock status has switched to the subsystem clock, and then stop the middle-speed on-chip oscillator.

① Set (1) the SELLOSC bit of the CKSEL register, and then start oscillating the low-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CKSEL</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>SELLOSC</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

② Use a software wait to wait for the oscillation of the low-speed on-chip oscillator to stabilize. Count the wait time (oscillation stabilization time: 210µs) using the timer function or another function. In this application note is always to operate the low-speed on-chip oscillator. For this reason, it does not perform oscillation stabilization wait of the low-speed on-chip oscillator.

③ Set(1) the CSS bit of the CKC register to specify the subsystem clock as the CPU/peripheral hardware clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CSS</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

④ Confirm that the CLS bit of the CKC register has changed to 1, clear (0) the MIOEN bit and stop the oscillating the middle-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
</tr>
<tr>
<td>x</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.6 Changing from middle-speed on-chip oscillator clock to high-speed system clock

When changing the CPU clock from the middle-speed on-chip oscillator clock to the high-speed system clock, set the oscillator and start oscillation using the following registers: clock operation mode control register (CMC), oscillation stabilization time select register (OSTS), clock operation status control register (CSC). Next, wait for the oscillation to stabilize using the oscillation stabilization time counter status register (OSTC).

After the oscillation stabilizes, set the high-speed system clock to fCLK using the system clock control register (CKC). Confirm that the status of the main system clock has changed to the high-speed system clock, and then stop the middle-speed on-chip oscillator.

① Set (1) the OSCSEL bit of the CMC register (when fx > 10MHz, set (1) the AMPH bit) to operate the X1 oscillator. Set (1) the EXCLK bit and OSCSEL bit when using the external clock.

<table>
<thead>
<tr>
<th>CMC</th>
<th>EXCLK</th>
<th>OSCSEL</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0/1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

AMPH bit: clear to 0 when the X1 oscillation clock is 10 MHz or lower.

② Using the OSTS register, select the oscillation stabilization time of the X1 oscillation circuit. This setting does not have to exist at the time the external clock is used.

Example: Set the following values for a wait of at least 102μs based on a 10 MHz resonator.

<table>
<thead>
<tr>
<th>OSTS</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>OSTS2</th>
<th>OSTS1</th>
<th>OSTS0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

③ Clear (0) the MSTOP bit of the CSC register to start oscillating the X1 oscillator. After the external clock is input to the external clock signal, to clear (0) the MSTOP bit.

<table>
<thead>
<tr>
<th>CSC</th>
<th>MSTOP</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>MIOEN</th>
<th>HIOSTOP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>x</td>
</tr>
</tbody>
</table>

④ Use the OSTC register to wait for oscillation of the X1 oscillator to stabilize. External clock is not required oscillation stabilization wait.

Example: Wait until the bits reach the following values for a wait of at least 102μs based on a 10 MHz resonator.

<table>
<thead>
<tr>
<th>OSTC</th>
<th>MOST8</th>
<th>MOST9</th>
<th>MOST10</th>
<th>MOST11</th>
<th>MOST13</th>
<th>MOST15</th>
<th>MOST17</th>
<th>MOST18</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
⑤ Set(1) the MCM0 bit of the CKC register to specify the high-speed system clock as the main system clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

⑥ Confirm that the MCS bit of the CKC register has changed to 1, clear (0) the MIOEN bit and stop the oscillating the middle-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

 Register setting values:
x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.7 Changing from low-speed on-chip oscillator clock to high-speed on-chip oscillator clock

When changing the CPU clock from the low-speed on-chip oscillator clock to the high-speed on-chip oscillator clock, start the oscillation using the clock operation status control register (CSC), then wait for the oscillation to stabilize using the timer function or another function. After the oscillation stabilization time has elapsed, set the high-speed on-chip oscillator clock to fCLK using the system clock control register (CKC). Confirm that the status of the CPU/peripheral hardware clock status has switched to the main system clock, and then stop the low-speed on-chip oscillator.

① Clear (0) the HIOSTOP bit of the CSC register, and then start oscillating the high-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
<td>HIOSTOP</td>
<td></td>
</tr>
<tr>
<td>x</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

② Use a software wait to wait for the oscillation of the high-speed on-chip oscillator to stabilize. Count the wait time (oscillation stabilization time: 65µs) using the timer function or another function.

③ Clear (0) the CSS bit of the CKC register to specify the main system clock as the CPU/peripheral hardware clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLS</td>
<td>CSS</td>
<td>MCS</td>
<td>MCM0</td>
<td>0</td>
<td>0</td>
<td>MCSI</td>
<td>MCM1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

④ Confirm that the CLS bit of the CKC register has changed to 0, clear (0) the SELLOSC bit of the subsystem clock select register (CKSEL) and stop the oscillating the low-speed on-chip oscillator. In this application note, for WUTMMCK0 bit of the subsystem clock supply mode control register (OSMC) is 1, does not stop the low-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CKSEL</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>SELLOSC</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Note: Changing the value of the MCM0 bit is prohibited while the CPU/peripheral hardware clock is operating with the subsystem clock.

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.8 Changing from low-speed on-chip oscillator clock to middle-speed on-chip oscillator clock

When changing the CPU clock from the low-speed on-chip oscillator clock to the middle-speed on-chip oscillator clock, start the oscillation using the clock operation status control register (CSC), then wait for the oscillation to stabilize using the timer function or another function. After the oscillation stabilization time has elapsed, set the middle-speed on-chip oscillator clock to \( f_{CLK} \) using the system clock control register (CKC). Confirm that the status of the CPU/peripheral hardware clock status has switched to the main system clock, and then stop the low-speed on-chip oscillator.

① Set (1) the MIOEN bit of the CSC register, and then start oscillating the middle-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
<td>HIOSTOP</td>
<td></td>
</tr>
<tr>
<td>x</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>x</td>
<td></td>
</tr>
</tbody>
</table>

② Use a software wait to wait for the oscillation of the middle-speed on-chip oscillator to stabilize. Count the wait time (oscillation stabilization time: 4\( \mu \)s) using the timer function or another function.

③ Clear(0) the CSS bit of the CKC register to specify the main system clock as the CPU/peripheral hardware clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLS</td>
<td>CSS</td>
<td>MCS</td>
<td>MCM0</td>
<td>0</td>
<td>0</td>
<td>MCS1</td>
<td>MCM1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

④ Confirm that the CLS bit of the CKC register has changed to 0, clear (0) the SELLOSC bit of the subsystem clock select register (CKSEL) and stop the oscillating the low-speed on-chip oscillator. In this application note, for WUTMMCK0 bit of the subsystem clock supply mode control register (OSMC) is 1, does not stop the low-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CKSEL</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>SELLOSC</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Note: Changing the value of the MCM0 bit is prohibited while the CPU/peripheral hardware clock is operating with the subsystem clock.

Register setting values:
- \( \times \): unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.9 Changing from low-speed on-chip oscillator clock to high-speed system clock

When changing the CPU clock from the low-speed on-chip oscillator clock to the high-speed system clock, set the oscillator and start oscillation using the following registers: clock operation mode control register (CMC), oscillation stabilization time select register (OSTS), clock operation status control register (CSC). Next, wait for the oscillation to stabilize using the oscillation stabilization time counter status register (OSTC).

After the oscillation stabilizes, set the high-speed system clock to fCLK using the system clock control register (CKC). Confirm that the status of the CPU/peripheral hardware clock has changed to the main system clock, and then stop the low-speed on-chip oscillator.

① Set (1) the OSCSEL bit of the CMC register (when fx > 10MHz, set (1) the AMPH bit) to operate the X1 oscillator. Set (1) the EXCLK bit and OSCSEL bit when using the external clock.

<table>
<thead>
<tr>
<th>CMC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EXCLK</td>
<td>OSCSEL</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>AMPH</td>
</tr>
<tr>
<td>0/1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0/1</td>
</tr>
</tbody>
</table>

AMPH bit: clear to 0 when the X1 oscillation clock is 10 MHz or lower.

② Using the OSTS register, select the oscillation stabilization time of the X1 oscillation circuit. This setting does not have to exist at the time the external clock is used.

Example: Set the following values for a wait of at least 102 μs based on a 10 MHz resonator.

<table>
<thead>
<tr>
<th>OSTS</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>OSTS2</td>
<td>OSTS1</td>
<td>OSTS0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

③ Clear (0) the MSTOP bit of the CSC register to start oscillating the X1 oscillator. After the external clock is input to the external clock signal, to clear (0) the MSTOP bit.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td></td>
</tr>
</tbody>
</table>

④ Use the OSTC register to wait for oscillation of the X1 oscillator to stabilize. External clock is not required oscillation stabilization wait.

Example: Wait until the bits reach the following values for a wait of at least 102 μs based on a 10 MHz resonator.

<table>
<thead>
<tr>
<th>OSTC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MOST8</td>
<td>MOST9</td>
<td>MOST10</td>
<td>MOST11</td>
<td>MOST13</td>
<td>MOST15</td>
<td>MOST17</td>
<td>MOST18</td>
</tr>
<tr>
<td>0/1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
⑤ Clear(0) the CSS bit of the CKC register to specify the main system clock as the CPU/peripheral hardware clock.

```
<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLS</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>CSS</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>MCS</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>MCM0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>MCM1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>
```

⑥ Confirm that the CLS bit of the CKC register has changed to 0, clear (0) the SELLOSC bit of the subsystem clock select register(CKSEL) and stop the oscillating the low-speed on-chip oscillator. In this application note, for WUTMMCK0 bit of the subsystem clock supply mode control register(OSMC) is 1, does not stop the low-speed on-chip oscillator.

```
<table>
<thead>
<tr>
<th>CKSEL</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>SELLOSC</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
```

Note: Changing the value of the MCM0 bit is prohibited while the CPU/peripheral hardware clock is operating with the subsystem clock.

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.10 Changing from high-speed system clock to high-speed on-chip oscillator clock

When changing the CPU clock from the high-speed system clock to the high-speed on-chip oscillator clock, start the oscillation using the clock operation status control register (CSC), then wait for the oscillation to stabilize using the timer function or another function. After the oscillation stabilization time has elapsed, set the high-speed on-chip oscillator clock to $f_{CLK}$ using the system clock control register (CKC). Confirm that the status of the main system clock status has switched to the main on-chip oscillator clock, and then stop the X1 oscillator.

① Clear (0) the HIOSTOP bit of the CSC register, and then start oscillating the high-speed on-chip oscillator.

```
<table>
<thead>
<tr>
<th></th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSC</td>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
<td>HIOSTOP</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>0</td>
</tr>
</tbody>
</table>
```

② Use a software wait to wait for the oscillation of the high-speed on-chip oscillator to stabilize. Count the wait time (oscillation stabilization time: 65µs) using the timer function or another function.

③ Clear (0) the MCM0 bit of the CKC register to specify the main on-chip oscillator clock as the main system clock.

```
<table>
<thead>
<tr>
<th></th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CKC</td>
<td>CLS</td>
<td>CSS</td>
<td>MCS</td>
<td>MCM0</td>
<td>0</td>
<td>0</td>
<td>MCS1</td>
<td>MCM1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
```

④ Confirm that the MCS bit of the CKC register has changed to 0, set (1) the MSTOP bit and stop the oscillating the X1 oscillator.

```
<table>
<thead>
<tr>
<th></th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSC</td>
<td>MSTOP</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
<td>HIOSTOP</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>0</td>
</tr>
</tbody>
</table>
```

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.11 Changing from high-speed system clock to middle-speed on-chip oscillator clock

When changing the CPU clock from the high-speed system clock to the middle-speed on-chip oscillator clock, start
the oscillation using the clock operation status control register (CSC), then wait for the oscillation to stabilize using the
timer function or another function. After the oscillation stabilization time has elapsed, set the middle-speed on-chip
oscillator clock to $f_{CLK}$ using the system clock control register (CKC). Confirm that the status of the main system clock
status has switched to the main on-chip oscillator clock, and then stop the X1 oscillator.

① Set (1) the MIOEN bit of the CSC register, and then start oscillating the middle-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>MSTOP</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>MIOEN</th>
<th>HIOSTOP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

② Use a software wait to wait for the oscillation of the middle-speed on-chip oscillator to stabilize. Count the wait
time (oscillation stabilization time: 4µs) using the timer function or another function.

③ Clear(0) the MCM0 bit of the CKC register to specify the main on-chip oscillator clock as the main system
clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>CLS</th>
<th>CSS</th>
<th>MCS</th>
<th>MCM0</th>
<th>0</th>
<th>0</th>
<th>MCS1</th>
<th>MCM1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

④ Confirm that the MCS bit of the CKC register has changed to 0, set (1) the MSTOP bit and stop the oscillating
the X1 oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>MSTOP</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>MIOEN</th>
<th>HIOSTOP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td>x</td>
</tr>
</tbody>
</table>

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
1.1.12 Changing from high-speed system clock to low-speed on-chip oscillator clock

When changing the CPU clock from the high-speed system clock to the low-speed on-chip oscillator clock, start the oscillation using the subsystem clock select register (CKSEL), then wait for the oscillation to stabilize using the timer function or another function. After the oscillation stabilization time has elapsed, set the low-speed on-chip oscillator clock to f_Clk using the system clock control register (CKC). Confirm that the status of the CPU/peripheral hardware clock status has switched to the subsystem clock, and then stop the X1 oscillator.

① Set (1) the SELLOSC bit of the CKSEL register, and then start oscillating the low-speed on-chip oscillator.

<table>
<thead>
<tr>
<th>CKSEL</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

② Use a software wait to wait for the oscillation of the low-speed on-chip oscillator to stabilize. Count the wait time (oscillation stabilization time: 210µs) using the timer function or another function. In this application note, it is always to operate the low-speed on-chip oscillator. For this reason, it does not perform oscillation stabilization wait of the low-speed on-chip oscillator.

③ Set (1) the CSS bit of the CKC register to specify the subsystem clock as the CPU/peripheral hardware clock.

<table>
<thead>
<tr>
<th>CKC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

④ Confirm that the CLS bit of the CKC register has changed to 1, set (1) the MSTOP bit and stop the oscillating the X1 oscillator.

<table>
<thead>
<tr>
<th>CSC</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MIOEN</td>
<td>HIOSTOP</td>
</tr>
</tbody>
</table>

Register setting values:
- x: unused bit; blank space; unchanged bit; -: reserved bits or unassigned bit
2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

### Table 2.1  Operation Confirmation Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU used</td>
<td>RL78/G11 (R5F1056A)</td>
</tr>
<tr>
<td>Operating frequencies</td>
<td>- High-speed on-chip oscillator clock: 24MHz</td>
</tr>
<tr>
<td></td>
<td>- Middle-speed on-chip oscillator clock: 4MHz</td>
</tr>
<tr>
<td></td>
<td>- Low-speed on-chip oscillator clock: 15kHz</td>
</tr>
<tr>
<td></td>
<td>- High-speed system clock: 20MHz</td>
</tr>
<tr>
<td></td>
<td>- CPU/peripheral hardware clock: 24MHz/20MHz/4MHz/15kHz&lt;sup&gt;Note&lt;/sup&gt;</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>3.0V (operating range 2.9V to 5.5V)</td>
</tr>
<tr>
<td></td>
<td>LVD operations ($V_{LVD}$): reset mode 2.81V (2.76V to 2.87V)</td>
</tr>
<tr>
<td>Integrated development</td>
<td>IAR Embedded Workbench V2.21.5</td>
</tr>
<tr>
<td>environment</td>
<td></td>
</tr>
<tr>
<td>C compiler</td>
<td>IAR C/C++ Compiler V2.21.1&lt;sup&gt;1.18333&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

Note: CPU/peripheral hardware clock settings are changed in the application.

3. Related Application Notes

Application notes related to this document are shown below. Please refer to these as needed.

RL78/I1D Operation State Switching IAR (R01AN3597E) Application Note
4. Hardware Explanation

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used in this application note.

![Figure 4.1 Hardware Configuration](image)

Note: 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

2. If a pin name starts with EVSS, connect the pin to VSS, if it starts with EVDD, connect it to VDD.

3. Make VDD higher than the RESET release voltage (VLVD) set in LVD.

4.2 Used Pin List

Table 4.1 provides List of Pins and Functions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Input/Output</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P137/INTP0</td>
<td>Input</td>
<td>Switch (SW1) input port</td>
</tr>
<tr>
<td>P20/AIN0</td>
<td>Input</td>
<td>A/D converter analog input port</td>
</tr>
<tr>
<td>P00</td>
<td>Output</td>
<td>LED (LED1) control port</td>
</tr>
<tr>
<td>P01</td>
<td>Output</td>
<td>LED (LED2) control port</td>
</tr>
<tr>
<td>P54</td>
<td>Output</td>
<td>LED (LED3) control port</td>
</tr>
<tr>
<td>P55</td>
<td>Output</td>
<td>LED (LED4) control port</td>
</tr>
<tr>
<td>P56</td>
<td>Output</td>
<td>LED (LED5) control port</td>
</tr>
</tbody>
</table>
5. Software Explanation

5.1 Operation Outline

This application enables the user to change the CPU clock and the operation mode using switch input. The CPU clock and the operating mode is changed in the order of 1 to 31 of Figure 1.1 operation mode status transition diagram.

(1) Input/output port initialization

- P00-P01 and P54-P56 pins: set as output ports (use to control LEDs)
- P137/INTP0 pin: set as input port (use for switch input)
- P20/ANI0 pin: set as analog input port (use as A/D conversion analog input channel)

(2) Clock generator initialization

<Setting conditions>

- Set the flash operation mode to HS (high-speed main) mode using user option byte (000C2H/010C2H).)
- High-speed on-chip oscillator clock frequency: set to 24 MHz
- Set the operation mode of the high-speed system clock pin to X1 oscillation, and connect a crystal resonator to the X1/P121 and X2/EXCLK/P122 pins.
- Select the main system clock (fMAIN) as the CPU/peripheral hardware clock (fCLK).

(3) Interrupt processing initialization

- Set the INTP0 pin valid edge to falling edge and enable switch input.
- Use the 12-bit interval timer to confirm switch input. The voltage level of the pin is checked approximately every 5 ms. If the voltage level matches twice consecutively, the switch input is recognized as valid (prevents chattering).
The CPU clock and operation mode change as follows each time the falling edge of a signal (switch) input to the P137/INTP0 pin is detected. The following is the CPU clock and operation mode after the switch is pressed.

Table 5.1  LED status (after the switch is pressed) (1/2)

<table>
<thead>
<tr>
<th>CPU clock</th>
<th>Operation mode</th>
<th>LED1</th>
<th>LED2</th>
<th>LED3</th>
<th>LED4</th>
<th>LED5</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) High-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(2) High-speed system clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(3) High-speed system clock</td>
<td>HALT mode</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(4) High-speed system clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(5) High-speed system clock</td>
<td>STOP mode</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(6) High-speed system clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(7) High-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(8) High-speed on-chip oscillator clock</td>
<td>HALT mode</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(9) High-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(10) High-speed on-chip oscillator clock</td>
<td>STOP mode</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(11) High-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(12) High-speed on-chip oscillator clock</td>
<td>SNOOZE mode</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(13) High-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(14) Middle-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>(15) High-speed system clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(16) Low-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>(17) High-speed system clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(18) Middle-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>CPU clock</td>
<td>Operation mode</td>
<td>LED1</td>
<td>LED2</td>
<td>LED3</td>
<td>LED4</td>
</tr>
<tr>
<td>---</td>
<td>-----------------------------------</td>
<td>---------------------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>(19)</td>
<td>Middle-speed on-chip oscillator clock</td>
<td>HALT mode</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(20)</td>
<td>Middle-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(21)</td>
<td>Middle-speed on-chip oscillator clock</td>
<td>STOP mode</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(22)</td>
<td>Middle-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(23)</td>
<td>Middle-speed on-chip oscillator clock</td>
<td>SNOOZE mode</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(24)</td>
<td>Middle-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(25)</td>
<td>Low-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(26)</td>
<td>Middle-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(27)</td>
<td>High-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>(28)</td>
<td>Low-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(29)</td>
<td>Low-speed on-chip oscillator clock</td>
<td>HALT mode</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(30)</td>
<td>Low-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>(31)</td>
<td>High-speed on-chip oscillator clock</td>
<td>Normal operation mode</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

After the CPU clock and operation mode have been changed according to steps 1 to 31 above, the falling edge of a signal (switch) input to the P137/INTP0 pin is detected, all LEDs are turned OFF, and the CPU goes to HALT mode (only RESET input in standby recovery).

In addition, if the CPU clock can’t be status transition to a certain period of time such as by oscillation failure of the crystal oscillator is all LEDs are turned OFF and end the status transition in error processing.

Note: Refer to the RL78/G11 User’s Manual for usage notes concerning this device.
5.2 Option Byte Settings
Table 5.1 lists the option byte settings.

<table>
<thead>
<tr>
<th>Address</th>
<th>Setting Value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>000C0H/010C0H</td>
<td>01101110B</td>
<td>Watchdog timer operation is stopped (count is stopped after reset)</td>
</tr>
<tr>
<td>000C1H/010C1H</td>
<td>01111111B</td>
<td>LVD operation ((V_{LVD})): reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V</td>
</tr>
<tr>
<td>000C2H/010C2H</td>
<td>11100000B</td>
<td>HS mode, HOCO: 24 MHz</td>
</tr>
<tr>
<td>000C3H/010C3H</td>
<td>10000100B</td>
<td>On-chip debugging enabled</td>
</tr>
</tbody>
</table>

5.3 Variables
Table 5.2 lists the global variables.

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-bit</td>
<td>g_int_cnt</td>
<td>Number of interval signal detection interrupts for 12-bit interval timer</td>
<td>R_MAIN_BtoD, R_MAIN_DtoB, R_MAIN_BtoC, R_MAIN_CtoD, R_MAIN_DtoE, R_MAIN_EtoD, R_MAIN_DtoC, R_MAIN_CtoE, R_MAIN_EtoC, R_MAIN_CtoB, R_MAIN_BtoE, R_MAIN_EtoB, r_it_interrupt</td>
</tr>
<tr>
<td>8-bit</td>
<td>g_int_flg</td>
<td>Confirm the external interrupt generation detection flag</td>
<td>R_MAIN_NOP_Loop, r_intc0_interrupt</td>
</tr>
</tbody>
</table>
### 5.4 Functions (subroutines)

Table 5.3 lists the functions (subroutines).

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
<th>Number of operating mode status transition diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_MAIN_AtoB</td>
<td>Status transition processing from (A) to (B)</td>
<td>(1)</td>
</tr>
<tr>
<td>R_MAIN_BtoD</td>
<td>Status transition processing from (B) to (D)</td>
<td>(2)</td>
</tr>
<tr>
<td>R_MAIN_DtoL</td>
<td>Status transition processing from (D) to (L)</td>
<td>(3)</td>
</tr>
<tr>
<td>R_MAIN_LtoD</td>
<td>Status transition processing from (L) to (D)</td>
<td>(4)</td>
</tr>
<tr>
<td>R_MAIN_DtoM</td>
<td>Status transition processing from (D) to (M)</td>
<td>(5)</td>
</tr>
<tr>
<td>R_MAIN_MtoC</td>
<td>Status transition processing from (M) to (D)</td>
<td>(6)</td>
</tr>
<tr>
<td>R_MAIN_DtoB</td>
<td>Status transition processing from (D) to (B)</td>
<td>(7)</td>
</tr>
<tr>
<td>R_MAIN_BtoF</td>
<td>Status transition processing from (B) to (F)</td>
<td>(8)</td>
</tr>
<tr>
<td>R_MAIN_FtoB</td>
<td>Status transition processing from (F) to (B)</td>
<td>(9)</td>
</tr>
<tr>
<td>R_MAIN_BtoG</td>
<td>Status transition processing from (B) to (G)</td>
<td>(10)</td>
</tr>
<tr>
<td>R_MAIN_GtoB</td>
<td>Status transition processing from (G) to (B)</td>
<td>(11)</td>
</tr>
<tr>
<td>R_MAIN_BtoH</td>
<td>Status transition processing from (B) to (H)</td>
<td>(12)</td>
</tr>
<tr>
<td>R_MAIN_HtoB</td>
<td>Status transition processing from (H) to (B)</td>
<td>(13)</td>
</tr>
<tr>
<td>R_MAIN_BtoC</td>
<td>Status transition processing from (B) to (C)</td>
<td>(14)</td>
</tr>
<tr>
<td>R_MAIN_CtoD</td>
<td>Status transition processing from (C) to (D)</td>
<td>(15)</td>
</tr>
<tr>
<td>R_MAIN_DtoE</td>
<td>Status transition processing from (D) to (E)</td>
<td>(16)</td>
</tr>
<tr>
<td>R_MAIN_EtoD</td>
<td>Status transition processing from (E) to (D)</td>
<td>(17)</td>
</tr>
<tr>
<td>R_MAIN_DtoC</td>
<td>Status transition processing from (D) to (C)</td>
<td>(18)</td>
</tr>
<tr>
<td>R_MAIN_CtoI</td>
<td>Status transition processing from (C) to (I)</td>
<td>(19)</td>
</tr>
<tr>
<td>R_MAIN_ItoC</td>
<td>Status transition processing from (I) to (C)</td>
<td>(20)</td>
</tr>
<tr>
<td>R_MAIN_CtoJ</td>
<td>Status transition processing from (C) to (J)</td>
<td>(21)</td>
</tr>
<tr>
<td>R_MAIN_JtoC</td>
<td>Status transition processing from (J) to (C)</td>
<td>(22)</td>
</tr>
<tr>
<td>R_MAIN_CtoK</td>
<td>Status transition processing from (C) to (K)</td>
<td>(23)</td>
</tr>
<tr>
<td>R_MAIN_KtoC</td>
<td>Status transition processing from (K) to (C)</td>
<td>(24)</td>
</tr>
<tr>
<td>R_MAIN_CtoE</td>
<td>Status transition processing from (C) to (E)</td>
<td>(25)</td>
</tr>
<tr>
<td>R_MAIN_EtoC</td>
<td>Status transition processing from (E) to (C)</td>
<td>(26)</td>
</tr>
<tr>
<td>R_MAIN_CtoB</td>
<td>Status transition processing from (C) to (B)</td>
<td>(27)</td>
</tr>
<tr>
<td>R_MAIN_BtoE</td>
<td>Status transition processing from (B) to (E)</td>
<td>(28)</td>
</tr>
<tr>
<td>R_MAIN_EtoN</td>
<td>Status transition processing from (E) to (N)</td>
<td>(29)</td>
</tr>
<tr>
<td>R_MAIN_NtoE</td>
<td>Status transition processing from (N) to (E)</td>
<td>(30)</td>
</tr>
<tr>
<td>R_MAIN_EtoB</td>
<td>Status transition processing from (E) to (B)</td>
<td>(31)</td>
</tr>
<tr>
<td>R_MAIN_NOP_Loop</td>
<td>Continuous NOP instruction execution processing</td>
<td>−</td>
</tr>
<tr>
<td>R_MAIN_END</td>
<td>A/D converter setting</td>
<td>−</td>
</tr>
<tr>
<td>R_MAIN_ERROR</td>
<td>End processing of status transition</td>
<td>−</td>
</tr>
<tr>
<td>R_MAIN_Set_SnoozeOn</td>
<td>Error processing of status transition</td>
<td>−</td>
</tr>
<tr>
<td>r_intc0_interrupt</td>
<td>Confirm the external interrupt generation</td>
<td>−</td>
</tr>
<tr>
<td>r_it_interrupt</td>
<td>12-bit interval timer interval signal detection</td>
<td>−</td>
</tr>
<tr>
<td>r_adc_interrupt</td>
<td>SNOOZE mode release processing</td>
<td>−</td>
</tr>
</tbody>
</table>
5.5 Function (subroutine) Specifications

The following are the sample code functions (subroutines) used in this application note.

[Function Name] R_MAIN_AtoB

Outline Status transition processing from (A) to (B)
Declaration void R_MAIN_AtoB(void)
Description Control LED lighting.
   (CPU clock: high-speed on-chip oscillator clock)
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_BtoD

Outline Status transition processing from (B) to (D)
Declaration void R_MAIN_BtoD(void)
Description Change the CPU clock from high-speed on-chip oscillator clock to high-speed
   system clock. After the clock is switched, control LED lighting.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_DtoL

Outline Status transition processing from (D) to (L)
Declaration void R_MAIN_DtoL(void)
Description Control LED lighting, then transition to HALT mode.
   (CPU clock stopped (when using high-speed system clock))
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_LtoD

Outline Status transition processing from (L) to (D)
Declaration void R_MAIN_LtoD(void)
Description Control LED lighting.
   (CPU clock: high-speed system clock)
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_DtoM

Outline Status transition processing from (D) to (M)
Declaration void R_MAIN_DtoM(void)
Description Control LED lighting, then transition to STOP mode.
   (Stop CPU clock (when using high-speed system clock))
Argument None
Return Value None
Notes None
<table>
<thead>
<tr>
<th>Function Name</th>
<th>R_MAIN_MtoD</th>
<th>R_MAIN_DtoB</th>
<th>R_MAIN_BtoF</th>
<th>R_MAIN_FtoB</th>
<th>R_MAIN_BtoG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>Status transition processing from (M) to (D)</td>
<td>Status transition processing from (D) to (B)</td>
<td>Status transition processing from (B) to (F)</td>
<td>Status transition processing from (F) to (B)</td>
<td>Status transition processing from (B) to (G)</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_MAIN_MtoD(void)</td>
<td>void R_MAIN_DtoB(void)</td>
<td>void R_MAIN_BtoF(void)</td>
<td>void R_MAIN_FtoB(void)</td>
<td>void R_MAIN_BtoG(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Control LED lighting. (CPU clock: high-speed system clock)</td>
<td>Change the CPU clock from high-speed system clock to high-speed on-chip oscillator clock. After the clock is switched, control LED lighting.</td>
<td>Control LED lighting, then transition to HALT mode. (CPU clock stopped when using high-speed on-chip oscillator clock)</td>
<td>Control LED lighting. (CPU clock: high-speed on-chip oscillator clock)</td>
<td>Control LED lighting, then transition to STOP mode. (CPU clock stopped when using high-speed on-chip oscillator clock)</td>
</tr>
<tr>
<td>Argument</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Notes</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>
[Function Name] R_MAIN_GtoB
Outline Status transition processing from (G) to (B)
Declaration void R_MAIN_GtoB(void)
Description Control LED lighting.
    (CPU clock: high-speed on-chip oscillator clock)
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_BtoH
Outline Status transition processing from (B) to (H)
Declaration void R_MAIN_BtoH(void)
Description Set A/D converter and control LED lighting.
    Then, transition to SNOOZE mode.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_HtoB
Outline Status transition processing from (H) to (B)
Declaration void R_MAIN_HtoB(void)
Description Set SNOOZE release and stop A/D converter.
    Then control LED lighting.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_BtoC
Outline Status transition processing from (B) to (C)
Declaration void R_MAIN_BtoC(void)
Description Change the CPU clock from high-speed on-chip oscillator clock to middle-speed
    on-chip oscillator clock. After the clock is switched, control LED lighting.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_CtoD
Outline Status transition processing from (C) to (D)
Declaration void R_MAIN_CtoD(void)
Description Change the CPU clock from middle-speed on-chip oscillator clock to high-speed
    system clock. After the clock is switched, control LED lighting.
Argument None
Return Value None
Notes None
### [Function Name] R_MAIN_DtoE

<table>
<thead>
<tr>
<th>Outline</th>
<th>Status transition processing from (D) to (E)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Declaration</td>
<td>void R_MAIN_DtoE(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Change the CPU clock from high-speed system clock to low-speed on-chip oscillator clock. After the clock is switched, control LED lighting.</td>
</tr>
<tr>
<td>Argument</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
<tr>
<td>Notes</td>
<td>None</td>
</tr>
</tbody>
</table>

### [Function Name] R_MAIN_EtoD

<table>
<thead>
<tr>
<th>Outline</th>
<th>Status transition processing from (E) to (D)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Declaration</td>
<td>void R_MAIN_EtoD(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Change the CPU clock from low-speed on-chip oscillator clock to high-speed system clock. After the clock is switched, control LED lighting.</td>
</tr>
<tr>
<td>Argument</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
<tr>
<td>Notes</td>
<td>None</td>
</tr>
</tbody>
</table>

### [Function Name] R_MAIN_DtoC

<table>
<thead>
<tr>
<th>Outline</th>
<th>Status transition processing from (D) to (C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Declaration</td>
<td>void R_MAIN_DtoC(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Change the CPU clock from high-speed system clock to middle-speed on-chip oscillator clock. After the clock is switched, control LED lighting.</td>
</tr>
<tr>
<td>Argument</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
<tr>
<td>Notes</td>
<td>None</td>
</tr>
</tbody>
</table>

### [Function Name] R_MAIN_CtoI

<table>
<thead>
<tr>
<th>Outline</th>
<th>Status transition processing from (C) to (I)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Declaration</td>
<td>void R_MAIN_CtoI(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Control LED lighting, then transition to HALT mode. (CPU clock stopped (when using middle-speed on-chip oscillator clock))</td>
</tr>
<tr>
<td>Argument</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
<tr>
<td>Notes</td>
<td>None</td>
</tr>
</tbody>
</table>

### [Function Name] R_MAIN_ItoC

<table>
<thead>
<tr>
<th>Outline</th>
<th>Status transition processing from (I) to (C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Declaration</td>
<td>void R_MAIN_ItoC(void)</td>
</tr>
<tr>
<td>Description</td>
<td>Control LED lighting. (CPU clock: middle-speed on-chip oscillator clock)</td>
</tr>
<tr>
<td>Argument</td>
<td>None</td>
</tr>
<tr>
<td>Return Value</td>
<td>None</td>
</tr>
<tr>
<td>Notes</td>
<td>None</td>
</tr>
</tbody>
</table>
[Function Name] R_MAIN_CtoJ

Outline  Status transition processing from (C) to (J)
Declaration void R_MAIN_CtoJ(void)
Description Control LED lighting, then transition to STOP mode.
(CPU clock stopped (when using middle-speed on-chip oscillator clock))
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_JtoC

Outline  Status transition processing from (J) to (C)
Declaration void R_MAIN_JtoC(void)
Description Control LED lighting.
(CPU clock: middle-speed on-chip oscillator clock)
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_CtoK

Outline  Status transition processing from (C) to (K)
Declaration void R_MAIN_CtoK(void)
Description Set A/D converter and control LED lighting.
Then, transition to SNOOZE mode.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_KtoC

Outline  Status transition processing from (K) to (C)
Declaration void R_MAIN_KtoC(void)
Description Set SNOOZE release and stop A/D converter.
Then control LED lighting.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_CtoE

Outline  Status transition processing from (C) to (E)
Declaration void R_MAIN_CtoE(void)
Description Change the CPU clock from middle-speed on-chip oscillator clock to low-speed on-chip oscillator clock. After the clock is switched, control LED lighting.
Argument None
Return Value None
Notes None
[Function Name] R_MAIN_EtoC

Outline  Status transition processing from (E) to (C)
Declaration void R_MAIN_EtoC(void)
Description Change the CPU clock from low-speed on-chip oscillator clock to middle-speed on-chip oscillator clock. After the clock is switched, control LED lighting.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_CtoB

Outline  Status transition processing from (C) to (B)
Declaration void R_MAIN_CtoB(void)
Description Change the CPU clock from middle-speed on-chip oscillator clock to high-speed on-chip oscillator clock. After the clock is switched, control LED lighting.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_BtoE

Outline  Status transition processing from (B) to (E)
Declaration void R_MAIN_BtoE(void)
Description Change the CPU clock from high-speed on-chip oscillator clock to low-speed on-chip oscillator clock. After the clock is switched, control LED lighting.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_EtoN

Outline  Status transition processing from (E) to (N)
Declaration void R_MAIN_EtoN(void)
Description Control LED lighting, then transition to HALT mode.  
(CPU clock stopped (when using low-speed on-chip oscillator clock))
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_NtoE

Outline  Status transition processing from (N) to (E)
Declaration void R_MAIN_NtoE(void)
Description Control LED lighting.  
(CPU clock: low-speed on-chip oscillator clock)
Argument None
Return Value None
Notes None
[Function Name] R_MAIN_EtoB

Outline Status transition processing from (E) to (B)
Declaration void R_MAIN_EtoB(void)
Description Change the CPU clock from low-speed on-chip oscillator clock to high-speed on-chip oscillator clock. After the clock is switched, control LED lighting.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_NOP_Loop

Outline Continuous NOP instruction execution processing
Declaration void R_MAIN_NOP_Loop(void)
Description Execute NOP instruction continuously. End processing when external interrupt generation detection flag is confirmed.
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_END

Outline End processing of status transition
Declaration void R_MAIN_END(void)
Description Disable interrupts. Control LED lighting (all off).
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_ERROR

Outline Error processing of status transition
Declaration void R_MAIN_ERROR(void)
Description Disable interrupts. Control LED lighting (all off). Loop processing within the function (Return is only reset input).
Argument None
Return Value None
Notes None

[Function Name] R_MAIN_AD_SnoozeOn

Outline A/D converter setting
Declaration void R_MAIN_AD_SnoozeOn(void)
Description Set A/D converter to hardware trigger wait mode with 12-bit interval timer interrupt signal. Enable SNOOZE mode and transition to A/D conversion wait status.
Argument None
Return Value None
Notes None
[Function Name] r_intc0_interrupt

Outline External interrupt generation detection flag confirmation processing
Declaration __interrupt void r_intc0_interrupt(void)
Description Confirm external interrupt generation detection flag with generation of external interrupt.
End processing when switch input level changes to high.
Argument None
Return Value None
Notes None

[Function Name] r_it_interrupt

Outline 12-bit interval timer interval signal detection interrupt count processing
Declaration __interrupt void r_it_interrupt(void)
Description Increment the RITCOUNT each time the 12-bit interval timer interrupt signal detection interrupt is generated.
Argument None
Return Value None
Notes None

[Function Name] r_adc_interrupt

Outline SNOOZE mode release processing
Declaration __interrupt void r_adc_interrupt(void)
Description Clear the AWC bit of the ADM2 register and release the SNOOZE mode.
Argument None
Return Value None
Notes None
5.6 Flowcharts

Figure 5.1 shows the entire flow for this application note.

![Overall Flowchart](image-url)
5.6.1 Main Processing

Figure 5.2, Figure 5.3, Figure 5.4, Figure 5.5 shows the flowchart for the main processing.

Figure 5.2 Main Processing (1/4)
Status transition (F)→(B)  
R_MAIN_FtoB()

- Release HALT mode (F), then transition to high-speed on-chip oscillator clock operation (B)

Status transition (B)→(G)  
R_MAIN_BtoG()

- Transition to STOP mod (G) while CPU is operating with high-speed on-chip oscillator clock (B)

Status transition (G)→(B)  
R_MAIN_GtoB()

- Release STOP mode (G), then transition to high-speed system clock operation (B)

Status transition (B)→(H)  
R_MAIN_BtoH()

- Transition to SNOOZE mode (H) while CPU is operating with high-speed on-chip oscillator clock (B)

Status transition (H)→(B)  
R_MAIN_HtoB()

- Release SNOOZE mode (H), then transition to high-speed on-chip oscillator operation (B)

Status transition (B)→(C)  
R_MAIN_BtoC()

- Transition CPU from high-speed on-chip oscillator clock operation (B) to middle-speed on-chip oscillator clock operation (C)

Status transition (C)→(D)  
R_MAIN_CtoD()

- Transition CPU from middle-speed on-chip oscillator clock operation (C) to high-speed system clock operation (D)

Status transition (D)→(E)  
R_MAIN_DtoE()

- Transition CPU from high-speed system clock operation (D) to low-speed on-chip oscillator clock operation (E)

Status transition (E)→(D)  
R_MAIN_EtoD()

- Transition CPU from low-speed on-chip oscillator clock operation (E) to high-speed system clock operation (D)

Status transition (D)→(C)  
R_MAIN_DtoC()

- Transition CPU from high-speed system clock operation (D) to middle-speed on-chip oscillator clock operation (C)

Status transition (C)→(I)  
R_MAIN_CtoI()

- Transition to HALT mode (I) while CPU is operating with middle-speed on-chip oscillator clock (C)

**Figure 5.3  Main Processing (2/4)**
Figure 5.4  Main Processing (3/4)
Set LED to OFF

End processing of status transition
R_MAIN_END()

return

Status transition (N)→(E)
R_MAIN_NtoE()

Release HALT mode (N), then transition to middle-speed on-chip oscillator clock operation (E)

Status transition (E)→(B)
R_MAIN_EtoB()

Transition CPU from low-speed on-chip oscillator clock operation (E) to high-speed on-chip oscillator clock operation (B)

Set LED to OFF

Figure 5.5  Main Processing (4/4)
5.6.2 Initialization Function

Figure 5.6 shows the flowchart for the initialization function.

![Flowchart for Initialization Function](attachment:image.png)

**Figure 5.6 Initialization Function**
5.6.3 System Function

Figure 5.7 shows the flowchart for system function.

![System Function Flowchart]

- R_Systeminit()
- Disuse peripheral I/O
  - Redirection function
- Set up I/O ports
  - R_PORT_Create()
- Set up CPU clock
  - R_CGC_Create()
- Set interrupt
  - R_IT_Create()
- Set interrupt
  - R_INTC_Create()
- Disabled the invalid memory access detection
  - IAWCTL register ← 00H
- return

**Figure 5.7 System Function**
5.6.4  Input/Output Port Settings

Figure 5.8 shows the flowchart for the input/output port settings.

```
R_PORT_Create()

Set analog input
Alternate-function pins

PMCO register ← 11111100B: Set P0.1 to P0.0 to digital input/output
PMC2 register ← 11110001B: Set P2.0 to analog input
PMC5 register ← 10111111B: Set P5.6 to digital input/output

P0 ← 00000011B: Set P0.1 to P0.0 to high-level output
P5 ← 01110000B: Set P5.6 to P5.4 to high-level output

PM0 ← 11111100B: Set P0.1 to p0.0 to input ports
PM2 ← 01110001B: Set P2.0 to input ports
PM4 ← 11111111B: Set P4.0 to input ports
PM5 ← 10001111B: Set P5.6 to P5.4 to out ports

return
```

**Figure 5.8 Input/Output Port Settings**

**Note:** Refer to the initialization flowchart in the RL78/G13 Initialization (R01AN2575E) Application Note for details on how to set unused ports.

**Caution:** When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met. Also make sure each unused input-only port is connected to V_DD or V_SS through a resistor.
### 5.6.5 Clock Generator Setting

Figure 5.9 shows the flowchart for setting the clock generator.

![Flowchart for setting the clock generator](image)

- **R_CGC_Create()**
- **Set Middle-speed on-chip oscillator clock**
  - MIOEN bit ← 0: Middle-speed on-chip oscillator stopped
- **Set high-speed system clock/subsystem clock**
  - CMC register ← 01010101B: X1 oscillation mode
  - OSTC register ← 00000111B
  - X1 clock: 10 MHz ≤ fX ≤ 20 MHz
- **Set clock operation controls**
  - MSTOP bit ← 1: X1 oscillator stopped
- **Set low-speed on-chip oscillator clock**
  - SELLOSC bit ← 1: Select low-speed on-chip oscillator clock as Subsystem clock
- **Oscillation stabilization wait time**
- **Select CPU/peripheral hardware clock (fCLK)**
  - OSMC register ← 10H: Provide 1 to 12-bit interval timer
  - CSS bit ← 0: Set main system clock (fMAIN) to CPU/peripheral hardware clock (fCLK)
  - MCM0 bit ← 0: Select main on-chip oscillator clock (fOCO) as main system clock (fMAIN)
  - MCM1 bit ← 0: Select high-speed on-chip clock as main on-chip oscillator clock (fOCO)

**Figure 5.9 Clock Generator Setting**
Clock operation mode setting

- Clock operation mode control register (CMC)
  - High-speed system clock pin operation mode: X1 oscillation mode
  - X1 clock oscillation frequency control: 10MHz ≤ fMX ≤ 20MHz

Symbol: CMC

<table>
<thead>
<tr>
<th>Bits 7-6</th>
<th>EXCLK</th>
<th>OSCSEL</th>
<th>High-seed oscillation clock pin operation mode</th>
<th>X1/P121 Port</th>
<th>X2/EXCLK/P122 Port</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1</td>
<td>0 0</td>
<td>0</td>
<td>input port mode</td>
<td>input port</td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>0 1</td>
<td>X1 oscillation mode</td>
<td>Crystal/ceramic resonator connection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>0 1</td>
<td>input port mode</td>
<td>input port</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>1 1</td>
<td>External clock input mode</td>
<td>input port</td>
<td>External clock input</td>
<td></td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>AMPH</th>
<th>Control of X1 clock oscillation frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1MHz ≤ fX ≤ 10MHz</td>
</tr>
<tr>
<td>1</td>
<td>10MHz &lt; fX ≤ 20MHz</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (Hardware) for details on how to set registers.
Operation control of clocks

- Clock operation status control register (CSC)
  - High-speed system clock operation control: X1 oscillator stopped
  - Middle-speed on-chip oscillator clock operation control: Middle-speed on-chip oscillator stopped
  - High-speed on-chip oscillator clock operation control: High-speed on-chip oscillator operating

Symbol: CSC

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>High-speed system clock operation control</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSTOP</td>
<td>X1 oscillation mode</td>
</tr>
<tr>
<td>0</td>
<td>X1 oscillator operating</td>
</tr>
<tr>
<td>1</td>
<td>X1 oscillator stopped</td>
</tr>
</tbody>
</table>

- Bit 7

<table>
<thead>
<tr>
<th>Bit 1</th>
<th>Middle-speed on-chip oscillator clock operation control</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIOEN</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

- Bit 0

<table>
<thead>
<tr>
<th>Bit 0</th>
<th>High-speed on-chip oscillator clock operation control</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIOSTOP</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (Hardware) for details on how to set registers.
CPU/peripheral hardware clock (fCLK) setting

- System clock control register (CKC)
  - Status of fCLK: main system clock
  - Selection of fCLK: high-speed on-chip oscillator clock (fIH)

Symbol: CKC

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLS</td>
<td>CSS</td>
<td>MCS</td>
<td>MCM0</td>
<td>0</td>
<td>0</td>
<td>MCS1</td>
<td>MCM1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bit 7

<table>
<thead>
<tr>
<th>CLS</th>
<th>Status of CPU/peripheral hardware clock (fCLK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Main system clock (fMAIN)</td>
</tr>
<tr>
<td>1</td>
<td>Subsystem clock (fSUB)</td>
</tr>
</tbody>
</table>

Bit 6

<table>
<thead>
<tr>
<th>CSS</th>
<th>Selection of CPU/peripheral hardware clock (fCLK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Main system clock (fMAIN)</td>
</tr>
<tr>
<td>1</td>
<td>Subsystem clock (fSUB)</td>
</tr>
</tbody>
</table>

Bit 5

<table>
<thead>
<tr>
<th>MCS</th>
<th>Status of main system clock (fMAIN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>High-speed on-chip oscillator clock (fIH)</td>
</tr>
<tr>
<td>1</td>
<td>High-speed system clock (fMX)</td>
</tr>
</tbody>
</table>

Bit 4

<table>
<thead>
<tr>
<th>MCM0</th>
<th>Main system clock (fMAIN) operation control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Selects high-speed on-chip oscillator clock (fIH) as main system clock (fMAIN)</td>
</tr>
<tr>
<td>1</td>
<td>Selects high-speed system clock (fMX) as main system clock (fMAIN).</td>
</tr>
</tbody>
</table>

Bit 1

<table>
<thead>
<tr>
<th>MCS1</th>
<th>Status of main on-chip oscillator clock (foco)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>High-speed on-chip oscillator clock (fIH)</td>
</tr>
<tr>
<td>1</td>
<td>Middle-speed on-chip oscillator clock (fIM)</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>MCS1</th>
<th>Main on-chip oscillator clock (foco) operation control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>High-speed on-chip oscillator clock (fIH)</td>
</tr>
<tr>
<td>1</td>
<td>Middle-speed on-chip oscillator clock (fIM)</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (Hardware) for details on how to set registers.
Operation speed mode control
  - Operation speed mode control register (OSMC)
    Selection of operation clock for 12-bit interval timer: low-speed on-chip oscillator clock

Symbol: OSMC

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>WUTMMCK0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bit 4

<table>
<thead>
<tr>
<th>WUTMMCK0</th>
<th>Selection of operation clock for 12-bit interval timer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Do not select low-speed on-chip oscillator clock</td>
</tr>
<tr>
<td>1</td>
<td>Select low-speed on-chip oscillator clock</td>
</tr>
</tbody>
</table>

Subsystem clock select
  - Subsystem clock select register (CKSEL)
    Subsystem clock select: Select low-speed on-chip oscillator clock

Symbol: CKSEL

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>SELLOSC</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>SELLOSC</th>
<th>Selection of low-speed on-chip oscillator clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Do not select low-speed on-chip oscillator clock</td>
</tr>
<tr>
<td>1</td>
<td>Select low-speed on-chip oscillator clock</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (Hardware) for details on how to set registers.
5.6.6 External Interrupt Setting

Figure 5.10 shows the flowchart for setting the external interrupt.

```
R_INTC_Create()

Disable all INTP interrupts

MK0L register
  PMK5-PMK0 bit ← 111111B :Interrupt processing disabled
MK1H register
  PMK11-PMK9 bit ← 111B :Interrupt processing disabled
MK2H register
  FOMK bit ← 1 :Interrupt processing disabled

IF0L register
  PIF5-PIF0 bit ← 111111B :Interrupt request signal not generated
IF1H register
  PIF11-PIF9 bit ← 111B :Interrupt request signal not generated
IF2H register
  FOIF bit ← 1 :Interrupt request signal not generated

Set interrupt priority level

PPR10 bit ← 1
PPR00 bit ← 1: Specify level 3 (low priority level)

Set external interrupt valid edge

EGP1 bit ← 0
EGN1 bit ← 1: Specify falling edge as INTP0 pin valid edge
```

Figure 5.10 External Interrupt Setting
Control of external interrupt valid edge

- External interrupt rising edge enable register (EGP0)
  Select valid edge for INTP0 pin: falling edge

Symbol: EGP0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EGP7</td>
<td>EGP6</td>
<td>EGP5</td>
<td>EGP4</td>
<td>EGP3</td>
<td>EGP2</td>
<td>EGP1</td>
<td>EGP0</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
</tr>
</tbody>
</table>

Symbol: EGN0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EGN7</td>
<td>EGN6</td>
<td>EGN5</td>
<td>EGN4</td>
<td>EGN3</td>
<td>EGN2</td>
<td>EGN1</td>
<td>EGN0</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>EGP1</th>
<th>EGN1</th>
<th>INTP0 pin valid edge selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Edge detection disabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Falling edge</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Rising edge</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Both rising and falling edges</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (Hardware) for details on how to set registers.
5.6.7 12-bit Interval Timer Setting

Figure 5.11 shows the flowchart for setting the 12-bit interval timer.

```
R_IT_Create()

- Reset 12-bit interval timer
  - TMKARES bit ← 1
  - TMKARES bit ← 0

- Supply clock to 12-bit interval timer
  - TMKAEN bit ← 1

- Stop 12-bit interval timer operation
  - ITMC register ← 0000H

- Disable 12-bit interval timer interrupt
  - TMKAMK bit ← 1

- Clear 12-bit interval timer interrupt request flag
  - TMKAIF bit ← 0

- Set interrupt priority level
  - TMKAPR1 bit ← 1
  - TMKAPR0 bit ← 1

- Select low-speed on-chip oscillator clock for 12-bit interval timer clock
  - TPS3 register ← 00H

- Set the compare value (5ms) of 12-bit interval timer
  - ITMC register ← 004AH

return
```

**Figure 5.11 12-bit Interval Timer Setting**
12-bit interval timer clock supply setting

- Peripheral enable register 2 (PER2)
  Enable clock supply to 12-bit interval timer.

Symbol: PER2

<table>
<thead>
<tr>
<th>Bit</th>
<th>TMKAEN</th>
<th>DOCEN</th>
<th>TKB0EN</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>0</td>
<td>x</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 7

- TMKAEN: Control of 12-bit interval timer input clock supply
  - 0: Stops input clock supply.
  - 1: Enables input clock supply.

12-bit interval timer interval signal detection interrupt (INTIT) setting

- Interrupt request flag register (IF1H)
  Clear TMKAIF interrupt source flag.
- Interrupt mask flag register (MK1H)
  Set TMKAMK interrupt mask.

Symbol: IF1H

<table>
<thead>
<tr>
<th>Bit</th>
<th>PIF11</th>
<th>PIF10</th>
<th>PIF9</th>
<th>PIF8</th>
<th>PIF7</th>
<th>KRIF</th>
<th>TMKAIF</th>
<th>ADIF</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 1

- TMKAIF: Interrupt request flag
  - 0: No interrupt request signal is generated
  - 1: Interrupt request signal is generated, interrupt request status

Symbol: MK1H

<table>
<thead>
<tr>
<th>Bit</th>
<th>PMK11</th>
<th>PMK10</th>
<th>PMK9</th>
<th>PMK8</th>
<th>PMK7</th>
<th>KRMK</th>
<th>TMKAMK</th>
<th>ADMK</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 1

- TMKAMK: Interrupt servicing control
  - 0: Interrupt servicing enabled
  - 1: Interrupt servicing disabled

Note: Refer to the RL78/G11 User’s Manual (Hardware) for details on how to set registers.
12-bit interval timer interval signal detection interrupt (INTIT) setting

- Interval timer control register (ITMC)
  Start 12-bit interval timer count operation.

Symbol: ITMC

<table>
<thead>
<tr>
<th></th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>2</th>
<th>11-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RINTE</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ITCMP11-ITCMP0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>04AH</td>
</tr>
</tbody>
</table>

Bit 15

<table>
<thead>
<tr>
<th>RINTE</th>
<th>12-bit interval timer operation control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Count operation stopped (count clear)</td>
</tr>
<tr>
<td>1</td>
<td>Count operation started</td>
</tr>
</tbody>
</table>

Bits 11-0

<table>
<thead>
<tr>
<th>ITCMP11-ITCMP0</th>
<th>Specification of 12-bit interval timer compare value</th>
</tr>
</thead>
<tbody>
<tr>
<td>04AH</td>
<td>These bits generate an interrupt at the fixed cycle (count clock cycles x (ITCMP setting value 04AH + 1)).</td>
</tr>
<tr>
<td>000H</td>
<td>Setting prohibited</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (Hardware) for details on how to set registers.
5.6.8 Main initializes settings

Figure 5.12 shows the flowchart for the main initializes settings.

Figure 5.12 Main initializes settings

Pin input edge detection interrupt (INTP0) setting

- Interrupt request flag register (IF0L)
  Clear the PIF0 interrupt source flag.
- Interrupt mask flag register (MK0L)
  Set PMK0 interrupt mask.

Symbol: IF0L

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIF5</td>
<td>PIF4</td>
<td>PIF3</td>
<td>PIF2</td>
<td>PIF1</td>
<td>PIF0</td>
<td>LVIF</td>
<td>WDTIF</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 2

PIF0

- 0  No interrupt request signal is generated
- 1  Interrupt request signal is generated, interrupt request status

Symbol: MK0L

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMK5</td>
<td>PMK4</td>
<td>PMK3</td>
<td>PMK2</td>
<td>PMK1</td>
<td>PMK0</td>
<td>LVIMK</td>
<td>WDTMK</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 2

PMK0

- 0  Interrupt servicing enabled
- 1  Interrupt servicing disabled

Note: Refer to the RL78/G11 User’s Manual (Hardware) for details on how to set registers.
5.6.9 Status Transition AtoB
Figure 5.13 shows the flowchart for status transition AtoB.

![Flowchart for Status Transition AtoB]

R_MAIN_AtoB()

Control LED lighting
(high-speed on-chip oscillator clock)

P5.4 bit ← 1: Set LED3 to OFF
P5.5 bit ← 1: Set LED4 to OFF
P5.6 bit ← 0: Set LED5 to ON

Control LED lighting
(CPU operation)

P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 0: Set LED2 to ON
PIF0 bit ← 0

Clear external interrupt request flag

Execute NOP instruction continuously.

CPU operation (NOP instruction execution)
R_MAIN_NOP_Loop()

return

Figure 5.13 Status Transition AtoB

5.6.10 CPU operation (NOP instruction execution)
Figure 5.14 shows the flowchart for the CPU operation (NOP instruction execution)

![Flowchart for CPU Operation (NOP instruction execution)]

R_MAIN_NOP_Loop()

Clear external interrupt generation detection flag

Execute NOP instruction
(512 times)

Is external interrupt generation detection flag 1?

NO

YES (branch when g_int_flg= 1)

return

Figure 5.14 CPU Operation (NOP instruction execution)
5.6.11 Status Transition BtoD

Figure 5.15 and Figure 5.16 show the flowchart for status transition BtoD.

![Flowchart](image)

**Figure 5.15 Status Transition BtoD (1/2)**
Start count of 12-bit interval timer

ITMC register ← 8001H

MCS bit = 1?

No

Interval detection interrupt generated time?

Yes (branch when g_int_cnt = 1)

R_MAIN_ERROR()

To status transition error processing

No

Disable interval detection interrupt

TMKAMK bit ← 1

Stop count of 12-bit interval timer

ITMC register ← 0000H

Stop high-speed on-chip oscillator

HIOSTOP bit ← 1

Control LED lighting (high-speed system clock)

P5.4 bit ← 0: Set LED3 to ON
P5.5 bit ← 1: Set LED4 to OFF
P5.6 bit ← 0: Set LED5 to ON

Control LED lighting (CPU operation)

P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 0: Set LED2 to ON

Clear external interrupt request flag

PIF0 bit ← 0

Enable external interrupt servicing

PMK0 bit ← 0

CPU operation (NOP instruction execution)
R_MAIN_NOP_Loop()

Execute NOP instruction continuously.

return

Figure 5.16 Status Transition BtoD (2/2)
5.6.12 Error Processing of Status Transition
Figure 5.17 shows the flowchart for error processing of status transition.

![Error Processing of Status Transition](image)

5.6.13 Status Transition DtoL
Figure 5.18 shows the flowchart for status transition DtoL.

![Status Transition DtoL](image)
5.6.14 Status Transition LtoD

Figure 5.19 shows the flowchart for status transition LtoD.

![Flowchart for Status Transition LtoD](image)

- **R_MAIN_LtoD()**
- **Control LED lighting (CPU operation)**
  - P0.0 bit ← 0: Set LED1 to ON
  - P0.1 bit ← 0: Set LED2 to ON
- **Clear external interrupt request flag**
  - PIF0 bit ← 0
- **CPU operation (NOP instruction execution)**
  - R_MAIN_NOP_Loop()
- **return**

**Figure 5.19 Status Transition LtoD**

5.6.15 Status Transition DtoM

Figure 5.20 shows the flowchart for status transition DtoM.

![Flowchart for Status Transition DtoM](image)

- **R_MAIN_DtoM()**
- **Control LED lighting (STOP mode)**
  - P0.0 bit ← 1: Set LED1 to OFF
  - P0.1 bit ← 1: Set LED2 to OFF
- **Clear external interrupt request flag**
  - PIF0 bit ← 0
- **STOP mode**
- **return**

**Figure 5.20 Status Transition DtoM**
5.6.16 Status Transition MtoD

Figure 5.21 shows the flowchart for status transition MtoD.

![Flowchart for status transition MtoD](image-url)

- **R_MAIN_MtoD()**
  - Control LED lighting (STOP mode)
    - P0.0 bit ← 0: Set LED1 to ON
    - P0.1 bit ← 0: Set LED2 to ON
  - Clear external interrupt request flag
    - PIF0 bit ← 0
  - CPU operation (NOP instruction execution)
    - R_MAIN_NOP_Loop()
  - return

**Figure 5.21 Status Transition MtoD**
5.6.17 Status Transition DtoB

Figure 5.22 and Figure 5.23 show the flowchart for status transition DtoB.

![Flowchart for Status Transition DtoB](image)

**Figure 5.22 Status Transition DtoB (1/2)**
Start 12-bit interval timer count

MCS bit = 0?

Interval detection interrupt generated time?

Yes (branch when g_int_cnt = 1)

R_MAIN_ERROR()

To status transition error processing

Disable interval detection interrupt

Stop 12-bit interval timer count

Stop X1 oscillator

Control LED lighting (high-speed on-chip oscillator clock)

Control LED lighting (CPU operation)

Clear external interrupt request flag

Enable external interrupt servicing

CPU operation (NOP instruction execution)

R_MAIN_NOP_Loop()

return

ITMC register ← 8001H

TMKAMK bit ← 1

Stop 12-bit interval timer count ITMC register ← 0000H

MSTOP bit ← 1

P5.4 bit ← 1: Set LED3 to OFF
P5.5 bit ← 1: Set LED4 to OFF
P5.6 bit ← 0: Set LED5 to ON

P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 0: Set LED2 to ON

PIF0 bit ← 0

PMK0 bit ← 0

Execute NOP instruction continuously.
5.6.18 Status Transition BtoF
Figure 5.24 shows the flowchart for status transition BtoF.

![Flowchart for Status Transition BtoF](image)

5.6.19 Status Transition FtoB
Figure 5.25 shows the flowchart for status transition FtoB.

![Flowchart for Status Transition FtoB](image)
5.6.20 Status Transition BtoG

Figure 5.26 shows the flowchart for status transition BtoG.

![Flowchart for status transition BtoG](image)

**Figure 5.26 Status Transition BtoG**

5.6.21 Status Transition GtoB

Figure 5.27 shows the flowchart for status transition GtoB.

![Flowchart for status transition GtoB](image)

**Figure 5.27 Status Transition GtoB**
5.6.22 Status Transition BtoH

Figure 5.28 shows the flowchart for status transition BtoH.

```
R_MAIN_BtoH()

Disable external interrupt

Set A/D SNOOZE mode
R_MAIN_AD_SnoozeOn()

Disable interval detection interrupt

Control LED lighting
(SNOOZE mode)

Start 12-bit interval timer count

STOP

return

PMK0 bit ← 1

Set A/D conversion execution to hardware trigger
with the 12-bit interval timer interrupt signal

TMKAMK bit ← 1

P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 1: Set LED2 to OFF

ITMC register ← 8FFFH
```

**Figure 5.28** Status Transition BtoH
5.6.23 A/D Converter Setting

Figure 5.29 shows the flowchart for setting the A/D converter.

```
R_MAIN_AD_SnoozeOn()
| Set A/D converter
| R_ADC_Create()
| Clear A/D conversion
| complete interrupt request flag
| ADIF bit ← 0
| Enable A/D conversion
| interrupt
| ADMK bit ← 0
| Use SNOOZE mode function
| AWC bit ← 1
| return
```

**Figure 5.29 A/D Converter Setting**

SNOOZE mode setting

- A/D converter mode register 2 (ADM2)
  - Set SNOOZE mode.

Symbol: ADM2

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADREFP1</td>
<td>ADREFP0</td>
<td>ADREFM</td>
<td>0</td>
<td>ADCRK</td>
<td>AWC</td>
<td>0</td>
<td>ADTYP</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>x</td>
<td>1</td>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 2

<table>
<thead>
<tr>
<th>AWC</th>
<th>Specification of SNOOZE mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Do not use the SNOOZE mode function</td>
</tr>
<tr>
<td>1</td>
<td>Use the SNOOZE mode function</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (hardware) for detailed explanations on how to set registers.
5.6.24 A/D Converter Initial Setting

Figure 5.30 shows the flowchart for setting the A/D converter.

![Flowchart for A/D Converter Initial Setting](image)

**Figure 5.30 A/D Converter Initial Setting**
A/D conversion time and operation mode settings

- A/D converter mode register 0 (ADM0)
  Control the A/D conversion operation.
  Specify the A/D conversion channel selection mode.

Symbol: ADM0

<table>
<thead>
<tr>
<th>Bit 6</th>
<th>Specification of A/D channel selection mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Select mode</td>
</tr>
<tr>
<td>1</td>
<td>Scan mode</td>
</tr>
</tbody>
</table>

Bits 5-1

<table>
<thead>
<tr>
<th>FR2</th>
<th>FR1</th>
<th>FR0</th>
<th>LV1</th>
<th>LV0</th>
<th>Mode</th>
<th>Conversion Time</th>
<th>Conversion clock (fCLK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Normal</td>
<td>Setting</td>
<td>Setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td></td>
<td>Setting</td>
<td>Setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td></td>
<td>Setting</td>
<td>Setting</td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
<td>0</td>
<td></td>
<td></td>
<td>Setting</td>
</tr>
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<td>0</td>
<td></td>
<td></td>
<td>Setting</td>
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<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
<td>40.5 μs</td>
<td>13.5 μs</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td>135 μs</td>
<td>33.75 μs</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
<td>108 μs</td>
<td>27 μs</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td>54 μs</td>
<td>13.5 μs</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
<td>54 μs</td>
<td>6.75 μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>ADC0</th>
<th>A/D voltage comparator operation control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Stops A/D enables comparator operation</td>
</tr>
<tr>
<td>1</td>
<td>Enables A/D voltage comparator operation</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (hardware) for detailed explanations on how to set registers.
A/D conversion trigger mode setting

- A/D converter mode register 1 (ADM1)
  Select the A/D conversion trigger mode.
  Specify the A/D conversion operation mode.

Symbol: ADM1

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADTMD1</td>
<td>ADTMD0</td>
<td>ADSCM</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ADTRS1</td>
<td>ADTRS0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Bits 7-6

<table>
<thead>
<tr>
<th>ADTMD1</th>
<th>ADTMD0</th>
<th>Selection of the A/D conversion trigger mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>—</td>
<td>Software trigger mode</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Hardware trigger no-wait mode</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Hardware trigger wait mode</td>
</tr>
</tbody>
</table>

Bit 5

<table>
<thead>
<tr>
<th>ADSCM</th>
<th>Specification of the A/D conversion mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Sequential conversion mode</td>
</tr>
<tr>
<td>1</td>
<td>One-shot conversion mode</td>
</tr>
</tbody>
</table>

Bits 1-0

<table>
<thead>
<tr>
<th>ADTRS1</th>
<th>ADTRS0</th>
<th>Selection of the hardware trigger signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>End of timer channel 01 count or capture interrupt signal (INTTM01)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Event signal selected by ELC</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Setting prohibited</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>12-bit interval timer interrupt signal (INTIT)</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (hardware) for detailed explanations on how to set registers.
Reference voltage source setting

- A/D converter mode register 2 (ADM2)
  Set the reference voltage source.

Symbol: ADM2

<table>
<thead>
<tr>
<th>Bit 7-6</th>
<th>Selection of the + side reference voltage source of the A/D converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>Supplied from VDD</td>
</tr>
<tr>
<td>0 1</td>
<td>Supplied from P20/AV REFP/ANI0</td>
</tr>
<tr>
<td>1 0</td>
<td>Supplied from the internal reference voltage (1.45 V)</td>
</tr>
<tr>
<td>1 1</td>
<td>Setting prohibited</td>
</tr>
</tbody>
</table>

Bit 5

<table>
<thead>
<tr>
<th>Bit 5</th>
<th>Selection of the - side reference voltage source of the A/D converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Supplied from VSS</td>
</tr>
<tr>
<td>1</td>
<td>Supplied from P21/AV REFM/ANI1</td>
</tr>
</tbody>
</table>

Bit 3

<table>
<thead>
<tr>
<th>Bit 3</th>
<th>Checking the upper and lower limit conversion result values</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The interrupt signal (INTAD) is output when ADLL register ≤ ADCR register ≤ register ADUL.</td>
</tr>
<tr>
<td>1</td>
<td>The interrupt signal (INTAD) is output when ADCR register &lt; ADLL register, and ADUL register &lt; ADCR register.</td>
</tr>
</tbody>
</table>

Bit 2

<table>
<thead>
<tr>
<th>Bit 2</th>
<th>Specification of the SNOOZE mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Do not use the SNOOZE mode function.</td>
</tr>
<tr>
<td>1</td>
<td>Use the SNOOZE mode function.</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>Bit 0</th>
<th>Selection of the A/D conversion resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10-bit resolution</td>
</tr>
<tr>
<td>1</td>
<td>8-bit resolution</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (hardware) for detailed explanations on how to set registers.
Conversion result comparison upper/lower limit settings

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Set conversion result comparison upper/lower limit values.

Symbol: ADUL

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADUL7</td>
<td>ADUL6</td>
<td>ADUL5</td>
<td>ADUL4</td>
<td>ADUL3</td>
<td>ADUL2</td>
<td>ADUL1</td>
<td>ADUL0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Symbol: ADLL

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADLL7</td>
<td>ADLL6</td>
<td>ADLL5</td>
<td>ADLL4</td>
<td>ADLL3</td>
<td>ADLL2</td>
<td>ADLL1</td>
<td>ADLL0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Input channel specification

- Analog input channel specification register (ADS)

Specify the input channel of the analog voltage to be A/D converted.

Symbol: ADS

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADISS</td>
<td>0</td>
<td>0</td>
<td>ADS4</td>
<td>ADS3</td>
<td>ADS2</td>
<td>ADS1</td>
<td>ADS0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bits 7, 4-0

<table>
<thead>
<tr>
<th>ADISS</th>
<th>ADS4</th>
<th>ADS3</th>
<th>ADS2</th>
<th>ADS1</th>
<th>ADS0</th>
<th>Analog input channel</th>
<th>Input source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ANI0</td>
<td>P20/ANI0 /AVREFP pin</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>ANI1</td>
<td>P21/ANI1 /AVREFM pin</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ANI2</td>
<td>P22/ANI2 pin</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>ANI3</td>
<td>P23/ANI3 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ANI16</td>
<td>P01/ANI16 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ANI17</td>
<td>P00/ANI17 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>ANI18</td>
<td>P33/ANI18 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ANI19</td>
<td>P32/ANI19 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ANI20</td>
<td>P31/ANI20 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>ANI21</td>
<td>P30/ANI21 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ANI22</td>
<td>P56/ANI22 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>–</td>
<td>PGAOUT(PGA output)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>–</td>
<td>Temperature sensor 0 output</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>–</td>
<td>Internal reference voltage output (1.45 V)</td>
</tr>
</tbody>
</table>

Note: Refer to the RL78/G11 User’s Manual (hardware) for detailed explanations on how to set registers.
5.6.25 Status Transition HtoB

Figure 5.31 shows the status transition HtoB.

```
R_MAIN_HtoB()

Stop A/D voltage converter operation
ADCE bit ← 0

Stop the clock to A/D converter
ADCN bit ← 0

Disable A/D conversion complete interrupt
ADMK bit ← 1

Stop 12-bit interval timer count
ITMC register ← 0000H

Control LED lighting (CPU operation)
P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 0: Set LED2 to ON

Clear external interrupt request flag
PIF0 bit ← 0

Enable external interrupt servicing
PMK0 bit ← 0

CPU operation (NOP instruction execution)
R_MAIN_NOP_Loop()

Execute NOP instruction continuously.

return
```

Figure 5.31 Status Transition HtoB
5.6.26 Status Transition BtoC

Figure 5.32 and Figure 5.33 shows the status transition BtoC.

```
R_MAIN_BtoC()

<table>
<thead>
<tr>
<th>No</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interval detection interrupt generated 1 times?</td>
</tr>
<tr>
<td>Yes (branch when g_int_cnt = 1)</td>
</tr>
</tbody>
</table>

PMK0 bit ← 1

MOCODIV register ← 00H: Set the middle-speed on-chip oscillator frequency to 4MHz

MIOEN bit ← 1

TMKAF bit ← 0

TMKAMK bit ← 0

ITMC register ← 8001H

Stop count of 12-bit interval timer

ITMC register ← 0000H

Select middle-speed on-chip oscillator clock as CPU/peripheral hardware clock

MCM1 bit ← 1

Clear interval detection interrupt request flag

TMKAF bit ← 0

Initialize counter of interval detection interrupt generation

A
```

Figure 5.32 Status Transition BtoC(1/2)
Figure 5.33 Status Transition BtoC(2/2)
5.6.27 Status Transition CtoD

Figure 5.34 and Figure 5.35 shows the status transition CtoD.

![Status Transition CtoD Diagram](image)

**Figure 5.34  Status Transition CtoD(1/2)**
Start count of 12-bit interval timer

MCS bit = 1?

Yes

Interval detection interrupt generated time?

Yes (branch when g_int_cnt = 1)

R_MAIN_ERROR() To status transition error processing

No

ITMC register ← 8001H

Disable interval detection interrupt

TMKAMK bit ← 1

Stop count of 12-bit interval timer

ITMC register ← 0000H

Middle-speed on-chip oscillator stopped

MIOEN bit ← 0

Control LED lighting
(high-speed system clock)

P5.4 bit ← 0: Set LED3 to ON
P5.5 bit ← 1: Set LED4 to OFF
P5.6 bit ← 0: Set LED5 to ON

Control LED lighting
(CPU operation)

P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 0: Set LED2 to ON

Clear external interrupt request flag

PIF0 bit ← 0

Enable external interrupt servicing

PMK0 bit ← 0

CPU operation (NOP instruction execution)
MAIN_NOP_Loop()

Execute NOP instruction continuously

return

Figure 5.35 Status Transition CtoD(2/2)
5.6.28 Status Transition DtoE

Figure 5.36 and Figure 5.37 shows the status transition DtoE.

```
R_MAIN_DtoE()

PMK0 bit ← 1
SELLOSC bit ← 1
CSS bit ← 1
SELLOSC bit ← 1
PMK0 bit ← 1

TMKAIF bit ← 0
TMKAMK bit ← 0

ITMC register ← 8001H

CLS bit = 1?

No

Interval detection interrupt generated time?

Yes (branch when g_int_cnt = 1)

R_MAIN_ERROR()

To status transition error processing

No

Interval detection interrupt generated time?

Yes (branch when g_int_cnt = 1)

R_MAIN_ERROR()

To status transition error processing

A
```

Figure 5.36 Status Transition DtoE(1/2)
Figure 5.37  Status Transition DtoE(2/2)
5.6.29 Status Transition EtoD

Figure 5.38 and Figure 5.39 shows the status transition EtoD.

![Diagram of R_MAIN_EtoD()](image)

- **Disable external interrupt**: PMK0 bit ← 1
- **Set oscillation stabilization time selection register**: OSTS register ← 07H
- **X1 oscillator operation**: MSTOP bit ← 0
- **Oscillation stabilization time elapsed?**
  - Yes (branch when OSCT register is FFH)
  - Select high-speed system clock as CPU/peripheral hardware clock: CSS bit ← 0
  - Clear interval detection interrupt request flag: TMKAIF bit ← 0
  - Enable interval detection interrupt: TMKAMK bit ← 0
  - Initialize interval detection interrupt generation counter

**Figure 5.38 Status Transition EtoD(1/2)**
Figure 5.39 Status Transition EtoD(2/2)
5.6.30 Status Transition DtoC

Figure 5.40 and Figure 5.41 shows the status transition DtoC.

![Flowchart of R_MAIN_DtoC()](image)

- **PMK0 bit ← 1**
- **MOCODIV register ← 00H**: Set the middle-speed on-chip oscillator frequency to 4MHz
- **MIOEN bit ← 1**
- **TMKAIF bit ← 0**
- **TMKAMK bit ← 0**
- **ITMC register ← 8001H**
- **ITMC register ← 0000H**
- **MCM0 bit ← 0**
- **TMKAIF bit ← 0**
- **Initialize counter of interval detection interrupt generation**

---

**Figure 5.40** Status Transition DtoC(1/2)
Start count of 12-bit interval timer

MCS bit = 0?

Yes

Interval detection interrupt generated time?

Yes (branch when g_int_cnt = 1)

R_MAIN_ERROR()

To status transition error processing

No

ITMC register ← 8001H

Disable interval detection interrupt

TMKAMK bit ← 1

Stop count of 12-bit interval timer

ITMC register ← 0000H

Stop X1 oscillator

MSTOP bit ← 1

Control LED lighting (middle-speed on-chip oscillator clock)
P5.4 bit ← 1: Set LED3 to OFF
P5.5 bit ← 0: Set LED4 to ON
P5.6 bit ← 1: Set LED5 to OFF

Control LED lighting (CPU operation)
P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 0: Set LED2 to ON

Clear external interrupt request flag

PIF0 bit ← 0

Enable external interrupt servicing

PMK0 bit ← 0

CPU operation (NOP instruction execution)
R_MAIN_NOP_Loop()

Execute NOP instruction continuously

return

Figure 5.41 Status Transition DtoC(2/2)
5.6.31 Status Transition CtoI
Figure 5.42 shows the status transition CtoI.

Figure 5.42 Status Transition CtoI

5.6.32 Status Transition ItoC
Figure 5.43 shows the status transition ItoC.

Figure 5.43 Status Transition ItoC
5.6.33 Status Transition CtoJ
Figure 5.44 shows the status transition CtoJ.

![Diagram of Status Transition CtoJ]

5.6.34 Status Transition JtoC
Figure 5.45 shows the status transition JtoC.

![Diagram of Status Transition JtoC]
5.6.35 Status Transition CtoK

Figure 5.46 shows the status transition CtoK.

![Diagram](image)

- **R_MAIN_CtoK()**
  - Disable external interrupt
  - Set A/D SNOOZE mode
    - R_MAIN_AD_SnoozeOn()
  - Disable interval detection interrupt
  - Control LED lighting (SNOOZE mode)
  - Start 12-bit interval timer count
  - STOP
  - return

- PMK0 bit ← 1
- Set A/D conversion execution to hardware trigger with the 12-bit interval timer interrupt signal
- TMKAMK bit ← 1
- P0.0 bit ← 0: Set LED1 to ON
- P0.1 bit ← 1: Set LED2 to OFF
- ITMC register ← 8FFFH

**Figure 5.46 Status Transition CtoK**
5.6.36 Status Transition KtoC

Figure 5.47 shows the status transition KtoC.

```
R_MAIN_KtoC()

Stop A/D voltage converter operation
ADCE bit ← 0

Stop the clock to A/D converter
ADCEN bit ← 0

Disable A/D conversion complete interrupt
ADMK bit ← 1

Stop 12-bit interval timer count
ITMC register ← 0000H

Control LED lighting (CPU operation)
P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 0: Set LED2 to ON

Clear external interrupt request flag
PIF0 bit ← 0

Enable external interrupt servicing
PMK0 bit ← 0

CPU operation (NOP instruction execution)
R_MAIN_NOP_Loop()

Execute NOP instruction continuously.

return
```

Figure 5.47 Status Transition KtoC
5.6.37 Status Transition CtoE

Figure 5.48 and Figure 5.49 shows the status transition CtoE.

![Diagram](image-url)

**Figure 5.48 Status Transition CtoE (1/2)**

1. **CtoE**
2. Disable external interrupt
3. Select low-speed on-chip oscillator clock as sub system clock
4. Select low-speed on-chip oscillator clock as CPU/peripheral hardware clock
5. Clear interval detection interrupt request flag
6. Enable interval detection interrupt
7. Initialize interval detection interrupt generation counter
8. Start 12-bit interval timer count

- **PMK0 bit** ← 1
- **SELOSC bit** ← 1
- **CSS bit** ← 1
- **TMKAIF bit** ← 0
- **TMKAMK bit** ← 0
- **CLS bit = 1?**
  - **Yes**
  - Interval detection interrupt generated time?
    - **Yes** (branch when g_int_cnt = 1)
      - **R_MAIN_ERROR()**
    - **No**
  - **No**

To status transition error processing

---

**Figure 5.49 Status Transition CtoE (2/2)**
Figure 5.49  Status Transition CtoE(2/2)
5.6.38 Status Transition EtoC

Figure 5.50 and Figure 5.51 shows the status transition EtoC.

![Diagram of status transition EtoC](image-url)

**Figure 5.50** Status Transition EtoC(1/2)
Start count of 12-bit interval timer

ITMC register ← 8001H

CLS bit = 0?

Yes

Interval detection interrupt generated time?

YES (branch when g_int_cnt = 1)

R_MAIN_ERROR()

To status transition error processing

No

Disable interval detection interrupt

TMKAMK bit ← 1

Stop count of 12-bit interval timer

ITMC register ← 0000H

Do not select low-speed on-chip oscillator clock as subsystem clock

SELOSC bit ← 0

Control LED lighting (middle-speed on-chip oscillator clock)

P5.4 bit ← 1: Set LED3 to OFF
P5.5 bit ← 0: Set LED4 to ON
P5.6 bit ← 1: Set LED5 to OFF

Control LED lighting (CPU operation)

P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 0: Set LED2 to ON

Clear external interrupt request request flag

PIF0 bit ← 0

Enable external interrupt servicing

PMK0 bit ← 0

CPU operation (NOP instruction execution)

R_MAIN_NOP_Loop()

Execute NOP instruction continuously

return

Figure 5.51 Status Transition EtoC(2/2)
5.6.39 Status Transition CtoB

Figure 5.52 and Figure 5.53 show the status transition CtoB.

R_MAIN_CtoB()

- Disable external interrupt
  - PMK0 bit ← 1
- High-speed on-chip oscillator operation
  - HIOSTOP bit ← 0
- Clear interval detection interrupt request flag
  - TMKAIF bit ← 0
- Enable interval detection interrupt
  - TMKAMK bit ← 0
- Initialize interval detection interrupt generation counter
- Start 12-bit interval timer count
  - ITMC register ← 8001H

No

Interval detection interrupt generated 1 time?
  - Yes (branch when g_int_cnt = 1)

Stop 12-bit interval timer count
  - ITMC register ← 0000H

Select high-speed on-chip oscillator clock as CPU/peripheral hardware clock
  - MCM1 bit ← 0

Clear interval detection interrupt request flag
  - TMKAIF bit ← 0

Initialize interval detection interrupt generation counter

Figure 5.52 Status Transition CtoB(1/2)
Figure 5.53  Status Transition CtoB(2/2)
5.6.40 Status Transition BtoE

Figure 5.54 and Figure 5.55 shows the status transition BtoE.

![Flowchart for Status Transition BtoE](image)

- **R_MAIN_BtoE()**
- Disable external interrupt
- Select low-speed on-chip oscillator clock as sub system clock
- Select low-speed on-chip oscillator clock as CPU/peripheral hardware clock
- Clear interval detection interrupt request flag
- Enable interval detection interrupt
- Initialize interval detection interrupt generation counter
- Start 12-bit interval timer count
- **ITMC register ← 8001H**
- **CLS bit = 1?**
  - Yes
  - Interval detection interrupt generated time?
    - Yes (branch when g_int_cnt = 1)
    - **R_MAIN_ERROR()**
    - No
  - No
- **To status transition error processing**
CPU operation (NOP instruction execution)
RMAIN_NOP_Loop()

A

Disable interval detection interrupt
TMKAMK bit ← 1

Stop 12-bit interval timer count
ITMC register ← 0000H

Stop high-speed on-chip oscillator
HIOSTOP bit ← 1

Control LED lighting (low-speed on-chip oscillator clock)
P5.4 bit ← 1: Set LED3 to OFF
P5.5 bit ← 0: Set LED4 to ON
P5.6 bit ← 0: Set LED5 to ON

Control LED lighting (CPU operation)
P0.0 bit ← 0: Set LED1 to ON
P0.1 bit ← 0: Set LED2 to ON

Clear external interrupt request flag
PIF0 bit ← 0

Enable external interrupt servicing
PMK0 bit ← 0

Execute NOP instruction continuously

Figure 5.55 Status Transition BtoE(2/2)
5.6.41 Status Transition EtoN

Figure 5.56 shows the status transition EtoN.

![Diagram of Status Transition EtoN]

5.6.42 Status Transition NtoE

Figure 5.57 shows the status transition NtoE.

![Diagram of Status Transition NtoE]
5.6.43 Status Transition EtoB

Figure 5.58 and Figure 5.59 show the status transition EtoB.

![Flowchart]

**Figure 5.58 Status Transition EtoB(1/2)**
Figure 5.59 Status Transition EtoB(2/2)
5.6.44 Status Transition End Processing

Figure 5.60 shows the flowchart for status transition end processing.

![Flowchart for Status Transition End Processing](chart.png)

Figure 5.60 Status Transition End Processing
5.6.45 External Interrupt Servicing

Figure 5.61 shows the flowchart for external interrupt servicing.

```
  r_intc0_interrupt()
   |
--- Confirm interrupt determination flag
   |
--- Clear interval detection interrupt request flag
   |
--- Disable interval detection interrupt
   |
--- Start 12-bit interval timer count
   |
   Is interval detection interrupt request flag 1?
   No
   |
   Yes (branch when TMKAIF bit = 1)
   |
--- Clear interval detection interrupt request flag
   |
   P137 bit = 1?
   No
   |
   Yes
   |
   No
   |
   Is interval detection interrupt request flag 1?
   Yes (branch when TMKAIF bit = 1)
   |
--- Clear interval detection interrupt request flag
   |
   P137 bit = 1?
   No
   |
   Yes
   |
   No
   |
--- Stop 12-bit interval timer count
   |
   return

Figure 5.61 External Interrupt Servicing
```
5.6.46 12-bit Interval Timer Interrupt Servicing
Figure 5.62 shows the flowchart for 12-bit interval timer interrupt servicing.

```
<table>
<thead>
<tr>
<th>r_it_interrupt()</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increment interval detection interrupt generation counter by 1</td>
</tr>
<tr>
<td>return</td>
</tr>
</tbody>
</table>
```

**Figure 5.62 12-bit Interval Timer Interrupt Servicing**

5.6.47 A/D Conversion Completion Interrupt Servicing
Figure 5.63 shows the flowchart for A/D conversion completion interrupt servicing.

```
<table>
<thead>
<tr>
<th>r_adc_interrupt()</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stop use of SNOOZE mode function</td>
</tr>
<tr>
<td>AWC ← 0</td>
</tr>
<tr>
<td>return</td>
</tr>
</tbody>
</table>
```

**Figure 5.63 A/D Conversion Completion Interrupt Servicing**
6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

RL78/G11 User’s Manual: Hardware (R01UH0637E)
RL78 Family User’s Manual: Software (R01US0015E)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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<tr>
<td>1.00</td>
<td>Jun. 27, 2017</td>
<td>—</td>
<td>First edition issued</td>
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   - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
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3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

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<table>
<thead>
<tr>
<th>Precaution</th>
<th>Description</th>
</tr>
</thead>
</table>
| **1. Handling of Unused Pins**                                            | Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.  
- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual. |
| **2. Processing at Power-on**                                             | The state of the product is undefined at the moment when power is supplied.  
- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.  
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.  
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified. |
| **3. Prohibition of Access to Reserved Addresses**                        | Access to reserved addresses is prohibited.  
- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed. |
| **4. Clock Signals**                                                      | After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.  
- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable. |
| **5. Differences between Products**                                       | Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.  
- The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product. |
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