RL78/G11

Ceramic Fan Heater with Human Sensor

R01AN4339EJ0100
Rev. 1.00
Jan.29, 2019

Introduction

This application note describes how to implement the ceramic fan heater with a human sensor by using the RL78/G11.

Target Device

RL78/G11

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Figure 1.1 shows the schematic system configuration.

After power on, the system starts operating in continuous operation mode. The PWM signal is output to control the fan, and the high-level signal is output to control the heater. By operating the switch, continuous operation mode is changed over to human sensor mode.

In continuous operation mode, the fan and heater are automatically stopped and the system shifts to human sensor mode four hours later in case of failure to stop the operation.

In human sensor mode, the fan and heater are controlled while the human sensor is detecting a target and for five minutes after the sensor no longer senses any target; then, the fan and heater are stopped.

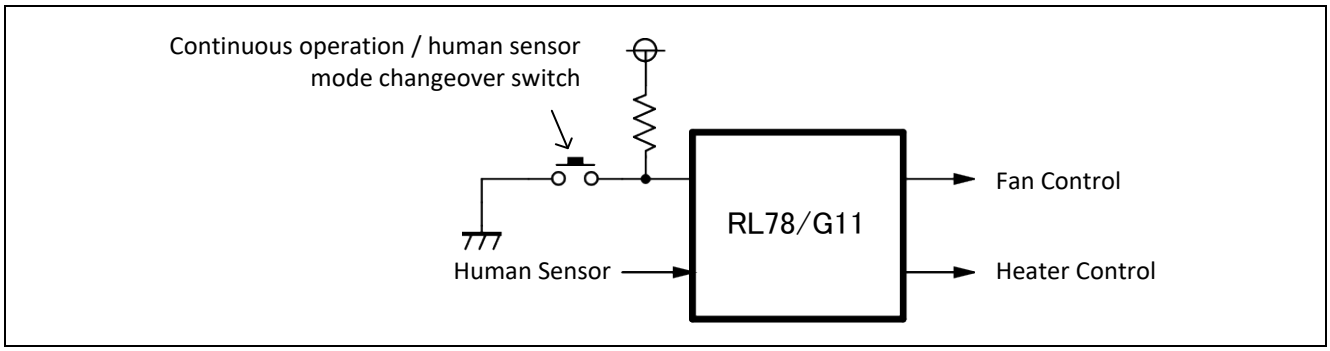

Figure 1.1 Schematic System Configuration

1.1 Human Sensor

This application system uses a module with a pyroelectric infrared sensor (hereinafter called a human sensor). According to the specifications, the system begins to monitor all around the sensor at some seconds after power on, and changes the output level of the signal to low when an object of approximately 35°C such as a human moves. When actually preparing application circuits, make sure to design them to satisfy the electrical characteristics.

Table 1.1 lists the peripheral functions used and applications.

Table 1.1 Peripheral Functions and Applications

Peripheral Function	Application
Timer array unit	PWM output for fan control
Interrupt function	Continuous operation mode/human sensor mode changeover, human sensor
P54	Signal output to heater control circuit
8-bit interval timer	Time measurement (5 minutes, 4 hours)

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G11（R5F1058A）
Operating frequencies	● High-speed on-chip oscillator clock (f_{HOCO})：24MHz ● CPU/peripheral hardware clock (f_{CLK})： 24MHz/48MHz
Operating voltage	5.0V（operation possible from 2.7 V to 5.5 V） LVD operation(V_{LVD})：Reset mode TYP. 2.75 V At the rising edge 2.76 V to 2.87 V At the falling edge 2.70 V to 2.81 V
Integrated development environment(CS+)	CS+ for CC V7.00.00 from Renesas Electronics Corp.
C compiler(CS+)	CC-RL V1.07.00 from Renesas Electronics Corp.
Integrated development environment(e^2studio)	e2studio V7.2.0 from Renesas Electronics Corp.
C compiler(e^2studio)	CC-RL V1.07.00 from Renesas Electronics Corp.
RL78/G11 code library	RL78/G11 code library V1.02.02.04 from Renesas Electronics Corp.

3. Related application notes

Application notes related to this document are shown below. Please refer to these as needed.

4. Hardware Explanation

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used in this application note.

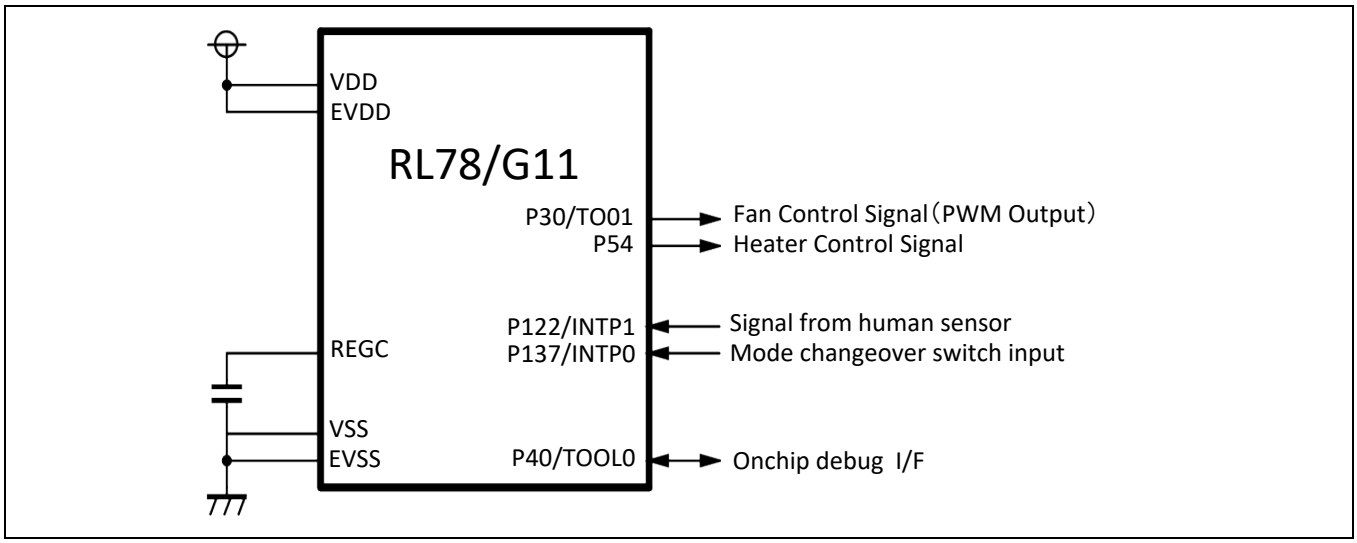

Figure 4.1 Hardware Configuration

Note: 1. This simplified circuit diagram was created to show an overview of connections only.
When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.
(Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

4.2 Used Pin List

Table 4.1 provides a list of pins and functions.

Table 4.1 List of Pins and Functions

Pin Name	Input/Output	Function
P30/TO01	Output	PWM output for fan control
P54	Output	Signal output to heater control circuit
P137/INTP0	Input	Continuous operation mode/human sensor mode changeover
P122/INTP1	Input	Signal input from human sensor

5. Software Explanation

5.1 Operation Outline

This section describes the sample code attached to this application note.

1. Initial settings
   - Initial setting for the ports
   - Initial setting for the clocks
   - Initial setting for the timer array units
   - Initial setting for the 8-bit interval timer

2. After completion of the initial settings, the system operates in continuous operation mode. The PWM signal is output from P30/TO01 (50% duty ratio). A high-level signal is output from P54. The 8-bit interval timer is started to count four hours. When four hours pass, PWM output is stopped and a low-level signal is output from P54. The system then enters human sensor mode and then STOP mode, and waits for the interrupt signal from the human sensor.

3. In continuous operation mode, on detecting that the mode changeover switch (P137) is pressed down, the count operation of the 8-bit interval timer is stopped. From detection of the falling edge of the input signal from the human sensor till detection of the rising edge, the PWM signal is output from P30/TO01 and a high-level signal is output from P54. On detecting the rising edge of the input signal from the human sensor, the count operation of the 8-bit interval timer is started, and five minutes later PWM output is stopped and a low-level signal is output from P54.

4. On detecting that the mode changeover switch (P137) is pressed down in human sensor mode, the system returns to continuous operation mode described in step 2.

5.2 Option Byte Settings

Table5.1 lists the option byte settings.

Table 5.1 Option Byte Settings

Address	Setting Value	Contents
000C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H	01111111B	LVD operation(V_{LVD}) : Reset mode TYP. 2.75 V At the rising edge 2.76 V to 2.87 V At the falling edge 2.70 V to 2.81 V
000C2H	11100000B	HS mode HOCO : 24 MHz
000C3H	10000100B	On-chip debugging enabled

5.3 Constants

Table 5.2 lists the constants used in the sample code.

Table 5.2 Constants Used in the Sample Code

定数名	設定値	内容
―	―	―

5.4 Variables

Table 5.3 lists the global variables.

Table 5.3 Variables

Type	Variable Name	Contents	Function Used
uint8_t	g_cycle	Operation mode parameter	main(), r_it8bit0_channel0_interrupt(), r_intc0_interrupt()
uint8_t	counter	Variable for time measurement	main(), r_it8bit0_channel0_interrupt(), r_intc0_interrupt()

5.5 Functions

Table 5.4 lists the functions.

Table 5.4 Functions

Function Name	Outline
R_MAIN_UserInit	Starts each function.
R_TAU0_Channel0_Start	Starts timer array unit 0 operation.
R_IT8Bit0_Channel0_Start	Starts 8-bit interval timer operation.
R_INTC0_Start	Starts INTP0 interrupt operation.
r_intc0_interrupt	Processes INTP0 interrupt.
R_IT_Start	Starts 12-bit interval timer operation.
R_IT8Bit0_Channel0_Stop	Stops 8-bit interval timer operation.
R_INTC1_Start	Starts INTP1 interrupt operation.
R_IT_Stop	Stops 12-bit interval timer operation.
r_intc1_interrupt	Processes INTP1 interrupt.
r_it8bit0_channel0_interrupt	Processes 8-bit interval timer interrupt.
R_TAU0_Channel0_Stop	Stops timer array unit 0 operation.

5.6 Function Specifications

The following tables list the sample code function specifications.

R_MAIN_UserInit

Outline	Initializes each function to use.	
Header	r_cg_macrodriver.h, r_cg_userdefine.h	
Declaration	void R_ MAIN_UserInit (void);	
Description	Initializes the variables.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_TAU0_Channel0_Start

Outline	Starts timer array unit 0 operation.	
Header	r_cg_tau.h	
Declaration	void R_TAU0_Channel0_Start (void)	
Description	Starts timer array unit 0 operation.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_IT8Bit0_Channel0_Start

Outline	Starts 8-bit interval timer operation.	
Header	r_cg_it8bit.h	
Declaration	void R_IT8Bit0_Channel0_Start (void)	
Description	Starts 8-bit interval timer operation.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_INTC0_Start

Outline	Starts INTP0 operation.	
Header	r_cg_intp.h	
Declaration	void R_INTC0_Start(void);	
Description	Clears the INTP0 interrupt flag and cancels the interrupt mask.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_intc0_interrupt

Outline	Processes INTP0 interrupt.	
Header	r_cg_intp.h	
Declaration	static void __near r_intc0_interrupt(void);	
Description	Removes switch chattering and changes over modes.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_IT_Start

Outline	Starts 12-bit interval timer operation.	
Header	r_cg_it.h	
Declaration	void R_IT_Start(void)	
Description	Starts 12-bit interval timer operation.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_IT8Bit0_Channel0_Stop

Outline	Stops 8-bit interval timer operation.	
Header	r_cg_it8bit.h	
Declaration	void R_IT8Bit0_Channel0_Stop (void)	
Description	Stops 8-bit interval timer operation.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_INTC1_Start

Outline	Starts INTP1 operation.	
Header	r_cg_intp.h	
Declaration	void R_INTC1_Start(void);	
Description	Clears the INTP1 interrupt flag and cancels the interrupt mask.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_IT_Stop

Outline	Stops 12-bit interval timer operation.	
Header	r_cg_it.h	
Declaration	void R_IT_Start(void)	
Description	Stops 12-bit interval timer operation.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_intc1_interrupt

Outline	Processes INTP1 interrupt.	
Header	r_cg_intp.h	
Declaration	static void __near r_intc1_interrupt(void);	
Description	Processes the human sensor interrupt.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_it8bit0_channel0_interrupt

Outline	Processes 8-bit interval timer interrupt.8	
Header	r_cg_it8bit.h	
Declaration	static void __near r_it8bit0_channel0_interrupt (void);	
Description	Processes the human sensor interrupt.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_TAU0_Channel0_Stop

Outline	Stops timer array unit 0 operation.	
Header	r_cg_tau.h	
Declaration	void R_TAU0_Channel0_Stop (void)	
Description	Stops timer array unit 0 operation.	
Arguments	None	None
Return Value	None	
Remarks	None	

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample code.

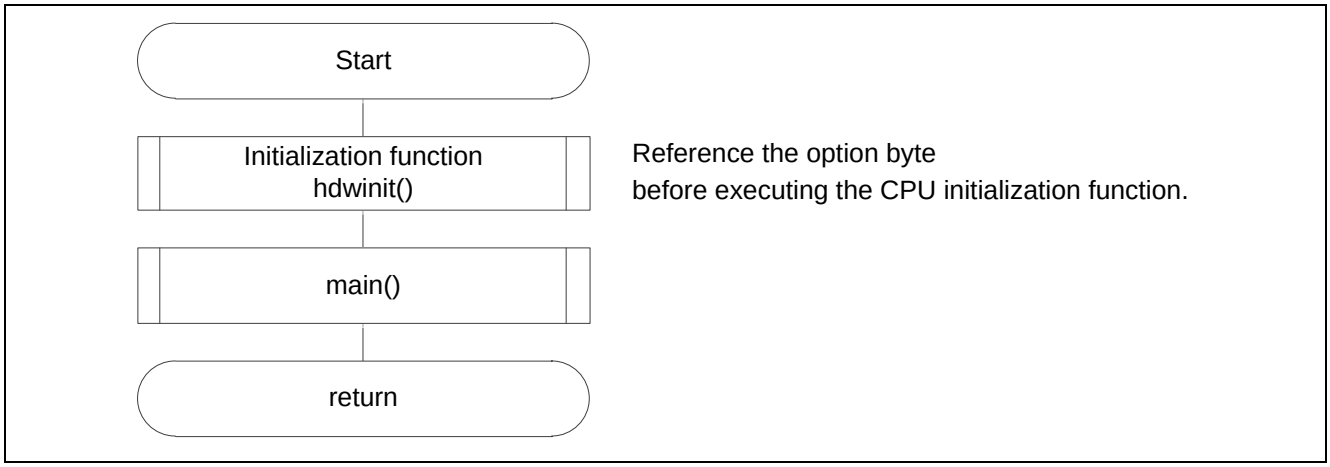

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

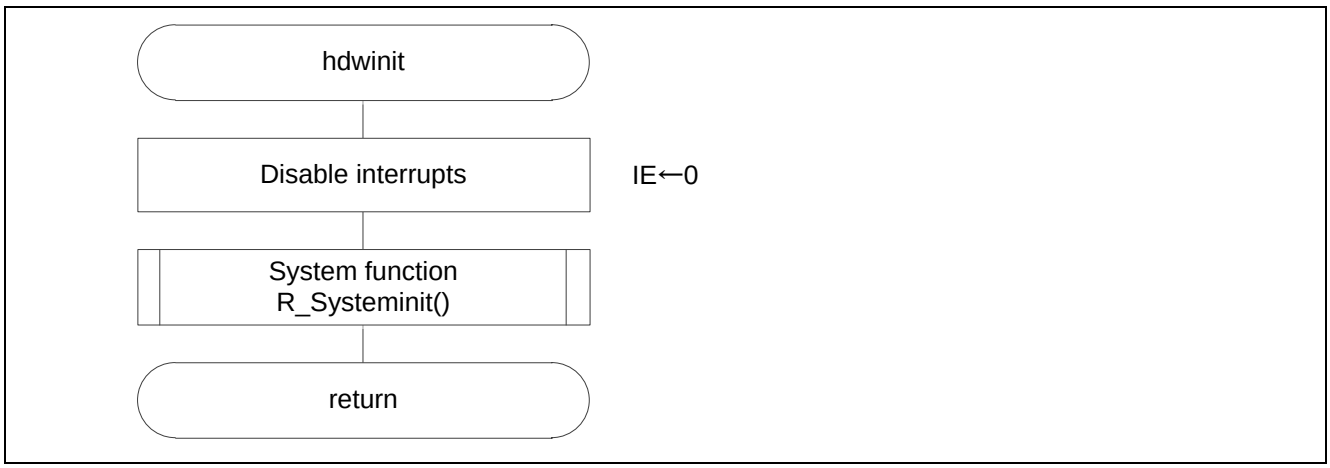

Figure 5.2 Initialization Function

5.7.2 System Function

Figure 5.3 shows the flowchart for system function

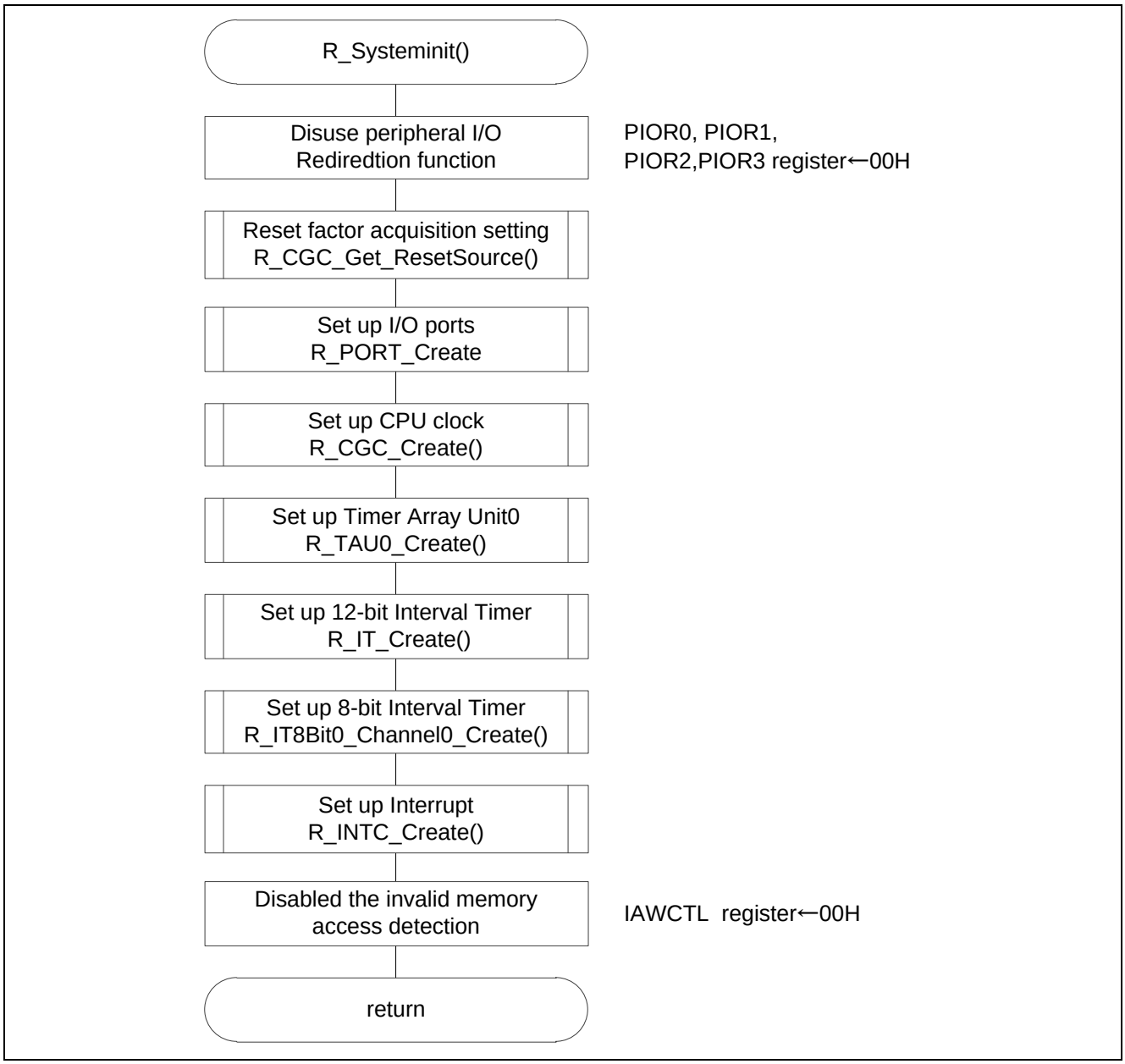

Figure 5.3 System Function

5.7.3 Acquisition of reset factor

Figure 5.4 shows the flowchart for the acquisition of reset factor.

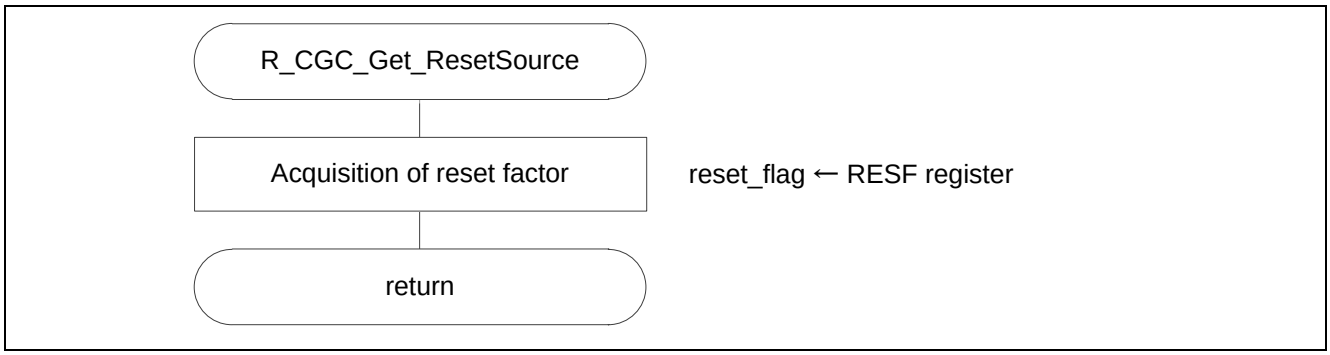

Figure 5.4 Acquisition of reset factor

5.7.4 Input/Output Port Settings

Figure 5.5 shows the flowchart for the input/output port settings.

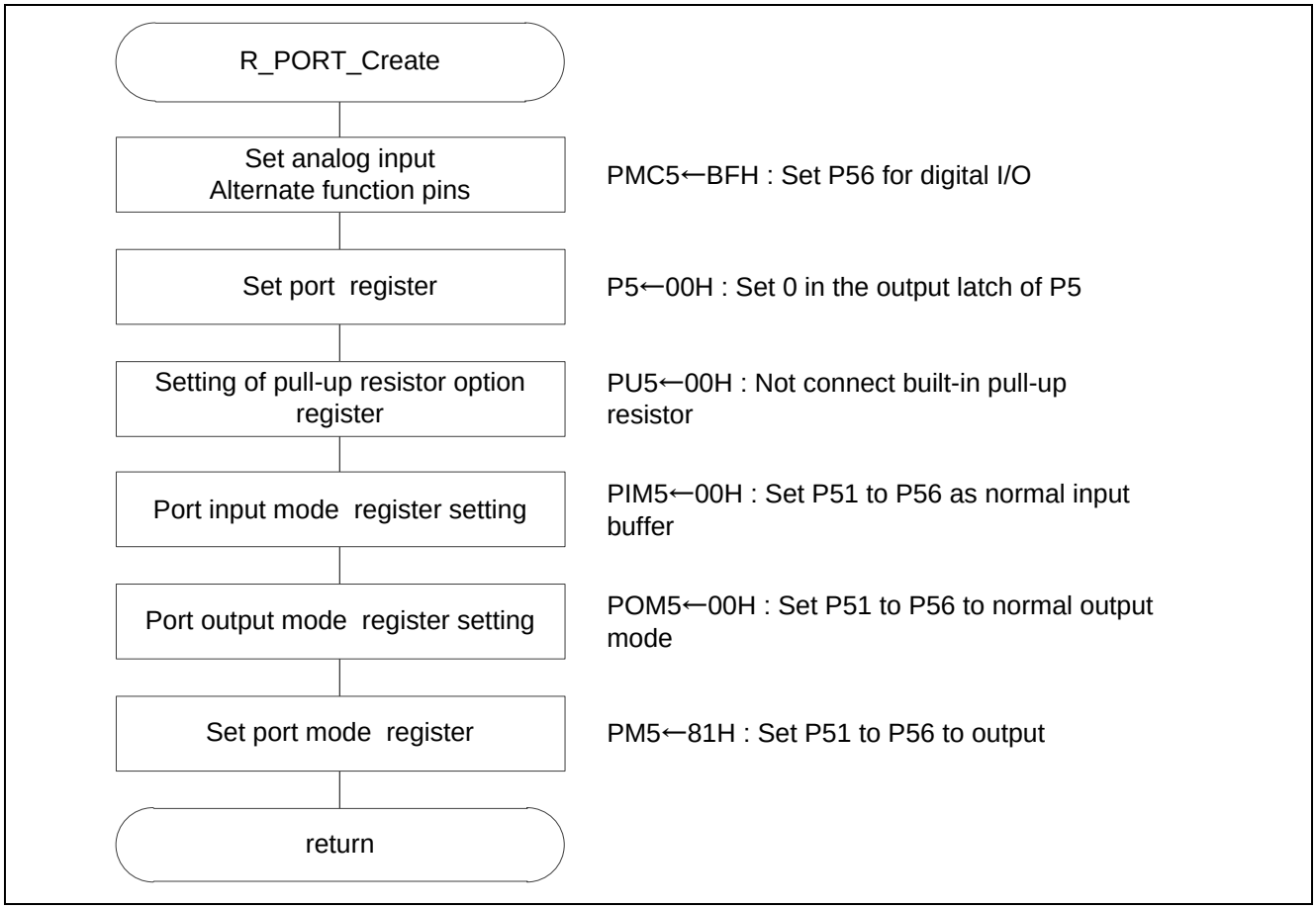

Figure 5.5 Input/Output Port Settings

Note: Refer to the initialization flowchart in the RL78/G13 Initialization (R01AN2575J) Application Note for details on how to set unused ports.

Caution: When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met. Also make sure each unused input-only port is connected to V_{DD} or V_{SS} through a resister.

5.7.5 Clock Generator Setting

Figure 5.6 shows the flowchart for setting the clock generator.

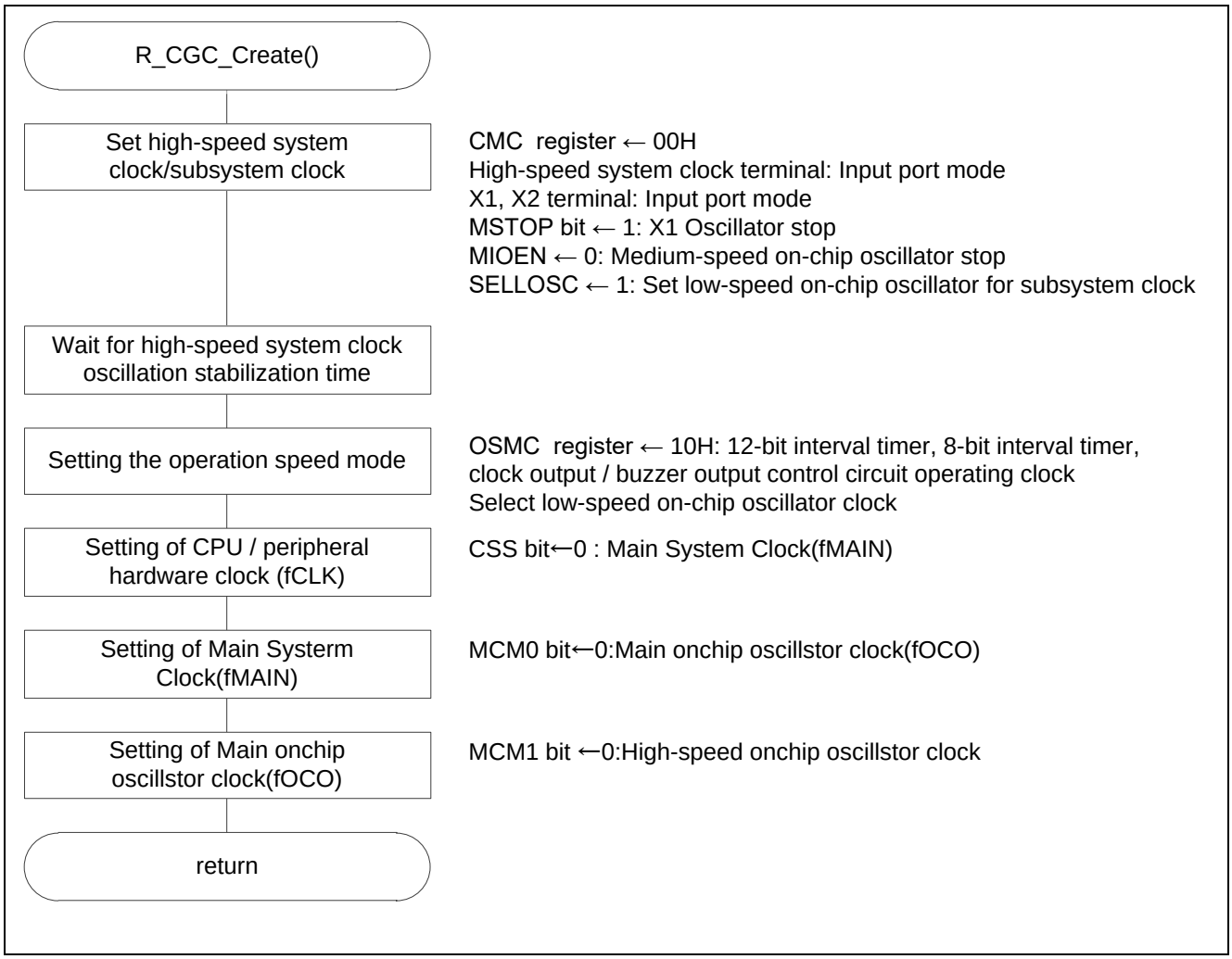

Figure 5.6 Clock Generator Setting

Setting clock operation mode

- Clock operation mode control register (CMC)

High-speed system clock pin operation mode: Input port mode

Symbol：CMC

7	6	5	4	3	2	1	0
EXCLK	OSCSEL	0	0	0	0	0	AMPH
0	**0**	0	0	0	0	0	**0**

Bits 7-6

EXCLK	OSCSEL	High-seed system clock pin operation mode	X1/P121 Port	X2/EXCLK/P122 Port
0	**0**	**Input port mode**	**Input port**	
0	1	**X1 oscillation mode**	**Crystal/ceramic resonator connection**	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Bit 0

AMPH	Control of X1 clock oscillation frequency
0	**1MHz ≦ f_X ≦ 10MHz**
1	10MHz < f_X ≦ 20MHz

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

Controlling clock operation

- Clock operation status control register (CSC)

High-speed system clock operation control: Stop X1 oscillator.

Middle-speed on-chip oscillator clock operation control: Stop middle-speed on-chip oscillator.

High-speed on-chip oscillator clock operation control: Operate high-speed on-chip oscillator.

Symbol：CSC

7	6	5	4	3	2	1	0
MSTOP	1	0	0	0	0	MIOEN	HIOSTOP
1	1	0	0	0	0	**0**	**0**

Bit 7

MSTOP	High-speed system clock operation control		
	X1 oscillation mode	External clock input mode	Input port mode
0	X1 oscillator operating	External clock from EXCLK pin is valid	Input port
1	**X1 oscillator stopped**	**External clock from EXCLK pin is invalid**	

Bit 1

MIOEN	Middle-speed on-chip oscillator clock operation control
0	**Middle-speed on-chip oscillator stopped**
1	Middle-speed on-chip oscillator operating

Bit 0

HIOSTOP	High-speed on-chip oscillator clock operation control
0	**High-speed on-chip oscillator operating**
1	High-speed on-chip oscillator stopped

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

Setting CPU/peripheral hardware clock (f_{CLK})

- System clock control register (CKC)

f_{CLK} status: Main system clock

f_{CLK} selection: Select high-speed on-chip oscillator clock (f_{IH}).

Symbol：CKC

7	6	5	4	3	2	1	0
CLS	CSS	MCS	MCM0	0	0	MCS1	MCM1
0	**0**	**0**	**0**	0	0	**0**	**0**

Bit 7

CLS	Status of CPU/peripheral hardware clock (f_{CLK})
0	**Main system clock (f_{MAIN})**
1	Subsystem clock (f_{SUB})

Bit 6

CSS	Selection of CPU/peripheral hardware clock (f_{CLK})
0	**Main system clock (f_{MAIN})**
1	Subsystem clock (f_{SUB})

Bit 5

MCS	Status of main system clock (f_{MAIN})
0	**High-speed on-chip oscillator clock f_{IH})**
1	High-speed system clock (f_{MX})

Bit 4

MCM0	Main system clock (f_{MAIN}) operation control
0	**Selects high-speed on-chip oscillator clock (f_{IH}) as main system clock (f_{MAIN})**
1	Selects high-speed system clock (f_{MX}) as main system clock (f_{MAIN}).

Bit 1

MCS1	Status of main on-chip oscillator clock (f_{oco})
0	**High-speed on-chip oscillator clock (f_{IH})**
1	Middle-speed on-chip oscillator clock (f_{IM})

Bit 0

MCM1	Main on-chip oscillator clock (f_{oco}) operation control
0	**High-speed on-chip oscillator clock (f_{IH})**
1	Middle-speed on-chip oscillator clock (f_{IM})

Controlling operation speed mode

- Operation speed mode control register (OSMC)

12-bit interval timer operation clock selection: Select low-speed on-chip oscillator clock.

Symbol：OSMC

7	6	5	4	3	2	1	0
0	0	0	WUTMMCK0	0	0	0	0
0	0	0	**1**	0	0	0	0

Bit 4

WUTMMCK0	Selection of operation clock for 12-bit interval timer
0	Do not select low-speed on-chip oscillator clock
1	**Select low-speed on-chip oscillator clock**

Selecting subsystem clock

- Subsystem clock select register (CKSEL)

Subsystem clock selection: Select low-speed on-chip oscillator clock.

Symbol：CKSEL

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SELLOSC
0	0	0	0	0	0	0	**1**

Bit 0

SELLOSC	Selection of low-speed on-chip oscillator clock
0	Do not select low-speed on-chip oscillator clock
1	**Select low-speed on-chip oscillator clock**

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

5.7.6 Setting Timer Array Unit 0

Figure 5.7 shows the flowchart for setting the timer array unit 0.

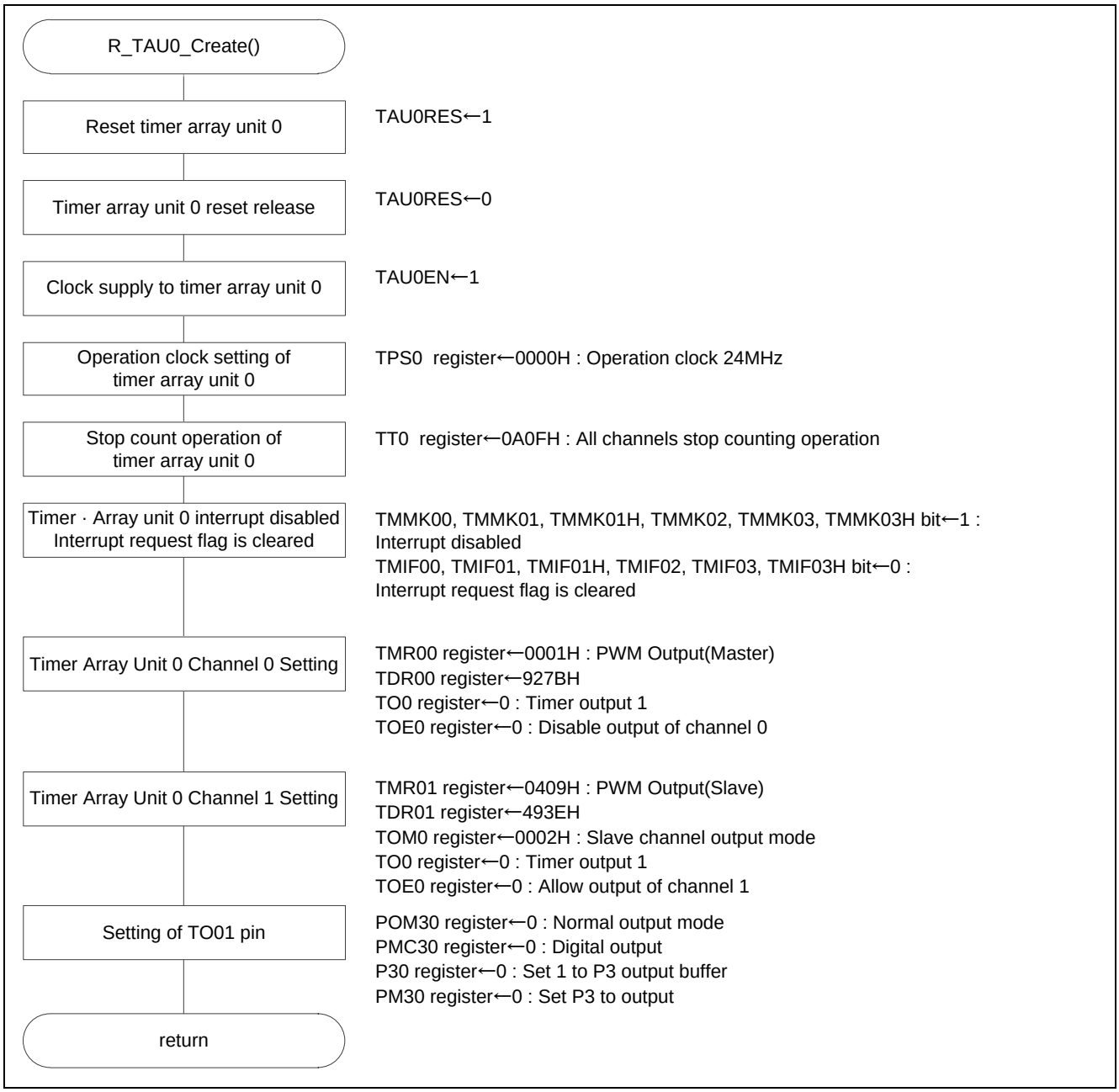

Figure 5.1 Setting Timer Array Unit 0

Controlling timer array unit 0 reset

- Peripheral reset control register 0 (PRR0)

Release the timer array unit 0 from the reset state.

Symbol : PRR0

7	6	5	4	3	2	1	0
0	IICA1RES	ADCRES	IICA0RES	0	SAU0RES	0	TAU0RES
0	x	x	x	0	x	0	**0/1**

Bit 0

TAU0RES	Reset control of timer array unit 0
0	Timer array unit is released from the reset state.
1	Timer array unit is in the reset state.

Starting clock supply to timer array unit 0

- Peripheral enable register 0 (PER0)

Start supplying clock to the timer array unit 0.

Symbol : PER0

7	6	5	4	3	2	1	0
0	IICA1EN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
0	x	x	x	0	x	0	**1**

Bit 0

TAU0EN	Control of timer array 0 unit input clock
0	Stops supply of input clock. • SFR used by the timer array unit 0 cannot be written.
1	**Supplies input clock.** **• SFR used by the timer array unit 0 can be read/written**

Setting timer clock frequency

- Timer clock select register 0 (TPS0)

Select the operation clock for the timer array unit 0.

Symbol：TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS031	PRS030	0	0	PRS021	PRS020	PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
x	x	x	x	x	x	x	x	x	x	x	x	**0**	**0**	**0**	**0**

Bits 3-0

PRS003	PRS002	PRS001	PRS000	Selection of operation clock (CK00)					
					f_{CLK}= 2MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz	f_{CLK}= 24MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	**24 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	313kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156 kHz	313 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

Setting channel 0 operation mode

- Timer mode register 00 (TMR00)

Select the operation clock (f_{MCK}).

Select the count clock.

Set software trigger start.

Set the operation mode.

Symbol：TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 15-14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CKm0 set by timer clock select register m (TPSm)**
0	1	Operation clock CKm2 set by timer clock select register m (TPSm)
1	0	Operation clock CKm1 set by timer clock select register m (TPSm)
1	1	Operation clock CKm3 set by timer clock select register m (TPSm)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits**
1	Valid edge of input signal input from the TImn pin In channels 0 and 1, valid edge of input signal selected by TIS0

Bits 10-8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
1	1	0	INTTMmn of the master channel is used as a start trigger, and the valid edge of the TImp pin input of the slave channel is used as an end trigger (capture trigger).
Other than above			Setting prohibited

Bits 7-6

CIS001	CIS000	Selection of TImn pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

Symbol：TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 3-0

MD 003	MD 002	MD 001	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	**0**	**0**	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		
The operation of each mode varies depending on MDmn0 bit (see table below).					

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD000	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation At that time, interrupt is not generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

Setting interval for PWM (master)

- Timer data register 00 (TDR00)

Set the compare value for PWM (master).

Symbol：TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**1**

Enabling timer output

- Timer output enable register 0 (TOE0)

Enable or disable timer output of each channel.

Symbol：TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE 07	TOE 06	TOE 05	TOE 04	TOE 03	TOE 02	TOE 01	TOE 00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	**0**

Bit 1

TOE01	Timer output enable/disable of channel 0
0	Timer output is disabled. Timer operation is not applied to the TOmn bit and the output is fixed. Writing to the TOmn bit is enabled and the level set in the TOmn bit is output from the TOmn pin.
1	Timer output is enabled. Timer operation is applied to the TOmn bit and an output waveform is generated. Writing to the TOmn bit is ignored.

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

Setting channel 1 operation mode

- Timer mode register 01 (TMR01)

Select the operating clock (f_{MCK}).

Select the count clock.

Set software trigger start.

Set the operation mode.

Symbol：TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 15-14

CKS001	CKS000	Selection of operation clock (fMCK) of channel 1
0	**0**	Operation clock CKm0 set by timer clock select register m (TPSm)
0	1	Operation clock CKm2 set by timer clock select register m (TPSm)
1	0	Operation clock CKm1 set by timer clock select register m (TPSm)
1	1	Operation clock CKm3 set by timer clock select register m (TPSm)

Bit 12

CCS00	Selection of count clock (fTCLK) of channel 1
0	Operation clock (fMCK) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin

Bits 10-8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 1
0	**0**	**0**	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7-6

CIS001	CIS000	Selection of TImn pin input valid edge
0	**0**	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Start trigger: Falling edge, Capture trigger: Rising edge

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

Symbol : TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bit 3-0

MD 003	MD 002	MD 001	Operation mode of channel 1	Corresponding function	Count operation of TCR
0	0	0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	**0**	**0**	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above			Setting prohibited		
The operation of each mode varies depending on MDmn0 bit (see table below).					

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD000	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation At that time, interrupt is not generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

Setting interval for PWM (slave)

- Timer data register 01 (TDR01)

Set the compare value for PWM (slave).

Symbol：TDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**0**

Enabling timer output

- Timer output enable register 0 (TOE0)

Enable or disable timer output of each channel.

Symbol：TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	**0**

Bit 1

TOE01	Timer output enable/disable of channel 1
0	Timer output is disabled. Timer operation is not applied to the TOmn bit and the output is fixed. Writing to the TOmn bit is enabled and the level set in the TOmn bit is output from the TOmn pin.
1	Timer output is enabled. Timer operation is applied to the TOmn bit and an output waveform is generated. Writing to the TOmn bit is ignored.

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

5.7.7 Setting 12-Bit Interval Timer

Figure 5.8 shows the flowchart for setting the 12-bit interval timer.

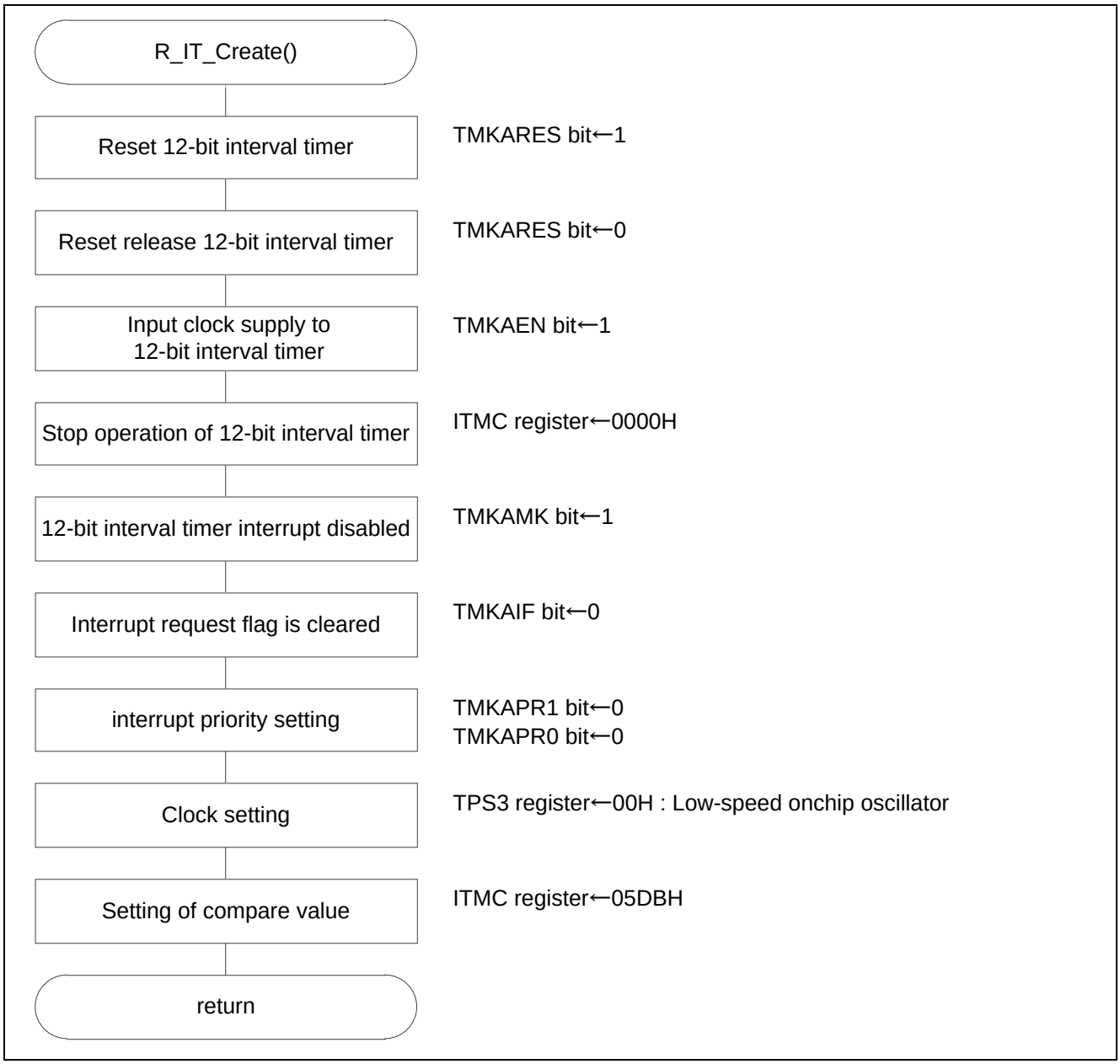

Figure 5.2 Setting 12-Bit Interval Timer

Controlling 12-bit interval timer reset

- Peripheral reset control register 2 (PRR2)

Release the 12-bit interval timer from the reset state.

Symbol：PRR2

7	6	5	4	3	2	1	0
TMKARES	0	DOCRES	0	0	0	0	TKB0RES
0/1	x	0	x	x	x	x	0

Enabling clock supply to 12-bit interval timer

- Peripheral enable register 2 (PER2)

Enable clock supply to the 12-bit interval timer.

Symbol：PER2

7	6	5	4	3	2	1	0
TMKAEN	0	DOCEN	0	0	0	0	TKB0EN
1	0	x	0	0	0	0	x

Bit 7

TMKAEN	Control of 12-bit interval timer input clock supply
0	Stops input clock supply. • SFR used by the 12-bit interval timer cannot be written. The read value is 0H. However, the SFR is not initialized.
1	Enables input clock supply. • SFR used by the 12-bit interval timer can be read and written.

Setting interval signal detection interrupt (INTIT) of 12-bit interval timer

- Interrupt request flag register (IF1H)

Clear the TMKAIF interrupt source flag.

- Interrupt mask flag register (MK1H)

Set the TMKAMK interrupt mask.

Symbol：IF1H

7	6	5	4	3	2	1	0
PIF11	PIF10	PIF9	PIF8	PIF7	KRIF	TMKAIF	ADIF
x	x	x	x	x	x	**0**	x

Bit 1

TMKAIF	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

Symbol：MK1H

7	6	5	4	3	2	1	0
PMK11	PMK10	PMK9	PMK8	PMK7	KRMK	TMKAMK	ADMK
x	x	x	x	x	x	**0**	x

Bit 1

TMKAMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Setting 12-bit interval timer count operation

- Interval timer control register (ITMC)

Clear the ITIF interrupt source flag.

Symbol：ITMC

15	14	13	2	11-0
RINTE	0	0	0	ITCMP11-ITCMP0
0	0	0	0	**05DBH**

Bit 15

RINTE	12-bit interval timer operation control
0	Count operation stopped (count clear)
1	Count operation started

Bits 11-0

ITCMP11-ITCMP0	Specification of the 12-bit interval timer compare value
0095H	These bits generate a fixed-cycle interrupt (count clock cycles x (ITCMP setting + 1)).
000H	Setting prohibit

Note: Refer to the RL78/G11 User's Manual (Hardware version) for details on how to set registers.

5.7.8 Setting 8-Bit Interval Timer

Figure 5.9 shows the flowchart for setting the 8-bit interval timer.

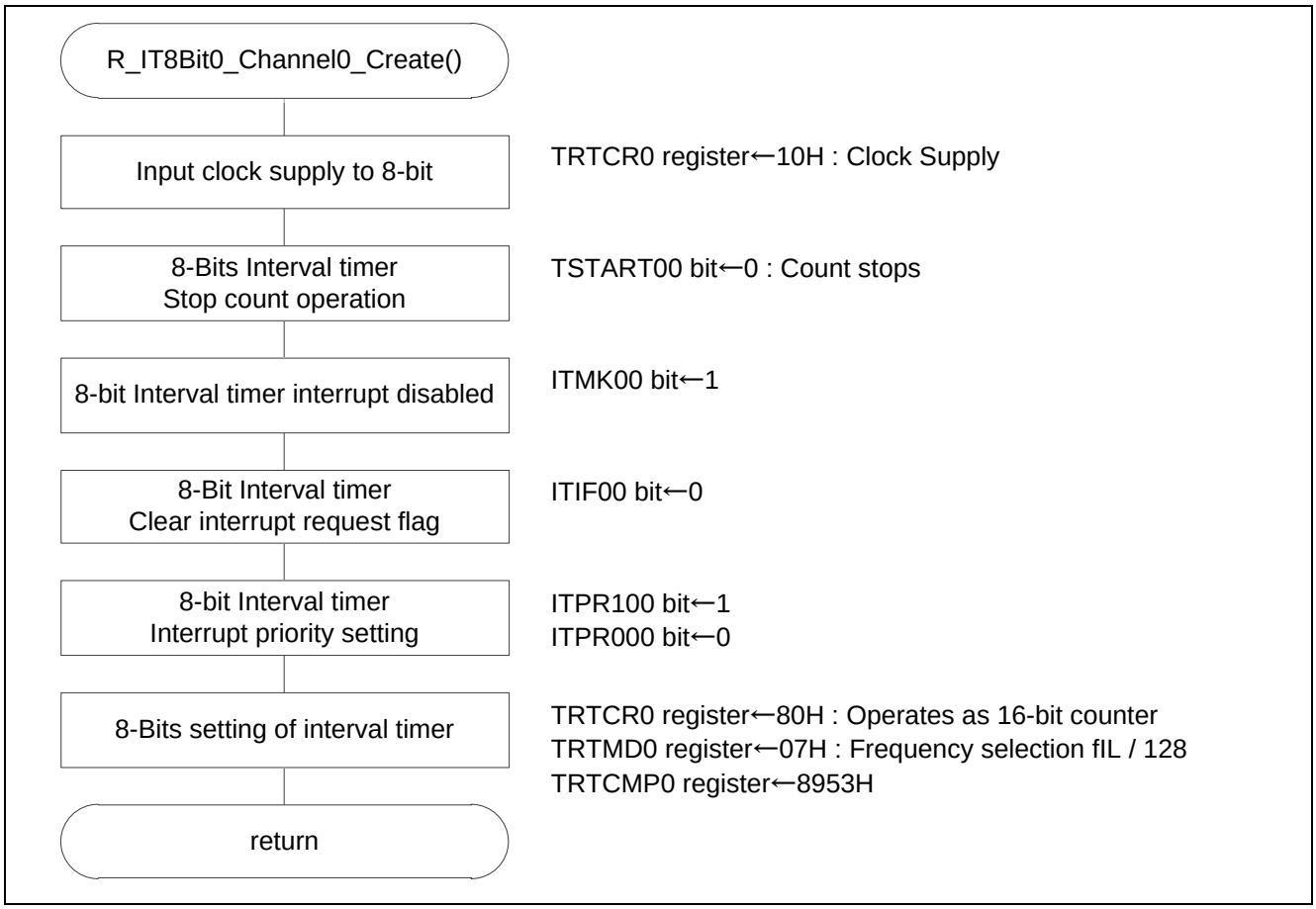

Figure 5.3 Setting 8-Bit Interval Timer

Setting 8-bit interval timer

- 8-bit interval timer control register 0

Enable clock supply to the 8-bit interval timer.

Mode select: Operate as 16-bit counter.

Symbol：TRTCR0

7	6	5	4	3	2	1	0
TCSMD0	0	0	TCLKENn	0	TSTART01	0	TSTART00
1	0	0	**1**	0	0	0	**1**

Bit 7

TCSMD0	Mode select
0	Operates as 8-bit counter
1	**Operates as 16-bit counter (channel 0 and channel 1 are connected)**

Bit 4

TCLKENn	8-bit interval timer clock enable
0	Clock is stopped
1	**Clock is supplied**

Bit 0

TSTART00	8-bit interval timer 1 count start
0	Count stops
1	**Count starts**

Setting division ratio and compare value for 8-bit interval timer

- 8-bit interval timer division register 0
- 8-bit interval timer compare register 0

Symbol：TRTMD0

7	6	5	4	3	2	1	0
-	TCK01			-	TCK00		
-	0	0	0	-	**1**	**1**	**1**

Bits 2, 1, 0

TCK00			8-bit interval timer 1 division select
2	1	0	
0	0	0	f_{IL}
0	0	1	$f_{IL}/2$
0	1	0	$f_{IL}/4$
0	1	1	$f_{IL}/8$
1	0	0	$f_{IL}/16$
1	0	1	$f_{IL}/32$
1	1	0	$f_{IL}/64$
1	**1**	**1**	$f_{IL}/128$

Symbol：TRTCMP0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**1**

5.7.9 Setting External Interrupts

Figure 5.10 shows the flowchart for setting the external interrupts.

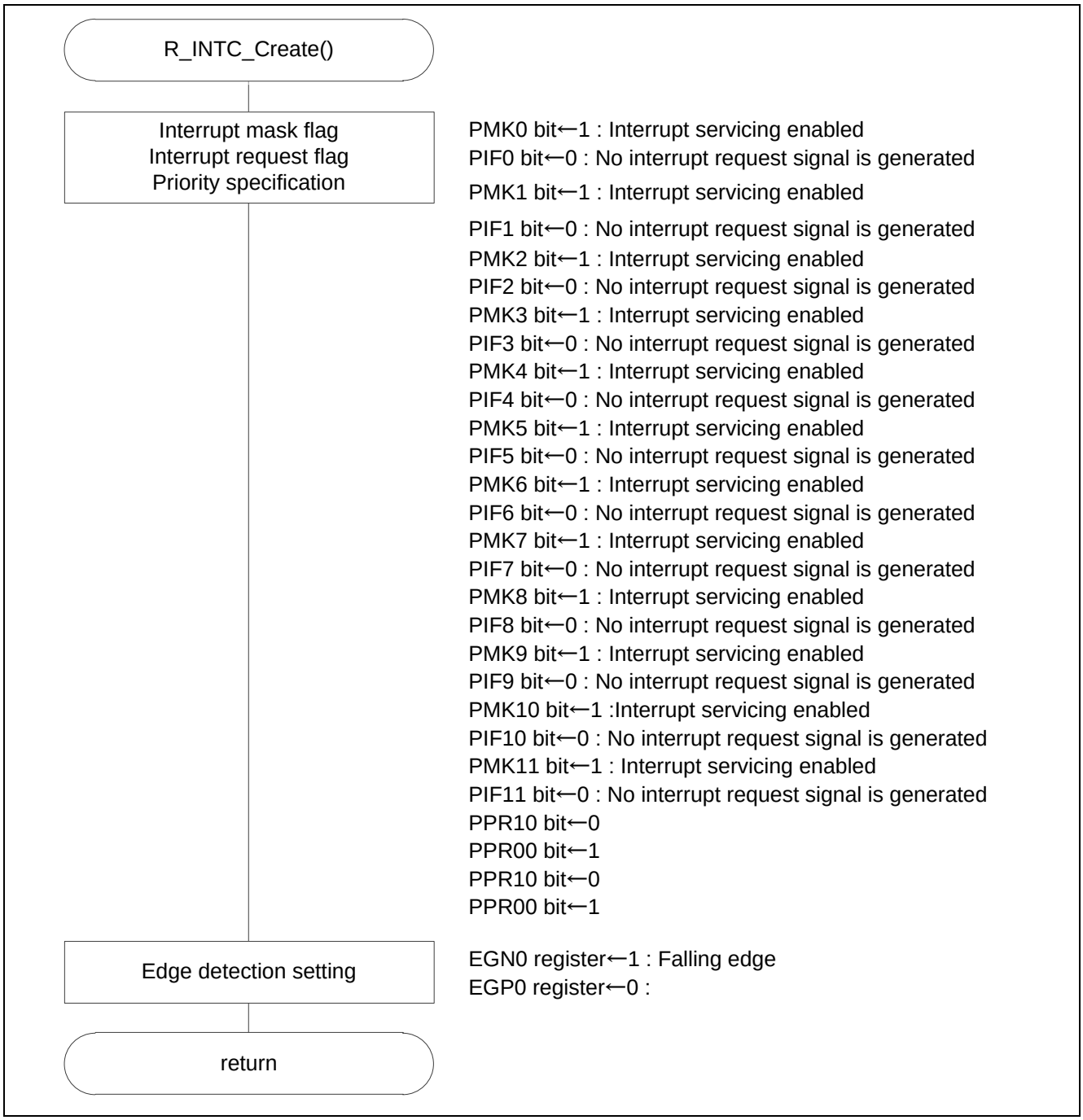

Figure 5.4 Setting External Interrupts

5.7.10 Main Function

Figure 5.11 shows the flowchart of the main function.

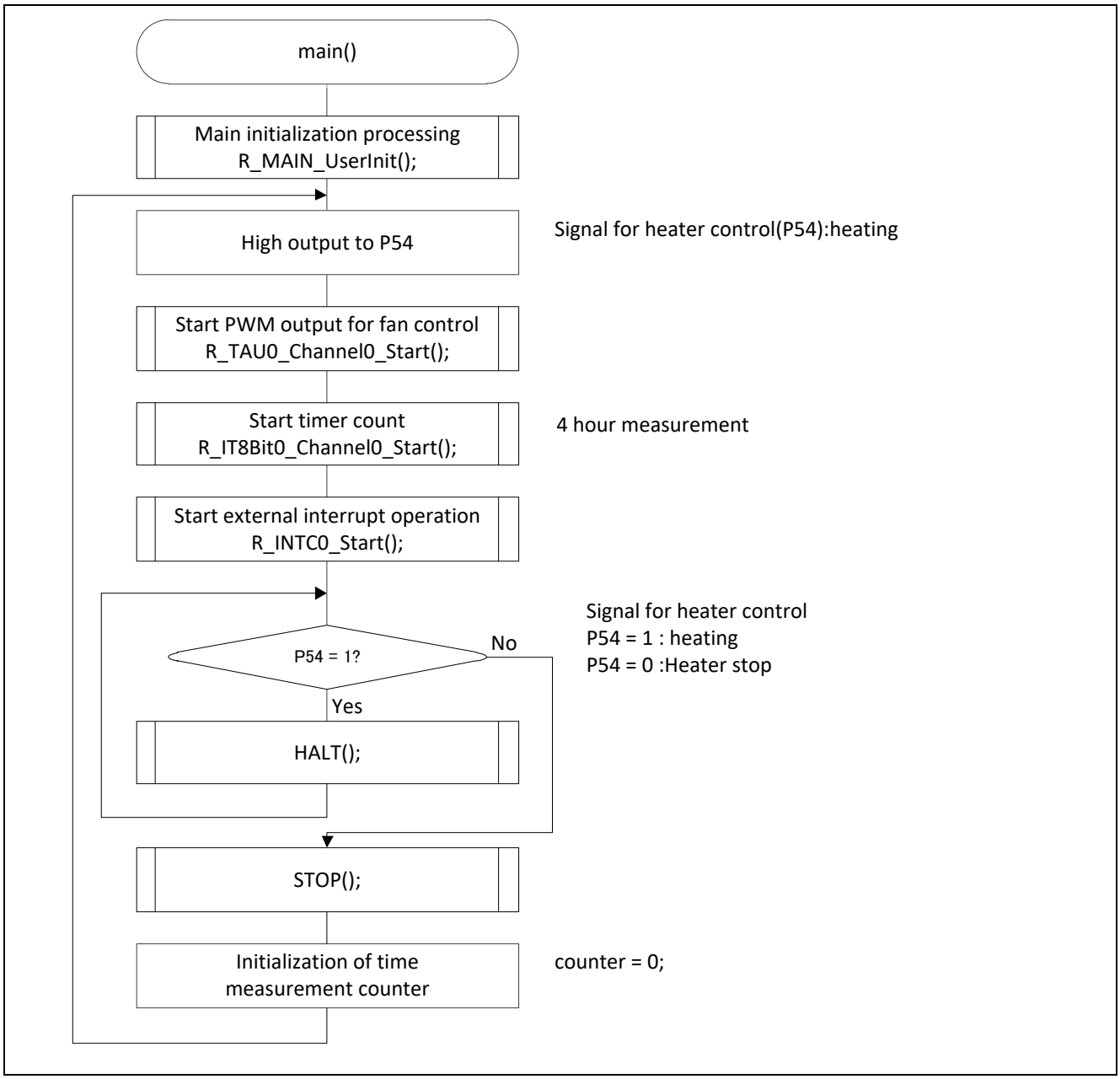

Figure 5.5 Main Function

5.7.11 Main Initialization Setting

Figure 5.12 shows the flowchart for the main initialization settings.

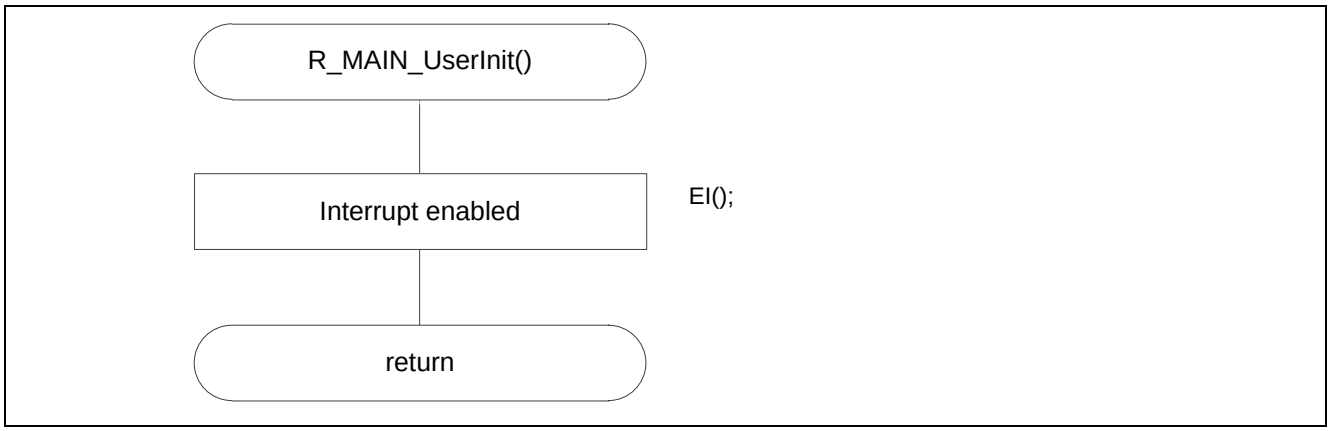

Figure 5.6 Main Initialization Setting

5.7.12 Starting Timer Array Unit 0 Operation

Figure 5.13 shows the flowchart for starting the timer array unit 0 operation.

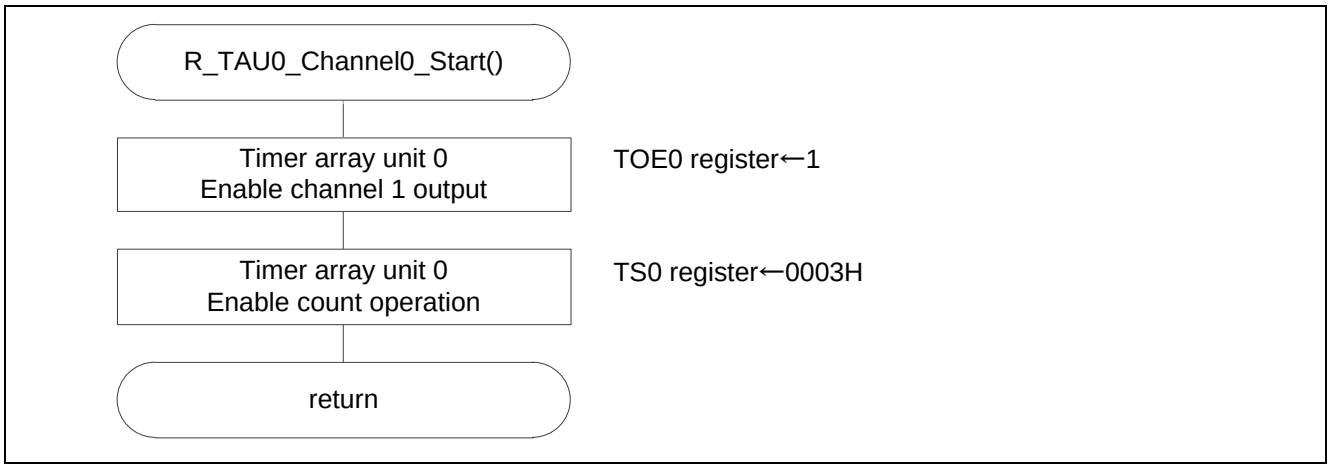

Figure 5.7 Starting Timer Array Unit 0 Operation

5.7.13 Starting 8-Bit Interval Timer Operation

Figure 5.14 shows the flowchart for starting the 8-bit interval timer operation.

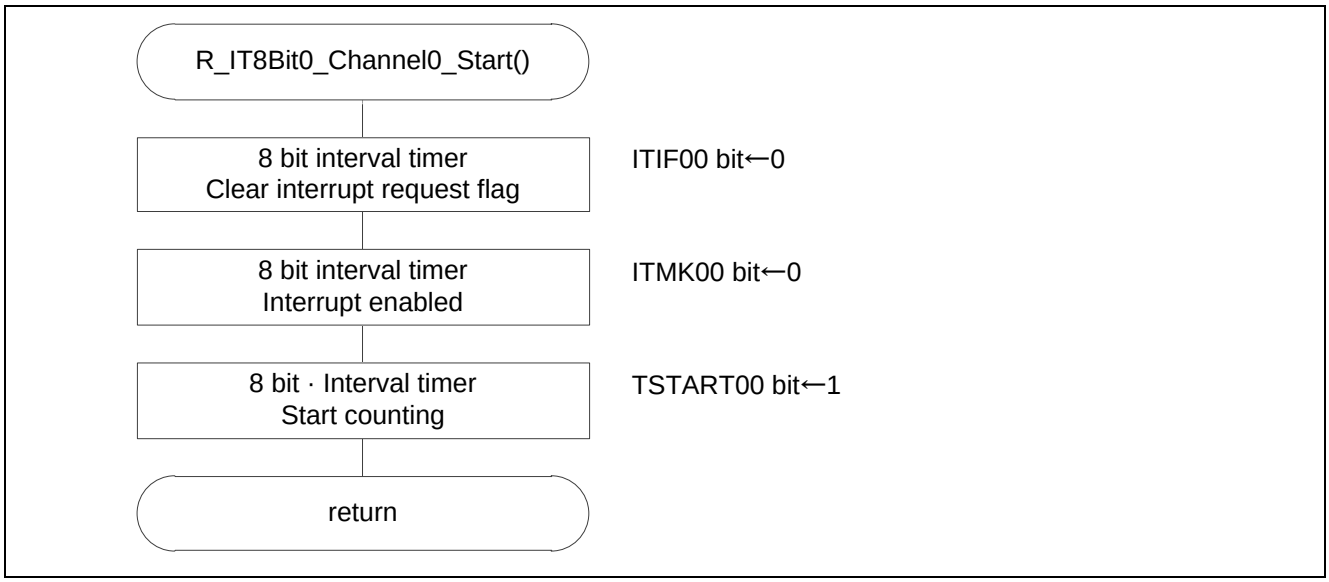

Figure 5.8 Starting 8-Bit Interval Timer Operation

5.7.14 Starting INTP0 Interrupt Operation

Figure 5.15 shows the flowchart for starting the INTP0 interrupt operation.

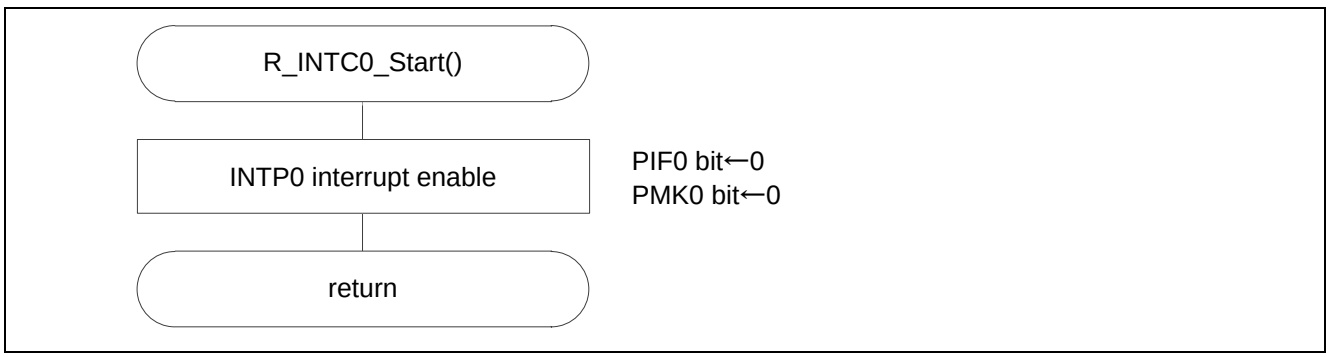

Figure 5.9 Starting INTP0 Interrupt Operation

5.7.15 Processing INTP0 Interrupt

Figure 5.16 shows the flowchart for processing the INTP0 interrupt.

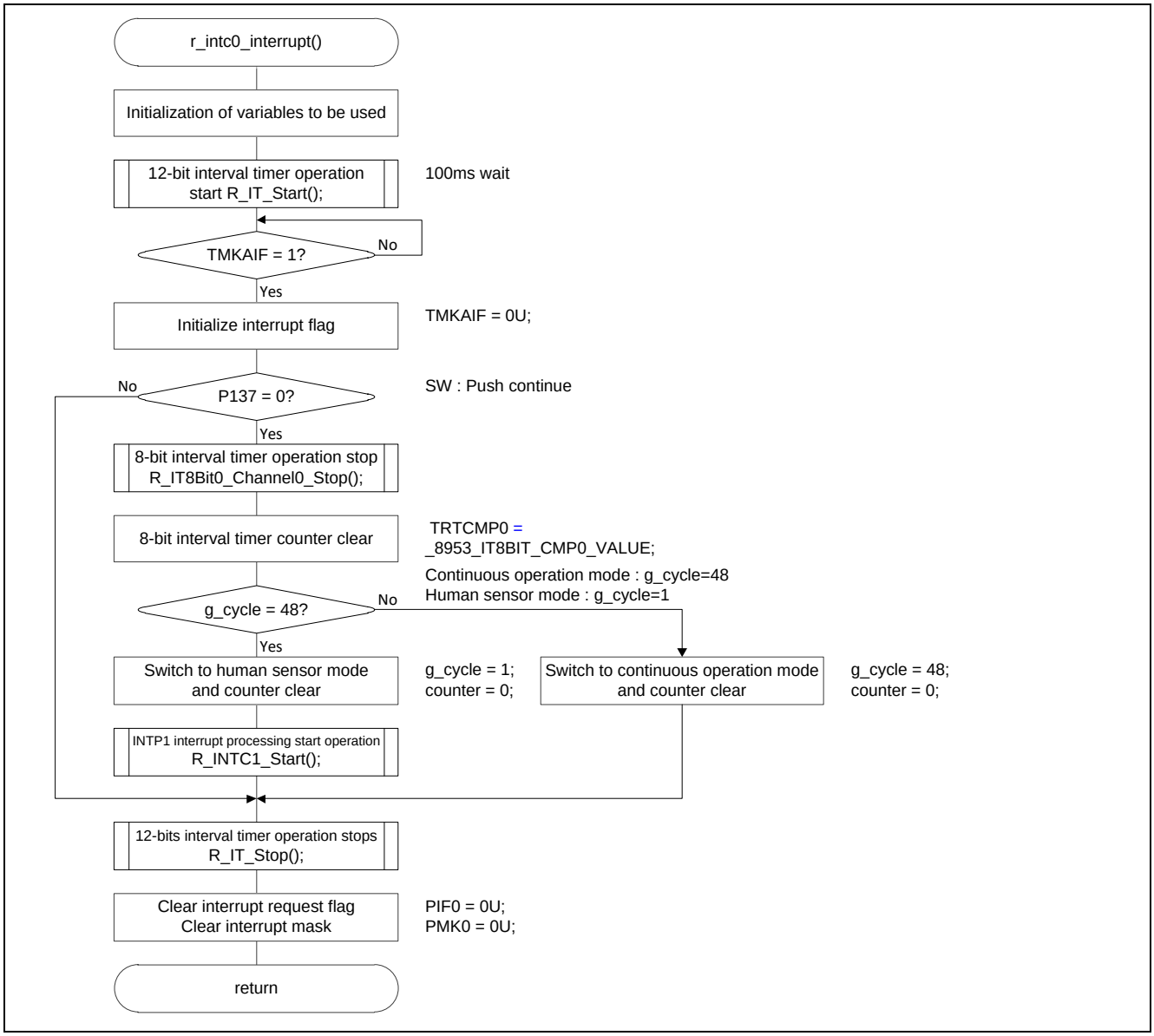

Figure 5.10 Processing INTP0 Interrupt

5.7.16 Starting 12-Bit Interval Timer Operation

Figure 5.17 shows the flowchart for starting the 12-bit interval timer operation.

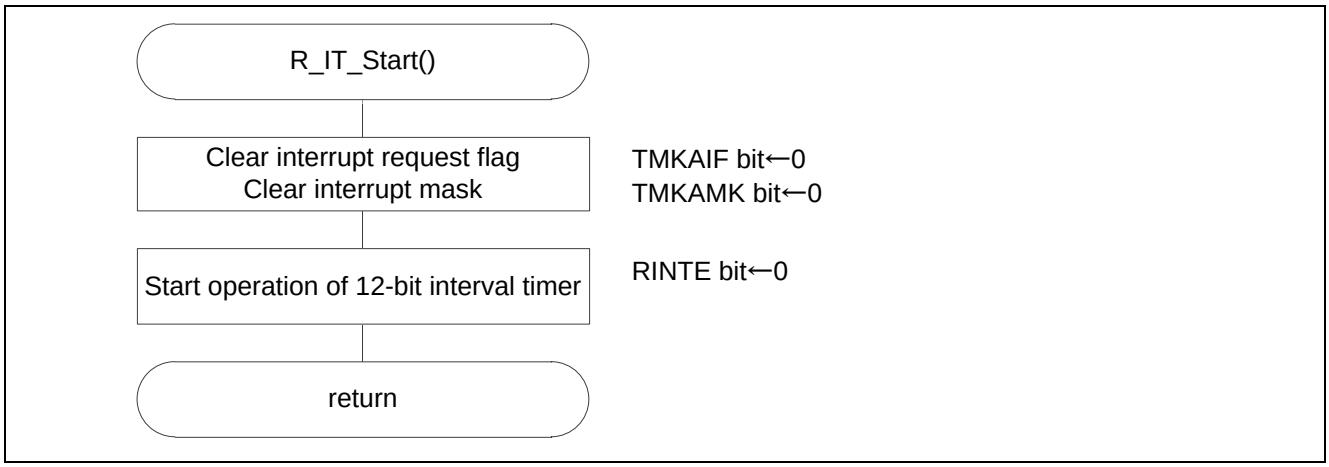

Figure 5.11 Starting 12-Bit Interval Timer Operation

5.7.17 Stopping 8-Bit Interval Timer Operation

Figure 5.18 shows the flowchart for stopping the 8-bit interval timer operation.

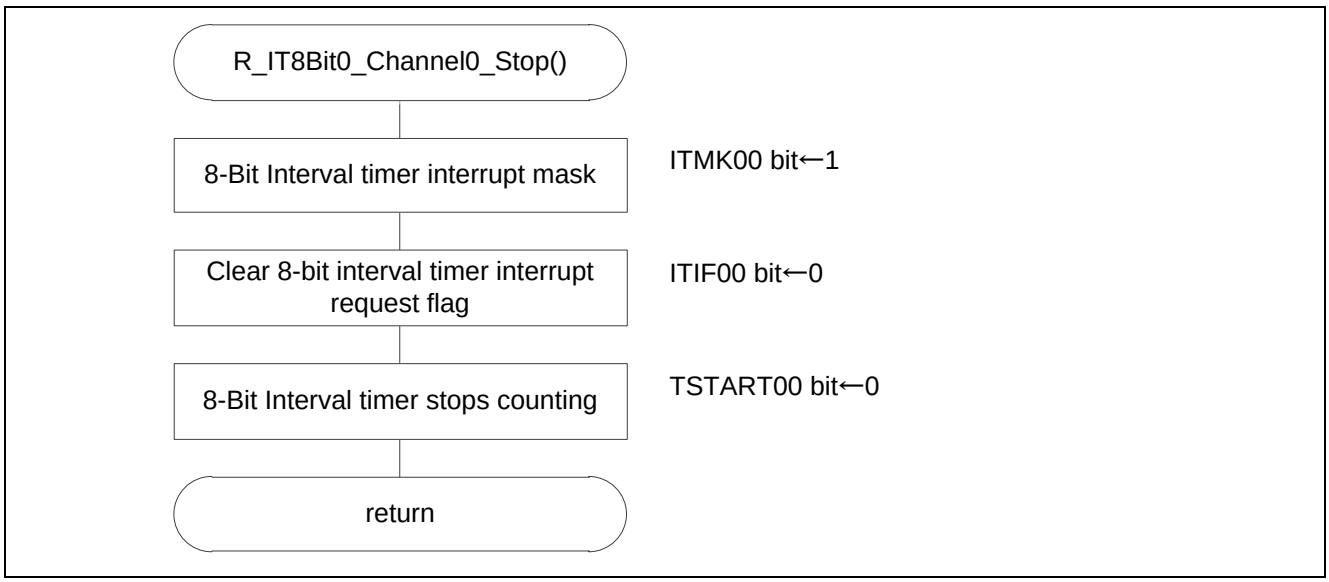

Figure 5.12 Stopping 8-Bit Interval Timer Operation

5.7.18 Starting INTP1 Interrupt Operation

Figure 5.19 shows the flowchart for starting the INTP1 interrupt operation.

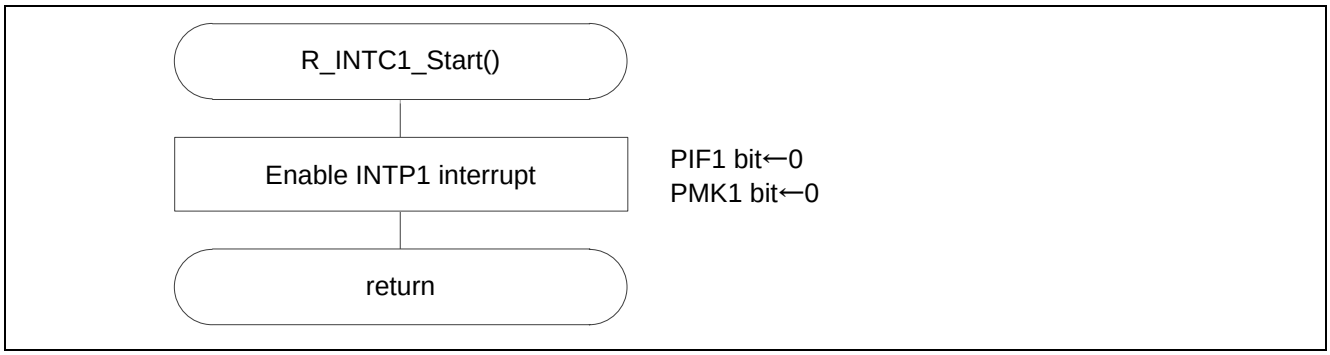

Figure 5.13 Starting INTP1 Interrupt Operation

5.7.19 Stopping 12-Bit Interval Timer Operation

Figure 5.20 shows the flowchart for stopping the 12-bit interval timer operation.

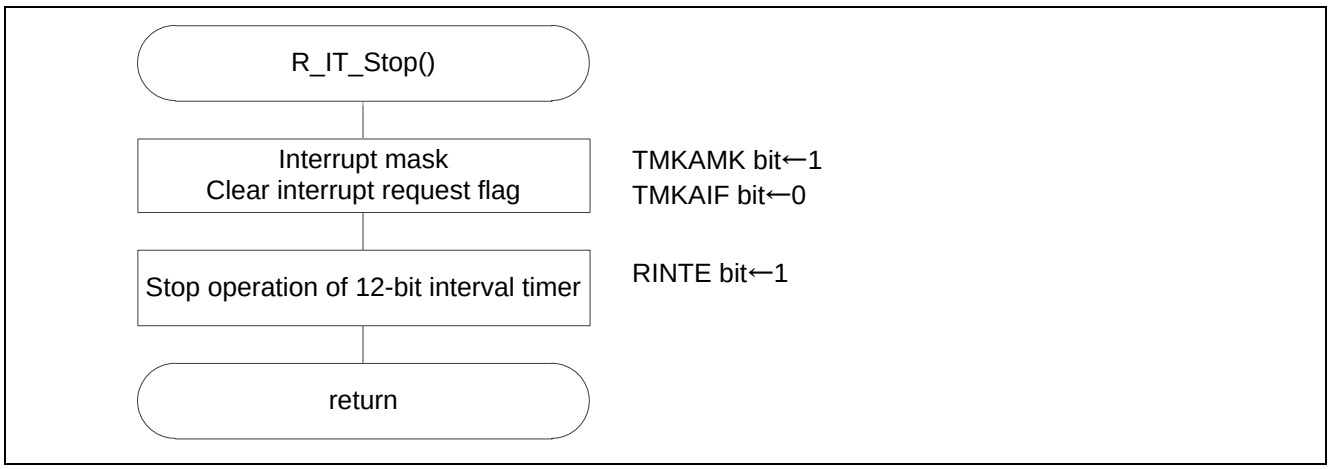

Figure 5.14 Stopping 12-Bit Interval Timer Operation

5.7.20 Processing INTP1 Interrupt

Figure 5.21 shows the flowchart for processing the INTP1 interrupt.

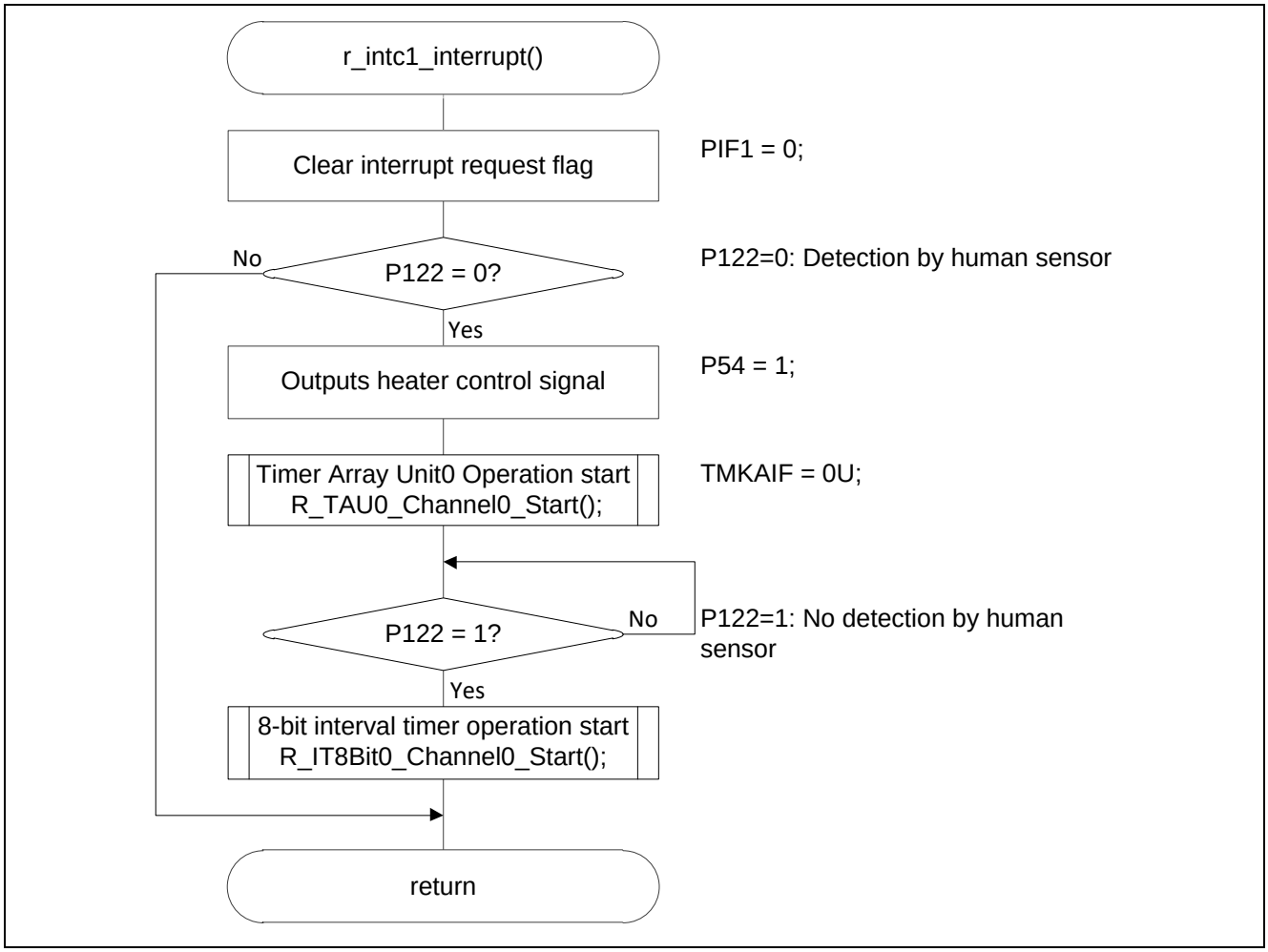

Figure 5.15 Processing INTP1 Interrupt

5.7.21 Processing 8-Bit Interval Timer Interrupt

Figure 5.22 shows the flowchart for processing the 8-bit interval timer interrupt.

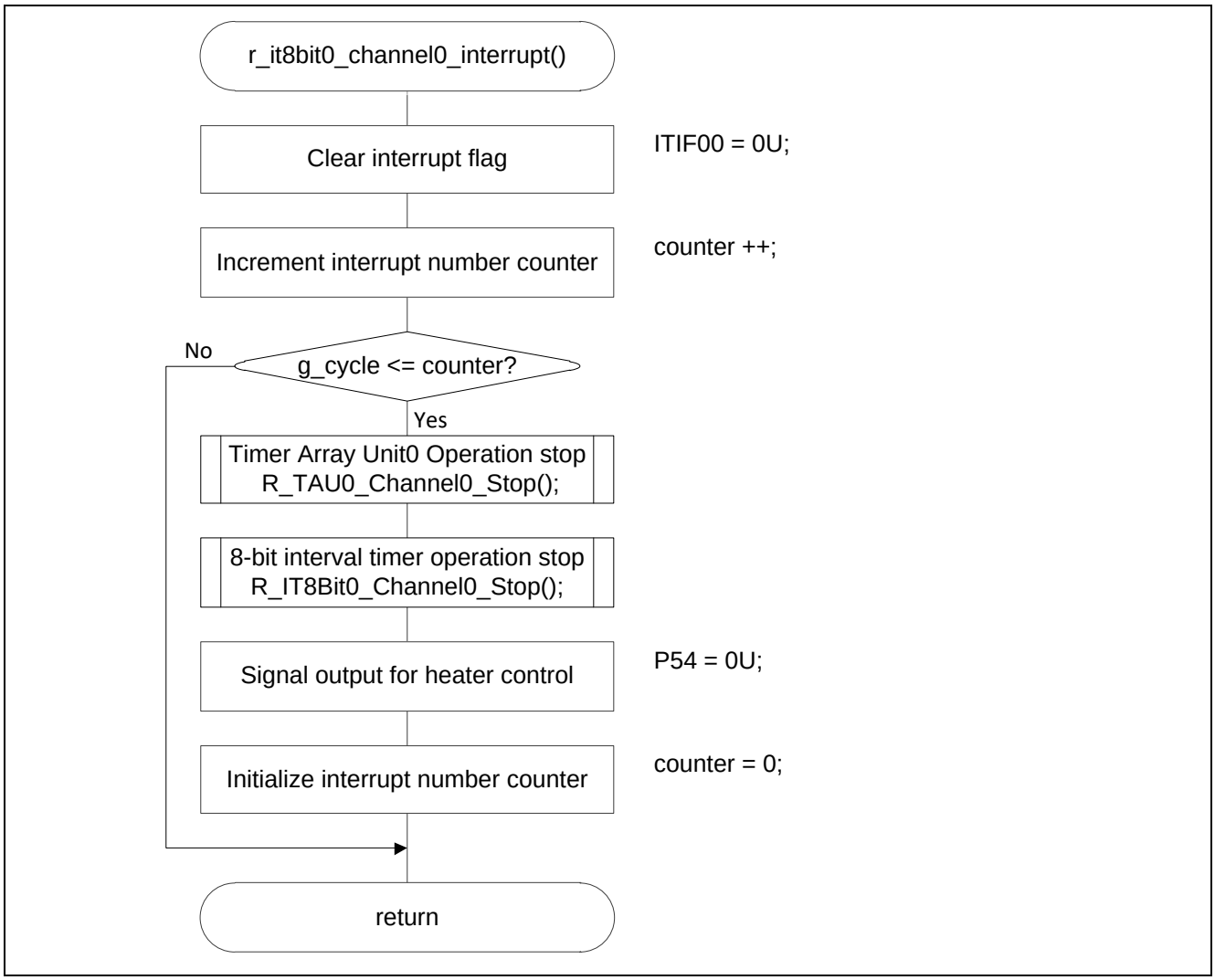

Figure 5.16 Processing 8-Bit Interval Timer Interrupt

5.7.22 Stopping Timer Array Unit 0 Operation

Figure 5.23 shows the flowchart for stopping the timer array unit 0 operation.

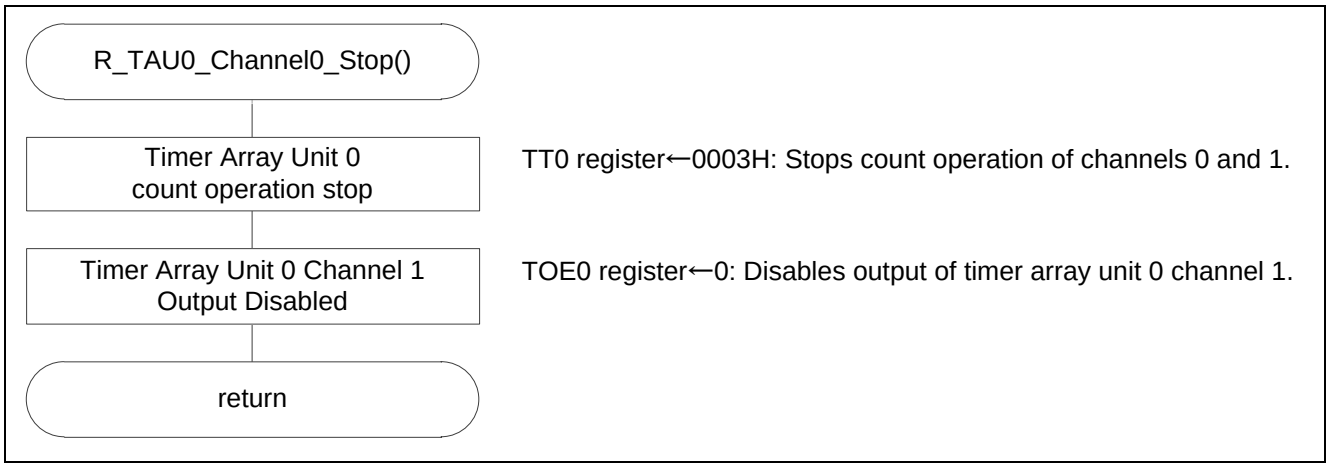

Figure 5.17 Stopping Timer Array Unit 0 Operation

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G11 User's Manual: Hardware (R01UH0637E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics website.)

Technical Updates/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Website and Support

Renesas Electronics Website
https://www.renesas.com/
Inquiries
http://www.renesas.com/contact

REVISION HISTORY	RL78/G11 Ceramic Fan Heater with Human Sensor

Rev.	Date	Description	
		Page	Summary
1.00	Jan.29, 2019	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.