RL78/G10

UART Transmission of A/D Conversion Results Average

Introduction

This application note explains how to perform UART transmission of A/D conversion result average. The A/D conversion of the analog voltage is carried out using the A/D converter of RL78/G10, and the average value of the A/D conversion results is transmitted by UART communication using a serial array unit (SAU).

Target Device

RL78/G10

When applying the sample program covered in this application note to another RL78 microcontroller, conduct an extensive evaluation to use.

Contents

1. Specifications

In this application note, performs the A/D conversion of the analog input voltage of four analog input pins (ANI0 to ANI3), and stores the conversion result in on-chip RAM at the same time.
Waits for the UART communication data 55H (the LSB first and no 8-bit parity) transmitted from the master connected to TI00 pin. The channel 0 of the timer array unit (TAU) is set as input pulse interval measurement, is measuring the 1-bit width of the UART communication transmitted from a master, and calculates the baud rate of UART communication of a master. Makes baud rate values of RL78/G10 UART transmission and above calculation same.
If UART transmission is ready, the average value of an A/D conversion result will be computed for every analog input pin, and the value will be transmitted to a master. Send data is the data converted into the ASCII code instead of binary data. The data for three characters is transmitted from the high-order-digit side for every analog input pin.

Table 1.1 shows the peripheral function to be used and its use.

Figure 1.1 shows the circuit configuration of baud rate measurement.

Figure 1.2 shows the timing chart of baud rate measurement operation outline.

Figure 1.3 shows the setup value to SAU calculation processing program.

Table 1.1 Peripheral Function to be Used and its Use

Peripheral Function	Use
A/D converter	Converts the level of the analog signal input.
Serial array unit 0	The channel 0 is used by the transmission function of UART.
Timer array unit 0 Channel 0 (TAU00)	The pulse interval inputted into TI00 pin is measured 4 times.

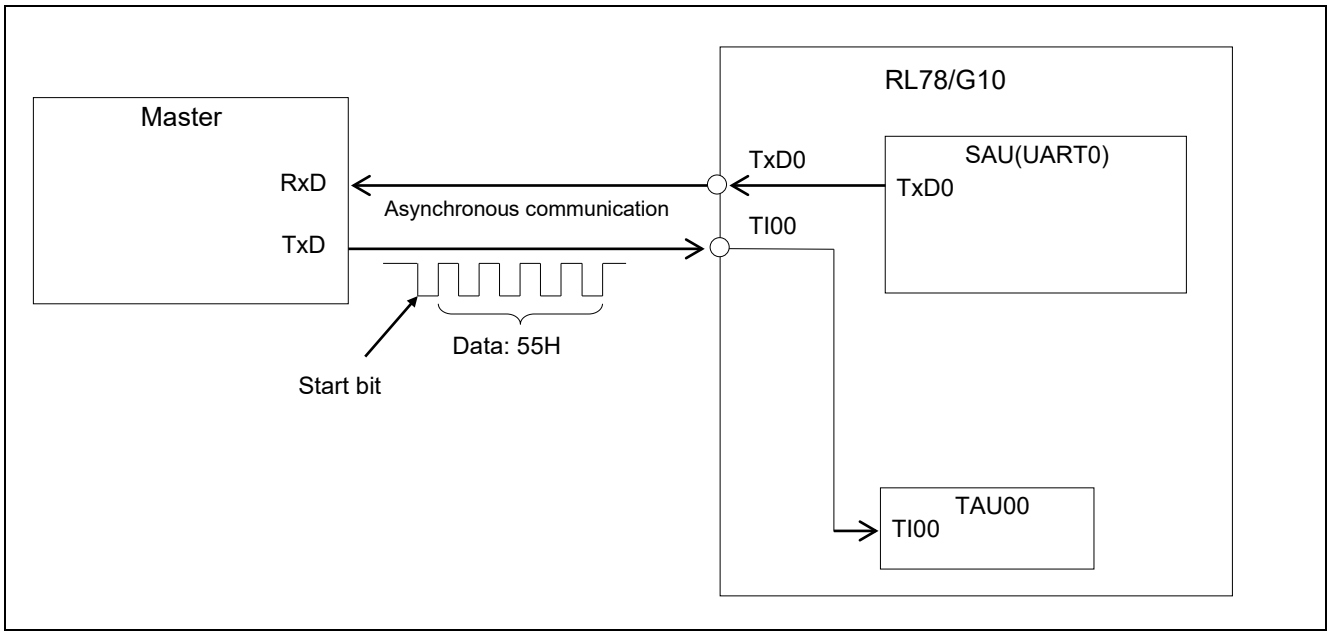


Figure 1.1 Circuit Configuration of Baud Rate Measurement

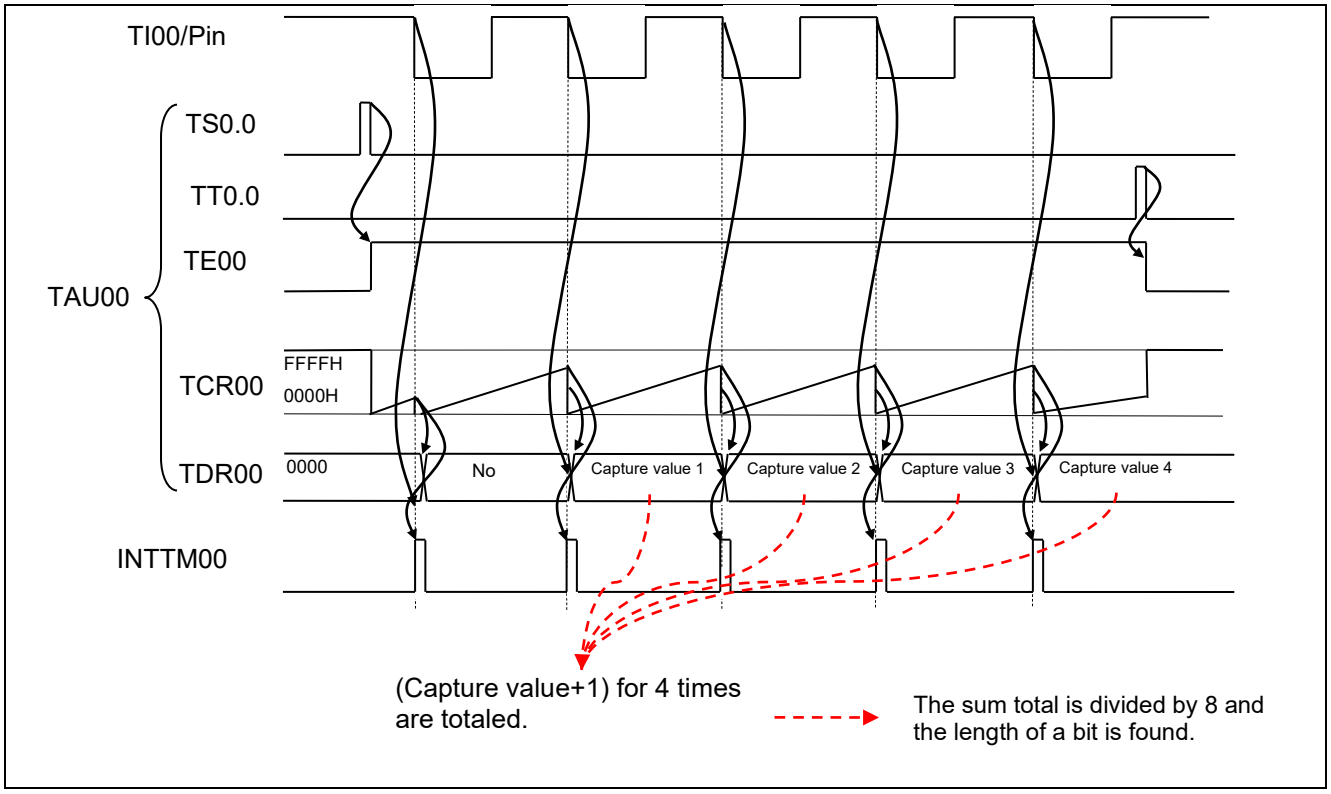


Figure 1.2 Timing Chart of Baud Rate Measurement Operation Outline

The baud rate of UART transmission is calculated from the measured bit length (the number of count clocks). The calculated baud rate (16-bit data length) is decided in the combination of dividing by the higher 7 bits of the SDR0nH register, and dividing in prescaler. Since the maximum which can carry out dividing with a setup of a SDR register is 256, performs 2-dividing by prescaler repeatedly until the calculation result becomes 256 or less, and sets the number of times of performing 2-dividing as SPS0 register. In order to make the error of baud rate calculation as small as possible, it is necessary to round off LSB of a SDR register. Specifically 1 is subtracted from the value which became 256 or less, and also the value which LSB is set as 0 is set to SDR0nH register.

Figure 1.3 shows the above-mentioned processing program. SPSDATA is a variable which stores the value set to SPS0 register, and DIVDATA is a variable which stores the value set to SDR0nH.

In addition, in consideration of program capacity, it does not support the transmission speed of 1200 bps or less here.

```
      CLRB    SPSDATA          ; set start data
SHIFTLOOP:
      CMPW    AX、   #101H     ; check divide ratio
      BC      $SHIFTEND        ; branch if LT 257
      INC     SPSDATA          ; count up SPS data
      SHRW    AX、   1         ; 1/2
      BR      $SHIFTLOOP       ; continue
SHIFTEND:
      DECW    AX               ; adjust
      MOV     A、    #11111110B ; get 7bits
      AND     A、    X
      MOV     DIVDATA、    A   ; set SDRH data
```

Checks whether the value has become 256 or less.

If it is not 256 or less, divides by 2 and adds 1 to the setup value of SPS0.

Rounds off and calculates the setup value to a SDR register.

Figure 1.3 Setup Value to SAU Calculation Processing Program

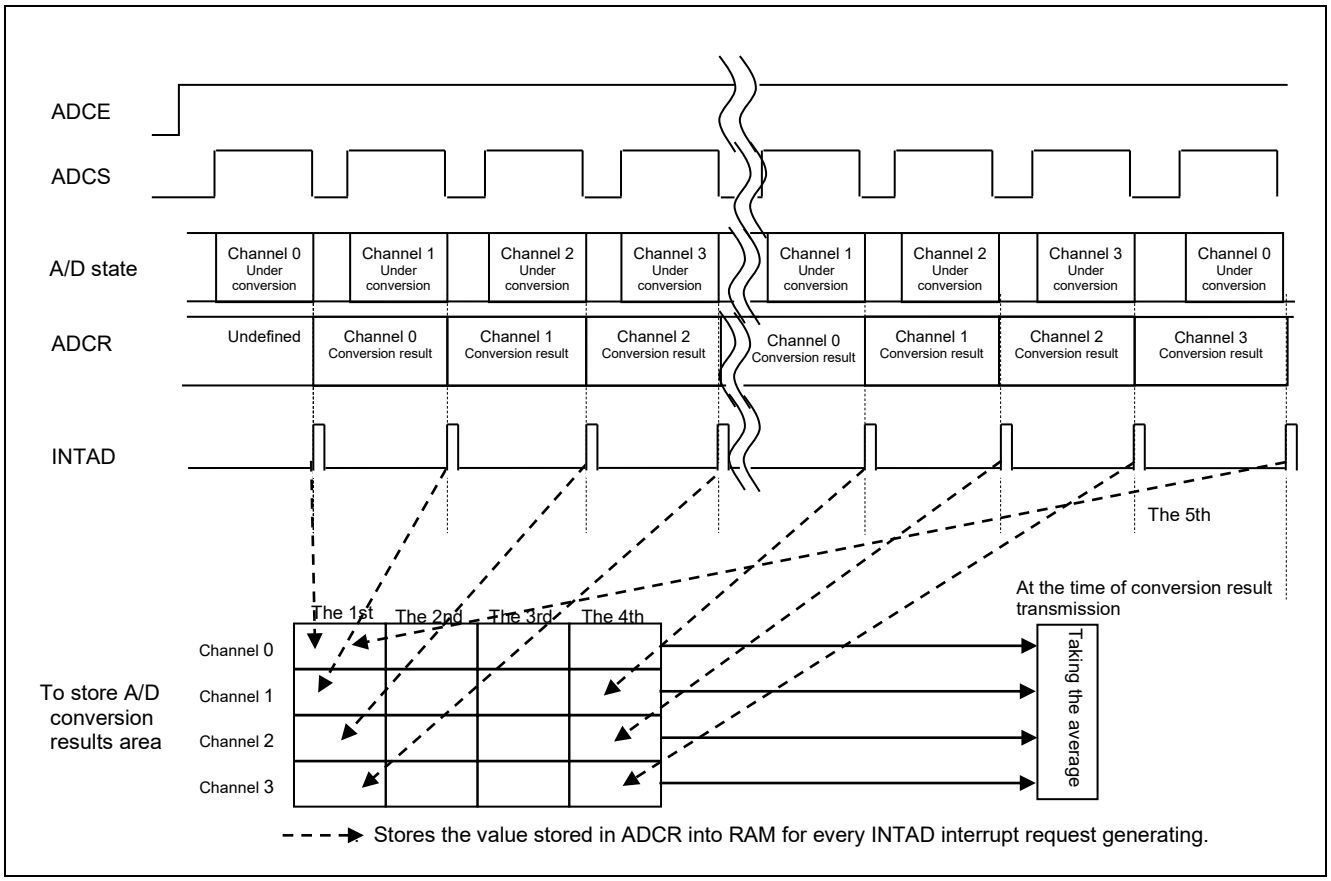


Figure 1.4 Outline of A/D Conversion and Conversion Result Storing Processing

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y16)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 20 MHz • CPU/peripheral hardware clock: 20 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) SPOR operating voltage: Rising edge voltage: 2.90V : Falling edge voltage: 2.84V
Integrated development environment (CubeSuite+)	CubeSuite+ V2.02.00 from Renesas Electronics Corp.
Assembler (CubeSuite+)	RA78K0R V1.90 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2.2.0.13 from Renesas Electronics Corp.
Assembler (e2studio)	KPIT GNURL78-ELF Toolchain V14.0.1 from Renesas Electronics Corp.
Board to be used	RL78/G10 target board (QB-R5F10Y16-TB)

3. Related Application Notes

The application notes related to this application note are listed below for reference.

- RL78/G10 Initialization (R01AN1454E) Application Note
- RL78/G10 A/D Conversion (R01AN1456E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

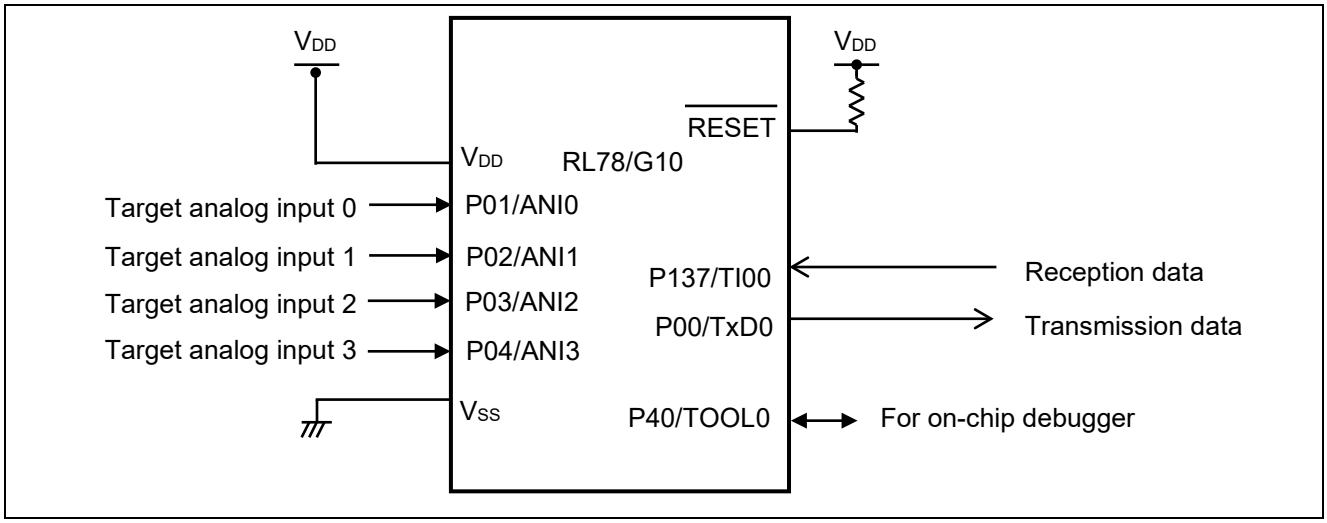


Figure 4.1 Hardware Configuration

Caution: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the reset release voltage (V_{SPOR}) that is specified as SPOR.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their function.

Table 4.1 Pins to be Used and their Function

Pin Name	I/O	Description
P01/ANI0	Input	A/D converter analog input port 0
P02/ANI1	Input	A/D converter analog input port 1
P03/ANI2	Input	A/D converter analog input port 2
P04/ANI3	Input	A/D converter analog input port 3
P137/TI00	Input	For baud rate measurement (UART communication input from the master)
P00/TxD0	Output	Output port for serial transmission data

5. Description of the Software

5.1 Operation Outline

In this application note, always performs the A/D conversion of the analog input voltage of four analog input pins (ANI0 to ANI3). The conversion results for 4 latest times are held to on-chip RAM for every analog input pin. If a falling edge (start bit of UART communication) is inputted into P137/TI00 pin, an input pulse interval will be measured. From the measurement results for a total of 4 times, the 1-bit width of the UART communication transmitted from a master is measured, and the baud rate of UART communication of a master is calculated. The setup value to SPS0 register and SDR0nH register which can realize the computed baud rate is calculated. And then, the channel 0 of SAU0 is set as UART transmission mode (8 bits, the LSB first, and no parity). Calculates the average value of the A/D conversion results stored in RAM, and transmits the data for three characters converted into the ASCII code from the high-order-digit side.

(1) Initializes ADC.

<Setting conditions>

- Sets P01/ANI0 to P04/ANI3 as analog signal input.
- Sets the A/D converter as 10-bit resolution, 4.6μs of conversion time, and channel 0 selection.

(2) Initializes TAU.

<Setting conditions>

- Sets the prescaler as CK00: f_{CLK} and CK01: $f_{CLK}/128$.
- Sets TI00 as the input pulse interval measurement of falling edge detection, and selects CK00 as a count clock.
- Sets the output of TI00 as disable.

(3) Sets the number of times of a capture as 5 times, and permits TAU00 interruption. Starts an A/D conversion and waits for capture completion.

(4) If INTAD interruption is received, changes a conversion channel, starts the next conversion, and stores the conversion result in RAM.

(5) If INTTM00 interruption is received, in the case of the 1st time of the beginning, counts down the number of times of a capture, and returns.

(6) If INTTM00 (2nd to 4th) is received, adds captured value to the accumulation variable of a capture, and counts down the number of times of a capture and returns.

(7) If the 5th INTTM00 interruption is received, makes INTTM00 interruption disable. Adds captured value to the accumulation variable of a capture, and counts down the number of times of a capture and returns. Calculates a baud rate after capture completion and then calculates setup values to SPS0 register and SDR0nH register. Stores the calculation result in a variable and returns from interruption.

(8) Initializes UART0 with the computed preset value. Changes the average value of an A/D conversion result into ASCII code, and transmits to a master sequentially from the channel 0.

(9) If the data transmission to the channel 3 is completed, operation of UART0 will be stopped and processing will be repeated from (3).

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H	11101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	11110111B	P125/RESET pin: RESET input (Internal pull-up resistor can be always connected.) SPOR voltage : Rising edge voltage: 2.90V : Falling edge voltage: 2.84V
000C2H	11111001B	HOCO: 20MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
CLKFREQ	**20000**	What expressed fCLK per kHz
CTXMODETxH	**10000000B**	Setting value of SCR00H
CTRXMODEL	**10010111B**	Setting value of SCR00L
CSMRDATATxH	**00000000B**	Setting value of SMR00H
CSMRDATATxL	**00100010B**	Setting value of SMR00L
DATANUM	**4** Note	The number of times of A/D conversion

Note A value when a definition file (DEV&UART.inc) defines control switch DATA4.
If DATA8 is defined, it can be set to 8, and the number of times of a sampling per channel can be increased, and accuracy can be raised.

5.4 List of Variables

Table 5.3 lists variables used by this sample program.

Table 5.3 Variables used for this Sample Program

Variable Name	Outline
CAPTUREL	Stores the accumulated value captured by TI00
CAPTUREH	Stores the overflow value of the accumulated value captured by TI00
SPSDATA	Stores setup value for SPS0 register
DIVDATA	Stores setup value for SDR0nH register
LPCOUNT	Counter for the number of TI00 capture control
ANIBUF	Buffer for A/D conversion data
ANIAVERAGE	Stores the average of A/D conversion data
SAVEPNT	Base pointer for storing of A/D conversion data
ADCHANNEL	Channel selection for A/D conversion

5.5 List of Functions (Subroutines)

Table 5.4 lists the functions (subroutines).

Table 5.4 Functions (Subroutines)

Function Name	Outline
RESET_START	Initialization of CPU in the case of reset/start
SINIPORT	Setup of I/O port
SINICLK	Setup of the clock generator
SINIADC	Setup of A/D converter
SINITAU	Setup of the timer array unit
SINIUART0	Initialization of UART0
TxASCIIDATA	Converts the A/D conversion result of each channel into ASCII and transmits to a master.
STxDATA	UART0 transmission processing
IINTAD	Interruption processing for end of an A/D conversion
IINTTM00	Interruption processing for completion of capture by TAU00

5.6 Function Specifications (Subroutines)

This section describes the specifications for the functions (subroutines) that are used in this sample program.

[Function Name] RESET_START

Synopsis	Initialization of CPU in the case of reset/start
Explanation	Calls main processing after setting up of the stack pointer and initialization of the hardware.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINIPORT

Synopsis	Setup of I/O port
Explanation	Sets up input port of analogue signal for A/D conversion.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINICLK

Synopsis	Setup of the clock generator
Explanation	Sets up the clock used for baud rate calculation.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINIADC

Synopsis	Setup of A/D converter
Explanation	Sets up A/D converter as 10-bit resolution, conversion time of 4.6μs, and the highest interruption priority.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINITAU

Synopsis	Setup of the timer array unit
Explanation	Sets up The timer array unit used for input pulse width measurement of TI00 pin.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINIUART0

Synopsis	Initialization of UART0
Explanation	Initializes UART0 which realizes the calculated baud rate.
Arguments	None（SPSDATA、DIVDATA）
Return value	None
Remarks	None

[Function Name] TxASCIIDATA

Synopsis	Converts the A/D conversion result of each channel into ASCII and transmits to a master.
Explanation	Changes lower 4 bits of A register into ASCII code and transmits it.
Arguments	A register : Converted data
Return value	None
Remarks	None

[Function Name] STxDATA

Synopsis	UART0 transmission
Explanation	Transmits the contents of the A register from UART.
Arguments	A register : Transmission data
Return value	None
Remarks	Transmission status is 00.

[Function Name] IINTAD

Synopsis	Interruption processing for end of an A/D conversion
Explanation	Starts by INTAD, stores conversion result to a buffer, and starts conversion of the next channel.
Arguments	None
Return value	None
Remarks	None

[Function Name] IINTTM00

Synopsis	Interruption processing for completion of capture by TAU00
Explanation	Calculates a setup value of UART0 to suit the baud rate of master by capturing 4 times of the falling edge interval of UART transmission (data 55H).
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

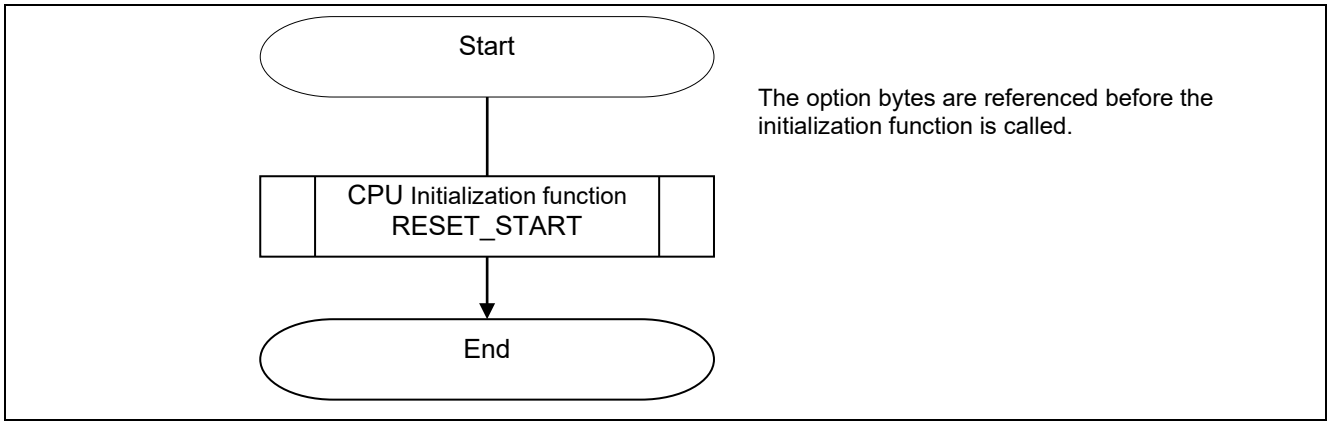


Figure 5.1 Flowchart of Overall

5.7.1 Initialization Function of CPU

Figure 5.2 shows the flowchart of initialization function of CPU.

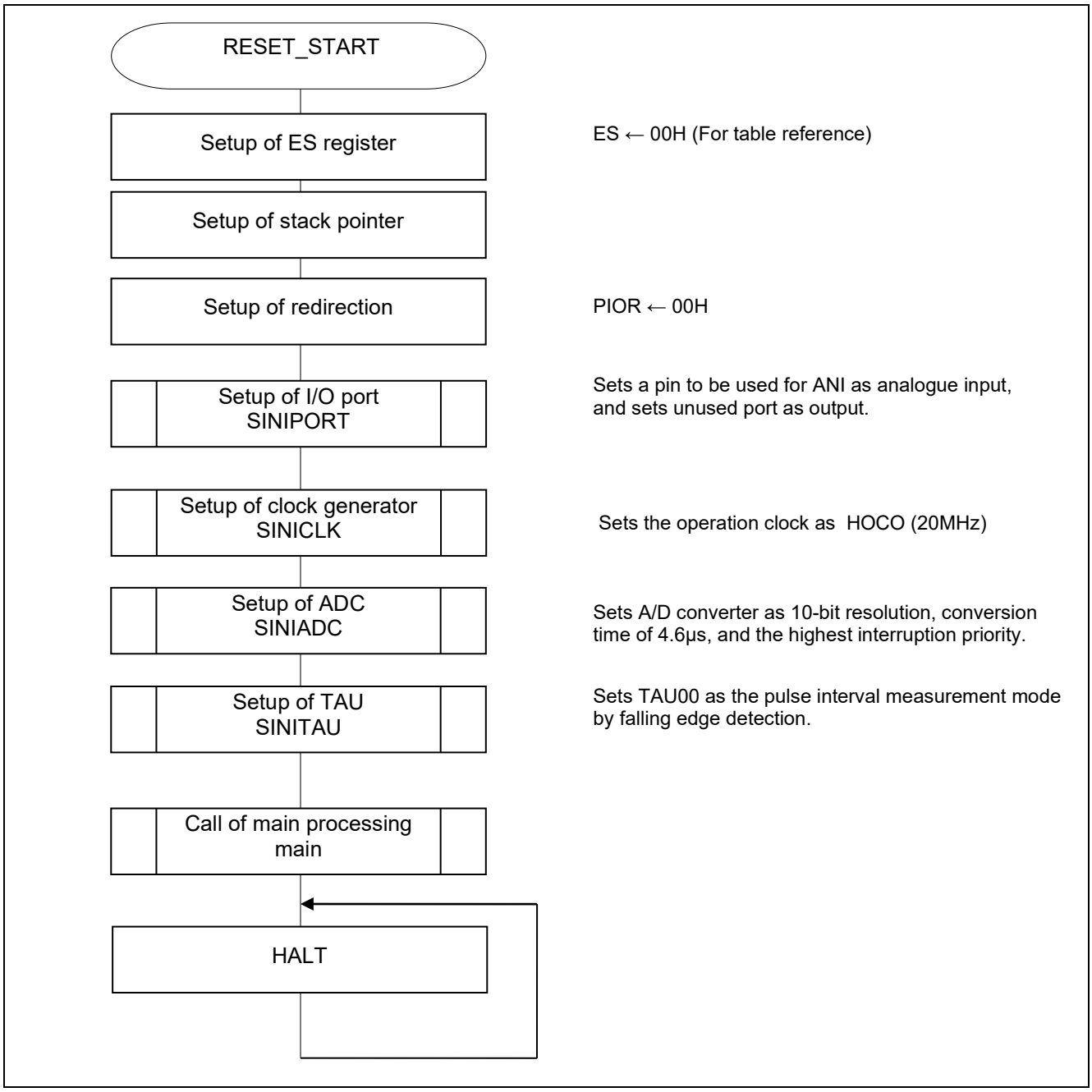


Figure 5.2 Initialization Function of CPU

5.7.2 Setup of I/O Port

Figure 5.3 shows the flowchart of I/O port setup.

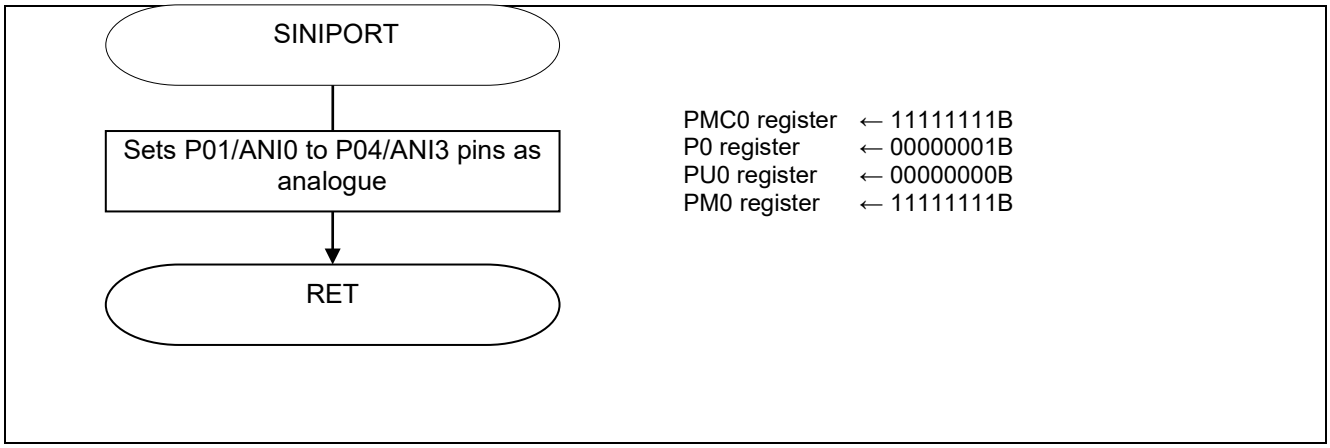


Figure 5.3 Setup of I/O Port

Note: Refer to RL78/G10 Initialization (R01AN1454EJ) Application Note "Flowchart" for the setup of the unused port.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setup of port mode

- Port mode control register 0 (PMC0)
  Setup of analog input or digital I/O.
- Port register 0 (P0)
  Output latches setup of each port.
- Pull-up resistor option register 0 (PU0).
  On-chip pull-up resistor selection
- Port mode register 0 (PM0)
  Selection of the I/O mode of each port.

Symbol: PMC0

7	6	5	4	3	2	1	0
1	1	1	PMC04	PMC03	PMC02	PMC01	1
1	1	1	**1**	**1**	**1**	**1**	1

Bit 4 ─ 1

PMC0n	P0n pin selects digital I/O or analog input. (n = 1–4)
0	Digital I/O (Combined use function except the analog input.)
1	Analog input

Caution: Refer to "RL78/G10 User's Manual: Hardware" for the setup of the register.

Symbol: P0

7	6	5	4	3	2	1	0
0	0	0	P04	P03	P02	P01	P00
0	0	0	x	x	x	x	**1**

Bit 0

P00	**P00 pin controls output data.**
0	Output 0
1	**Output 1**

Symbol: PM0

7	6	5	4	3	2	1	0
1	1	1	PM04	PM03	PM02	PM01	PM00
1	1	1	**1**	**1**	**1**	**1**	**1**

Bit 4 ─ 1

PM0n	**P0n pin selects I/O mode.**
0	Output mode (Output buffer on)
1	**Input mode (Output buffer off)**

Symbol: PU0

7	6	5	4	3	2	1	0
0	0	0	PU04	PU03	PU02	PU01	PU00
0	0	0	**0**	**0**	**0**	**0**	**0**

Bit 4 ─ 1

PU0n	**P0n selects on-chip pull-up resistor (n = 0-4)**
0	**Does not connect on-chip pull-up resistor.**
1	Connects on-chip pull-up resistor.

Caution: Refer to **“**RL78/G10 User's Manual: Hardware” for the setup of the register.

5.7.3 Setup of Clock Generator

Figure 5.4 shows the flowchart of clock generator.

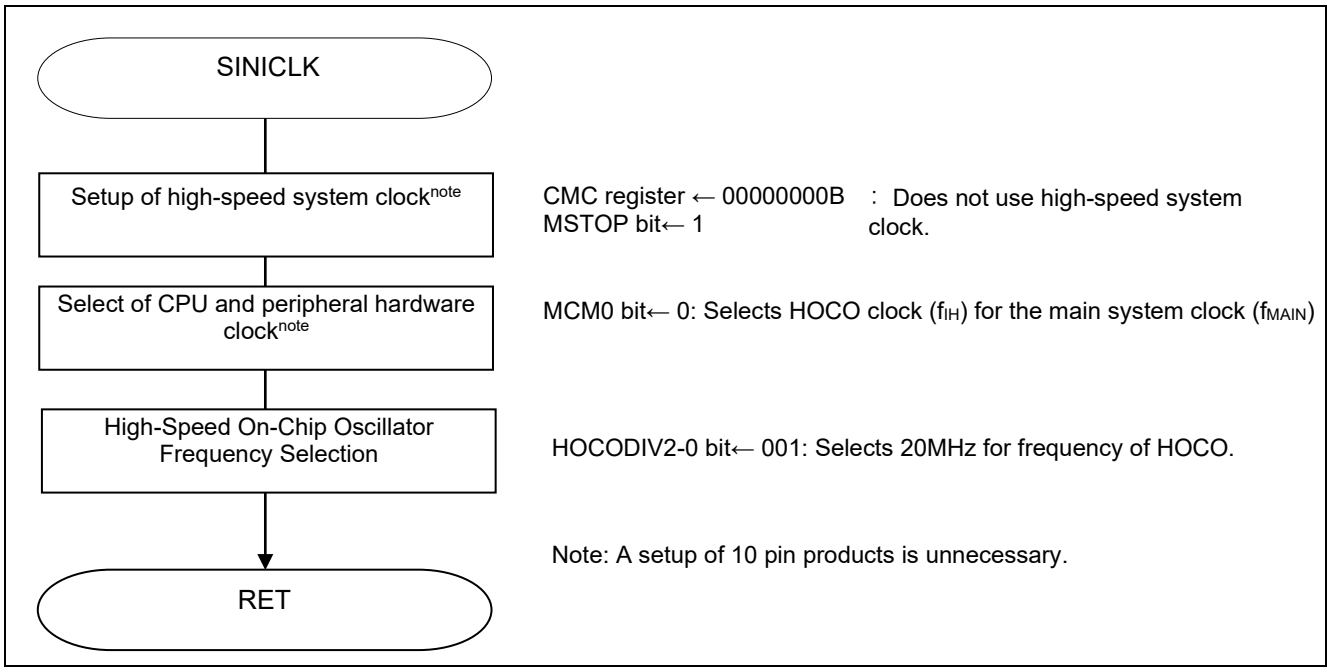


Figure 5.4 Setup of Clock Generator

Note: Refer to RL78/G10 Initialization (R01AN1454EJ) Application Note "Flowchart" for the setup of CPU clock (SINICLK).

Setup of clock operation mode

・Clock Operation Mode Control Register (CMC)
Sets the operation mode of the X1/P121/(INTP3) and X2/EXCLK/P122/(INTP2) pins, and to select a gain of the oscillator.
Symbol: CMC

7	6	5	4	3	2	1	0
EXCLK	OSCSEL	0	0	0	0	0	AMPH
0	**0**	0	0	0	0	0	**0**

Bit 7 ─ 6

EXCLK	OSCSEL	High-speed system clock pin operation mode	X1/P121/(INTP3) pin	X2/EXCLK/P122/(INTP2) pin
0	**0**	Input port mode	Input port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	0	External clock input mode	Input port	External clock input

Bit 0

AMPH	Control of X1 clock oscillation frequency
0	**1 MHz≦fX≦10 MHz**
1	10 MHz＜fX≦20 MHz

Caution: Refer to "RL78/G10 User's Manual: Hardware" for the setup of the register.

Selection of System clock

・System clock control register (CKC)
Selects a main system clock.

Symbol: CKC

7	6	5	4	3	2	1	0
0	0	MCS	MCM0	0	0	0	0
0	0	0	**0**	0	0	0	0

Bit 4

MCM0	Main system clock (f_{MAIN}) operation control
0	Selects the high-speed on-chip oscillator clock (f_{IH}) as the main system clock (f_{MAIN}).
1	Selects the high-speed system clock (fMX) as the main system clock (fMAIN).

Selection of **high-speed on-chip oscillator frequency**

・High-speed on-chip oscillator frequency selection register (HOCODIV)
Selects the frequency of the high-speed on-chip oscillator.

Symbol: HOCODIV

7	6	5	4	3	2	1	0
0	0	0	0	0	HOCODIV2	HOCODIV1	HOCODIV0
0	0	0	0	0	**0**	**0**	**1**

Bit 2 ─ 0

HOCODIV 2	HOCODIV 1	HOCODIV 0	High-speed on-chip oscillator clock frequency selection
0	**0**	**1**	**20MHz**
0	1	0	10MHz
0	1	1	5MHz
1	0	0	2.5MHz
1	0	1	1.25MHz
Other than above			Setting prohibited

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

5.7.4 Setup of A/D Converter

Figure 5.5 shows the flowchart of A/D converter setup.

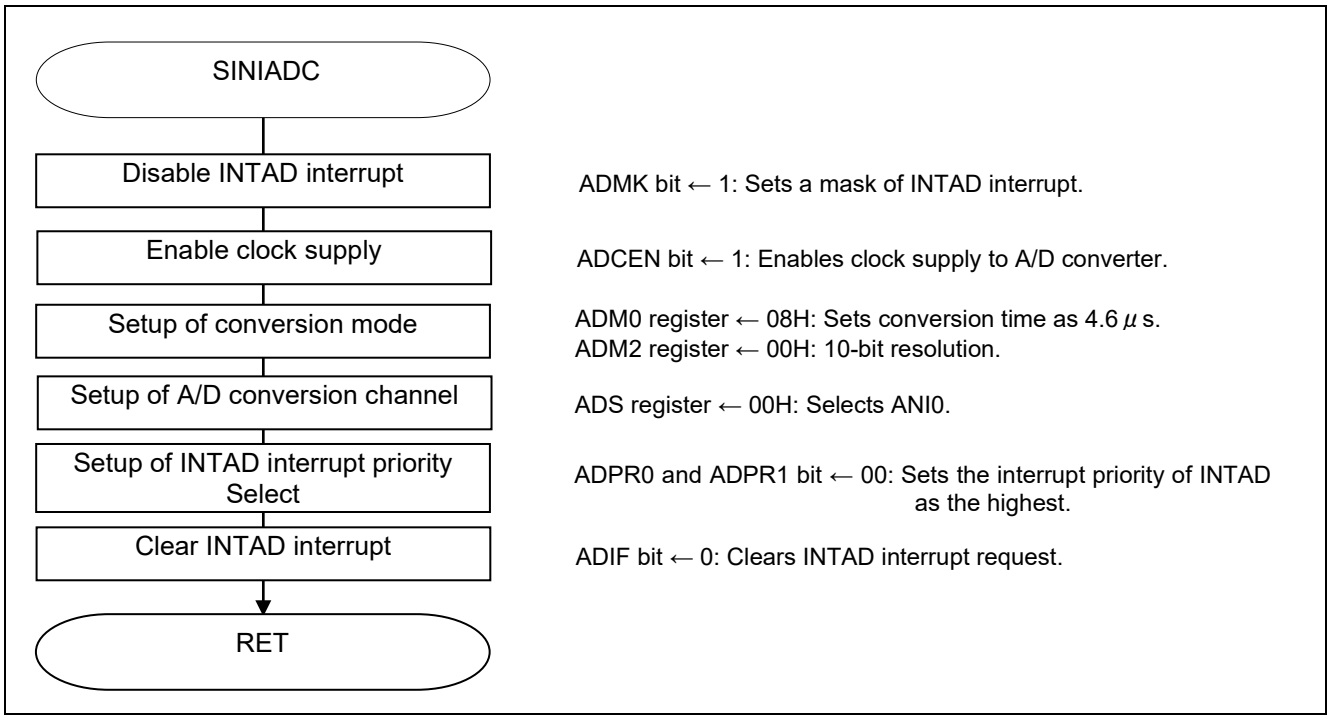


Figure 5.5 Setup of A/D Converter

Setup of AD converter operation mode

☐ Peripheral enable register 0 (PER0)

Clock supply of A/D converter.

・A/D converter mode register 0 (ADM0)

Setup of A/D conversion time.

・A/D converter mode register 0 (ADM2)

Setup of A/D conversion resolution.

・A/D converter mode register 0 (ADS)

Specification of conversion channel.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN[Note]	CMPEN[Note]	ADCEN	IICA0EN[Note]	0	SAU0EN	0	TAU0EN
x	x	**1**	x	0	x	0	0

Note 16-pin products only.

Bit 5

ADCEN	Control of input clock supply for A/D converter.
0	Stops input clock supply. ・SFR used by the A/D converter cannot be written. ・The A/D converter is in the reset status.
1	Supplies input clock. ・SFR used by the A/D converter can be read/written.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	0	0	FR1	FR0	0	LV0	ADCE
0	0	0	**0**	**1**	0	**0**	0

Bit 4, 3, 1

A/D converter mode register 0 (ADM0)			Conversion Clock	Number of Conversion Clock	Conversion Time	Conversion Time Selection (μs)				
FR1	FR0	LV0				fCLK = 1.25 MHz	fCLK = 2.5 MHz	fCLK = 5 MHz	fCLK = 10 MHz	fCLK = 20 MHz
0	0	**0**	$f_{CLK}/8$	**23 f_{AD}** (Number of sampling clock: 9 f_{AD})	184 /f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	18.4	9.2
0	**1**		**$f_{CLK}/4$**		**92 /f_{CLK}**			18.4	9.2	**4.6**
1	0		$f_{CLK}/2$		46 /f_{CLK}		18.4	9.2	4.6	Setting prohibited
1	1		f_{CLK}		23 /f_{CLK}	18.4	9.2	4.6	Setting prohibited	
0	0	1	$f_{CLK}/8$	17 f_{AD} (Number of sampling clock: 3 f_{AD})	136 /f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	13.6	6.8μs
0	1		$f_{CLK}/4$		68 /f_{CLK}			13.6	6.8	3.4μs
1	0		$f_{CLK}/2$		34 /f_{CLK}		13.6	6.8	3.4	Setting prohibited
1	1		f_{CLK}		17 /f_{CLK}	13.6	6.8	3.4	Setting prohibited	

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Symbol: ADM2

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ADTYP
0	0	0	0	0	0	0	**0**

Bit 1

ADTYP	Selection of A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Symbol: ADS

7	6	5	4	3	2	1	0
0	0	0	0	0	ADS2[Note]	ADS1	ADS0
0	0	0	0	0	0	**0**	**0**

Note 16-pin products only.

Bit 1, 0

ADS1	ADS0	Analog input channel	Input source
0	**0**	**ANI0**	**P01/ANI0 pin**
0	1	ANI1	P02/ANI1 pin
1	0	ANI2	P03/ANI2 pin
1	1	ANI3	P04/ANI3 pin

Setup of INTAD interrupt

・Interrupt request flag register (IF0H)

Clears interrupt request flag.

・Interrupt mask flag register (MK0H)

Setup of interrupt mask.

Symbol: IF0H

7	6	5	4	3	2	1	0
0	0	0	0	0	KRIF	ADIF	TMIF01
0	0	0	0	0	x	**0**	x

Bit 1

ADIF	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status.

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Symbol: MK0H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRMK	ADMK	TMMK01
1	1	1	1	1	x	**1**	x

Bit 1

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Setup of interrupt priority

・Priority order specification flag registers (PR00H, PR10H)

Setup of interrupt priority

Symbol: PR00H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRPR0	ADPR0	TMPR001
1	1	**1**	1	1	x	**0**	x

Symbol: PR10H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRPR1	ADPR1	TMPR101
1	1	**1**	1	1	x	**0**	x

Bit 1 (PR10H), Bit 1 (PR00H)

xxPR1x	xxPR0x	Priority level selection
0	**0**	**Selects level 0 (high priority level)**
0	1	Selects level 1
1	0	Selects level 2
1	1	Selects level 3 (low priority level)

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

5.7.5 Setup of Timer Array Unit

Figure 5.6 shows the flowchart of timer array unit setup.

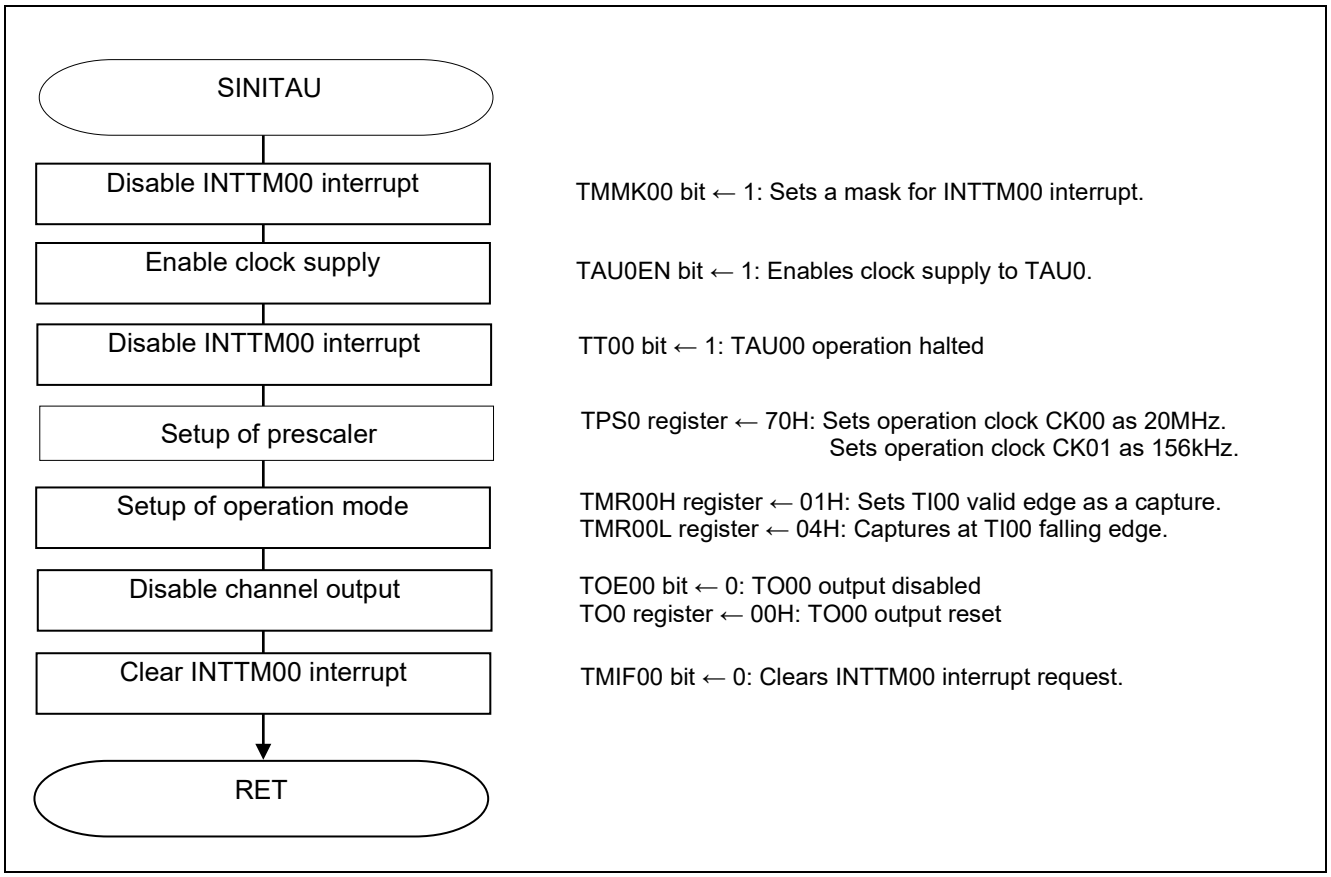


Figure 5.6 Setup of Timer Array Unit

Starting clock supply to the timer array unit

・Peripheral enable register 0 (PER0)

Starts clock supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN[Note]	CMPEN[Note]	ADCEN	IICA0EN[Note]	0	SAU0EN	0	TAU0EN
x	x	x	x	0	x	0	**1**

Note 16-pin products only.

Bit 0

TAU0EN	Control of input clock supply for the timer array unit.
0	Stops supply of input clock. ☐ SFR used by the timer array unit cannot be written. ☐ The timer array unit is in the reset status.
1	Supplies input clock. ☐ SFR used by the timer array unit can be read/written.

Setup of the timer clock frequency

・Timer clock select register 0 (TPS0)

Selects the operation clock of timer array unit 0.

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
0	**1**	**1**	**1**	**0**	**0**	**0**	**0**

Bit 7 – 4, 3 – 0

PRS 0k3	PRS 0k2	PRS 0k1	PRS 0k0	Selection of operation clock (CK0k) (k = 0, 1)					
					f_{CLK}= 1.25MHz	f_{CLK}= 2.5MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz
0	**0**	**0**	**0**	**f_{CLK}**	1.25 MHz	2.5 MHz	5 MHz	10 MHz	**20 MHz**
0	0	0	1	$f_{CLK}/2$	625 kHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{CLK}/2^2$	313 kHz	625 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156 kHz	313 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	78 kHz	156 kHz	313 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	39 kHz	78 kHz	156 kHz	313 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39 kHz	78 kHz	156 kHz	313 kHz
0	**1**	**1**	**1**	**$f_{CLK}/2^7$**	9.8 kHz	19.5 kHz	39 kHz	78 kHz	**156 kHz**
1	0	0	0	$f_{CLK}/2^8$	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz	78 kHz
1	0	0	1	$f_{CLK}/2^9$	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz
1	1	0	0	$f_{CLK}/2^{12}$	313 Hz	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz
1	1	0	1	$f_{CLK}/2^{13}$	152 Hz	313 Hz	625 Hz	1.22 kHz	2.5 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78Hz	152 Hz	313 Hz	625 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	39Hz	78Hz	152 Hz	313 Hz	625 Hz

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Setup of channel 0 operation mode

・Timer mode register 00 (TMR00H, TMR00L)

Selection of the operation clock (f_{MCK}).
Selection of the count clock.
Select the 16 or 8-bit timer.
Specifying the start trigger and capture trigger.
Selection of the valid edge of the timer input.
Setting of the operation mode.

Symbol: TMR00H

7	6	5	4	3	2	1	0
CKS001	0	0	CCS00	0	STS002	STS001	STS000
0	0	0	**0**	0	**0**	**0**	**1**

Bit 7

CKS001	Selection of operation clock (f_{MCK}) of channel 0
0	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
1	1 Operation clock CK01 set by timer clock select register 0 (TPS0)

Bit 4

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS0n1 bit**
1	Valid edge of input signal from the TI0n pin

Bit 2 - 0

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	**0**	**1**	Valid edge of the TI00 pin input is used as the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	When the channel is used as a slave channel with the one-shot pulse output, PWM output function, or multiple PWM output function: The interrupt request signal of the master channel (INTTM0n) is used as the start trigger.
1	1	0	When the channel is used as a slave channel in two-channel input with one-shot pulse output function: The interrupt request signal of the master channel (INTTM0n) is used as the start trigger. A valid edge of the TI03 pin input of the slave channel is used as the end trigger.
Other than above			Setting prohibited

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Symbol: TMR00L

7	6	5	4	3	2	1	0
CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	0	**0**	**1**	**0**	**0**

Bit 7 - 6

CIS001	CIS000	Selection of TI00 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STS0n2 to STS0n0 bits is other than 010B, set the CIS0n1 to CIS0n0 bits to 10B.		

Bit 3 - 1

MD 003	MD 002	MD 001	Setting of operation mode of channel 0	Corresponding function	Count operation of TCR
0	**0**	**0**	Interval timer mode	Interval timer/Square wave output/Divider function/PWM output (master)	Down count
0	**1**	**0**	Capture mode	Input pulse interval measurement/Twochannel input with one-shot pulse output function (slave)	Up count
0	1	1	Event counter mode	External event counter	Down count
1	0	0	One-count mode	Delay counter/One-shot pulse output/Twochannel input with one-shot pulse output function (master)/PWM output (slave)	Down count
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Up count
Other than above			Setting prohibited		
The operation of each mode changes depending on the operation of MD0n0 bit (refer to the table below).					

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Bit 0

Operation mode (Value set by the MD0n3 to MD0n1 bits (refer to the table above)).	**MD 000**	**Setting of starting counting and interrupt**
・Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	**0**	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
・Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
・One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, a timer interrupt is not generated.
	1	Start trigger is valid during counting operation At that time, a timer interrupt is not generated.
・Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, a timer interrupt is not generated.
Other than above		Setting prohibited

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Setup of output value of timer output pin

・Timer output register 0 (TO0)

Sets the output value of timer output pin of each channel.

Symbol: TO0

7	6	5	4	3	2	1	0
0	0	0	0	TO03Note	TO02 Note	TO01	TO00
0	0	0	0	x	x	x	**0**

Note 16-pin products only.

Bit 0

TO00	Timer output of channel 0
0	Timer output value is “0”.
1	Timer output value is “1”.

Setup of disabling timer output

・Timer output enable register 0 (TOE0)

Sets enabling/disabling timer output of each channel.

Symbol: TOE0

7	6	5	4	3	2	1	0
0	0	0	0	TOE03Note	TOE02Note	TOE01	TOE00
0	0	0	0	x	x	x	**0**

Note 16-pin products only.

Bit 0

TOE00	Timer output enable/disable of channel 0
0	Disable output of timer. Without reflecting on TO00 bit timer operation, to fixed the output. Writing to the TO0n bit is enabled
1	Enable output of timer. Reflected in the TO0n bit timer operation, to generate the output waveform. Writing to the TO00 bit is disabled (writing is ignored).

Caution: Refer to **“**RL78/G10 User's Manual: Hardware” for the setup of the register.

Setup of the timer capture completion interrupt

- interrupt request flag register (IF0L)
  Clears the interrupt request flag.
- Interrupt mask flag registers (MK0L)
  Sets the interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
0	x	x	x	x	x	x	x

Bit 7

TMIF00	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
1	x	x	x	x	x	x	x

Bit 7

TMMK00	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

5.7.6 Initialization of UART0

Figure 5.7 shows the flowchart of initialization of UART0.

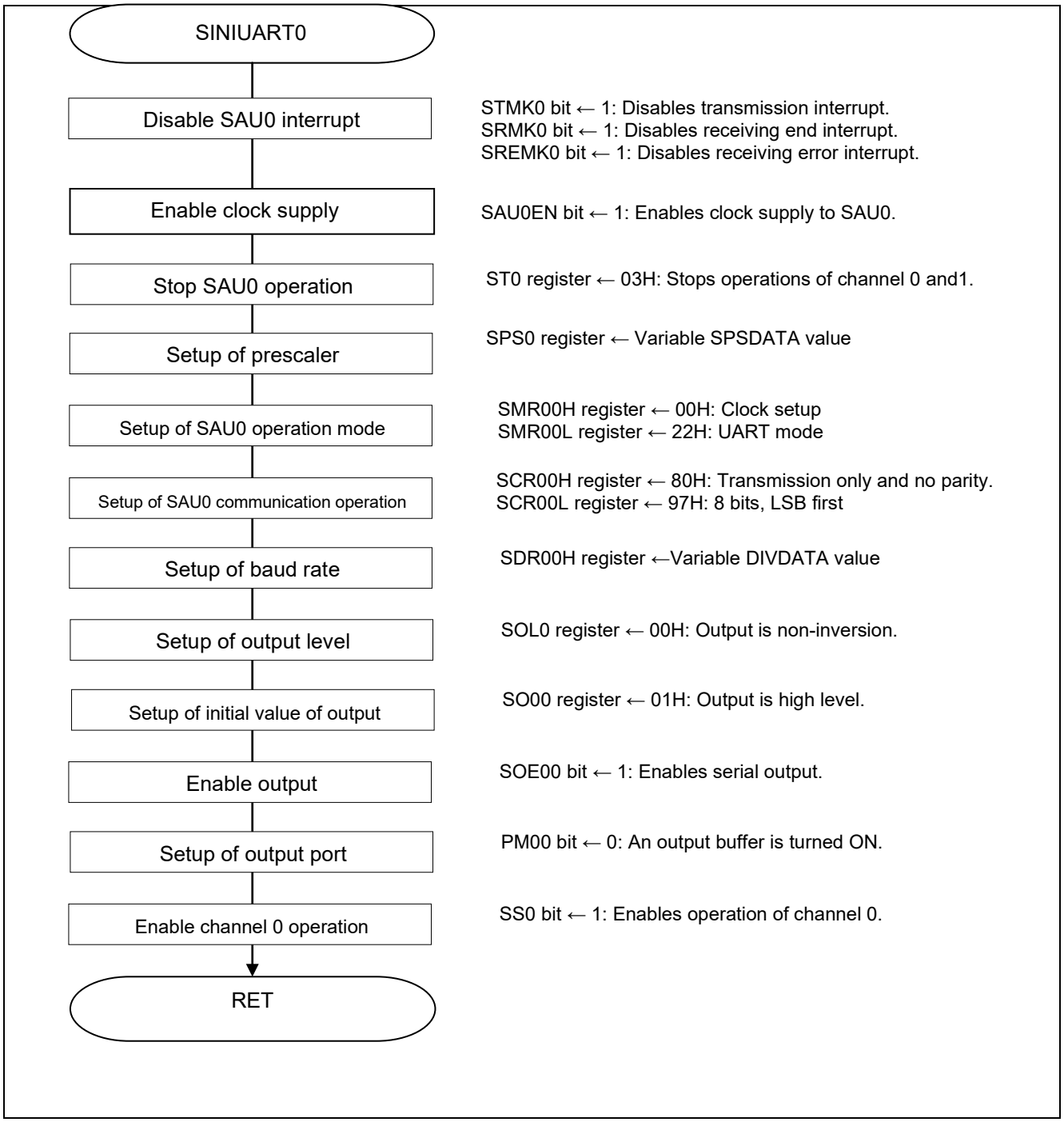


Figure 5.7 Initialization of UART0

Start supplying clock to the serial array unit 0.

・peripheral enable register 0 (PER0)

Starts supplying clock to the serial array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN Note	CMPEN Note	ADCEN	IICA0EN Note	0	SAU0EN	0	TAU0EN
x	x	x	x	0	**1**	0	x

Note 16-pin products only.

Bit 7

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops supply of input clock. ・SFR used by serial array unit 0 cannot be written. ・SFR used by serial array unit 0 cannot be written.
1	Enables input clock supply. ・SFR used by serial array unit 0 can be read/written.

Setup of the serial clock frequency.

・Serial clock select register 0 (SPS0)

Selects the operation clock of serial array unit 0.

Symbol: SPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
0	**1**	**1**	**1**	**0**	**0/1**	**0/1**	**0/1**

Bit 7 – 4, 3 – 0

PRS 0n3	PRS 0n2	PRS 0n1	PRS 0n0	Section of operation clock (CKn) (n = 0, 1)					
					f_{CLK} = 1.25MHz	f_{CLK} = 2.5MHz	f_{CLK} = 5MHz	f_{CLK} = 10MHz	f_{CLK} = 20MHz
0	**0**	**0**	**0**	**f_{CLK}**	1.25 MHz	2.5 MHz	5 MHz	10 MHz	**20 MHz**
0	**0**	**0**	**1**	**$f_{CLK}/2$**	625 kHz	1.25 MHz	2.5 MHz	5 MHz	**10 MHz**
0	**0**	**1**	**0**	**$f_{CLK}/2^2$**	313 kHz	625 kHz	1.25 MHz	2.5 MHz	**5 MHz**
0	**0**	**1**	**1**	**$f_{CLK}/2^3$**	156 kHz	313 kHz	625 kHz	1.25 MHz	**2.5 MHz**
0	**1**	**0**	**0**	**$f_{CLK}/2^4$**	78 kHz	156 kHz	313 kHz	625 kHz	**1.25 MHz**
0	**1**	**0**	**1**	**$f_{CLK}/2^5$**	39 kHz	78 kHz	156 kHz	313 kHz	**625 kHz**
0	**1**	**1**	**0**	**$f_{CLK}/2^6$**	19.5 kHz	39 kHz	78 kHz	156 kHz	**313 kHz**
0	**1**	**1**	**1**	**$f_{CLK}/2^7$**	9.8 kHz	19.5 kHz	39 kHz	78 kHz	**156 kHz**
1	0	0	0	$f_{CLK}/2^8$	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz	78 kHz
1	0	0	1	$f_{CLK}/2^9$	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz
1	1	0	0	$f_{CLK}/2^{12}$	313 Hz	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz
1	1	0	1	$f_{CLK}/2^{13}$	152 Hz	313 Hz	625 Hz	1.22 kHz	2.5 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78Hz	152 Hz	313 Hz	625 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	39Hz	78Hz	152 Hz	313 Hz	625 Hz

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Setup of the transmission channel operation mode.

・Serial mode register 00 (SMR00H, SMR00L)

Interrupt source

operation mode

Selection of the transfer clock.

Selection of f_{MCK}.

Symbol: SMR00H

7	6	5	4	3	2	1	0
CKS 00	CCS 00	0	0	0	0	0	0
0	**0**	0	0	0	0	0	0

SMR00L

7	6	5	4	3	2	1	0
0	0	1	0	0	MD 002	MD 001	MD 000
0	0	1	0	0	**0**	**1**	**0**

Bit 7 （SMR00H）

CKS00	Selection of operation clock (f_{MCK}) of channel 0
0	Operation clock CK00 set by the SPS0 register.
1	Operation clock CK01 set by the SPS0 register.

Bit 6 （SMR00H）

CCS00	Selection of transfer clock (f_{TCLK}) of channel 0
0	Divided operation clock f_{MCK} specified by the CKS00 bit.
1	Clock input fSCK from the SCKp pin (slave transfer in CSI mode).

Bit 2 - 1 （SMR00L）

MD002	MD001	Setting of operation mode of channel 0
0	0	CSI mode
0	**1**	UART mode
1	0	Simplified I2C mode
1	1	Setting prohibited

Bit 0 （SMR00L）

MD000	Selection of interrupt source of channel 0
0	Transfer end interrupt
1	Buffer empty interrupt (Occurs when data is transferred from the SDR0nL register to the shift register.)

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Setup of communication operation setting of transmission channel

・Serial communication operation setting register 00 (SCR00H, SCR00L)

Sets data length, data transfer sequence, and operation data.

Symbol: SCR00H

7	6	5	4	3	2	1	0
TXE00	RXE00	DAP00	CKP00	0	EOC00	PTC001	PTC000
1	**0**	0	0	0	**0**	**0**	**0**

Bit 7 - 6

TXE00	RXE00	Setting of operation mode of channel 0
0	0	Disable communication
0	1	Reception only
1	**0**	Transmission only
1	1	Transmission/reception

Bit 2

EOC00	Selection of masking of error interrupt signal (INTSRE0)
0	**Masks** error interrupt INTSRE0 (INTSR0 is not masked).
1	Enables generation of error interrupt INTSRE0 (INTSR0 is masked if an error occurs).

Bit 1 - 0

PTC001	PTC000	Setting of parity bit in UART mode	
		Transmission	Reception
0	**0**	Does not output the parity bit.	Receives without parity.
0	1	Outputs 0 parity	No parity judgment.
1	0	Outputs even parity.	Judged as even parity.
	1	Outputs odd parity.	Judges as odd parity.

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Symbol: SCR00L

7	6	5	4	3	2	1	0
DIR00	0	SLC001	SLC000	0	1	1	DLS000
1	0	**0**	**1**	0	1	1	**1**

Bit 7

DIR00	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	Inputs/outputs data with LSB first.

Bit 5 - 4

SLC001	SLC000	Setting of stop bit in UART mode
0	0	No stop bit
0	**1**	Stop bit length = 1 bit
1	0	Stop bit length = 2 bits
1	1	Setting prohibited

Bit 0

DLS000	Setting of data length in CSI and UART modes
0	7-bit data length (stored in bits 0 to 6 of the SDR0nL register)
1	8-bit data length (stored in bits 0 to 7 of the SDR0nL register)

Setup of transmission channel transfer clock

・Serial data register 00 (SDR00H, SDR00L)

Transfer clock frequency: Undefined

Symbol: SDR00H (a register that sets the division ratio)

7	6	5	4	3	2	1	0
0/1	**0/1**	**0/1**	**0/1**	**0/1**	**0/1**	**0/1**	0

SDR00L (a transmit/receive buffer register)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit 7 – 1 (SDR00H)

SDR00H[7:1]							Transfer clock setting by dividing the operating clock
0	0	0	0	0	0	0	$f_{MCK}/2$
0	0	0	0	0	0	1	$f_{MCK}/4$
0	0	0	0	0	1	0	$f_{MCK}/6$
0	0	0	0	0	1	1	$f_{MCK}/8$
・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	・ ・
1	1	1	1	1	1	0	$f_{MCK}/254$
1	1	1	1	1	1	1	$f_{MCK}/256$

Caution: Refer to “RL78/G10 User's Manual: Hardware” for the setup of the register.

Setup of output level

・Serial output level register 0 (SOL0)

Output: Non-inversion

Symbol: SOL0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SOL00
0	0	0	0	0	0	0	**0**

Bit 0

SOL00	Selects inversion of the level of the transmit data of channel 0 in UART mode (n = 0、1)
0	Communication data is output as is.
1	Communication data is inverted and output.

Setup of initial output level

・Serial output register 0 (SO0)

Initial output: 1

Symbol: SO0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SO01	SO00
0	0	0	0	0	0	x	**1**

Bit 0

SO00	Serial data output of channel 0
0	Serial data output value is “0”.
1	Serial data output value is “1”.

Data output enabling of each channel

・Serial output enable register 0 (SOE0/SOE0L)

Output is enabled.

Symbol: SOE0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SOE01	SOE00
0	0	0	0	0	0	x	**1**

Bit 0

SOE00	Serial output enable or stop of channel 0
0	Stops output by serial communication operation.
1	Enables output by serial communication operation.

Caution: Refer to “RL78/G10 User’s Manual: Hardware” for the setup of the register.

Setup of interrupt mask

・Interrupt mask flag register 0L (MK0L)

Disables interrupt servicing.

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	x	**1**	**1**	**1**	x	x	x

Bit 5 - 3

SREMK0	SRMK0	STMK0	Interrupt servicing control
0	0	0	Interrupt servicing enabled
1	**1**	**1**	Interrupt servicing disabled

Setup ports

・Port register 0 (P0)

・Port mode register 0 (PM0)

Sets a port for transmitting data and receiving data respectively.

Symbol: P0

7	6	5	4	3	2	1	0
0	P06Note	P05 Note	P04	P03	P02	P01	P00
0	x	x	x	x	x	x	**1**

Note 16-pin products only.

Bit 0

P00	Output data control (in output mode)
0	Output 0
1	Output 1

Symbol: PM0

7	6	5	4	3	2	1	0
1	PM06 Note	PM05 Note	PM04	PM03	PM02	PM01	PM00
1	x	x	x	x	x	**1**	**0**

Note 16-pin products only.

Bit 1

PM01	P01 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 0

PM00	P00 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution: Refer to “RL78/G10 User’s Manual: Hardware” for the setup of the register.

Entering the communication wait status

・Serial channel start register 0 (SS0)

Starts the operation.

Symbol: SS0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SS01	SS00
0	0	**0**	**0**	**0**	0	0	**1**

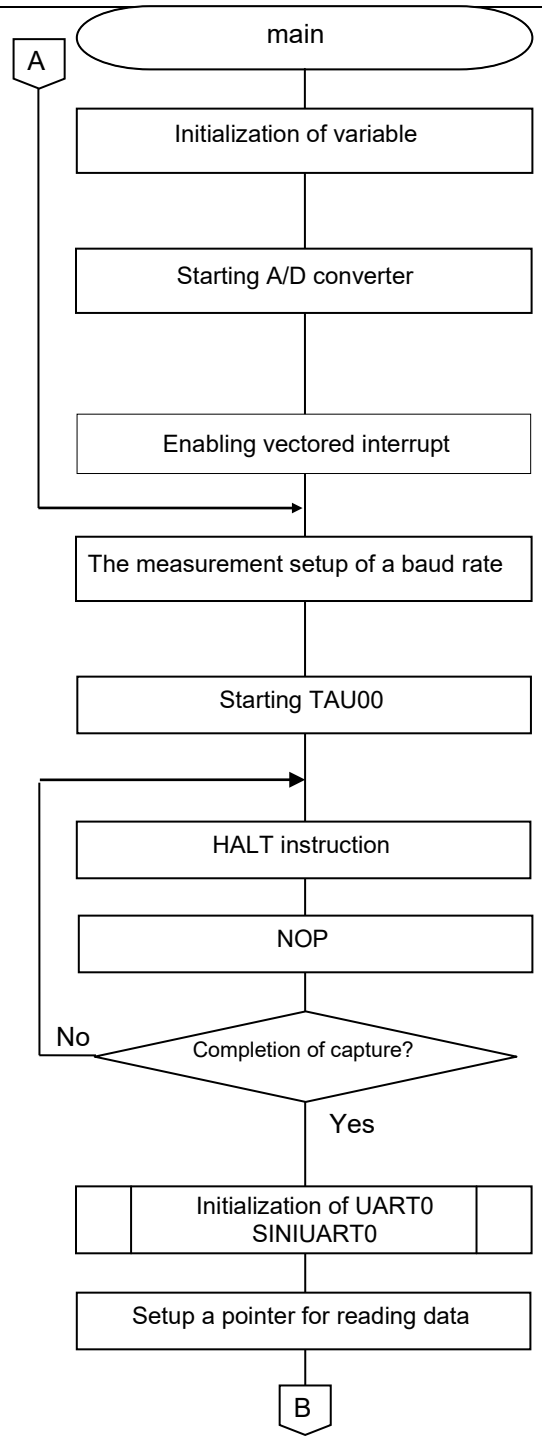
Bit 0

SS00	Operation start trigger of channel 0
0	No trigger operation
1	Sets the SE00 bit to 1 to suspend communication.

Caution: Refer to “RL78/G10 User’s Manual: Hardware” for the setup of the register.

5.7.7 Main Processing

Figure 5.8, Figure 5.9, and Figure 5.10 show the flowchart of main processing.



Clears buffer areas and storage area of average.
Variable SAVEPNT ← #LOWW ANIBUFF: For conversion data storing
Variable ADCHANNEL ← 1: Next conversion channel

ADCE bit ← 1: Enables A/D voltage comparator operation
ADIF bit ← 0: Clears INTAD interrupt request.
ADMK bit ← 0: Resets interrupt mask (XXMK).
ADCS bit ← 1: Starts A/D conversion.

IE bit ← 1: Vectored interrupt enabled

Variable SPSDATA ← 00H: Initializes prescaler.
Variable LPCOUNT ← 5 : Initializes the measurement counter.
Variable CAPTUREL ← 8 : Initializes the capture value.
Variable CAPTUREH ← 0 : Initializes the capture value.

TMIF00 bit ← 0 : Clears interrupt request.
TMMK00 bit ← 0 : Resets interrupt mask
TS0.0 bit ← 1 : Starts TAU00.

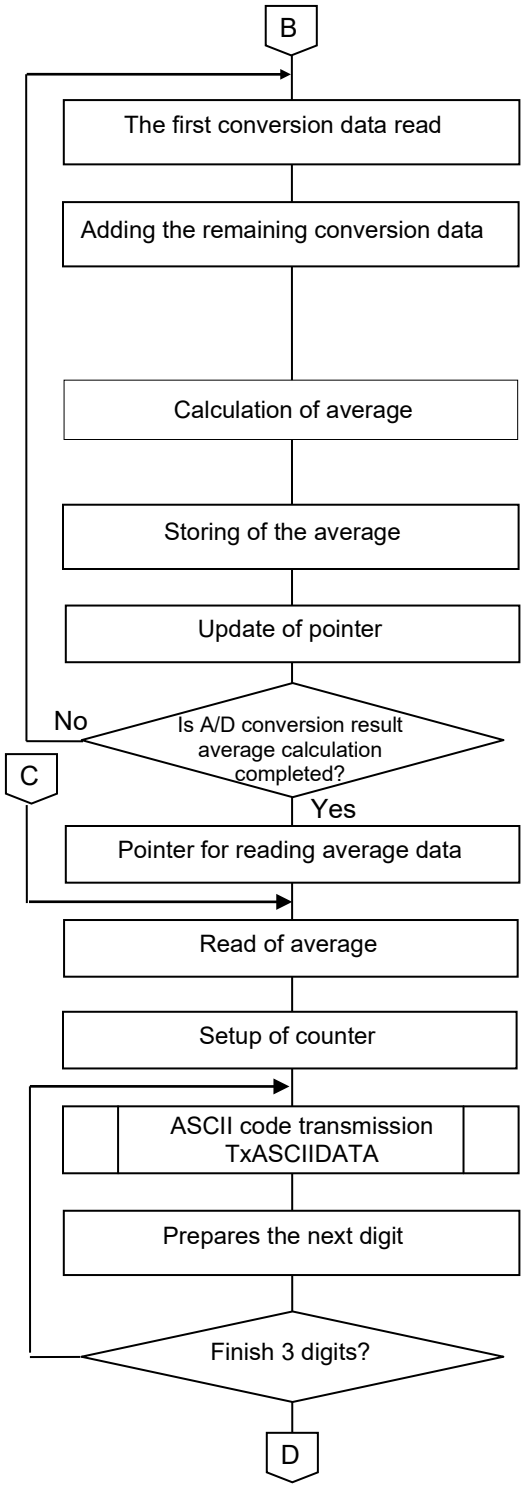
Waits for completion of capture in HALT mode.

Waits for input pulse interval measurement completion (LPCOUNT＝0).

Initializes UART0 according to the baud rate of the master.

HL register ← #LOWW ANIBUFF:
Sets a pointer for reading A/D Conversion Result.

Figure 5.8 Main Processing (1/3)



AX register ← [HL]: Reads the first conversion data.

AX register ← AX register + [HL+n]
: Adds the remaining conversion data.
n: 8, 16, 32……(Offset of conversion data.)
Definition of DATA4: Adds data for four pieces.
Definition of DATA8: Adds data for eight pieces.

AX register ← Shifts AX register to the right by the number of following bits.
Definition of DATA4: Shifts to the 2-bit right. (Divides it by 4.)
Definition of DATA8: Shifts to the 3-bit right. (Divides it by 8.)

[HL+64] ← AX register: Stores average to buffer of each channel.

L register ← L register + 2
: Updates a pointer to the following channel.

HL register ← #LOWW ANIAVERAGE
: A pointer for average data.

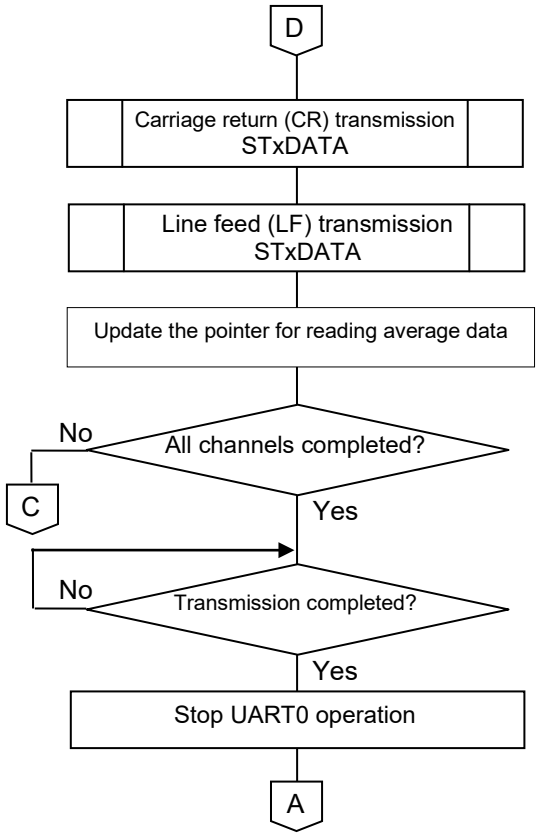
AX register ← [HL]: Reads average data.

B register ← 3: Sets the number of digits of transmission data.

Changes lower 4 bits of A register into an ASCII code, and transmits from UART0.

AX register ←Shifts AX register to the 4-bit left.

Figure 5.9 Main Processing (2/3)



Sets 0DH (CR code) to A register and calls transmitting subroutine. (UART transmission)

Sets 0AH (LF code) to A register and calls transmitting subroutine. (UART transmission)

L register ← L register + 2
: Updates a pointer to the following channel.

Performs the transmission for all channels.

If transmission of all the channels finishes, waits for the completion of transmitting of UART.

Stop UART0 operation and waits for the following request to send.

Figure 5.10 Main Processing (3/3)

Starting of the AD converter

・A/D converter mode register 0 (ADM0)

Starts A/D conversion.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	0	0	FR1	FR0	0	LV0	ADCE
1	0	0	0	1	0	0	**1**

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation (conversion stopped/standby status)
1	Enables conversion operation (conversion operation status)

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Enabling A/D converter interrupt

・Interrupt mask flag registers (MK0H)

Cancels the interrupt mask.

Symbol: MK0H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRMK	ADMK	TMMK01
1	1	1	1	1	x	**1**	x

Bit 1

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution: Refer to “RL78/G10 User’s Manual: Hardware” for the setup of the register.

Control of UART0 transmission

- Serial status register 00 (SSR00)
  Confirms completion of transmission.
- Serial channel stop register 0 (ST0)
  Stops UART0 operation.

Symbol: SSR00

7	6	5	4	3	2	1	0
0	TSF00	BFF00	0	0	0	PEF00	OVF00
0	**0/1**	**0/1**	0	0	0	x	x

Bit 6

TSF00	Communication status indication flag of channel 0
0	Communication is stopped or suspended.
1	Communication is in progress.

Bit 5

BFF00	Buffer register status indication flag of channel 0
0	Valid data is not stored in the SDR00L register.
1	Valid data is stored in the SDR00L register.

Symbol: ST0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ST01	ST00
0	0	0	0	0	0	x	**1**

Bit 0

ST00	Operation stop trigger of channel 0
0	No trigger operation
1	Clears the SE00 bit to 0 and stops the communication operation

Caution: Refer to “RL78/G10 User’s Manual: Hardware” for the setup of the register.

5.7.8 ASCII Conversion Processing

Figure 5.11 shows the flowchart of ASCII conversion processing.

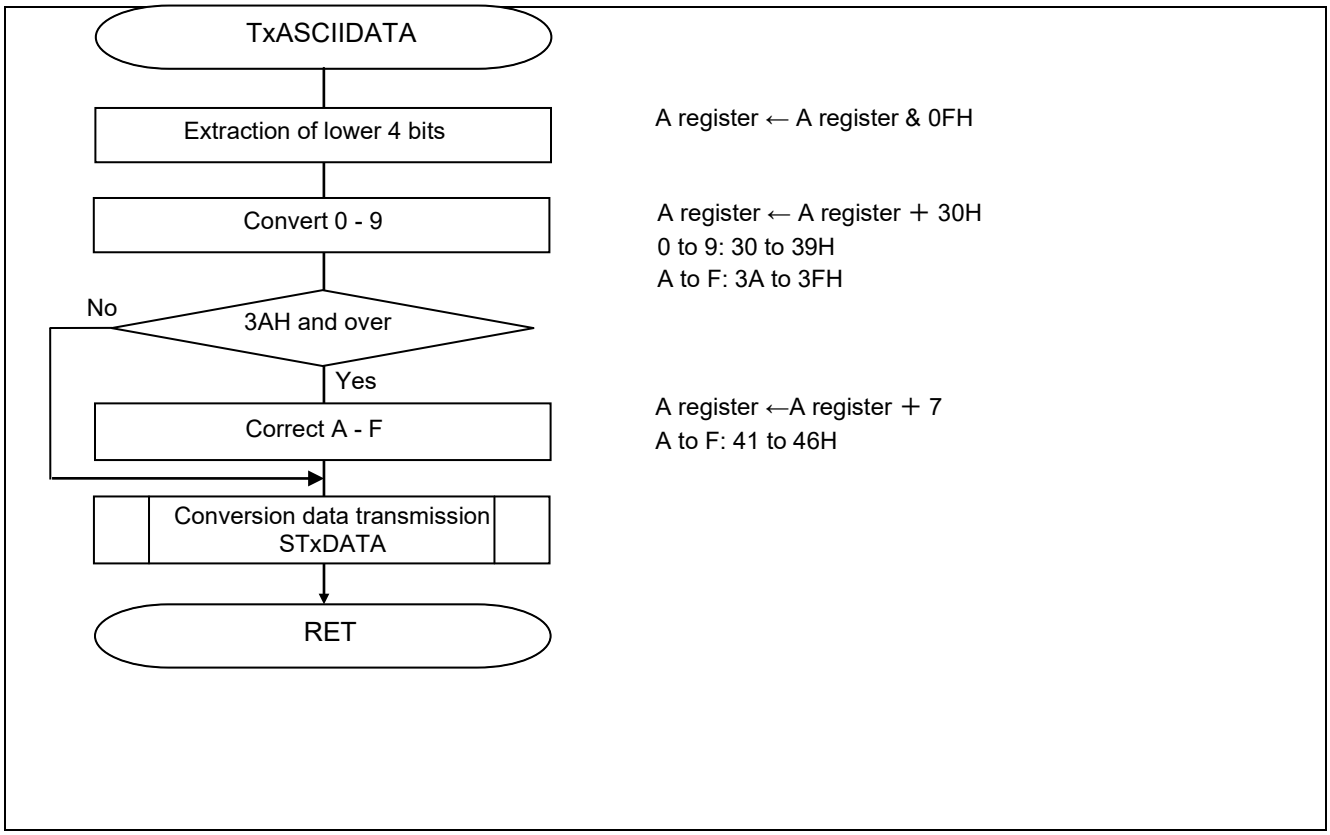


Figure 5.11 ASCII Conversion Transmission

5.7.9 UART Transmission Processing

Figure 5.12 shows the flowchart of ASCII conversion transmission and UART transmission processing.

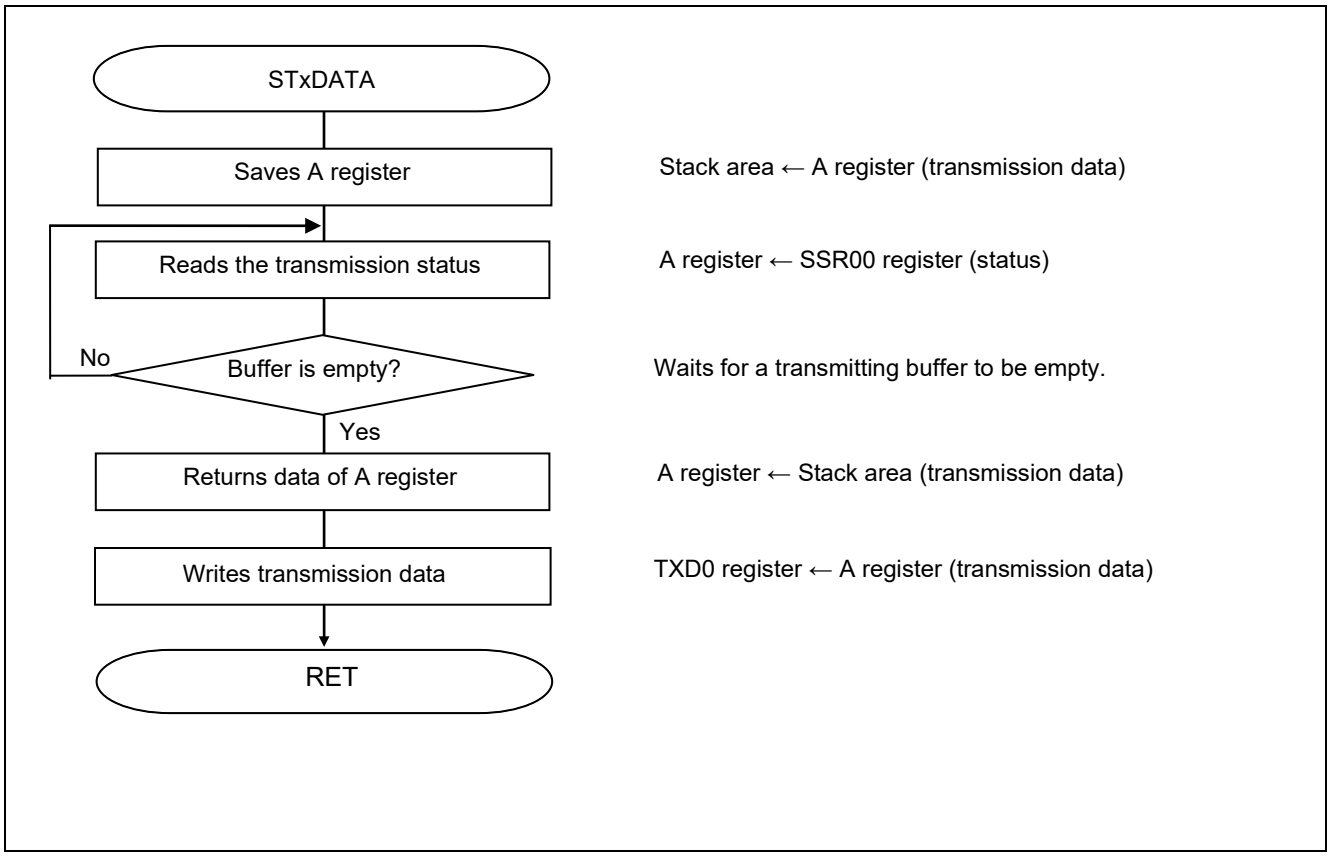


Figure 5.12 UART Transmission Processing

UART0 transmitting timing check

・Serial status register 00 (SSR00)

Confirms transmit data writing enabled.

Symbol: SSR00

7	6	5	4	3	2	1	0
0	TSF00	BFF00	0	0	0	PEF00	OVF00
0	x	**0/1**	0	0	0	x	x

Bit 5

BFF00	Buffer register status indication flag of channel 0
0	Valid data is not stored in the SDR00L register.
1	Valid data is stored in the SDR00L register.

UART0 data transmission

・Serial data register 00（TXD0）

Transmit data writing.

Symbol: TXD0

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
Transmit data							

Caution: Refer to “RL78/G10 User’s Manual: Hardware” for the setup of the register.

5.7.10 A/D Conversion End Interrupt Processing

Figure 5.13 shows the flowchart of A/D conversion end interrupt processing.

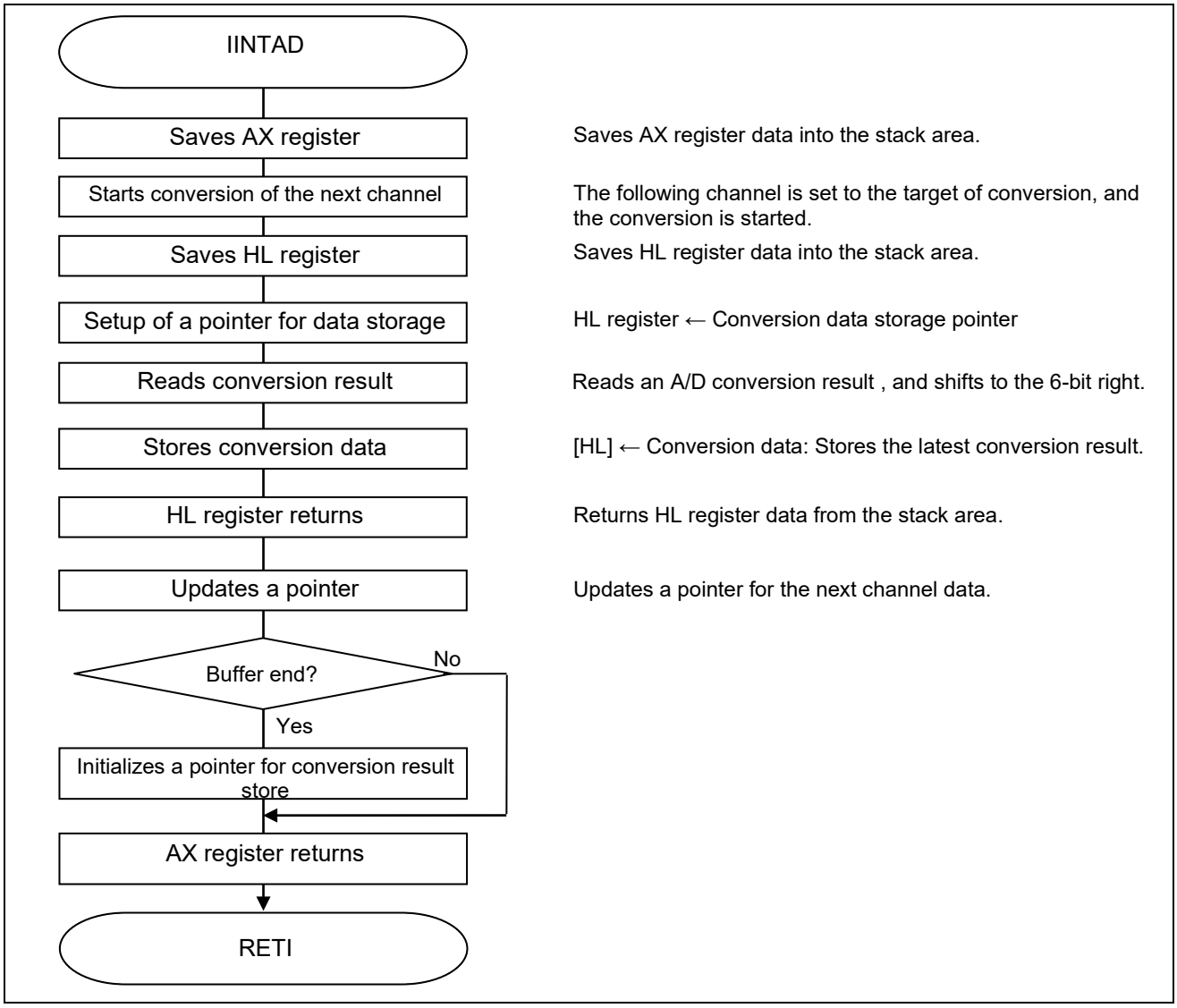


Figure 5.13 A/D Conversion End Interrupt Processing

5.7.11 IINTTM00 Interrupt Processing

Figure 5.14 and Figure 5.15 show the flowchart of IINTTM00 interrupt processing.

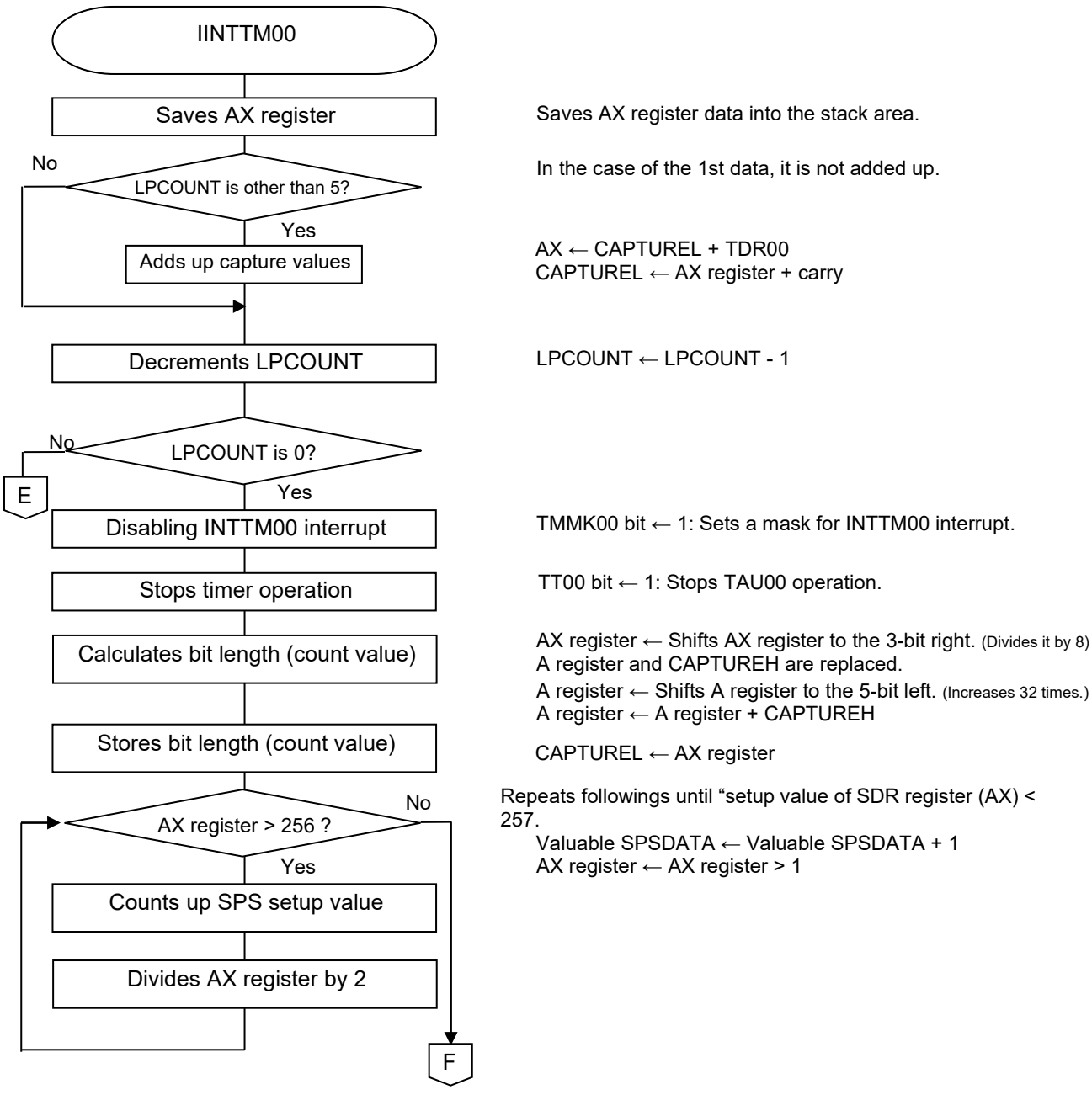


Figure 5.14 IINTTM00 Interrupt Processing (1/2)

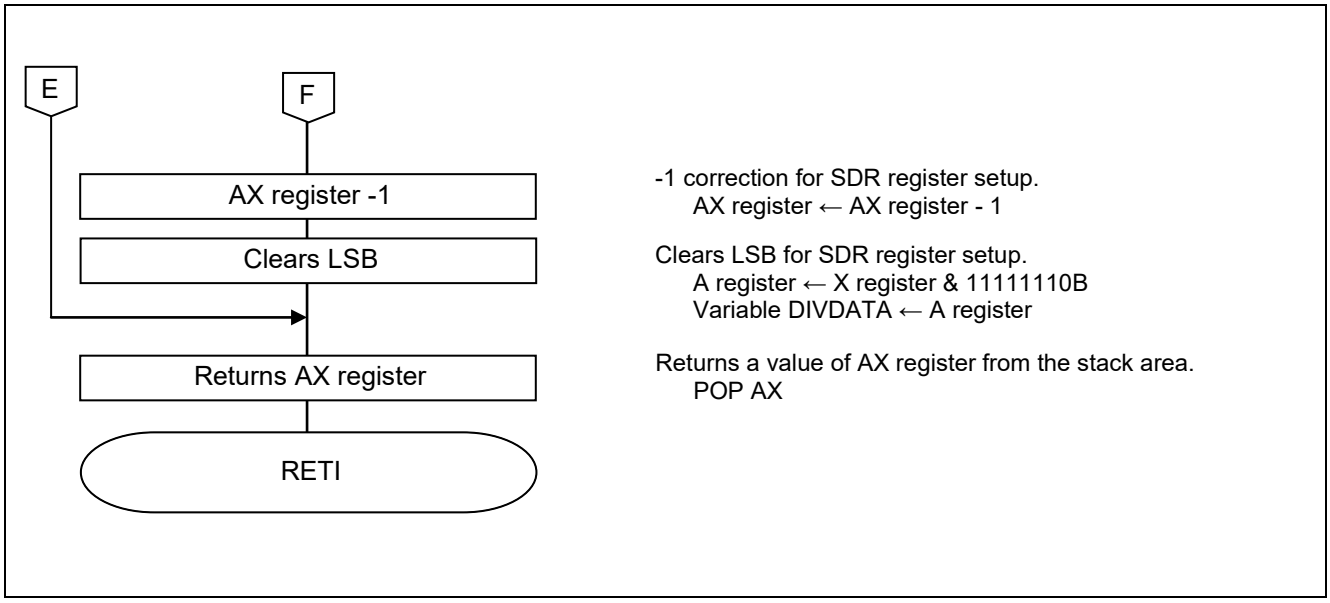


Figure 5.15 IINTTM00 Interrupt Processing (2/2)

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G10 User's Manual: Hardware (R01UH0384E)
RL78 Family User's Manual: Software (R01US0015E)
(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2014.09.25	-	First Edition
1.10	2022.09.30	6	Delete IAR information from Table 2.1

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.