RL78/G10

Timer Array Unit (Pulse Interval Measurement) CC-RL

Introduction

This application note describes how the timer array unit (TAU) measures time intervals between pulses. This unit measures the time elapsed between pulses which arrive at the timer input pin (TI00). Then, it stores the measured value in the on-chip RAM.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note provides an example of measuring intervals between input pulses on channel 0 of the timer array unit (TAU). Each time a valid edge is detected on the timer input pin (TI00), the count value of the timer is captured to measure the pulse interval. The measurement result is stored in the on-chip RAM.

Table 1.1 lists the peripheral functions to be used and their uses. Figure 1.1 presents the outline of the pulse interval measurement.

Table 1.1 Required Peripheral Functions and their Uses

Peripheral function	Use
Timer array unit channel 0	Measurement of the time interval between input pulses on the timer input pin (TI00)
TI00	Input pin for pulse signals

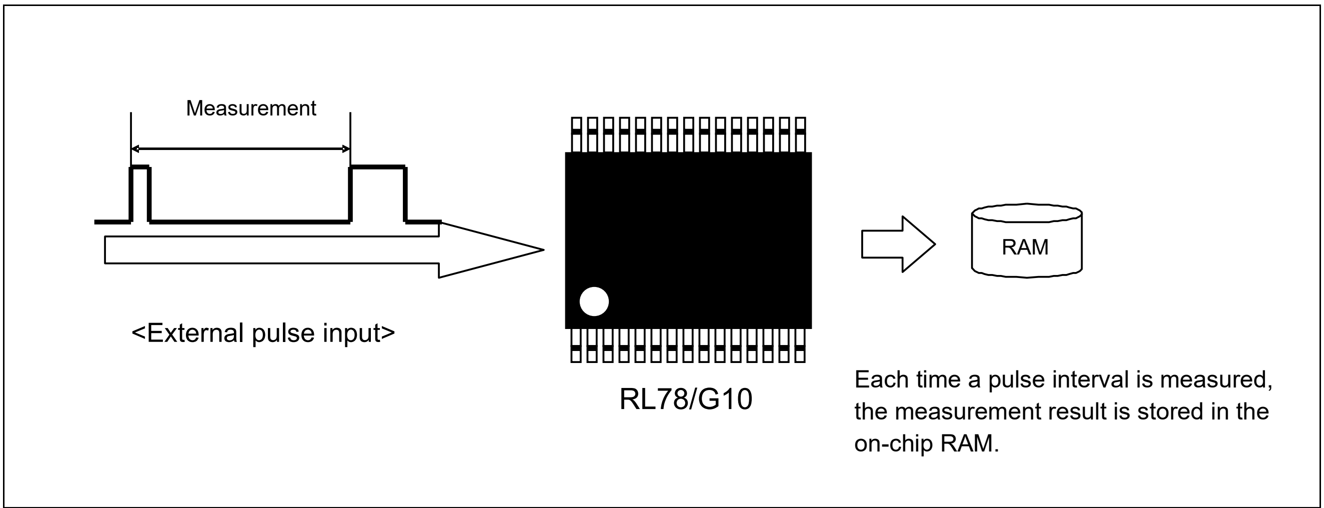

Figure 1.1 Outline of Pulse Interval Measurement

1.1 Maximum Frequency of Measurable Input Pulses

In this sample code, the maximum frequency of measurable input pulses is determined by the processing time of an INTTM00 interrupt. It takes 15 clocks for this sample code to complete interrupt processing after starting it. With the worst value of the interrupt response time (16 clocks) added to this, it takes 31 clocks, equal to a frequency of 770 kHz.

In this case, the interval between each input pulse is measured. If occasional measurement is allowed, the maximum frequency is the same as that of the timer input signal.

In order to measure a frequency of 770 kHz or higher, it is possible to perform DMA transfer. If the timer count clock is 6 MHz, the interval between pulses that can be input can be estimated to be approximately 2 count clocks or more. This is almost the same as the maximum frequency of timer input signals (should be assumed to be 2 MHz for safety).

1.2 Minimum Frequency of Measurable Input Pulses

The minimum frequency of measurable input pulses is determined by the overflow time of a 16-bit timer. In this application note, since a 6-MHz count clock is used for operation, counting with 16 bits allows measurement for up to approximately 92 Hz (If, in this case, the occurrence of overflow is allowed only once, this is equivalent to measuring time with 17 bits, allowing measurement for up to 46 Hz).

This sample code performs operation with up to 16 bits by default. To carry out measurement with 17 bits, change “$SET(SMALL)” to “$RESET(SMALL)” in the beginning of r_main.asm and perform a build. This reduces the minimum frequency in half, but doubles the memory necessary to store measurement data.

To measure the interval between pulses with a frequency less than this, change the setting of the TPS0 register to lower the frequency of the count clock (fMCK). The measurement accuracy is reduced but measurable frequencies can be lowered.

1.3 Measurement Results

The measurement results stored in the on-chip RAM vary depending on whether “$SET(SMALL)” or “$RESET(SMALL)” is used.

(1) If “$SET(SMALL)” is used

The correct measurement results are within the range of 0006H to 0FFFFH. If an overflow occurs, the measurement result is 0000.

Measurement results are stored from the end of the storage area (results are little-endian).

The start of the area The end of the area

Eighth value	Seventh value	Sixth value	...	Third value	Second value	First value

(2) If “$RESET(SMALL)” is used

Measurement results are represented in 17 bits, and reliable data are in the range from 0006H to 0FFFFH. Data within the range of 10000H to 1FFFFH are correct only if pulses with a frequency of more than approximately 46 Hz are input. The measurement results are stored as 4-byte data in the storage area.

The start of the area The end of the area

Eighth value		Seventh value	...	Second value	First value	
Value of TDR00	Value of TSR00	Value of TDR00	...	Value of TSR00	Value of TDR00	Value of TSR00

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y16ASP)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 20 MHz • CPU/peripheral hardware clock: 20 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 to 5.5 V.) SPOR operation: falling down 2.84V, falling up 2.90V (Reset occurrence: VDD<2.82V, Reset release: VDD>=2.88V)
Integrated development environment(CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
Assembler(CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment(e^2 studio)	e^2 studio V4.1.0.018 from Renesas Electronics Corp.
Assembler(e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment(IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.3 from IAR Systems.
Assembler(IAR)	IAR Assembler for Renesas RL78 V4.21.2.2420 from IAR Systems.
Board to be used	RL78/G10 target board (QB-R5F10Y16-TB).

3. Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G10 Initialization CC-RL (R01AN2668E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

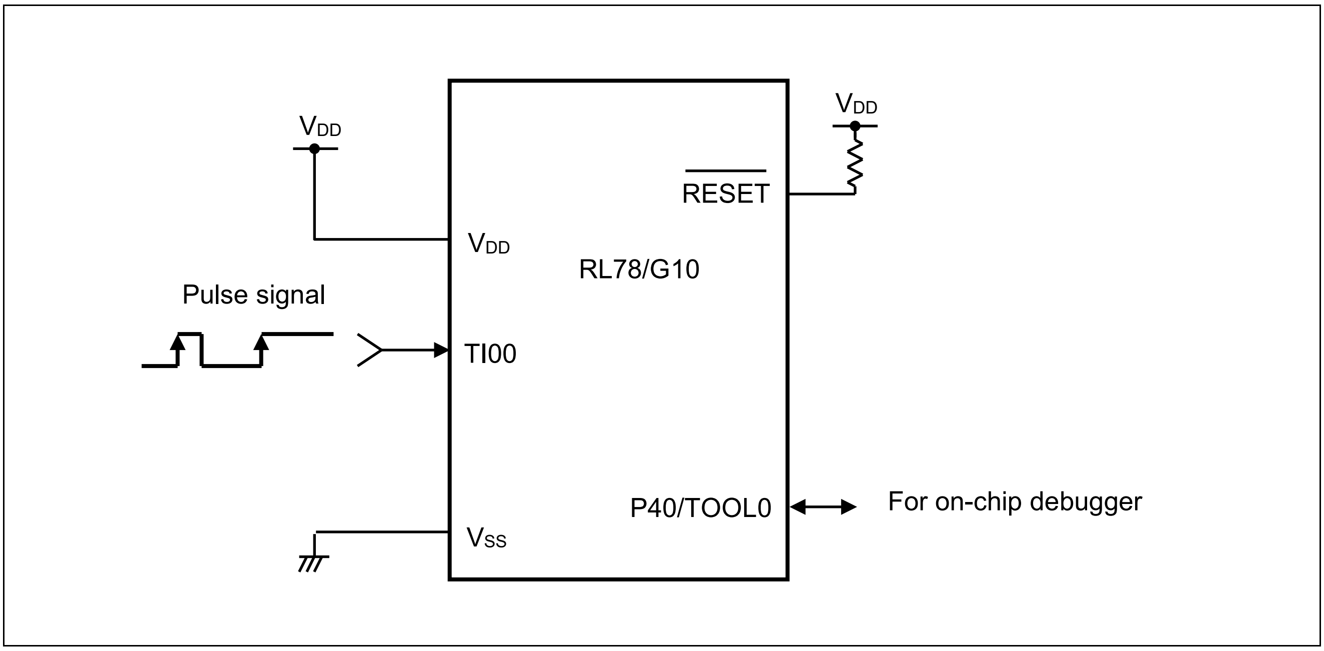

Figure 4.1 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the reset release voltage (V_{SPOR}) that is specified as SPOR.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pin to be Used and Its Function

Pin Name	I/O	Description
P13/TI00	Input	Inputs pulse signals to the 16-bit timer 00.

5. Description of the Software

5.1 Operation Outline

Each time a rising edge (valid edge) is detected on the timer input pin (TI00), the sample code described in this application note captures the count value of the timer and measures the time interval between pulses which arrive at the timer input pin (TI00). When a timer interrupt (INTTM00) occurs upon completion of the capture, the sample code calculates the pulse interval and stores the calculation result in the on-chip RAM.

(1) Initialize the TAU.
<Conditions for setting>

- Use the P13/TI00 pin (for 20/24-pin products. P00/TI00 for 30-pin products) to input pulses.
- Set the operation clock of TAU channel 0 to f_{CLK}/4.
- Set TAU channel 0 to the capture mode.
- Selects “rising edge detection” as the input edge on the TI00 pin.
- Selects the TI00 pin input valid edge to trigger the capture.

(2) Set the TS00 bit of the timer channel start register 0 (TS0) to 1 to enable count operation. This clears the timer count register (TCR00) to 0000H and starts counting.

(3) When a valid edge is detected, the value of the timer count register (TCR00) is captured and put into the timer data register (TDR00). A timer interrupt (INTTM00) occurs upon completion of the capture. The timer count register (TCR00) is cleared to 0000H and the TAU waits for the next valid edge input.
An invalid value is captured when a timer interrupt (INTTM00) occurs upon completion of the first capture. This data is not used.

(4) In the processing of a timer interrupt (INTTM00) which occurs upon completion of the second capture, the timer data register (TDR00)’s value (pulse width) is stored in the on-chip RAM.

(5) The operation described in (4) is repeated eight times. Then, the TAU transitions to the HALT state.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	01111111B	LVD reset mode 2.81 V (2.76 to 2.87 V)
000C2H	11100000B	HS mode HOCO: 24 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constant that is used in this sample program.

Table 5.2 Constant for the Sample Program

Constant	Setting	Description
CAPTIMES	8	Indicates the number of times measurement is performed.

5.4 List of Variables

Table 5.3 lists the global variables.

Table 5.3 Global Variables

Type	Variable Name	Contents	Function Used
8 bits	RPWCNT	The number of remaining attempts to measure pulse intervals	main() IINTTM00
16-bit array Note 1	RPWLENG	Pulse interval measurement values	main() IINTTM00

Note 1. 17-bit length. 32-bit length for measurement.

5.5 List of Functions (Subroutines)

Table 5.4 lists the functions (subroutines) that are used by this sample program.

Table 5.4 List of Functions (Subroutines)

Function Name	Outline
SSTARTPW	TAU0 channel 0 start processing
IINTTM00	INTTM00 interrupt processing

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] SSTARTPW

Synopsis	TAU0 channel 0 start processing
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] IINTTM00

Synopsis	INTTM00 interrupt processing
Explanation	This function stores the measured value of the pulse time interval into RPWLENG.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

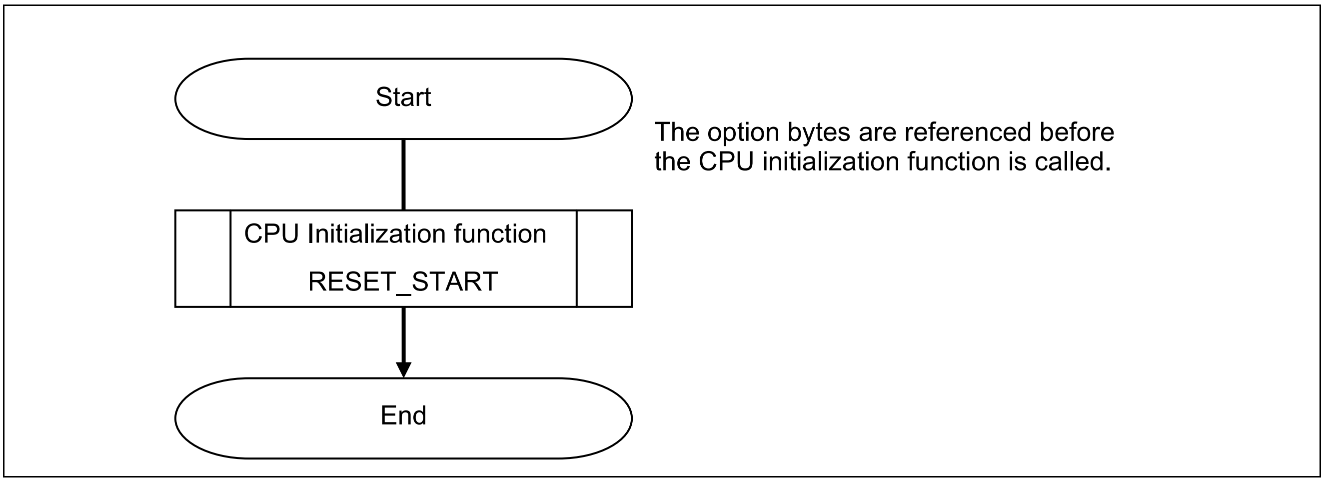

Figure 5.1 Overall Flow

5.7.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

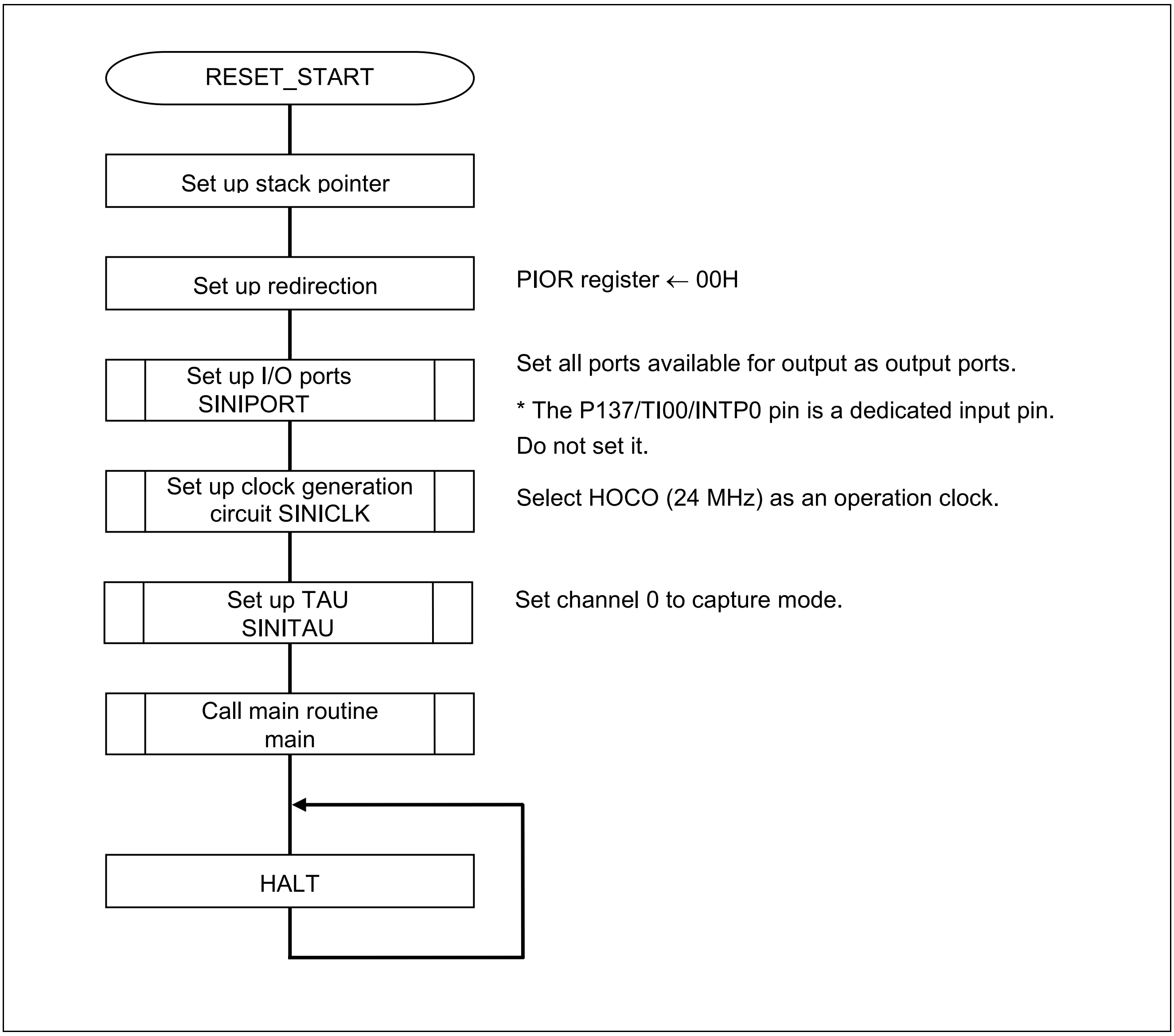

Figure 5.2 CPU Initialization Function

5.7.2 I/O Port Setup

Figure 5.3 shows the flowchart for setting up the I/O ports.

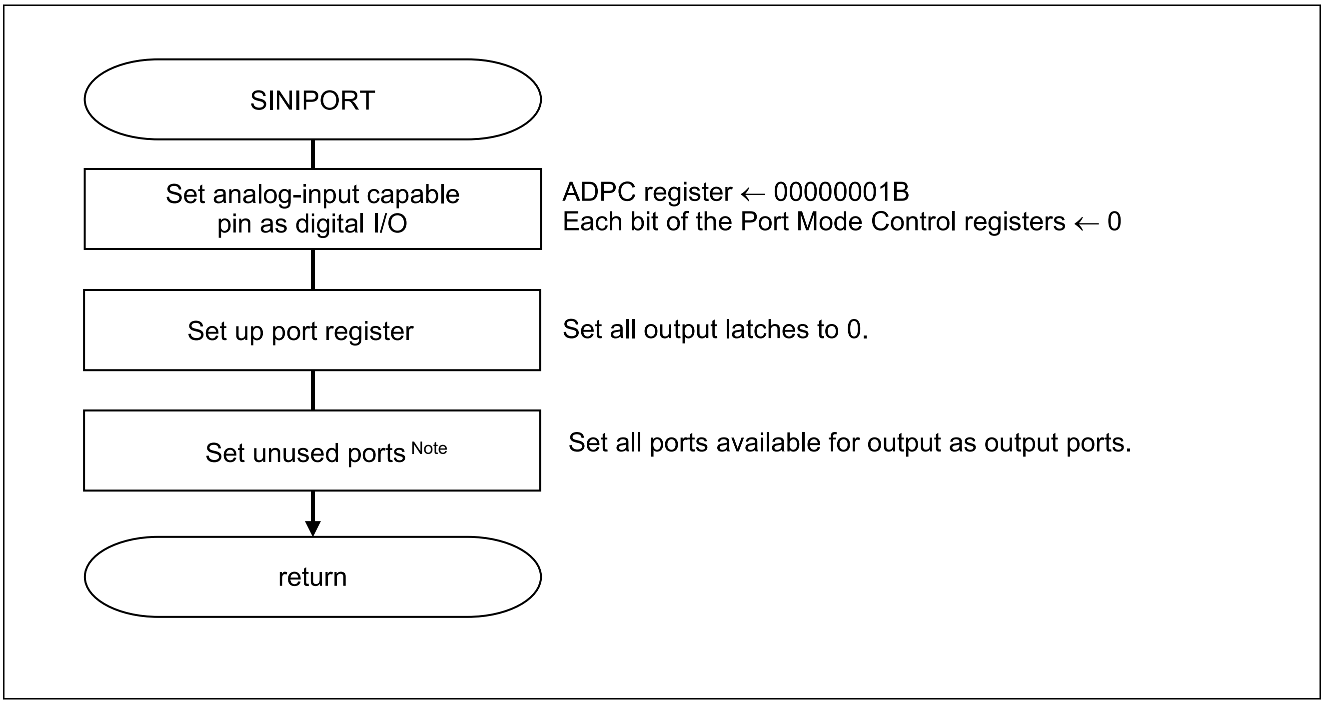

Figure 5.3 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G10 Initialization Application Note (R01AN1454E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.7.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for clock generation circuit setup.

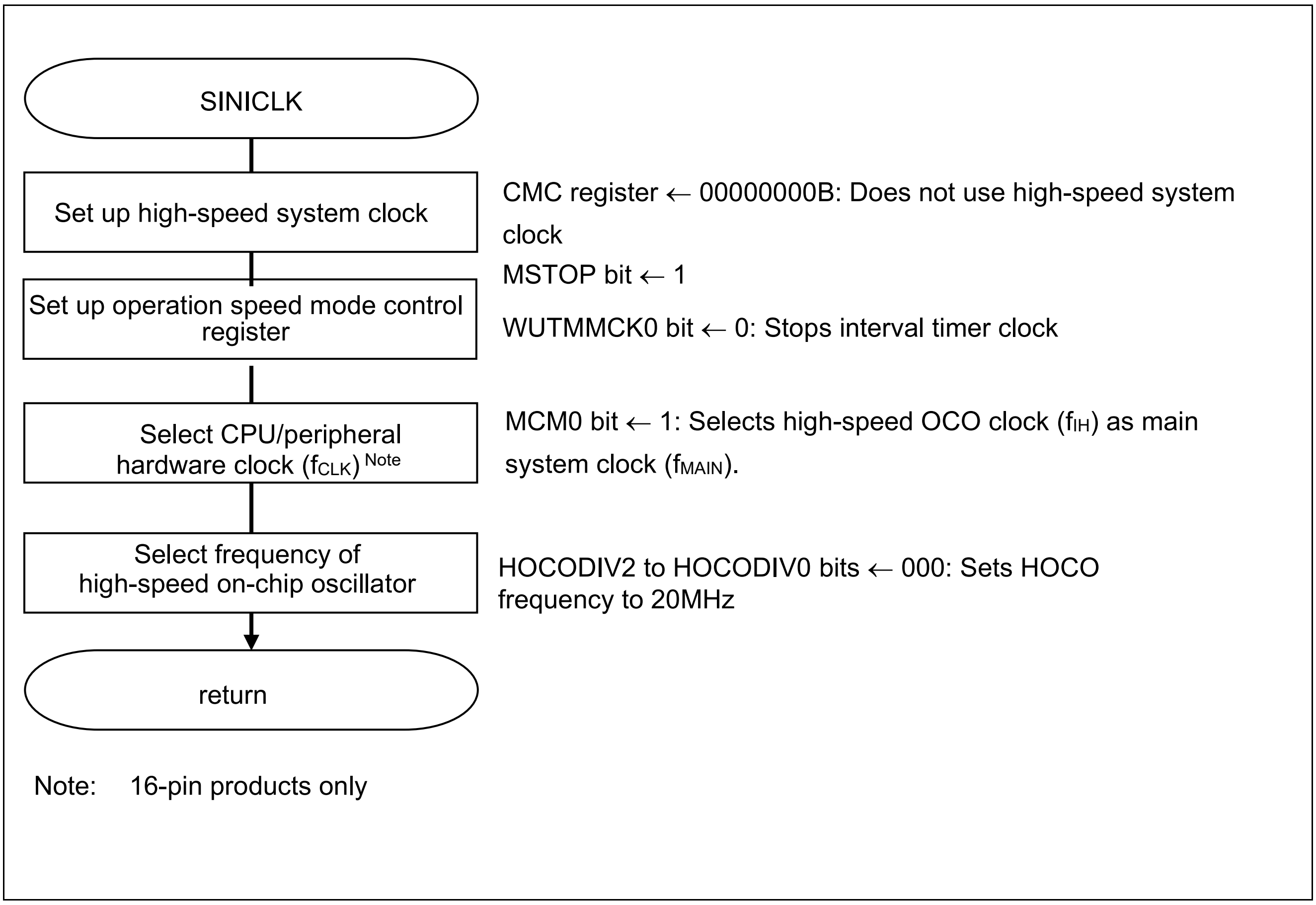

Figure 5.4 Clock Generation Circuit Setup

Caution: For details on the procedure for setting up the clock generation circuit (SINICLK), refer to the section entitled "Flowcharts" in RL78/G10 Initialization Application Note (R01AN1454E).

5.7.4 Timer Array Unit Setup

Figure 5.5 shows the flowchart for setting up the timer array unit.

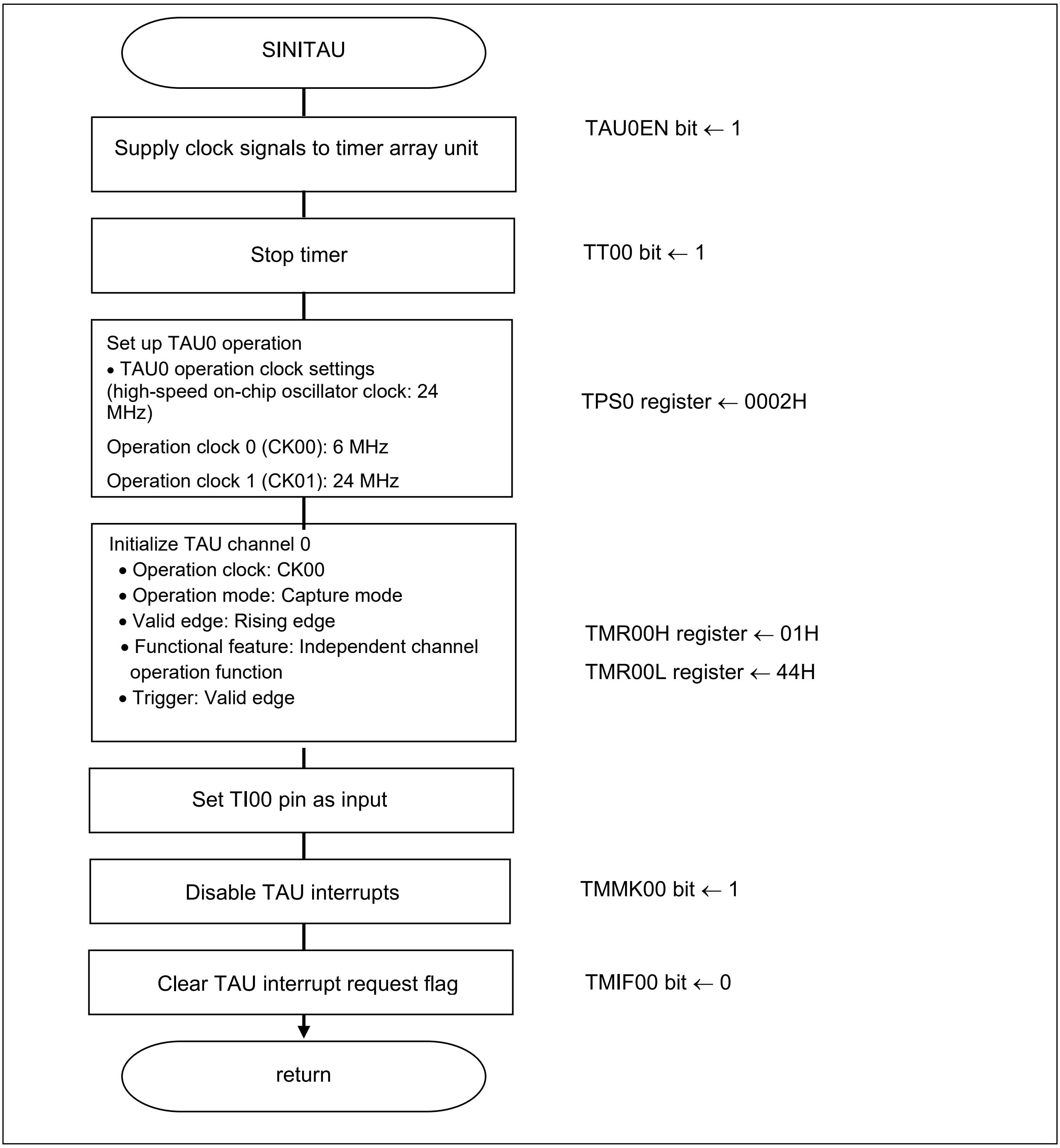

Figure 5.5 Timer Array Unit Setup

(1) Starting clock signal supply to the timer array unit

- Peripheral enable register 0 (PER0)
  Start supplying clock to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN 注	0	ADCEN	IICA0EN Note	0	SAU0EN	0	TAU0EN
x	0	x	x	0	x	0	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops supply of input clock.
1	**Supplies input clock.**

Note: 16-pin products only
Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

(2) Configuring the clock frequency

- Timer clock select register 0 (TPS0)
  Select an operation clock for CK00

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
					f_{CLK} = 1.25MHz	f_{CLK} = 2.5MHz	f_{CLK} = 5MHz	f_{CLK} = 10MHz	f_{CLK} = 20MHz
0	0	0	0	f_{CLK}	1.25MHz	2.5MHz	5MHz	10MHz	20MHz
0	0	0	1	$f_{CLK}/2$	625kHz	1.25MHz	2.5MHz	5MHz	10MHz
0	**0**	**1**	**0**	$f_{CLK}/2^2$	**313kHz**	**625kHz**	**1.25MHz**	**2.5MHz**	**5MHz**
0	0	1	1	$f_{CLK}/2^3$	156kHz	313kHz	625kHz	1.25MHz	2.5MHz
0	1	0	0	$f_{CLK}/2^4$	78kHz	156kHz	313kHz	625kHz	1.25MHz
0	1	0	1	$f_{CLK}/2^5$	39kHz	78kHz	156kHz	313kHz	625kHz
0	1	1	0	$f_{CLK}/2^6$	19.5kHz	39kHz	78kHz	156kHz	313kHz
0	1	1	1	$f_{CLK}/2^7$	9.8kHz	19.5kHz	39kHz	78kHz	156kHz
1	0	0	0	$f_{CLK}/2^8$	4.9kHz	9.8kHz	19.5kHz	39kHz	78kHz
1	0	0	1	$f_{CLK}/2^9$	2.5kHz	4.9kHz	9.8kHz	19.5kHz	39kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22kHz	2.5kHz	4.9kHz	9.8kHz	19.5kHz
1	0	1	1	$f_{CLK}/2^{11}$	625Hz	1.22kHz	2.5kHz	4.9kHz	9.8kHz
1	1	0	0	$f_{CLK}/2^{12}$	313Hz	625Hz	1.22kHz	2.5kHz	4.9kHz
1	1	0	1	$f_{CLK}/2^{13}$	152Hz	313Hz	625Hz	1.22kHz	2.5kHz
1	1	1	0	$f_{CLK}/2^{14}$	78Hz	152Hz	313Hz	625Hz	1.22kHz
1	1	1	1	$f_{CLK}/2^{15}$	39Hz	78Hz	152Hz	313Hz	625Hz

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

(3) Controlling the channel trigger operation

- Timer channel stop register 0 (TT0)
  Select the TAU0 stop trigger.

Symbol: TT0

7	6	5	4	3	2	1	0
0	0	0	0	TT03 注	TT02 注	TT01	TT00
0	0	0	0	0	0	0	**1**

Bit 0

TT00	Operation stop trigger of channel 0
0	No trigger operation
1	**Operation is stopped (stop trigger is generated).**

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

(4) Setting up the operation mode of channel 0

Timer mode register 00 (TMR00H, TMR00L)

Select an operation clock (f_{MCK}).

Select a count clock.

Set up the start trigger and capture trigger

Select the valid edge of TI00 pin.

- Set up the operation mode.

Symbol: TMR00H

7	6	5	4	3	2	1	0
CKS001	0	0	CCS00	0	STS002	STS001	STS000
0	0	0	**0**	0	**0**	**0**	**1**

Bit 7

CKS001	Selection of operation clock (f_{MCK}) of channel 0
0	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	Operation clock CK01 set by timer clock select register 0 (TPS0)

Bit 4

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of the input signal from the TI00 pin

Bits 2-0

STS 002	STS 001	STS 000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	**0**	**1**	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Symbol: TMR00L

7	6	5	4	3	2	1	0
CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**1**	0	0	**0**	**1**	**0**	**0**

Bits 7-6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	**1**	**Rising edge**
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bits 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Counting operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/Square wave output/Divider function /PWM output (master)	Counting down
0	**1**	**0**	1/**0**	**Capture mode**	**Input pulse interval measurement**	**Counting up**
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of the MD000 bit operation varies depending on each operation mode (see the table below).

Operation mode (Value set by the MD003 to MD001 bits) (See the above table)	MD000	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) **• Capture mode (0, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.7.5 Main Processing

Figure 5.6 shows the flowchart for main processing.

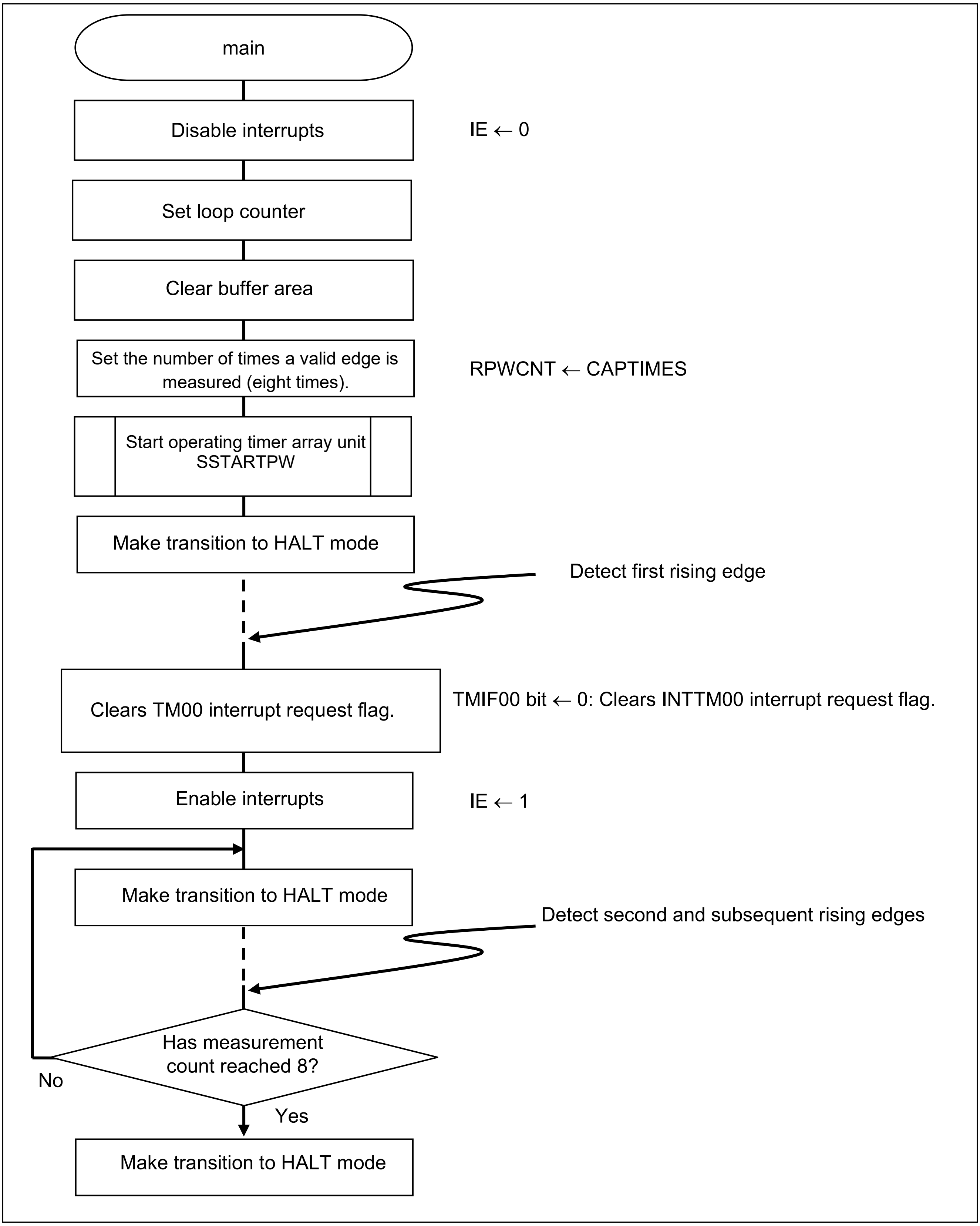

Figure 5.6 Main Processing

5.7.6 Timer Array Unit Startup

Figure 5.7 shows the flowchart for starting the operation of the timer array unit.

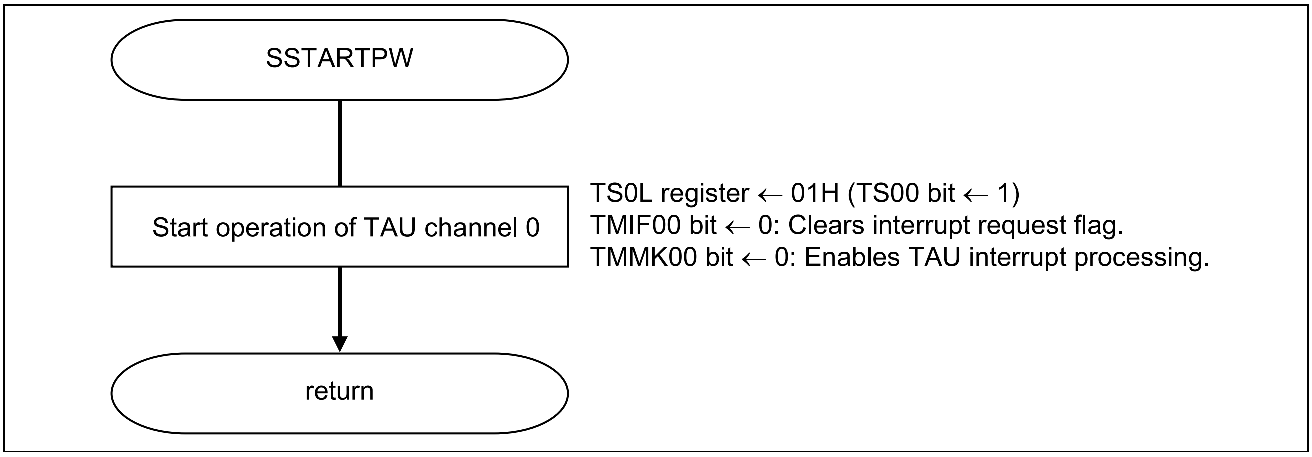

Figure 5.7 Timer Array Unit Startup

(1) Configuring the interrupt request flag

- Clear the timer interrupt request flag.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
0	x	x	x	x	x	x	x

Bit 6

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

(2) Configuring the interrupt mask

- Unmask timer interrupts.

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
0	x	x	x	x	x	x	x

Bit 6

TMMK00	Interrupt processing control
0	**Interrupt processing enabled**
1	Interrupt processing disabled

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

(3) Configuring the timer channel startup

- Enable timer count operation.

Symbol: TS0

7	6	5	4	3	2	1	0
0	0	0	0	TS03 Note	TS02 Note	TS01	TS00
0	0	0	0	x	x	x	**1**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.**

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.7.7 INTTM00 Interrupt Processing

Figure 5.8 shows the flowchart for INTTM00 interrupt processing.

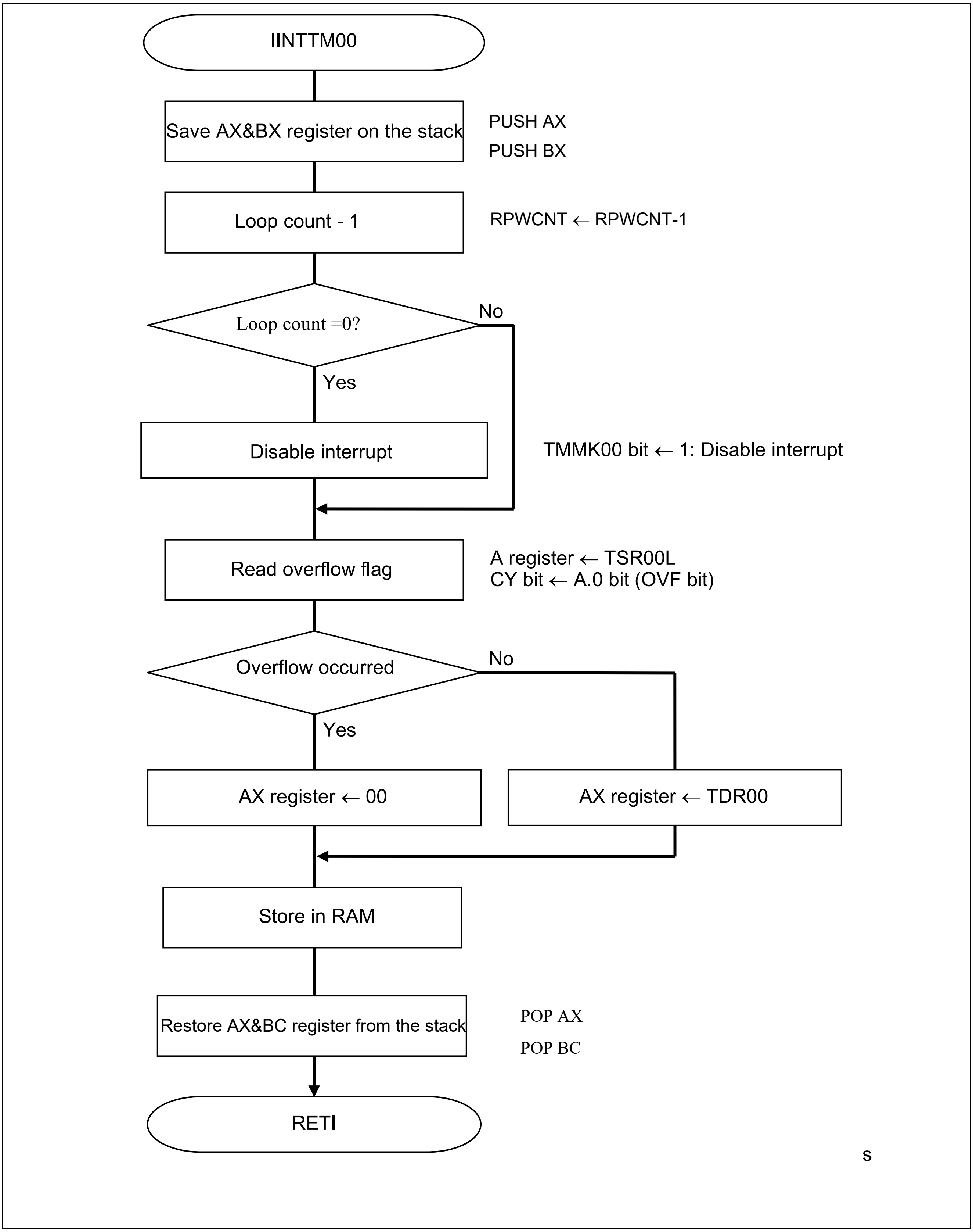

Figure 5.8 INTTM00 Interrupt Processing

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G10 User's Manual: Hardware Rev.3.00 (R01UH0384E)

RL78 Family User's Manual: Software Rev.2.20 (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 28. 2016	—	First edition issued
1.10	June. 24. 2022	5	Operation check condition is updated.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   - A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   - The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   - Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   - Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   - After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   - Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   - Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
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(Rev.5.0-1 October 2020)

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