Introduction

This application note explains how to use the dual input one-shot pulse output function to control the switched-mode power supply (SMPS or flyback converter).

Target Device

RL78/G10 16-pin (Part name: R5F10Y47, R5F10Y46, R5F10Y44)
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1. Basic Functions

The dual input one-shot pulse output function in the timer array can output a variation of one-shot pulses by changing the pin polarity of the timer output, triggering a valid edge of the timer input pin.

The following is an example of a current-controlled flyback converter using this function.

![Figure 1-1 Circuit Example](image)

GD: PWM signal
Ids: Drain source current
ZCD: Zero Current Detection signal
Peak: Peak current detection signal
Rs: Shunt resistor
Is: Secondary-side current

The MCU detects the peak signal of the current (Ids) during the ON state of switching device Q1 when the ZCD (Zero Current Detection) signal indicates the current (Is) flowing through the transformer coil is zero. Using these two edge signals for the timer module, the MCU then controls the Ids by outputting the one-shot pulse to Q1.
1.1 Peak Current Detection

Transistor Q2 is used to detect the peak current of Ids. Transistor Q2’s base and emitter pins are connected to both sides of shunt resistor Rs, which is connected to the Q1 source pin. The Q2 collector pin is connected to timer input pin TI03. As Ids increases, the Rs end-to-end voltage reaches the Vbe voltage of Q2 (∼0.6V). This turns Q2 ON and switches the input signal of TI03 to Low. This edge becomes the trigger to switch timer output pin TO03 to Low.

The timing of peak current detection shown in Figures 1-3.

![Peak Current Output Detection Using External Circuit](image1)

**Figure 1-2** Peak Current Output Detection Using External Circuit

![Timing Chart (peak current detection)](image2)

**Figure 1-3** Timing Chart (peak current detection)
1.2 ZCD Signal Detection

This application detects the zero timing of secondary-side current $I_s$ using the winding voltage of the transformer, as shown in Figure 1-4. The method used to detect this zero current $I_s$ is called Zero Current Detection (ZCD). When Q1 turns OFF, the energy accumulated in the transformer is transferred to the secondary side (winding). Because $I_s$ flows in the same direction as the diode on the secondary side, power is supplied to the output capacitor and the load. When all of the accumulated energy is transferred from the transformer, the ZCD signal goes to Low. This edge is input to timer input pin T10x and the PWM signal switches to High.

The timing of ZCD signal detection as shown in Figures 1-5.
2. Pin Assignment Example

Table 2-1 shows RL78/G10 pin assignments for the circuit example described above.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Port</th>
<th>A/D</th>
<th>Comparator</th>
<th>SIF</th>
<th>Timer</th>
<th>External</th>
<th>Other</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>P41</td>
<td></td>
<td></td>
<td></td>
<td>TI03</td>
<td>INTP2</td>
<td></td>
<td>Peak current detection</td>
</tr>
<tr>
<td>2</td>
<td>P40</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>KR0</td>
<td>TO01/</td>
<td>TOOL0/ (PCLBUZ0)</td>
</tr>
<tr>
<td>3</td>
<td>P125</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>KR1</td>
<td></td>
<td>RESET</td>
</tr>
<tr>
<td>4</td>
<td>P137</td>
<td></td>
<td></td>
<td></td>
<td>TI00</td>
<td>INTP0</td>
<td></td>
<td>ZCD signal detection</td>
</tr>
<tr>
<td>5</td>
<td>P122</td>
<td></td>
<td>(INTP2)</td>
<td></td>
<td></td>
<td>X2/</td>
<td></td>
<td>EXCLK</td>
</tr>
<tr>
<td>6</td>
<td>P121</td>
<td></td>
<td>(INTP3)</td>
<td></td>
<td></td>
<td>X1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>Vss</td>
<td></td>
<td></td>
<td></td>
<td>GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>Vdd</td>
<td></td>
<td></td>
<td></td>
<td>5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>P00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SO00/</td>
<td></td>
<td>INTP1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TXD0</td>
<td></td>
<td></td>
<td>SIO00/</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RXD0/ SDA00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>P01</td>
<td>ANI0</td>
<td></td>
<td></td>
<td></td>
<td>SIO00/</td>
<td></td>
<td>KR2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RXD0/ SDA00</td>
<td></td>
<td></td>
<td>SIO00/</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SIO00/</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>P02</td>
<td>ANI1</td>
<td>VOUT0</td>
<td></td>
<td></td>
<td>SCK00/</td>
<td></td>
<td>KR3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SIO00/</td>
<td></td>
<td>PCLBUZ0</td>
</tr>
<tr>
<td>12</td>
<td>P03</td>
<td>ANI2</td>
<td>IVCMP0</td>
<td></td>
<td></td>
<td>TO00</td>
<td></td>
<td>KR4/ (INTP1)</td>
</tr>
<tr>
<td>13</td>
<td>P04</td>
<td>ANI3</td>
<td>IVREF0</td>
<td></td>
<td></td>
<td>TI01/</td>
<td></td>
<td>KR5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TO01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>P05</td>
<td>ANI4</td>
<td></td>
<td></td>
<td></td>
<td>SO01</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TI02/</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TO02</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>P06</td>
<td>ANI5</td>
<td>SCLA0/ SIO1</td>
<td></td>
<td></td>
<td>SCLA0/</td>
<td></td>
<td>INTP3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SIO1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>P07</td>
<td>ANI6</td>
<td>SDA0/ SCK01</td>
<td></td>
<td></td>
<td>SDA0/</td>
<td></td>
<td>TO03</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SCK01</td>
<td></td>
<td>PWM signal</td>
</tr>
</tbody>
</table>
3. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 3.1 Operation Check Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller used</td>
<td>RL78/G10 (R5F10Y47, R5F10Y46, R5F10Y44)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>• High-speed on-chip oscillator (HOCO) clock: 20MHz</td>
</tr>
<tr>
<td></td>
<td>• CPU/peripheral hardware clock: 20MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) SPOR detection voltage: Rising edge voltage: 2.90V</td>
</tr>
<tr>
<td></td>
<td>: Falling edge voltage: 2.84V</td>
</tr>
<tr>
<td>Integrated development environment</td>
<td>CS+ for CC V3.01.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>(CS+)</td>
<td>Assembler (CS+) CC-RL V1.01.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development environment</td>
<td>e² studio V4.1.0.018 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>(e² studio)</td>
<td>Assembler (e² studio) CC-RL V1.01.00 from Renesas Electronics Corp.</td>
</tr>
</tbody>
</table>

4. Peripheral Function Settings

The following tables describe the peripheral function settings for RL78/G10.

Table 4-1 Peripheral Function Settings

<table>
<thead>
<tr>
<th>Function</th>
<th>Ch</th>
<th>Setting</th>
</tr>
</thead>
</table>
| TAU               | Ch0,3| • For switching  
|                   |      | • Operating mode: dual input one-shot pulse output  
|                   |      |   TI00: peak current detection  
|                   |      |   TI03: ZCD signal detection  
|                   |      |   TO03: PWM signal output  
| 12-bit interval timer| -   | • For main interval count (200us interval)                                                  |

Table 4-2 Option Byte Setting

<table>
<thead>
<tr>
<th>Address</th>
<th>Setting Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000C0H</td>
<td>1110 1110B</td>
<td>• Watchdog timer not used</td>
</tr>
</tbody>
</table>
| 000C1H  | 1111 0111B    | • SPOR detection voltage:  
|          |               |   Falling edge: VDD < 2.84V  
|          |               |   Rising edge: VDD >= 2.90V                                                                  |
| 000C2H  | 1111 1001B    | • High-speed on-chip oscillator (20MHz)                                                            |
| 000C3H  | 1000 0101B    | • Enables on-chip debug operation                                                                |
5. Flowcharts

5.1 Main and Peripheral Function Initialization

The following flowchart is an example of main processing and peripheral function initialization.

![Main Processing Flow Diagram](image-url)
5.2 Clock Generation Circuit Initialization

The following flowchart is an example of the clock generation circuit initialization.

Initialize clock

Set CMC register
- Input port mode
- $1\text{MHz} \leq f_x \leq 10\text{MHz}$

Set MSTOP bit
- Input port

Set MCM0 bit
- Select $f_{MX}$ as $f_{MAIN}$

Set OSMC register
- Supply $f_{IL}$

Set HIOSTOP bit
- Start high-speed on-chip oscillator clock

end

Figure 5-2 Clock Generation Circuit Initialization Flowchart
5.3 TAU Initialization

The following flowchart shows the initialization of the timer array unit (TAU).

![TAU Initialization Flowchart (1)]
Set TMR03H register
  • Operating clock: CK00
  • Count clock: CK00
  • Channel operation: slave channel
  • Timer operation: operate as 16-bit timer
  • Start trigger: dual input one-shot pulse

Set TMR03L register
  • Valid edge: falling edge
  • Operating mode: capture mode
  • Start trigger disabled during count

Set TDR03 register
  • Initial value: 0

Set TOM0 register
  • Channel 3 slave channel output mode

Set TOL0 register
  • Channel 3 positive logic output

Set TO0 register
  • Channel 3 output: 0

Set TOE0 register
  • Channel 3 output enabled

Set PMC0 register
  • TO03 digital I/O

Set P0 register
  • TO03: 0 output

Set PM0 register
  • TO03: output mode

end

Figure 5-4  TAU Initialization Flowchart (2)
5.4 12-bit Interval Timer Initialization

The following flowchart shows the initialization of the 12-bit interval timer.

```
Initialize 12-bit interval timer

Set PER0 register
  • Supply bit interval timer input clock

Set ITMCH register
  • Stop counter

Set ITMK bit
  • Disable interrupt processing

Set ITIF bit
  • Clear interrupt request flag

Set ITPR1, 0 registers
  • Priority level: level 3

Set ITMCH, ITMCL registers
  • Compare value: 2

end
```

Figure 5-5  12-bit Interval Timer Initialization Flowchart
6. Switching Waveform

The following shows the switching waveform for this example.

![Switching Waveform Diagram]

CH1: Peak current detection signal (TI03)
CH2: ZCD signal (TI00)
CH3: PWM signal (TO03)

Figure 6-1  Switching Waveform
7. Sample Code
The sample code is available on the Renesas Electronics Website.

8. Documents for Reference
RL78/G10 User's Manual: Hardware (R01UH0384E)
RL78 Family User's Manual: Software (R01US0015E)
(The latest versions of the documents are available on the Renesas Electronics Website.)
Technical Updates/Technical Brochures
(The latest versions of the documents are available on the Renesas Electronics Website.)

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Inquiries
• http://www.renesas.com/contact/
<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Feb. 03, 2016</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
</tr>
</thead>
</table>
| 1. Handling of Unused Pins | Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.  
- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual. |
| 2. Processing at Power-on | The state of the product is undefined at the moment when power is supplied.  
- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.  
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.  
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- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed. |
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- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable. |
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