RL78/G10

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Temperature Sensor Control Using UART Communication

Introduction

This application note describes how to control the temperature sensor by using the serial array unit (UART communication) of the RL78/G10.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcontroller, modify the program according to the specifications of the microcontroller and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

When turned on, the RL78/G10 enters STOP mode and waits for the UART communication. When the RL78/G10 receives 00H, the standby release request, from the correspondent device, it enters normal mode and waits for data from the correspondent device. If receiving no data within 15 seconds, the RL78/G10 again enters STOP mode.

When the RL78/G10 receives AAH in normal mode, it acquires the temperature data of the temperature sensor and sends the data to the correspondent device. After that, it continues to acquire the temperature data of the temperature sensor every five minutes. It sends the temperature data to the correspondent device once every minute. However, if the acquired data is different from the previous data, it immediately sends the data to the correspondent device. When it receives A0H, the temperature data acquisition stop data, it stops acquiring the temperature data of the temperature sensor and returns to STOP mode.

If the RL78/G10 receives undefined data, it determines the data invalid and continues operation.

Table 1.1 shows the received data and the corresponding functions.

Table 1.1 Received Data and Corresponding Functions

Received Data	Function
00H	Standby release request: shifts from STOP mode to normal mode.
AAH	Temperature data transmission request: sends temperature data to the correspondent device.
A0H	Standby request: shifts from normal mode to STOP mode.

Figure 1.1 shows the system configuration outline.

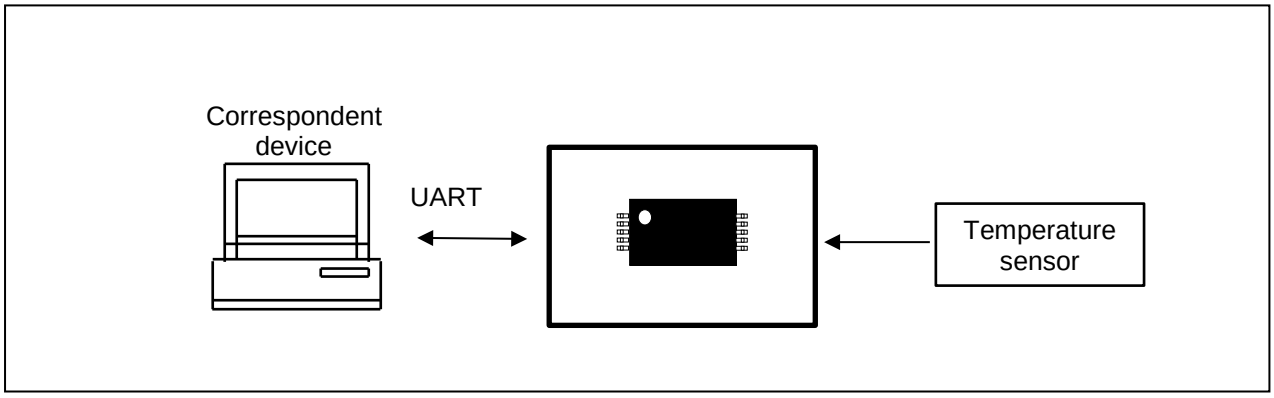

Figure 1.1 the system configuration

1.1 Temperature Sensor

The system described in this application note uses the temperature sensor that outputs the value in proportion to the voltage. When actually designing the circuits, be sure to satisfy the electrical characteristics.
The measurement temperature range of the used temperature sensor is -40°C to +125°C. The relationship between the voltage and temperature is expressed as follows:
Vout = 10 mV/°C × (Temperature°C) + 500 mV. For example, 100 mV (-40°C), 500 mV (0°C), 750 mV (+25°C).

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y17ASP)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 5 MHz • CPU/peripheral hardware clock: 5 MHz
Operating voltage	5.0 V (can run on a voltage range of 4.5 V to 5.5 V.) SPOR operation: 2.16 V at fall, 2.11 V at rise
Integrated development environment (CS+)	CS+ for CC V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.1.0.022 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.04.00 from Renesas Electronics Corp.

3. Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G10 Initialization (R01AN2668E) Application Note

4. Hardware Descriptions

4.1 Hardware Configuration

Figure 4.1 shows an example of the hardware configuration for the system described in this application note.

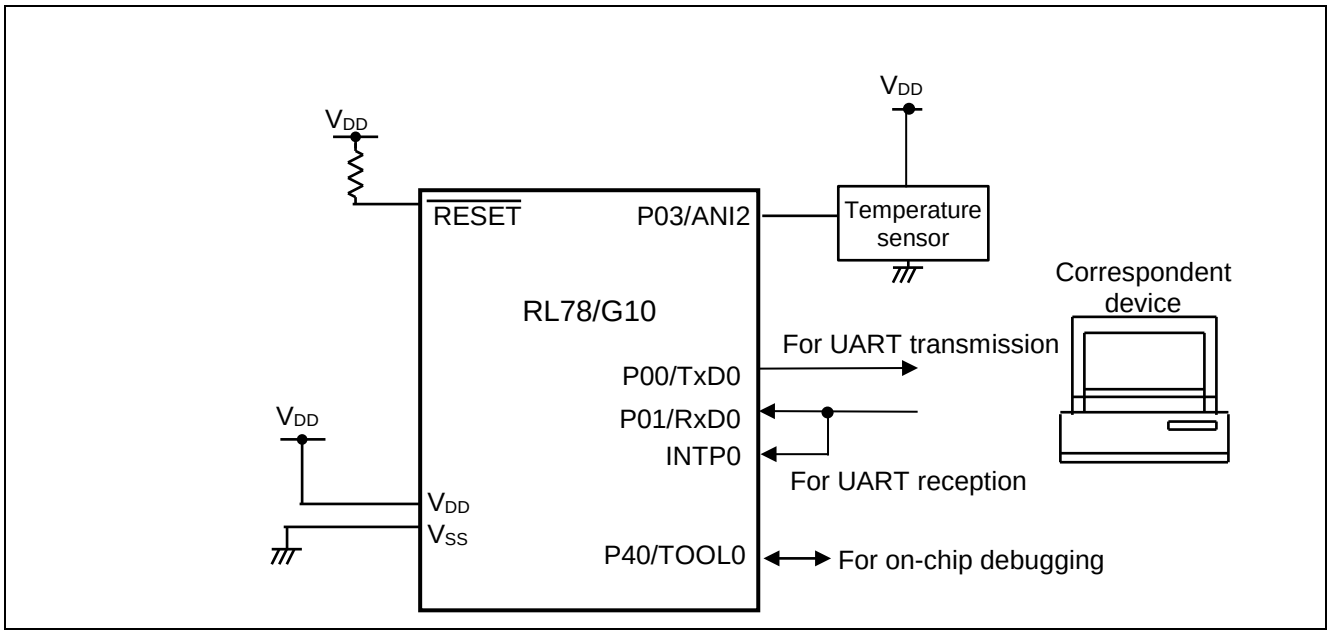

Figure 4.1 the hardware configuration used for this application

Notes: 1. The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied (input-only ports should be each connected to V_{DD} or V_{SS} via a resistor).

2. VDD must be equal to or greater than the reset release voltage (V_{SPOR}) specified with SPOR.

4.2 List of Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Description
P00/TxD0	Output	UART transmission port
P01/RxD0	Input	UART reception port
P03/ANI2	Input	Temperature sensor
P137/INTP0	Input	Shock sensor input port
P40/TOOL0	I/O	For on-chip debugging
P125/RESET	Input	Reset port

5. Software Descriptions

5.1 Operation Summary

The sample program covered in this application note uses the A/D converter to convert the analog voltages of the temperature sensor to digital data. When the system receives the data transmission request from the correspondent device, the system sends the data acquired from the temperature sensor to the correspondent device.

(1) Makes the initial settings for the UART.

<Conditions for setting UART>

- SAU0 channel 0 is used as UART.
- Data is 8 bits long.
- Data is transferred with LSB first.
- No parity is set.
- The standard level setting is used for received data.
- The transfer rate is 9600 bps.
- The reception end interrupt (INTSR0) and transmission end interrupt (INTST0) are used.
- The INTSR0 and INTST0 interrupt priority levels are low (level 3).

(2) After placing the system in UART communication standby status by using the serial channel start register, executes the STOP instruction. Returns from STOP mode by the INTP0 interrupt.

- If the data received is AAH when the reception end interrupt (INTSR0) occurs after releasing the system from STOP mode, acquires the temperature data of the temperature sensor and sends the data to the correspondent device. Replaces the character data with the character code based on the ASCII coding.

Item	Description					
Received data	AAH					
Transmission data	D0	D1	D2	D3	D4	D5
	Fixed value 54H: T	Fixed value 61H: a	Sign of temperature 2bH: + 2dH: -	Tens place of temperature data	Ones place of temperature data	First decimal place of temperature data

Example: For +25.5°C, 54H, 61H, 2bH, 02H, 05H, 05H

- After transmitting the data, executes the HALT instruction and waits for the next timing of temperature data acquisition (A/D conversion start).

5.2 List of Option Byte Settings

Table 5.1shows the option byte settings.

Table 5.1Option Byte Settings

Address	Setting	Description
000C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	11111111B	SPOR detection voltage: 2.16 V at fall; 2.11 V at rise
000C2H	11111011B	HOCO: 5 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Variables

Table 5.2lists the global variables.

Table 5.2Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	g_uart_RxData	Reception data	main()
uint16_t	g_adc_ResultT	Got data from temperature sensor	main()
uint16_t	g_adc_ResultTN	Got data from temperature sensor	main()
uint8_t	g_uart_Tx_a_Data[6]	Transmission data a	main()
uint8_t	g_uart_Tx_b_Data[6]	Transmission data b	main()

5.4 List of Functions (Subroutines)

Table 5.3 lists the functions (subroutines).

Table 5.3 List of Functions (Subroutines)

Function (Subroutine) Name	Outline
R_SAU0_Start	Starts count operation of UART0.
R_SAU0_SendMessage	Send message operation of serial array unit channel 0.
R_SAU0_SendByte	Send byte operation of serial array unit channel 0.
r_sau0_transmission_interrupt	Transmission interrupt operation of serial array unit channel 0.
r_sau0_reception_interrupt	Reception interrupt operation of serial array unit channel 0 to buzzer.

5.5 Function Specifications

This section gives the specifications of the functions used in the sample program.

[Function Name] R_SAU0_Start		
Synopsis	Start operation of the serial array unit channel 0(UART0).	
Header	r_cg_sau.h	
Declaration	void R_SAU0_Start(void)	
Explanation	Starts operation of the serial array unit channel 0(UART0).	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_SAU0_SendMessage		
Synopsis	Send message operation of the serial array unit channel 0.	
Header	r_cg_sau.h	
Declaration	void R_SAU0_SendMessage(void)	
Explanation	Send message operation of the serial array unit channel 0.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_SAU0_SendByte		
Synopsis	Send 1 byte	
Header	r_cg_sau.h	
Declaration	void R_SAU0_SendBye(void)	
Explanation	Send 1 byte	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] r_sau0_transmission_interrupt		
Synopsis	Transmission flug	
Header	r_cg_sau.h	
Declaration	void r_sau0_transmission_interrupt (void)	
Explanation	Transmission flug.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] r_sau0_reception_interrupt		
Synopsis	Reception interrupt	
Header	r_cg_sau.h	
Declaration	r_sau0_reception_interrupt(void)	
Explanation	Reception interrupt.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] main		
Synopsis	Main function	
Declaration	—	
Explanation	Main processing function of the sample program.	
Arguments	None	
Return value	None	
Remarks	None	

5.6 Flowcharts

Figure 5.1 shows an overall flow of the sample program described in this application note.

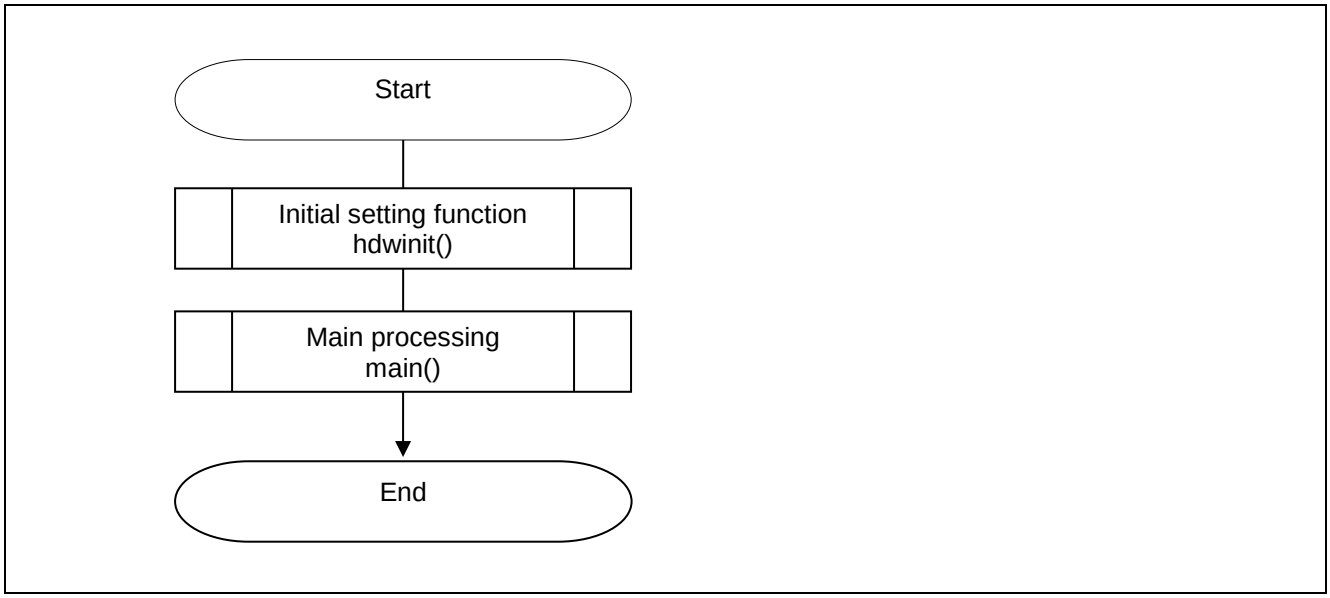

Figure 5.1 the hardware configuration used for this application

5.6.1 Initial Setting Function

Figure 5.2 shows the flowchart of the initial setting function.

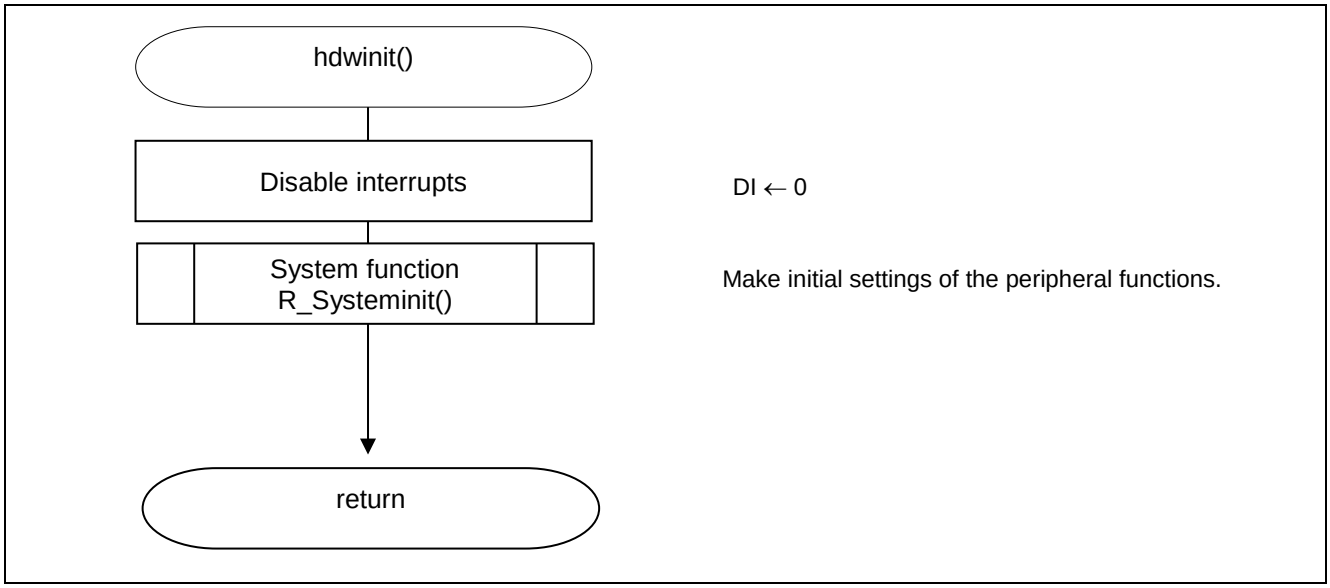

Figure 5.2 Initial Setting Function

5.6.2 System Function

Figure 5.3 shows the flowchart of the system function.

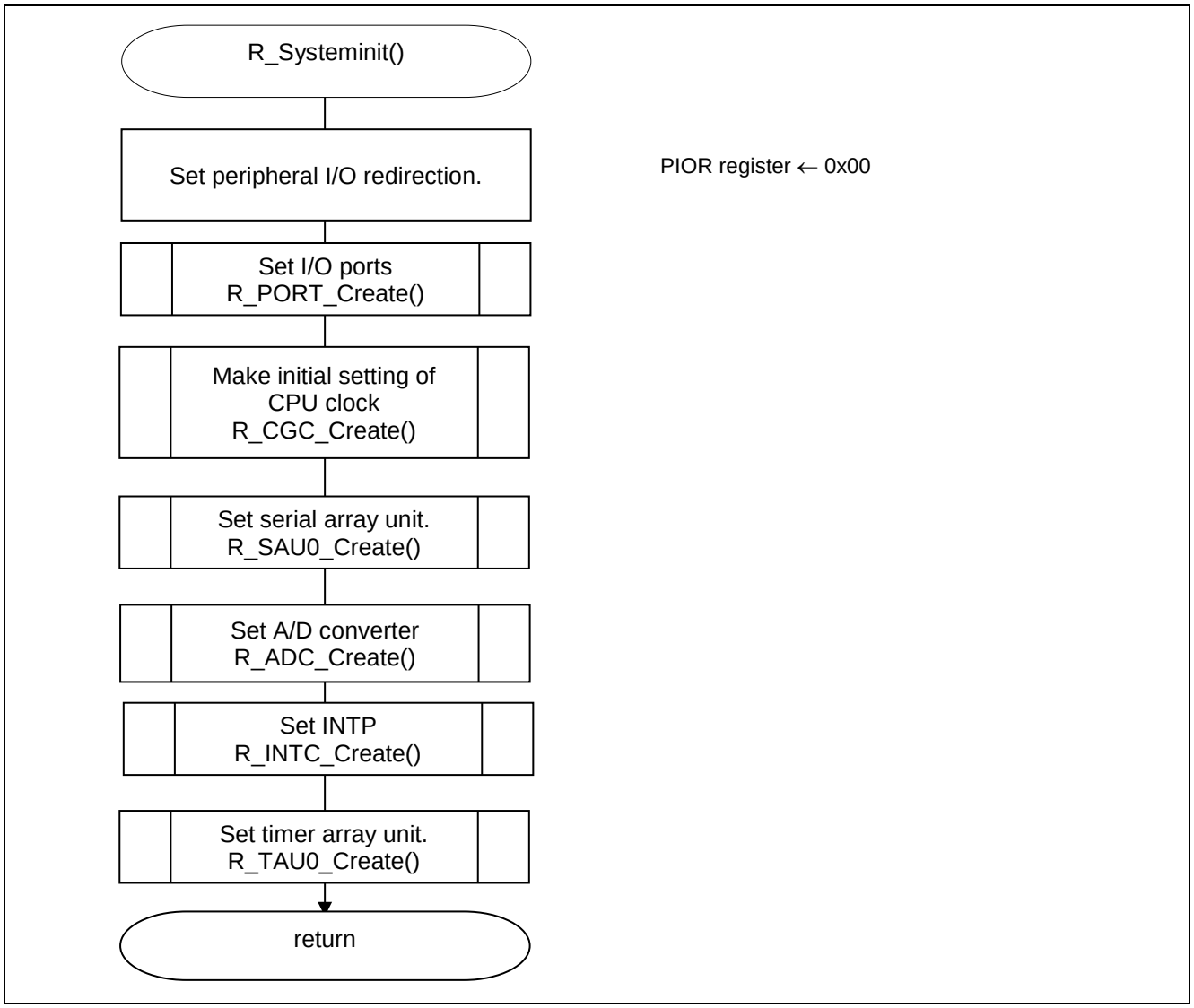

Figure 5.3 System Function

5.6.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

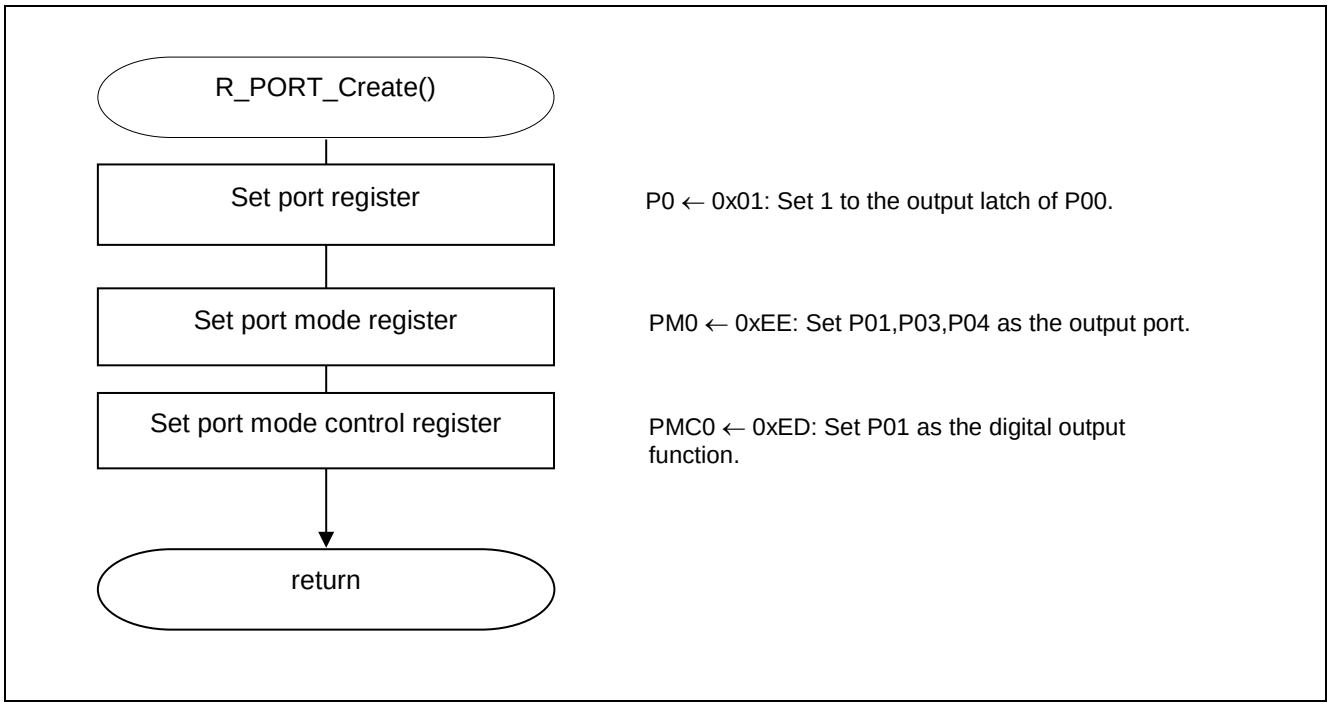

Figure 5.4 I/O Port Setup

Notes: 1. For details on register setting when using the ports as the alternate functions of the peripheral functions, refer to the RL78/G10 User's Manual: Hardware.

2. Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.6.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

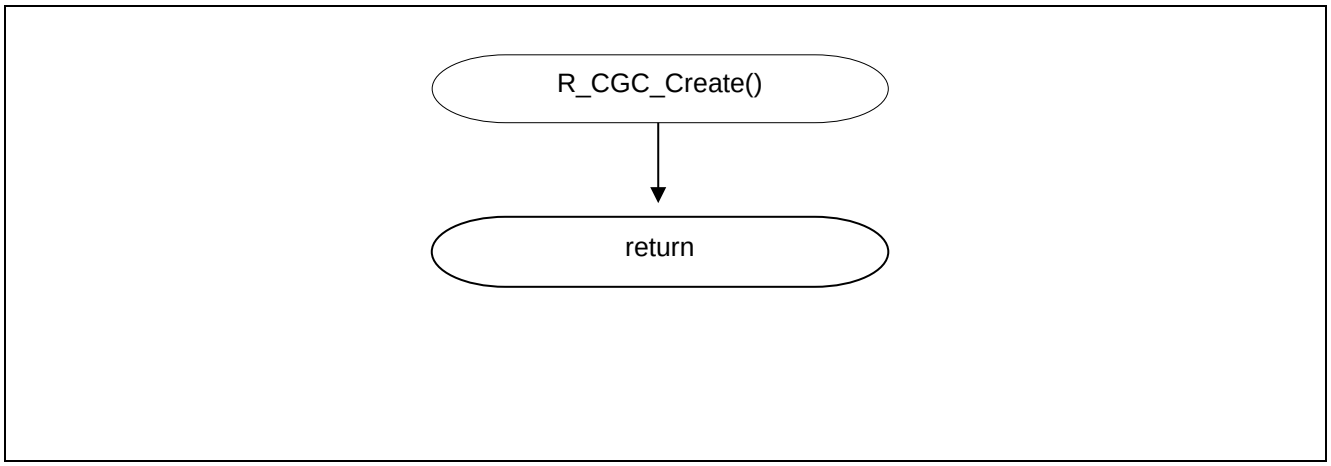

Figure 5.5 CPU Clock Setup

5.6.5 A/D converter Setup

Figure 5.6 shows the flowchart for setting up the A/D converter.

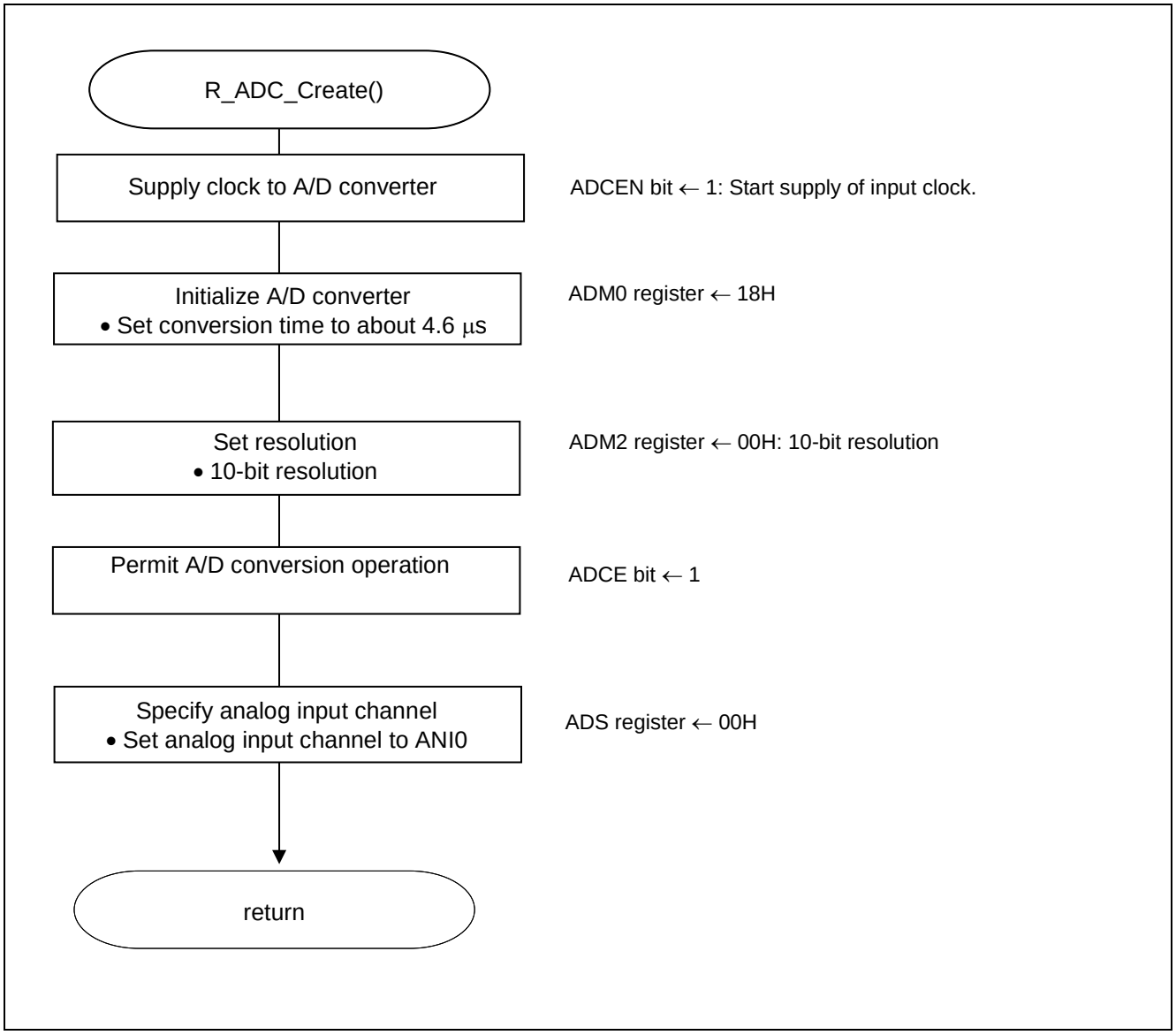

Figure 5.6 A/D Converter Setup

Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN Note	0	ADCEN	IICA0EN Note	0	SAU0EN	0	TAU0EN
x	0	**1**	x	x	x	0	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Note 16-pin products only.

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Setting up the A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	0	0	FR1	FR0	0	LV0	ADCE
x	0	0	**0**	**1**	0	**0**	**1**

Bits 4, 3, and 1

(1) 10-Bit Resolution A/D Conversion Time Selection

ADM0			Conversion Clock	Number of Conversion Clock	Conversion Time	Conversion Time Selection [μs]				
FR1	FR0	LV0				f_{CLK} = 1.25 MHz	f_{CLK} = 5 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	**f_{CLK} = 20 MHz**
0	0	**0**	$f_{CLK}/8$	23 f_{AD} (Number of sampling clock: 9 f_{AD})	$184/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	18.4	9.2
0	**1**		**$f_{CLK}/4$**		**$92/f_{CLK}$**			18.4	9.2	**4.6**
1	0		$f_{CLK}/2$		$46/f_{CLK}$		18.4	9.2	4.6	Setting prohibited
1	1		f_{CLK}		$23/f_{CLK}$	18.4	9.2	4.6	Setting prohibited	
0	0	1	$f_{CLK}/8$	17 f_{AD} (Number of sampling clock: 5 f_{AD})	$136/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	18.4	6.8
0	1		$f_{CLK}/4$		$68/f_{CLK}$			18.4	9.2	3.4
1	0		$f_{CLK}/2$		$34/f_{CLK}$		13.6	9.2	4.6	Setting prohibited
1	1		f_{CLK}		$17/f_{CLK}$	13.6	6.8	4.6	Setting prohibited	

(2) 8-Bit Resolution A/D Conversion Time Selection

ADM0			Conversion Clock	Number of Conversion Clock	Conversion Time	Conversion Time Selection [μs]				
FR1	FR0	LV0				f_{CLK} = 1.25 MHz	f_{CLK} = 5 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz
0	0	0	$f_{CLK}/8$	21 f_{AD} (Number of sampling clock: 9 f_{AD})	$168/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	16.8	8.4
0	1		$f_{CLK}/4$		$84/f_{CLK}$			16.8	8.4	4.2
1	0		$f_{CLK}/2$		$43/f_{CLK}$		16.8	8.4	4.2	Setting prohibited
1	1		f_{CLK}		$21/f_{CLK}$	16.8	8.4	4.2	Setting prohibited	
0	0	1	$f_{CLK}/8$	15 f_{AD} (Number of sampling clock: 3 f_{AD})	$120/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	12.0	6.0
0	1		$f_{CLK}/4$		$60/f_{CLK}$			12.0	6.0	3.0
1	0		$f_{CLK}/2$		$30/f_{CLK}$		12.0	6.0	3.0	Setting prohibited
1	1		f_{CLK}		$15/f_{CLK}$	12.0	6.0	3.0	Setting prohibited	

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Setting up the resolution

- A/D converter mode register 2 (ADM2)
  Sets the resolution.

Symbol: ADM2

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ADTYP
0	0	0	0	0	0	0	**0**

Bit 0

ADTYP	Resolution of A/D conversion
0	**10-bit resolution**
1	8-bit resolution

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Specifying the input channel

- Analog input channel specification register (ADS)
  Specifies the input channel for the analog voltage to be subjected to A/D conversion.

Symbol: ADS

7	6	5	4	3	2	1	0
0	0	0	0	0	ADS2 Note1	ADS1	ADS0
0	0	0	0	0	**0**	**1**	**0**

10-pin products

ADS1	ADS0	Analog input channel	Input source
0	0	ANI0	P01/ANI0 pin
0	1	ANI1	P02/ANI1 pin
1	**0**	**ANI2**	**P03/ANI2 pin**
1	1	ANI3	P04/ANI3 pin

16-pin products

ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	ANI0	P01/ANI0 pin
0	0	1	ANI1	P02/ANI1 pin
0	**1**	0	ANI2	P03/ANI2 pin
0	1	1	ANI3	P04/ANI3 pin
1	0	0	ANI4	P05/ANI4 pin
1	0	1	ANI5	P10/ANI5 pin
1	1	0	ANI6	P11/ANI6 pin
1	1	1	Internal reference voltage (0.815 V (typ.)) Note2	—

5.6.6 Timer array unit Setup

Figure 5.7 shows the flowchart for setting up the timer array unit.

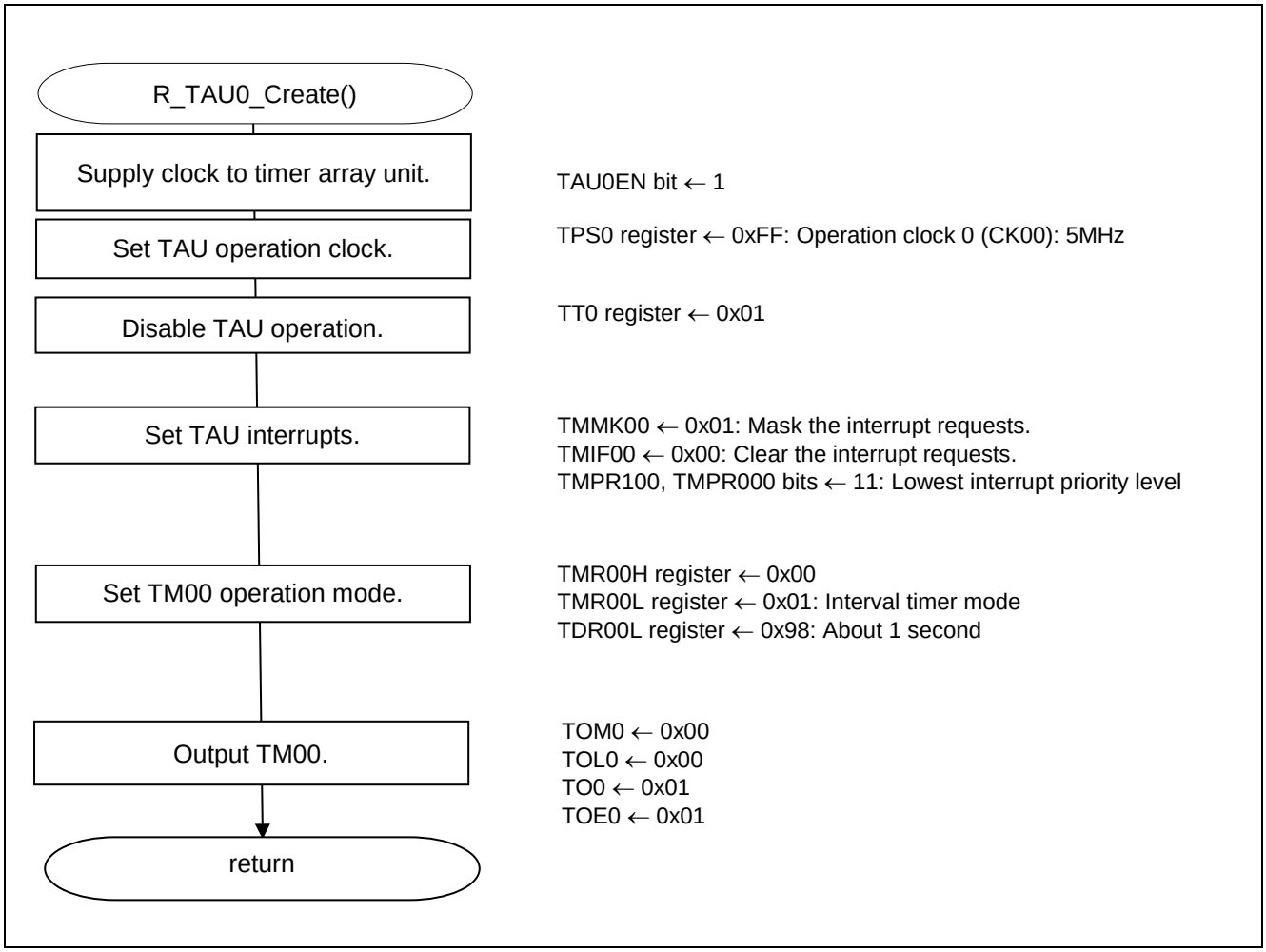

Figure 5.7 Timer Array Unit Channel0 Setup

Starting clock supply to the timer array unit 0
Peripheral enable register 0 (PER0)
Start supplying clock to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN[Note]	CMPEN[Note]	ADCEN	IICA0EN[Note]	0	SAU0EN	0	TAU0EN
0	0	x	0	0	x	0	**1**

bit 0

TAU0EN	**Control of timer array unit 0 input clock supply**
0	Stops supply of input clock.
1	**Supplies input clock.**

Note: 16-pin products only.
Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Stop timer channel

Timer channel stop register 0 (TT0, TTH0(8-bit mode))
Select timer channel to stop operation.

Symbol：TTH0、TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TTH03	0	TTH01	0	0	0	0	0	TT03	TT02	TT01	TT00
0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	**1**	**1**

bit n

TT0n	**Operation stop trigger of channel n (n=0 to 3)**
0	No trigger operation
1	**TE0n is cleared to 0, and counting operation is stopped**

Configuring the timer clock frequency

Timer clock select register 0 (TPS0)

Select an operation clock for timer array unit 0.

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000		Selection of operation clock (CK00)				
					f_{CLK}= 1.25MHz	f_{CLK}= 2.5MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	**f_{CLK}=** 20MHz
0	0	0	0	f_{CLK}	1.25 MHz	2.5 MHz	5 MHz	10 MHz	**20 MHz**
0	0	0	1	$f_{CLK}/2$	625 kHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{CLK}/2^2$	313 kHz	625 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156 kHz	313 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	78 kHz	156 kHz	313 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	39 kHz	78 kHz	**156 kHz**	313 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39 kHz	78 kHz	156 kHz	313 kHz
0	1	1	1	$f_{CLK}/2^7$	9.8 kHz	19.5 kHz	39 kHz	78 kHz	156 kHz
1	0	0	0	$f_{CLK}/2^8$	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz	78 kHz
1	0	0	1	$f_{CLK}/2^9$	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz
1	1	0	0	$f_{CLK}/2^{12}$	313 Hz	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz
1	1	0	1	$f_{CLK}/2^{13}$	152 Hz	313 Hz	625 Hz	1.22 kHz	2.5 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78 Hz	152 Hz	313 Hz	625 Hz	1.22 kHz
1	**1**	**1**	**1**	$f_{CLK}/2^{15}$	39 Hz	78 Hz	**152 Hz**	313 Hz	625 Hz

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Timer interrupt

- Interrupt mask flag registers（MK0L）
  Interrupt mask selection
- Interrupt request flag registers（IF0L）
  clear interrupt request
- Priority specification flag registers（PR00L、PR10L）
  low priority selection

Symbol：MK0L

bit 7,6

××MK××	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol：IF0L

bit 7,6

××IF××	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol：PR00L、PR10L

bit 7

TMPR100	TMPR000	Priority Level Selection
0	0	Specifying level 0(high priority)
0	1	Specifying level 1
1	0	Specifying level 2
1	**1**	**Specifying level 3(low priority)**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the operation mode of channel 0

Timer mode register 01 (TMR01H, TMR01L)
Select an operation clock (fMCK).
Select a count clock.
Set up the start trigger and capture trigger
Select the valid edge of TI00 pin.
Set up the operation mode.

Symbol：TMR01H、TMR01L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 0n1	0	0	CCS 0n	SPLIT 0n	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0
1	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

CKS0n1	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)

CCS0n	Selection of count clock (f_{TCLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits
1	Valid edge of the input signal from the TI00 pin

SPLIT0n	Selection of count clock (f_{TCLK}) of channel 0
0	16bit timer operation
1	8bit timer operation

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Bit 7-6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bit 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Counting operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/Square wave output/Divider function /PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

Operation mode (Value set by the MD003 to MD001 bits) (See the above table)	MD000	Setting of starting count and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Setting the interval timer cycle time

Timer data register 01 (TDR01H, TDR01L)
Setting delay time

Symbol：TDR01H、TDR01L

TDR01H　　TDR01L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
×	×	×	×	×	×	×	×	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**1**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Enabling the timer output

timer putout register 0 (TO0)
setting putout 0
Timer output enable register 0 (TOE0)
Enable/disable the timer output for each channel.

Symbol：TO0

7	6	5	4	3	2	1	0
0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	**0**	**0**	1	**0**

bit 1

TO01	**Timer output of channel n**
0	Timer output value is “0”
1	**Timer output value is “1”**

Symbol：TOE0

7	6	5	4	3	2	1	0
0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	1	**0**

bit 1

TOE01	**Timer output enable/disable of channel 0**
0	**Disables the timer output.** **Timer operation is not reflected in the TO00 bit, and the output is fixed.** **Writing to the TO00 bit is allowed.**
1	**Enables the timer output.** **Timer operation is reflected in the TO00 bit, and output waveform is generated.** **Writing to the TO00 bit is ignored.**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.6.7 Timer array unit Start

Figure 5.8 shows the flowchart for starting the timer array unit.

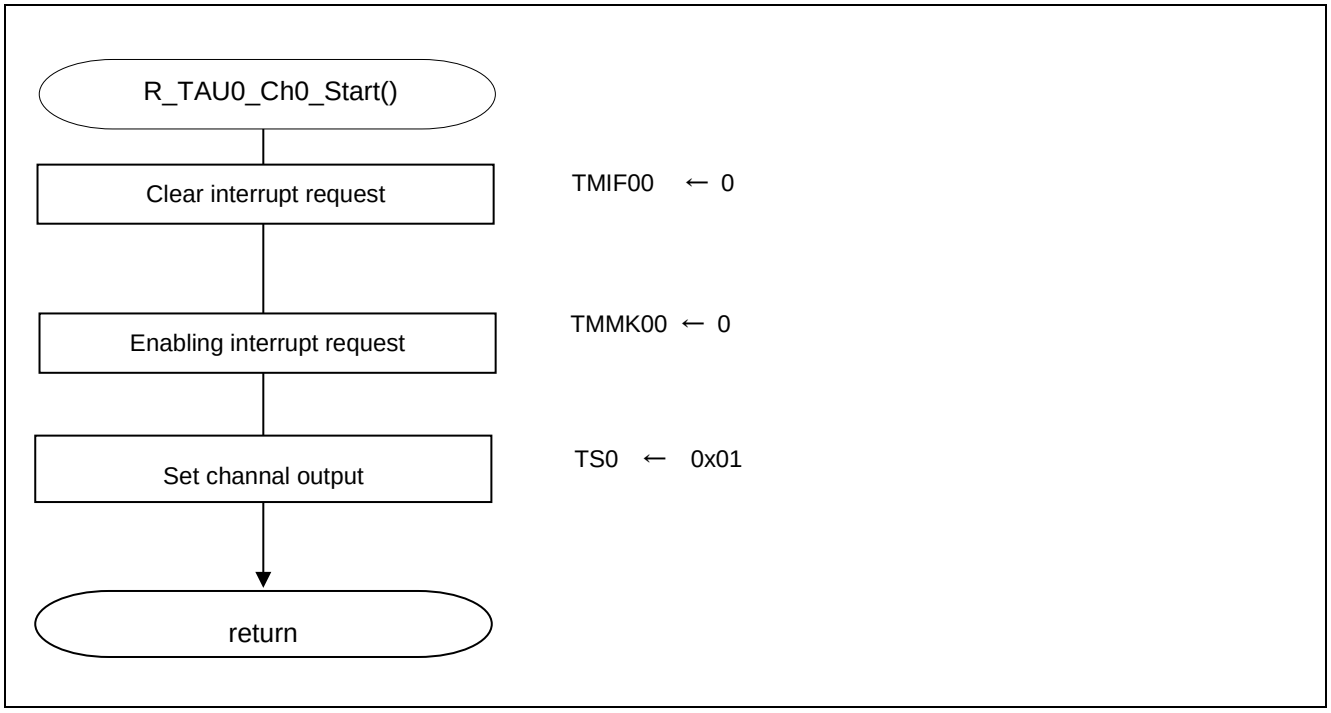

Figure 5.8 Timer Array Unit Channel0 Start

5.6.8 Timer array unit Stop

Figure 5.9 shows the flowchart for stopping the timer array unit.

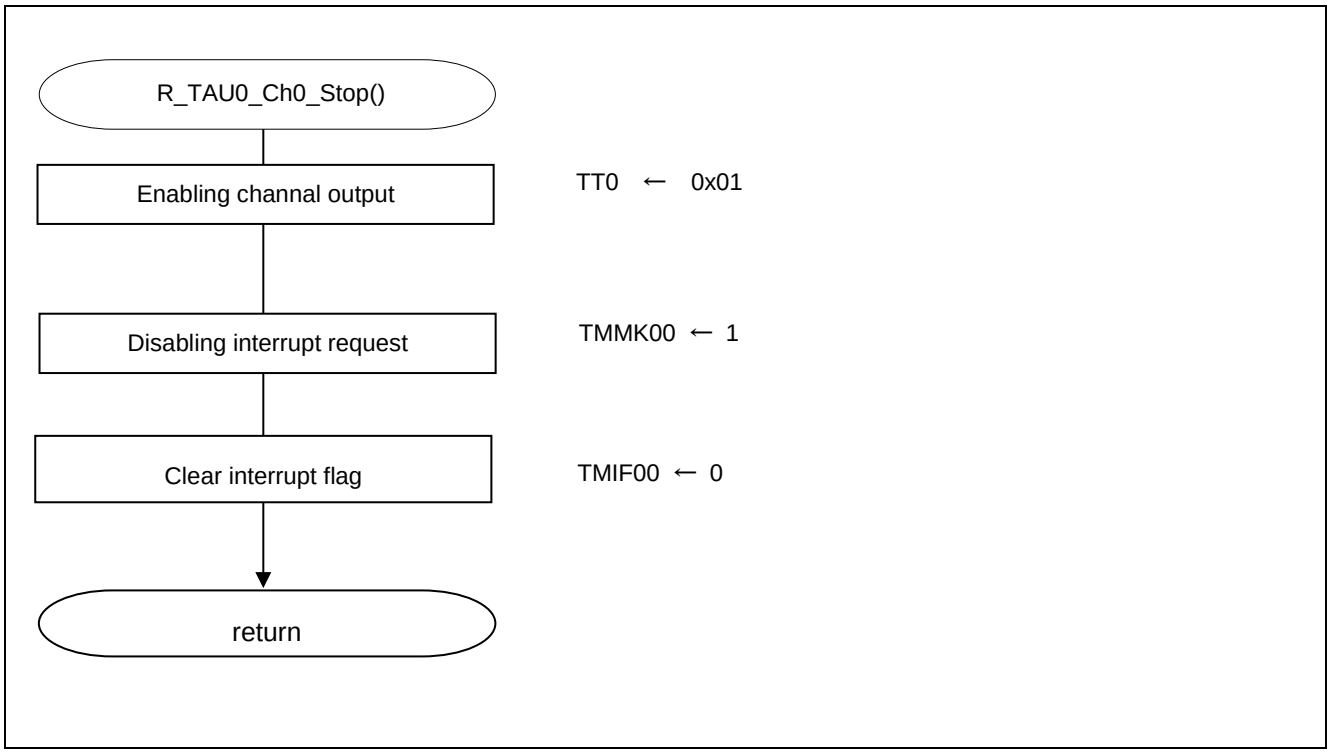

Figure 5.9 Timer Array Unit Stop

5.6.9 Timer array unit interrupt

Figure 5.10 shows the flowchart for setting the timer array unit interrupt.

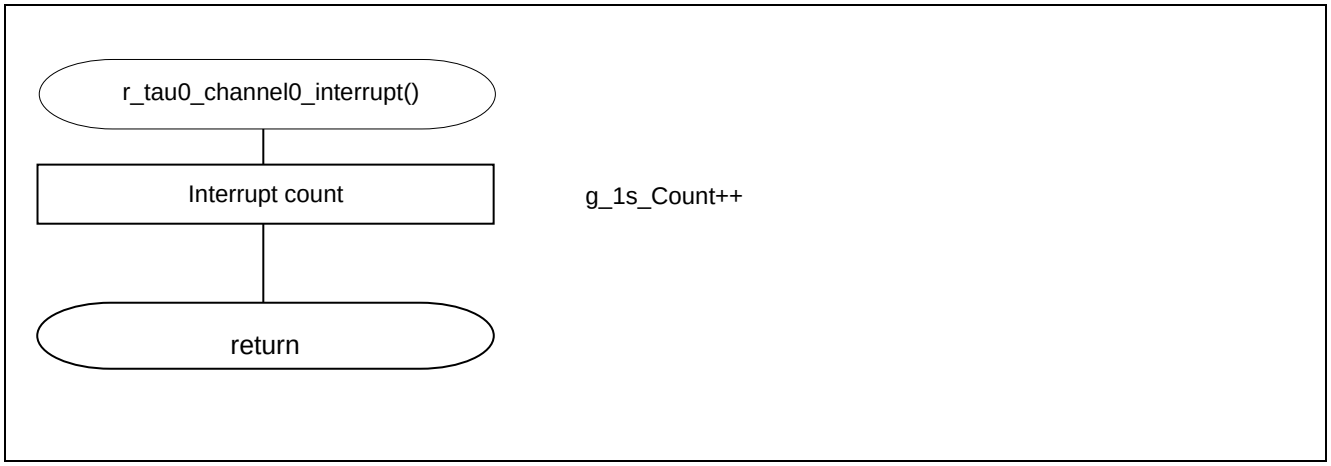

Figure 5.10 Timer Array Unit Interrupt

5.6.10 Serial Array Unit Setup(UART0)

Figure 5.11, Figure 5.12, and Figure 5.13 show the flowcharts for setting up UART0.

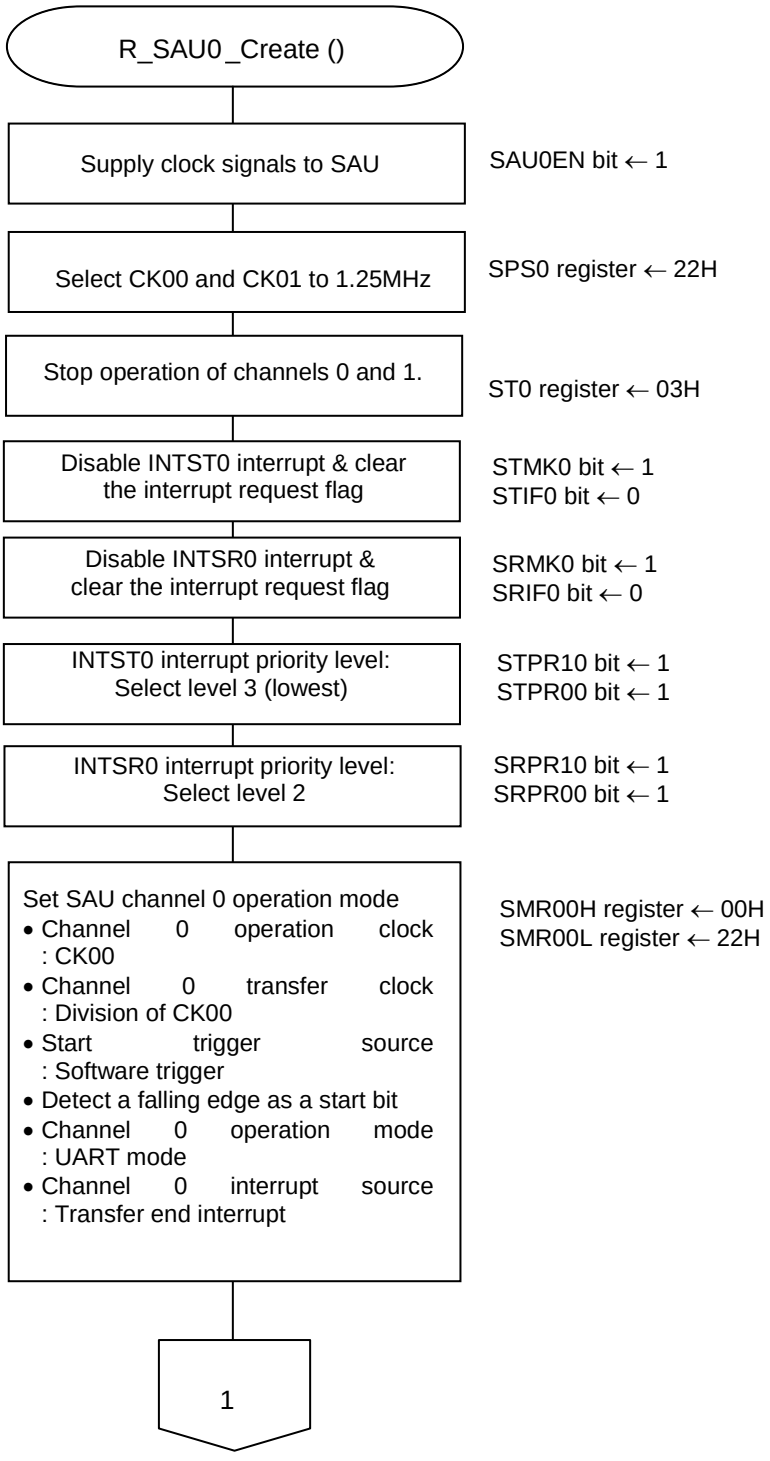

Figure 5.11 UART0 Setup (1/3)

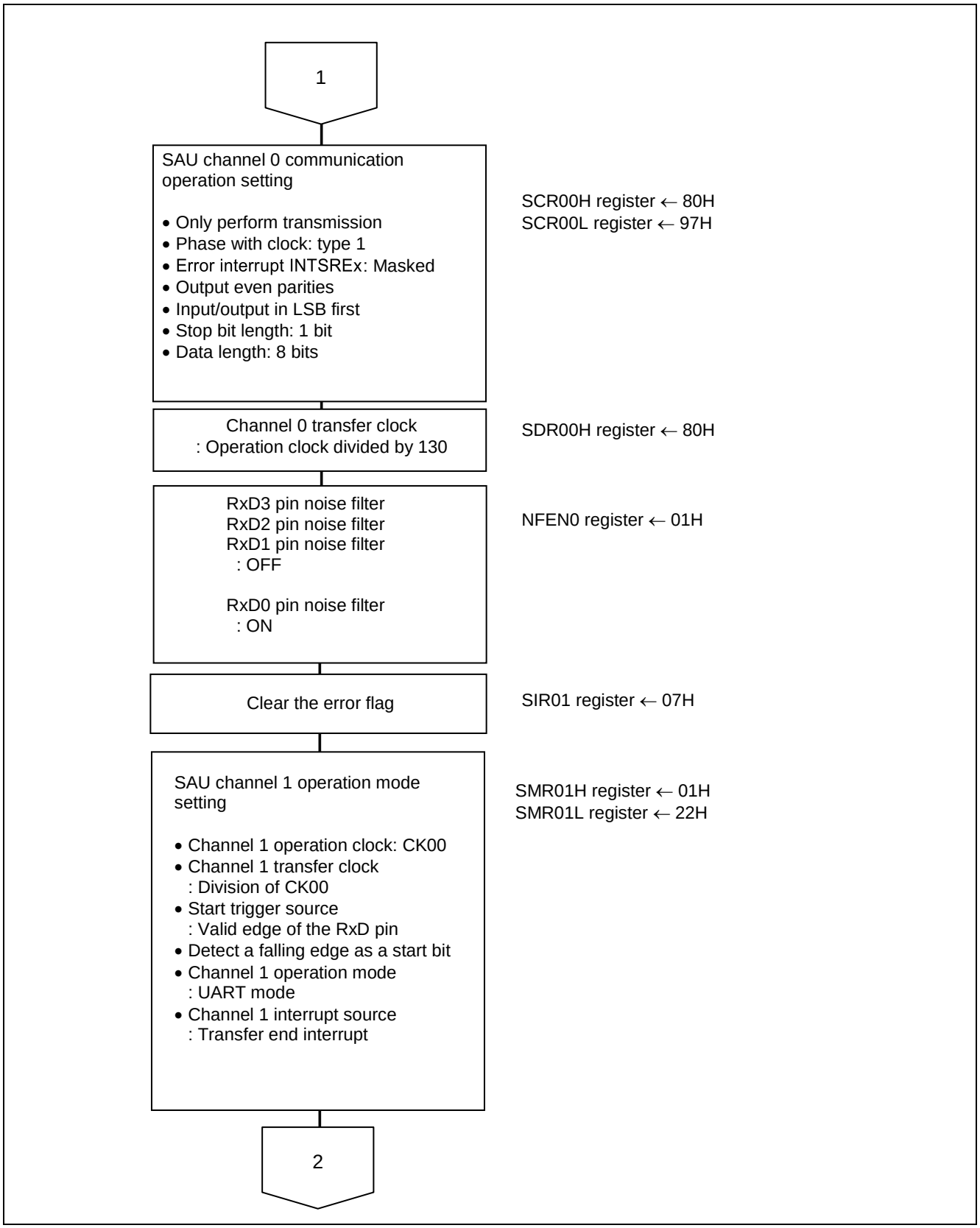

Figure 5.12 UART0 Setup (2/3)

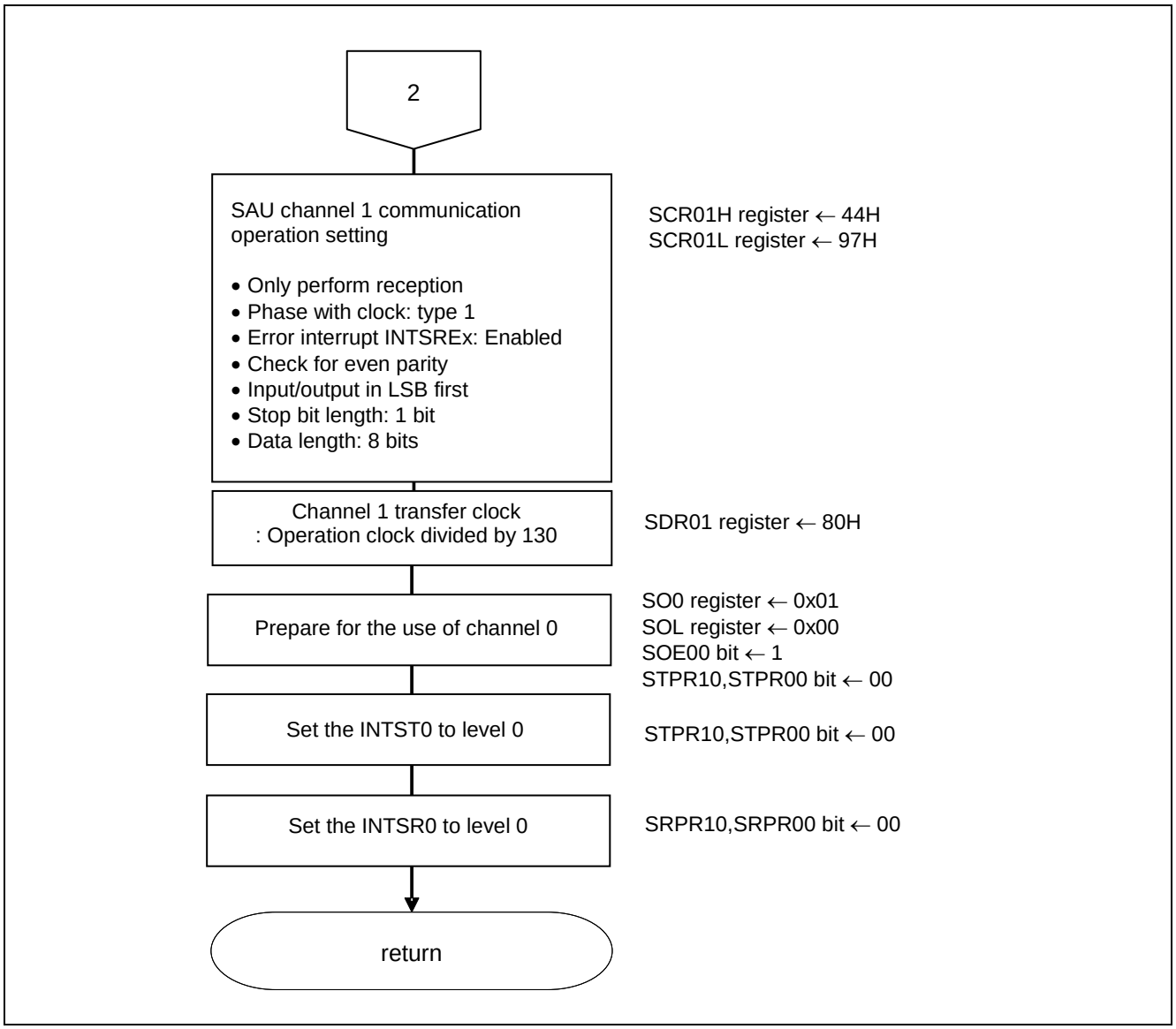

Figure 5.13 UART0 Setup (3/3)

Start supplying clock to the SAU

- Peripheral enable register 0 (PER0)
  Start supplying clock signals.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN[Note]	0	ADCEN	IICA0EN[note]	0	SAU0EN	0	TAU0EN
x	0	x	x	0	**1**	0	x

Bits 2

SAUmEN	Control of serial array unit n input clock supply
0	Stops supply of input clock.
1	**Enables supply of input clock.**

Selecting a serial clock

- Serial clock selection register m (SPS0)
  Select an operation clock for SAU.

Symbol: SPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
0	**0**	**1**	**0**	**0**	**0**	**1**	**0**

Bits 7 to 0

PRS 0n3	PRS 0n2	PRS 0n1	PRS 0n0	Selection of operation clock (CK0n) (n = 0 to 1)					
					f_{CLK}= 1.25MHz	f_{CLK}= 2.5MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz
0	0	0	0	f_{CLK}	1.25 MHz	2.5 MHz	5 MHz	10 MHz	20 MHz
0	0	0	1	$f_{CLK}/2$	625 kHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
0	**0**	**1**	**0**	$f_{CLK}/2^2$	313 kHz	625 kHz	**1.25 MHz**	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156 kHz	313 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	78 kHz	156 kHz	313 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	39 kHz	78 kHz	156 kHz	313 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39 kHz	78 kHz	156 kHz	313 kHz
0	1	1	1	$f_{CLK}/2^7$	9.8 kHz	19.5 kHz	39 kHz	78 kHz	156 kHz
1	0	0	0	$f_{CLK}/2^8$	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz	78 kHz
1	0	0	1	$f_{CLK}/2^9$	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz
1	1	0	0	$f_{CLK}/2^{12}$	313 Hz	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz
1	1	0	1	$f_{CLK}/2^{13}$	152 Hz	313 Hz	625 Hz	1.22 kHz	2.5 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78 Hz	152 Hz	313 Hz	625 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	39 Hz	78 Hz	152 Hz	313 Hz	625 Hz

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Transmission channel operation mode setting

Serial mode register 00 (SMR00H, SMR00L)

Interrupt source

Operation mode

Transfer clock selection

f_{MCK} selection

Symbol: SMR00H, SMR00L

SMR00H SMR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 00	CCS 00	0	0	0	0	0	STS 00	0	0	1	0	0	MD 002	MD 001	MD 000
0	**0**	0	0	0	0	0	**0**	0	0	1	0	0	**0**	**1**	**0**

Bit 15

CKS00	Channel 0 operation clock (f_{MCK}) selection
0	**Prescaler output clock CK00 configured by the SPS0 register**
1	Prescaler output clock CK01 configured by the SPS0 register

Bit 14

CCS00	Channel 0 transfer clock (TCLK) selection
0	**Clock obtained by dividing the operation clock f_{MCK} specified by the CKS00 bit.**
1	Clock input from the SCK pin.

Bit 8

STS00	Selection of start trigger factor
0	**Only the software trigger is valid.**
1	Valid edge of the RxD pin (selected for UART reception)

Bits 2 and 1

MD002	MD001	Channel 0 operation mode setting
0	0	CSI mode
0	**1**	**UART mode**
1	0	Simplified I^2C mode
1	1	Setting prohibited

Bit 0

MD000	Channel 0 interrupt source selection
0	**Transfer end interrupt**
1	Buffer empty interrupt

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Transmission channel communication operation setting

Serial communication operation setting register 00 (SCR00H, SCR00L)
Data length setting, data transfer order, error interrupt signal mask availability, and operation mode

Symbol: SCR00H, SCR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE00	RXE00	DAP00	CKP00	0	EOC00	PTC001	PTC000	DIR00	0	SLC001	SLC000	0	1	DLS001	DLS000
1	**0**	**0**	**0**	0	**0**	**1**	**0**	**1**	0	**0**	**1**	0	1	**1**	**1**

Bit 15 and 14

TXE00	RXE00	Channel 0 operation mode setting
0	0	Communication prohibited
0	1	Reception Only
1	**0**	**Transmission only**
1	1	Both transmission and reception

Bit 10

EOC00	Error interrupt signal (INTSRE0) mask availability selection
0	**Error interrupt INTSRE0 is masked**
1	Generation of error interrupt INTSREx is enabled

Bit 9 and 8

PTC001	PTC000	Parity bit setting in UART mode	
		Transmission	Reception
0	0	No parity bit is output	Data is received without parity
0	1	0 parity is output	No parity check is made
1	**0**	**Even parity is output**	**Check is made for even parity**
1	1	Odd parity is output	Check is made for odd parity

Bit 7

DIR00	Selection of data transfer order in CSI and UART modes
0	Input and output in MSB first
1	**Input and output in LSB first**

Bit 5 and 4

SLC001	SLC000	Stop bit setting in UART mode
0	0	No stop bit
0	**1**	**Stop bit length = 1 bit**
1	0	Stop bit length = 2 bits
1	1	Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Symbol: SCR00H, SCR00L

SCR00H SCR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE 00	RXE 00	DAP 00	CKP 00	0	EOC 00	PTC 001	PTC 000	DIR 00	0	SLC 001	SLC 000	0	1	DLS 001	DLS 000
1	**0**	**0**	**0**	0	**0**	**1**	**0**	**1**	0	**0**	**1**	0	1	**1**	**1**

Bit 1 and 0

DLS001	DLS000	Data length setting in CSI mode
0	1	9-bit data length
1	0	7-bit data length
1	**1**	**8-bit data length**
Others		Setting prohibited

Transmission channel transfer clock setting

Serial data register 00（SDR00h,SDR00L）
transfer clock frequency : f_{MCK}/130（≒9600Hz）

Symbol：SDR00H,SDR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**0**	**0**	**0**	**0**	**0**	**0**	0	x	x	x	x	x	x	x	x

Bit 15-9

SDR00[15:9]							period of operation clock（f_{MCK}）transfer setting
0	0	0	0	0	0	0	f_{MCK} /2
0	0	0	0	0	0	1	f_{MCK} /4
0	0	0	0	0	1	0	f_{MCK} /6
0	0	0	0	0	1	1	f_{MCK} /8
・	・	・	・	・	・	・	・
・	・	・	・	・	・	・	・
1	**0**	**0**	**0**	**0**	**0**	**0**	**f_{MCK} /130**
・	・	・	・	・	・	・	・
・	・	・	・	・	・	・	・
1	1	1	1	1	1	0	f_{MCK} /254
1	1	1	1	1	1	1	f_{MCK} /256

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Reception channel operation mode setting

- Serial mode register 01 (SMR01H, SMR01L)
  Interrupt source
  Operation mode
  Transfer clock selection
  f_{MCK} selection

Symbol: SMR01H, SMR01L

SCR01H SCR01L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 01	CCS 01	0	0	0	0	0	STS 01	0	SIS 010	1	0	0	MD 012	MD 011	MD 010
0	**0**	0	0	0	0	0	**1**	0	**0**	1	0	0	**0**	**1**	**0**

Bit 15

CKS01	Channel 1 operation clock (f_{MCK}) selection
0	**Prescaler output clock CK00 configured by the SPS0 register**
1	Prescaler output clock CK01 configured by the SPS0 register

Bit 14

CCS01	Channel 1 transfer clock (TCLK) selection
0	**Clock obtained by dividing the operation clock f_{MCK} specified by the CKS01 bit**
1	Clock input from the SCK pin

Bit 8

STS01	Start trigger source selection
0	Only software trigger is valid
1	**Valid edge of the RxD pin (selected during UART reception)**

Bit 6

SIS010	Control of receive data level inversion on channel 1 in UART mode
0	**Falling edge is detected as a start bit**
1	Rising edge is detected as a start bit

Bits 2 and 1

MD012	MD011	Channel 1 operation mode setting
0	0	CSI mode
0	**1**	**UART mode**
1	0	Simplified I^2C mode
1	1	Setting prohibited

Bit 0

MD010	Channel 1 interrupt source selection
0	**Transfer end interrupt**
1	Buffer empty interrupt

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Reception channel communication operation setting

- Serial communication operation setting register 01 (SCR01H, SCR01L)
  Data length setting, data transfer order, error interrupt signal mask availability, and operation mode

Symbol: SCR01H, SCR01L

SCR01H								SCR01L							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXE01	RXE01	DAP01	CKP01	0	EOC01	PTC011	PTC010	DIR01	0	SLC011	SLC010	0	1	DLS011	DLS010
0	**1**	**0**	**0**	0	**1**	**1**	**0**	**1**	0	**0**	**1**	0	1	**1**	**1**

Bits 15 and 14

TXE01	RXE01	Channel 1 operation mode setting
0	0	Communication prohibited
0	**1**	**Reception only**
1	0	Transmission only
1	1	Both transmission and reception

For UART reception, wait for 4 f_{CLK} clock cycles or more before setting SS01 to 1, after setting the RXE01 bit of the SCR01 register to 1.

Bit 10

EOC01	Error interrupt signal (INTSRE1) mask availability selection
0	Error interrupt INTSRE1 is masked
1	**Generation of error interrupt INTSRE1 is enabled**

Bits 9 and 8

PTC011	PTC010	Parity bit setting in UART mode	
		Transmission	Reception
0	0	No parity bit is output	Data is received without parity
0	1	0 parity is output	No parity check is made
1	**0**	Even parity is output	**Check is made for even parity**
1	1	Odd parity is output	Check is made for odd parity

Bit 7

DIR01	Selection of data transfer order in CSI and UART modes
0	Input and output in MSB first
1	**Input and output in LSB first**

Bits 5 and 4

SLC011	SLC010	Stop bit setting in UART mode
0	0	No stop bit
0	**1**	**Stop bit length = 1 bit**
1	0	Stop bit length = 2 bits
1	1	Setting prohibited

Symbol: SCR01H, SCR01L

SCR01H | SCR01L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXE 01	RXE 01	DAP 01	CKP 01	0	EOC 01	PTC 011	PTC 010	DIR 01	0	SLC 011	SLC 010	0	1	DLS 011	DLS 010
0	**1**	**0**	**0**	0	**1**	**1**	**0**	**1**	0	**0**	**1**	0	1	**1**	**1**

Bits 1 and 0

DLS011	DLS010	Data length setting in CSI mode
0	1	9-bit data length
1	0	7-bit data length
1	**1**	**8-bit data length**
others		Setting prohibited

Reception transfer clock setting

- Serial data register 01 (SDR01H, SDR01L)
  Transfer clock frequency: $f_{MCK}/208$ (≈ 9600 Hz)

Symbol: SDR01H, SDR01L

SCR01H | SCR01L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**0**	**0**	**1**	**1**	**0**	**1**	0	x	x	x	x	x	x	x	x

Bits 15 to 9

SDR01[15:9]							Transfer clock setting by dividing operation clock (f_{MCK})
0	0	0	0	0	0	0	f_{MCK} /2
0	0	0	0	0	0	1	f_{MCK} /4
0	0	0	0	0	1	0	f_{MCK} /6
0	0	0	0	0	1	1	f_{MCK} /8
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	**0**	**0**	**0**	**0**	**0**	**0**	**f_{MCK} /130**
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	f_{MCK} /254
1	1	1	1	1	1	1	f_{MCK} /256

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

set putout level

・Serial Output Level Register0（SOL0）

Output : no inversion

Symbol : SOL0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SOL00
0	0	0	0	0	0	0	**0**

bit 0

SOL00	Selects inversion of the level of the transmit data of channel 0 in UART mode
0	**Communication data is output as is**
1	Communication data is inverted and output

Symbol : PR00L（10pin）

7	6	5	4	3	2	1	0
TMPR000	TMPR001H	SREPR00	SRPR00	STPR00 CSIPR000 IICPR000	PPR01	PPR00	WDTIPR0
x	x	x	**0**	**0**	x	x	x

Symbol : PR10L（10pin）

TMPR100	TMPR101	SREPR10	SRPR00	STPR10 CSIPR100 IICPR100	PPR11	PPR10	WDTIPR1
x	x	x	**0**	**0**	x	x	x

ビット５－３

xxPR1x	xxPR0x	Priority Level Selection
0	**0**	**Specifying level 0(high priority)**
0	1	Specifying level 1
1	0	Specifying level 2
1	1	Specifying level 3（low priority）

5.6.11 External Interrupt Setup

Figure 5.14,Figure 5.15 and Figure 5.16 shows the flowchart for setting up the external interrupts.

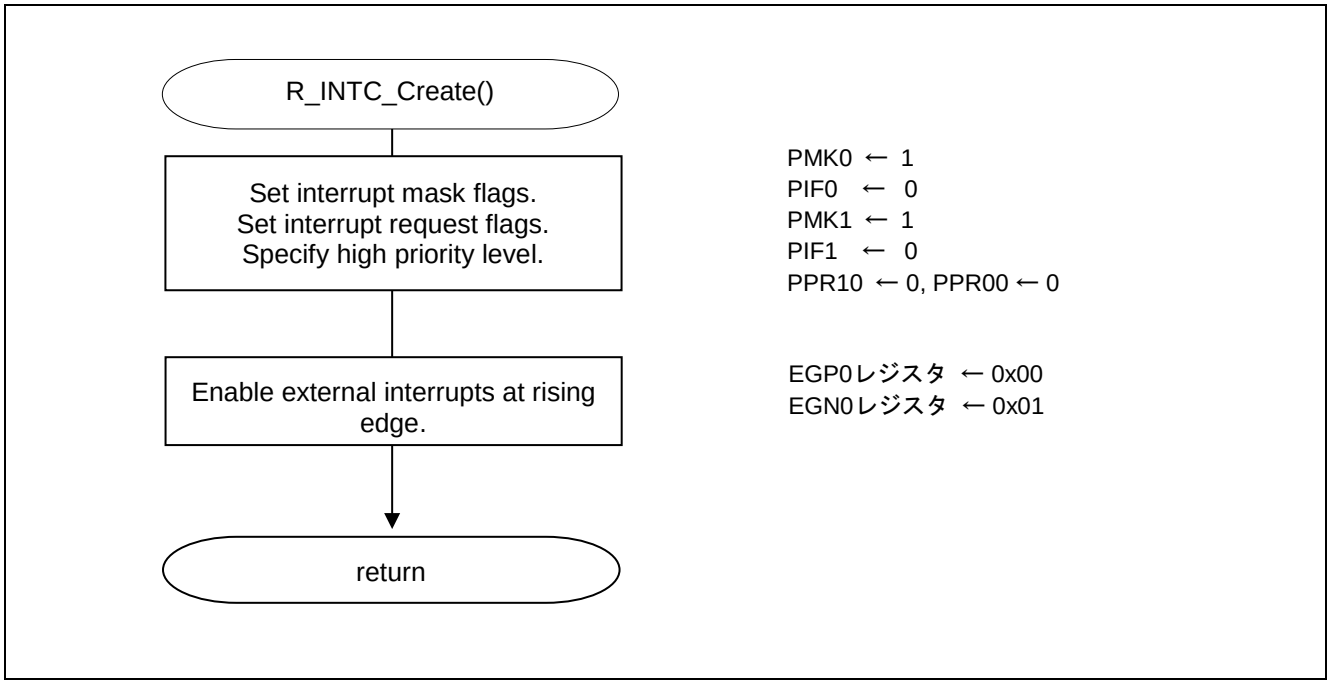

Figure 5.14 External Interrupt Setup

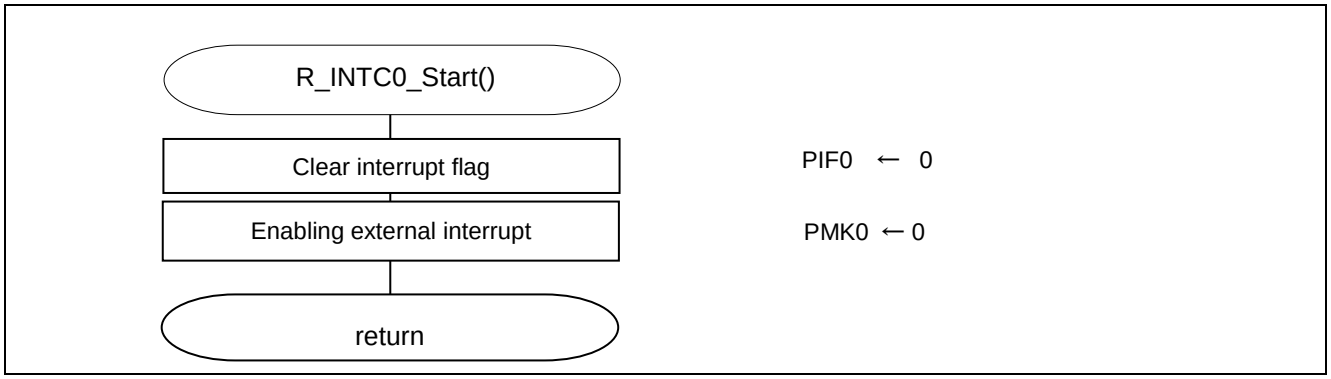

Figure 5.15 External Interrupt Start

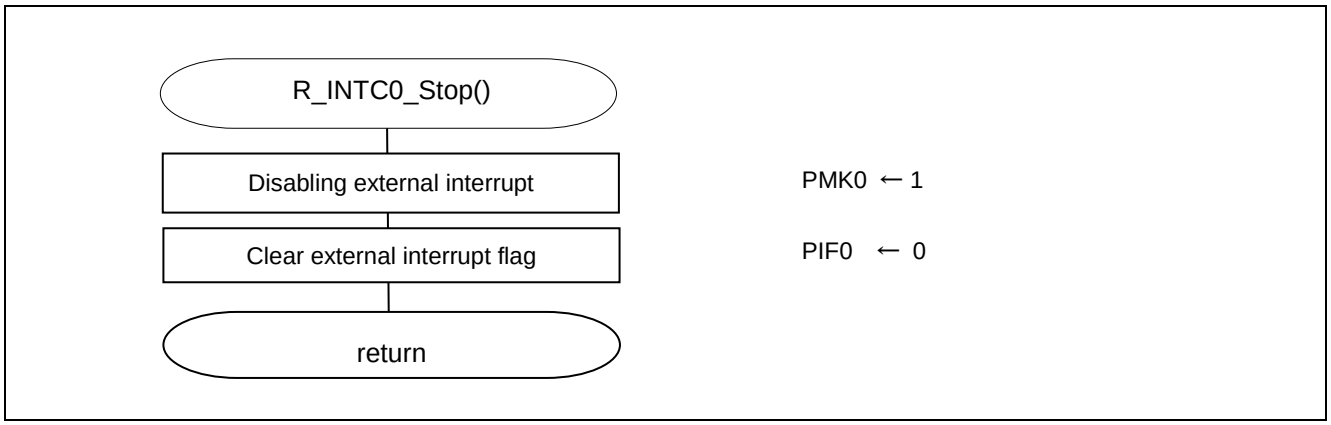

Figure 5.16 External Interrupt Stop

5.6.12 Main Processing

Figure 5.17 shows the flowchart of the main processing.

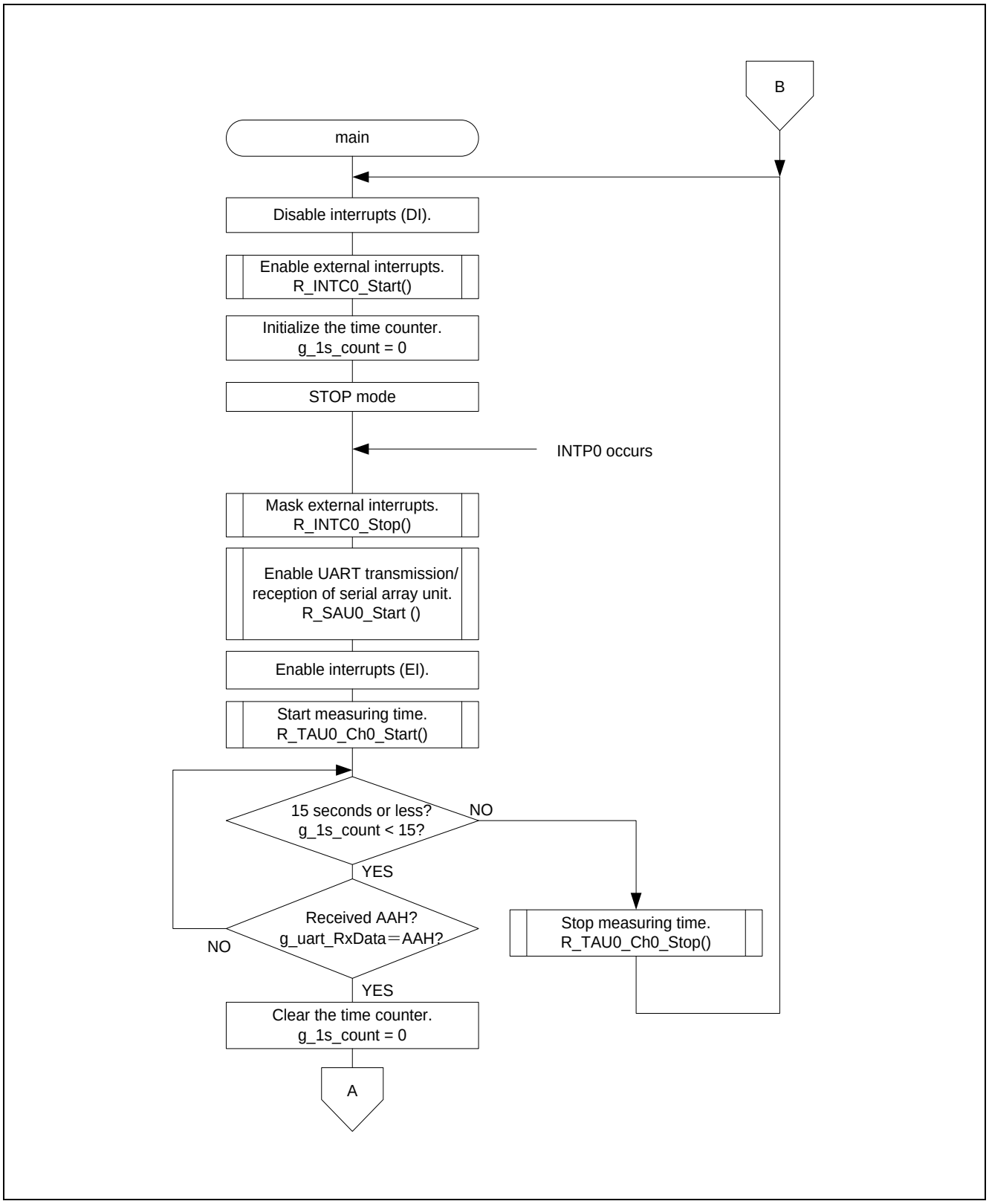

Figure 5.17 Main Processing Flowchart

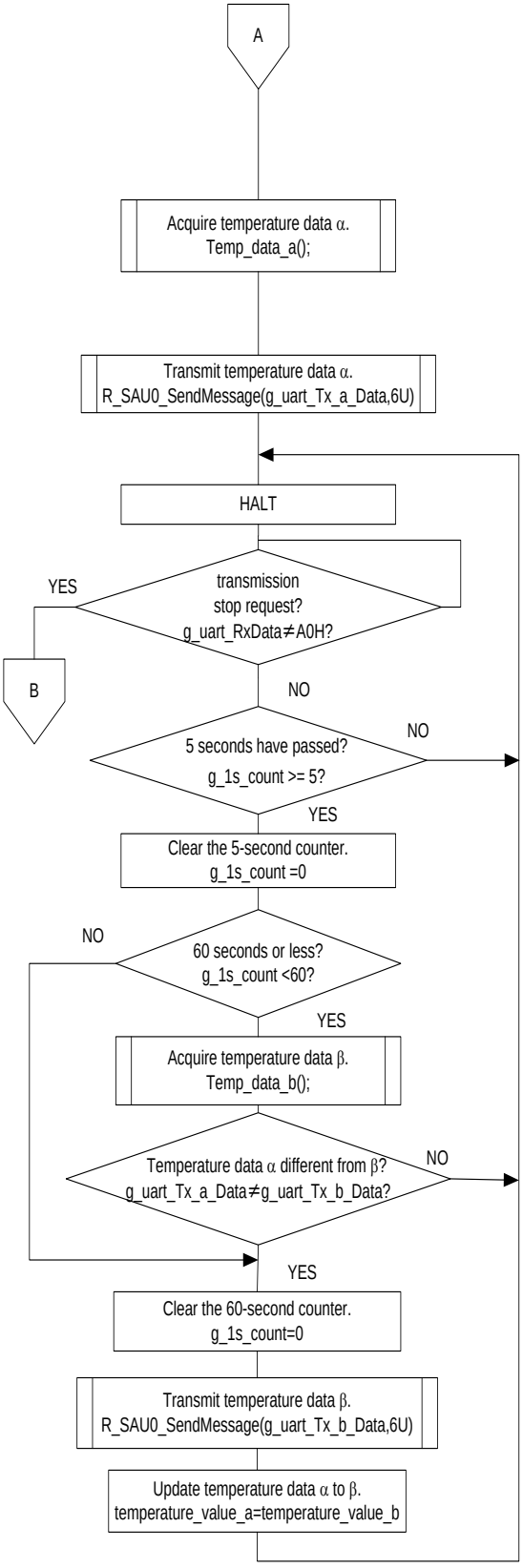

Figure 5.18 Flowchart for Main Processing (2/2)

5.6.13 Temperature Data Acquisition Flowcharts

Figure 5.19,Figure 5.20 , Figure 5.21show the flowcharts for acquiring temperature data.

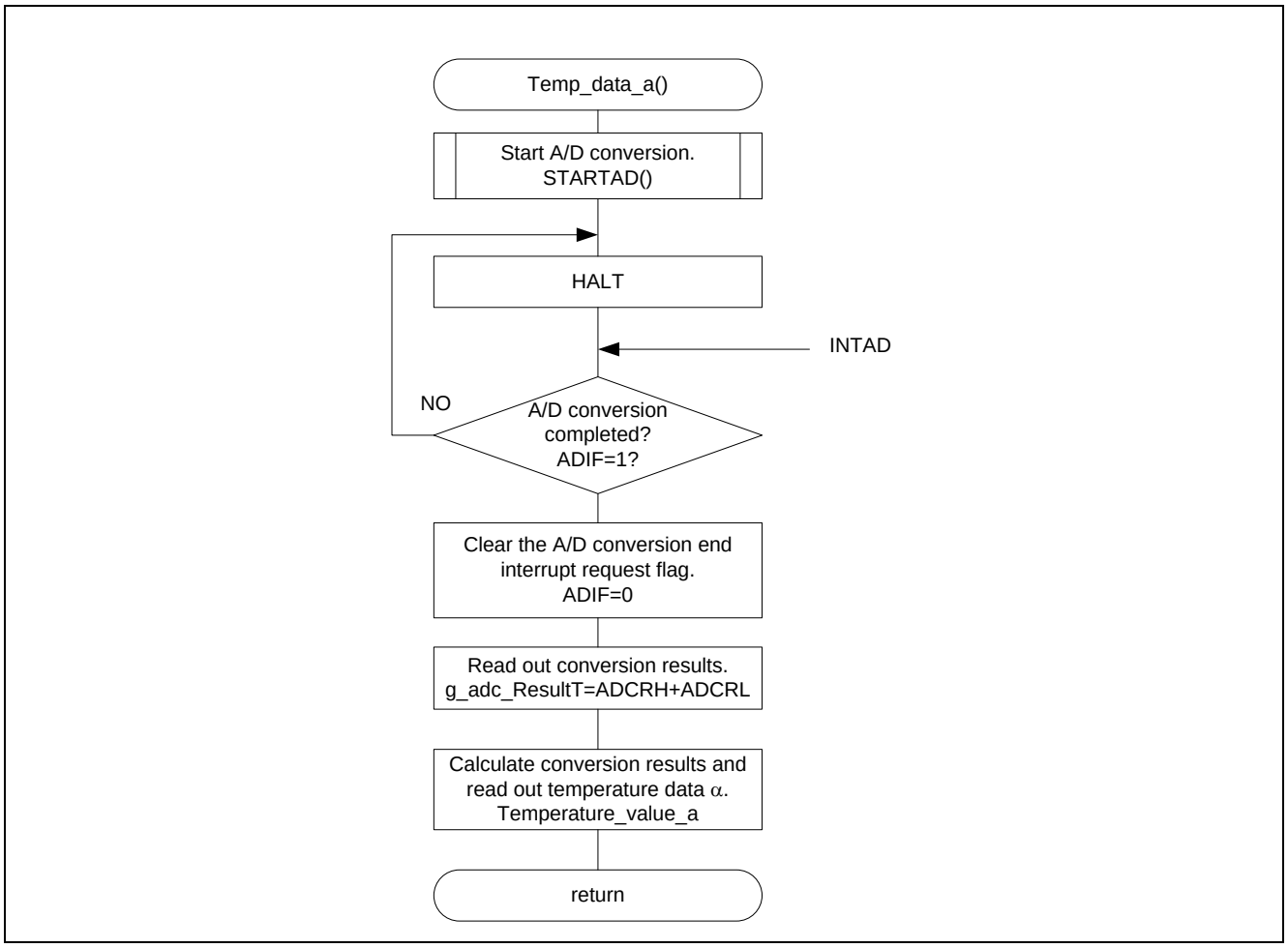

Figure 5.19 Flowchart for Processing Temperature Data (a)

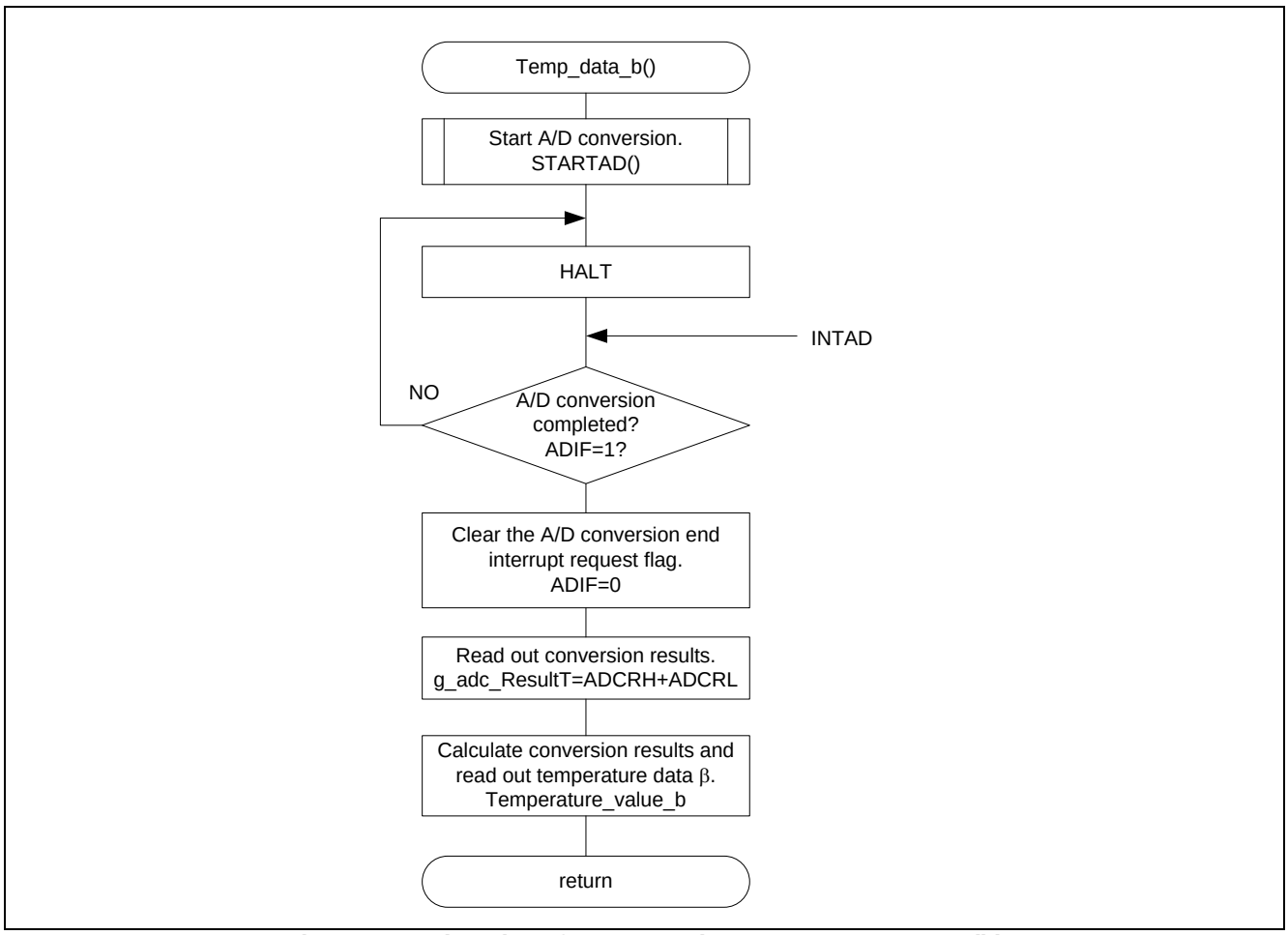

Figure 5.20 Flowchart for Processing Temperature Data (b)

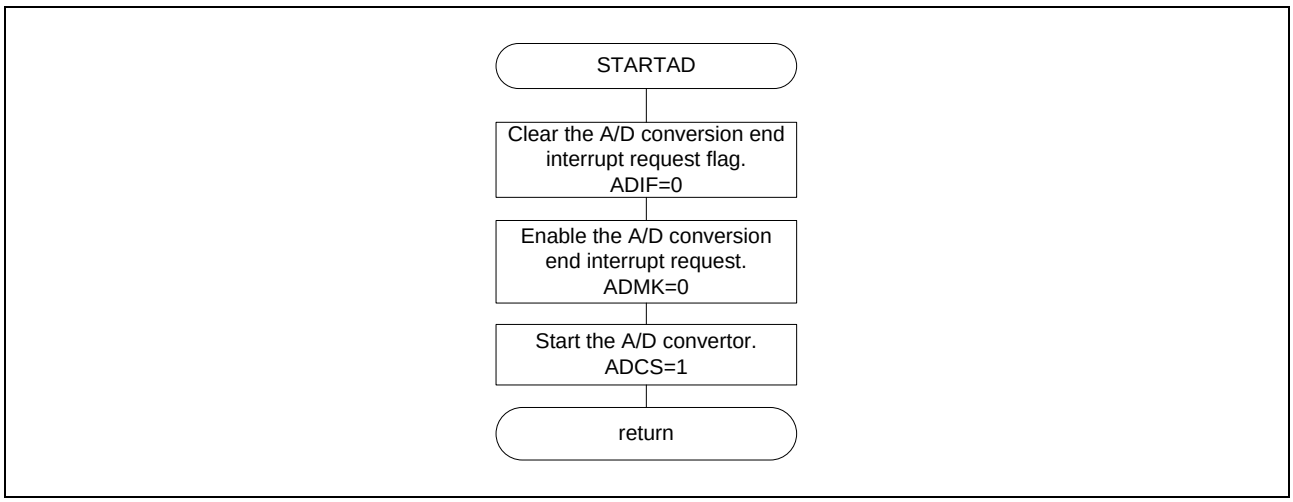

Figure 5.21 Flowchart for Processing STARTAD

5.6.14 Serial Operation Start Function

Figure 5.22 shows the flowchart for the UART0 operation start function.

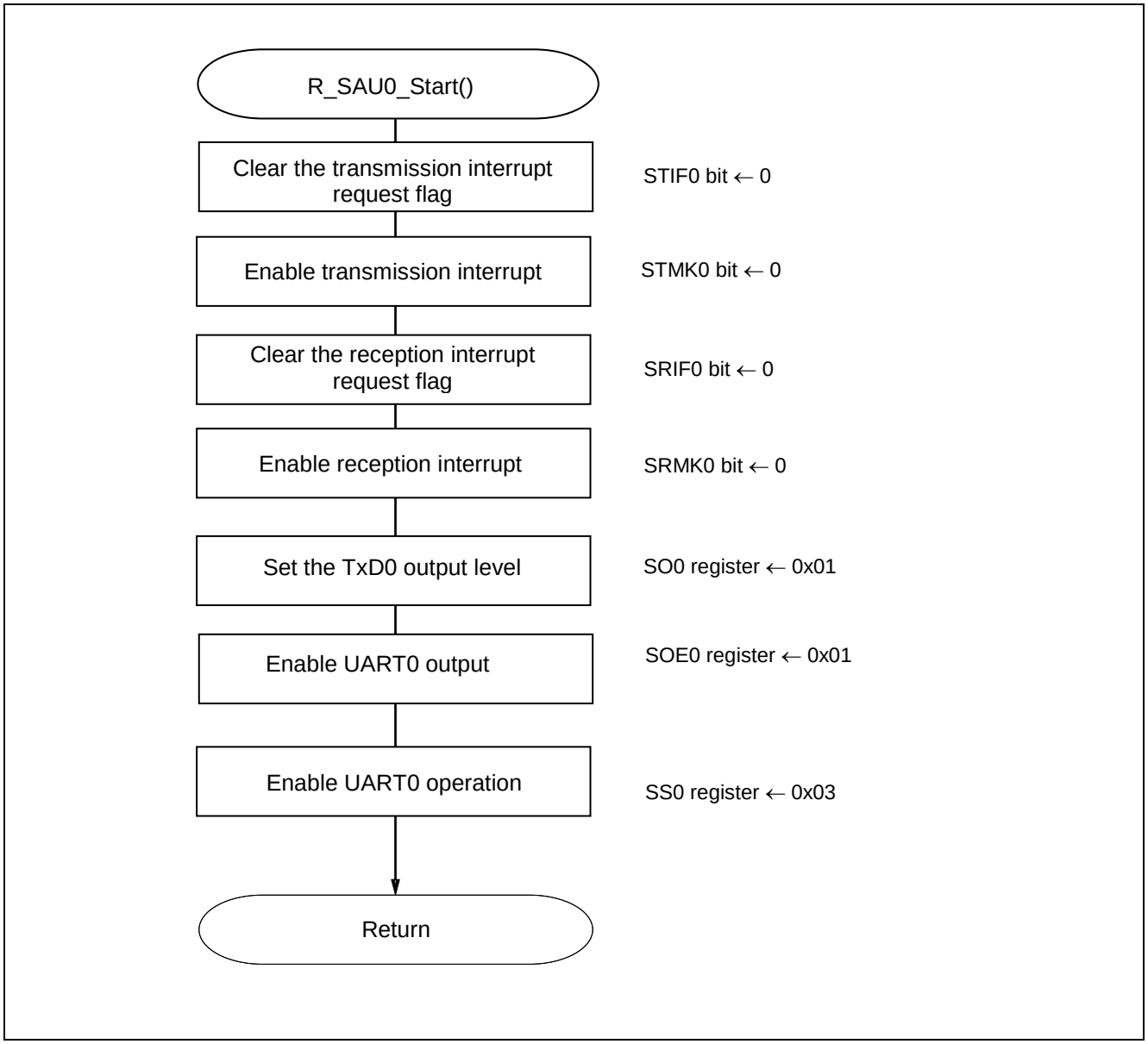

Figure 5.22 Serial Array Unit Operation Start Function

Interrupt setting

- Interrupt request flag register (IF0L)
  Clear the interrupt request flag
- Interrupt mask flag register (MK0L)
  Cancel interrupt mask

Symbol: IF0L (for 10-pin products)

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
x	x	**0**	**0**	**0**	x	x	x

SREIF0	SRIF0	STIF0	Interrupt request flag
0	**0**	**0**	**No interrupt request signal is generated**
1	**1**	**1**	**Interrupt request is generated, interrupt request status**

Symbol: MK0L (10-pin products)

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	x	**0**	**0**	**1**	x	x	x

SREMK0	SRMK0	STMK0	Interrupt processing control
0	**0**	**0**	**Enables interrupt processing.**
1	**1**	**1**	**Disable interrupt processing**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Transition to communication wait state

- Serial channel start register 0 (SS0)
  Operation start

Symbol: SS0

7	6	5	4	3	2	1	0
0	0	0	0	SS03	SS02	SS01	SS00
0	0	0	0	x[Note]	x	**1**[Note]	**1**

Bits 3 to 0

SS0n	Channel n operation start trigger
0	Trigger operation is not performed
1	**SE0n is set to 1, and a communication wait state is entered.**

Note For UART reception, wait for 4 f_{CLK} clock cycles or more before setting SS0n to 1, after setting the RXE0n bit of the SCR0n register to 1.

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.6.15 Temperature Data Transmission Function

Figure 5.23 shows the flowchart for the temperature data transmission function.

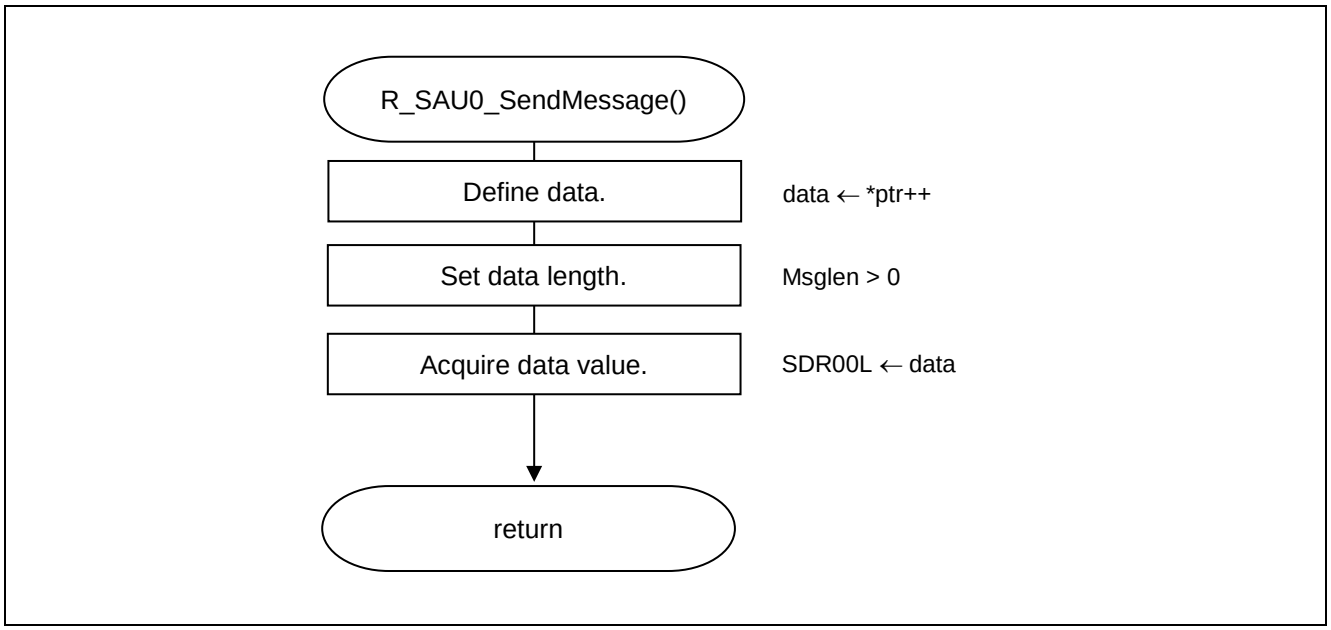

Figure 5.23 Temperature Data Transmission Function

5.6.16 Reception Error Interrupt Function

Figure 5.24 shows the flowchart for the UART0 reception error interrupt function.

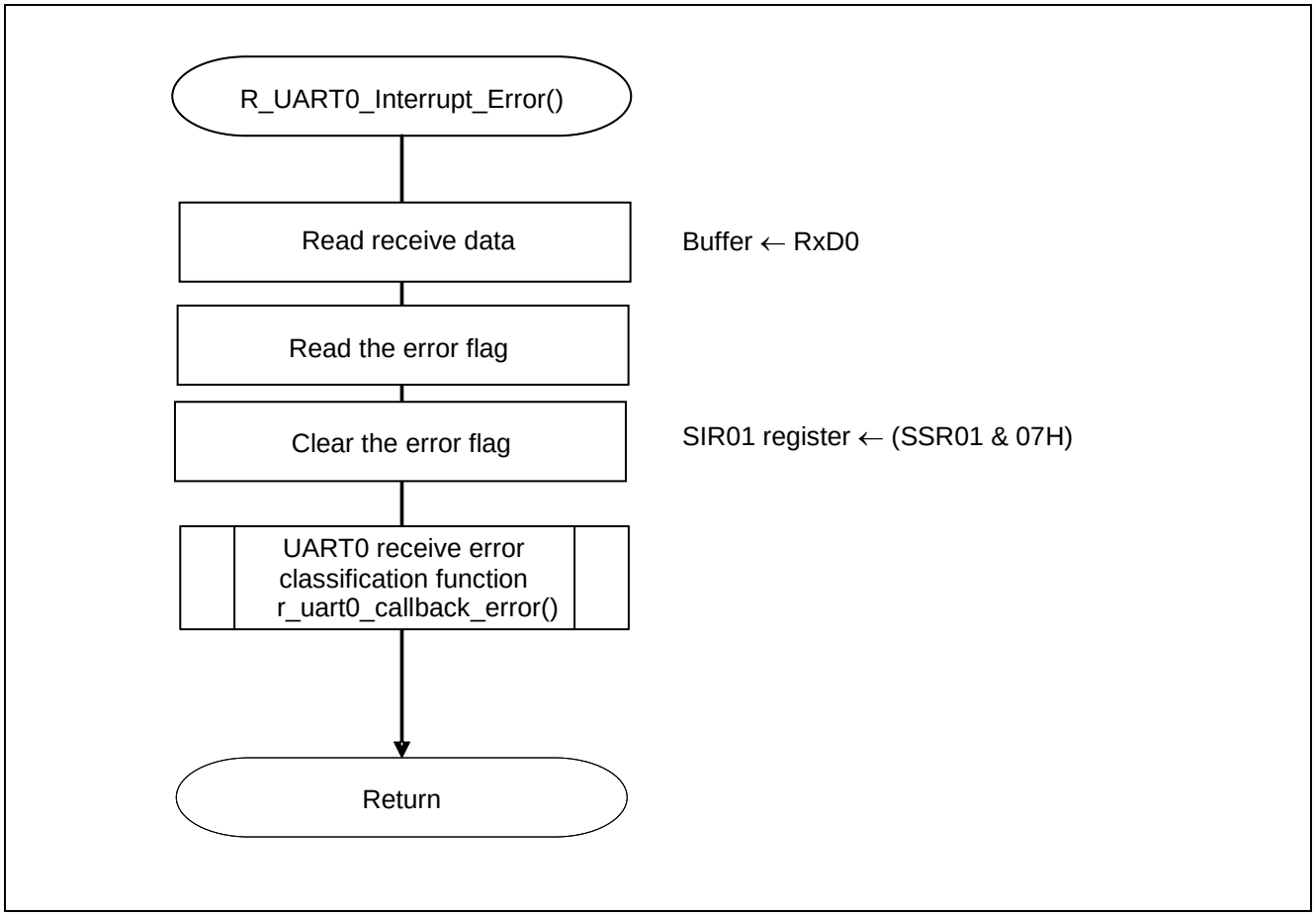

Figure 5.24 Reception Error Interrupt Function

5.6.17 Reception Error Classification Function

Figure 5.25 shows the flowchart for the UART0 reception error classification function.

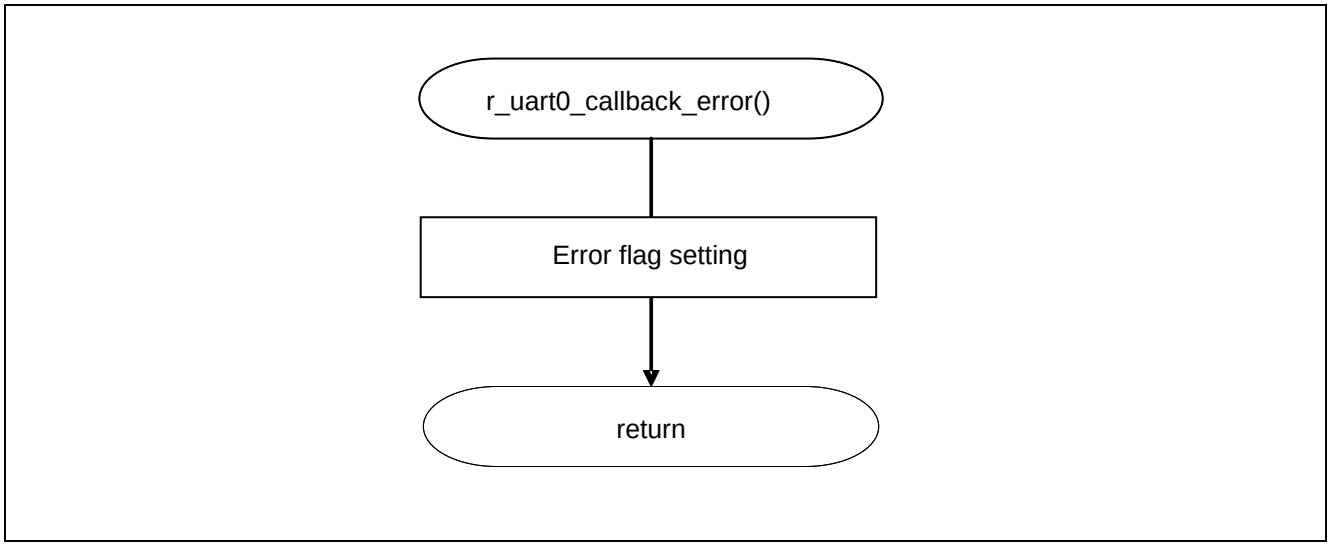

Figure 5.25 Reception Error Classification Function

5.6.18 Interrupt Processing

Figure 5.26 shows the flowchart of interrupt setup.

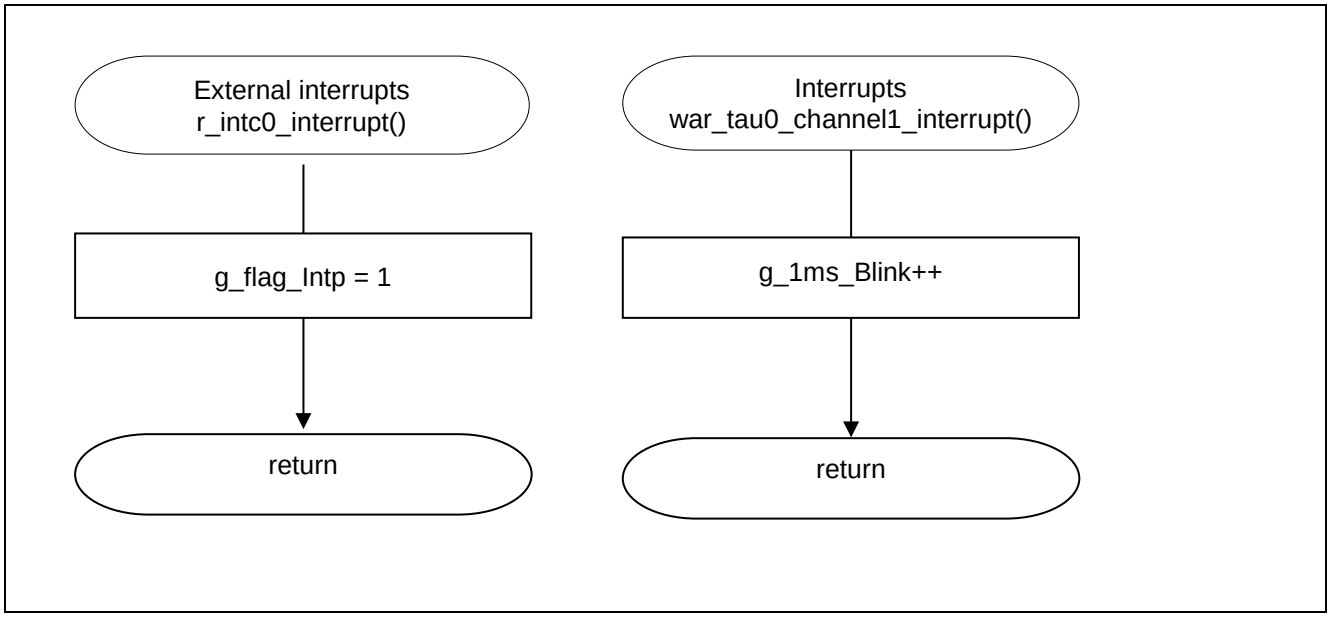

Figure 5.26 Flowchart of Interrupt Processing

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Revision History <revision history,rh>

Rev.	Date	Description	
		Page	Summary
1.00	2018.4.13	-	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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