Interval Timer Using Interrupt Function of Watchdog Timer
(With Clock Correction)

Introduction
This application note explains realizing method of the interval timer which uses interval interruption of a watchdog timer (WDT), without using a timer array unit (TAU). In this application note, frequency calibration is performed by software and interval timer accuracy is raised to less than ±3%. (Less than or equal to ±3% of accuracy is actual measurement in ambient temperature 25°C.)

Target Device
RL78/G10

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.
Contents

1. Specifications .................................................................................................................3
    1.1 Accuracy Calibration of Interval Time ...........................................................................6
    1.2 Accuracy Calibration of Interval Time during Operation ..............................................7
    1.3 Actual Measured Value of Interval Timer (Reference) ..................................................8

2. Operation Check Conditions ...........................................................................................9

3. Related Application Note ...............................................................................................9

4. Description of the Hardware ........................................................................................10
    4.1 Hardware Configuration Example ..............................................................................10
    4.2 List of Pins to be Used .............................................................................................10

5. Description of the Software ..........................................................................................11
    5.1 Operation Outline .....................................................................................................11
    5.2 List of Option Byte Settings ....................................................................................14
    5.3 List of Constants .......................................................................................................14
    5.4 List of Variables .......................................................................................................15
    5.5 List of Functions (Subroutines) ................................................................................16
    5.6 Function Specifications ............................................................................................17
    5.7 Flowcharts ...............................................................................................................19
        5.7.1 CPU Initialization Function ...............................................................................20
        5.7.2 I/O Port Setup ..................................................................................................21
        5.7.3 Clock Generation Circuit Setup .........................................................................23
        5.7.4 INTP0 Initialization .........................................................................................24
        5.7.5 INTWDTI Initialization ...................................................................................27
        5.7.6 Main Processing ..............................................................................................30
        5.7.7 Interval Setup ..................................................................................................31
        5.7.8 INTWDTI Generation Period Measurement (BC register, WDT counter clear) ....32
        5.7.9 INTWDTI Generation Period Measurement ....................................................33
        5.7.10 INTP0 Interrupt Processing ............................................................................34
        5.7.11 INTWDTI Interrupt Processing .......................................................................35

6. Sample Code ..................................................................................................................39

7. Documents for Reference .............................................................................................39
1. Specifications

In this application note, the interval timer which can be set up from 100 ms to 500 ms (every 100 ms) using WDT is realized. The interval timer counts and generates the interval time for 100 ms. The main program stands by interruption (INTWDTI) of a watchdog timer in the STOP mode after initial setting of an interval timer. The interval time for 100 ms measures the number of times of generating of INTWDTI at counting by software. The interval time for 100 ms is calibrated by adjusting this number of times of counting.

The LED drive will be reversed if the setup interval time (100 ms to 500 ms) lapses. Interval time is set up by the number of times of keypress of SW1 (INTP0). When SW1 is pressed, INTP0 occurs and it counts up the number of times of having been pressed. Interval time is set as 100 ms after reset, and whenever SW1 is pressed, 100 ms is added. When SW1 is pressed in the state of 500 ms interval time, an interval returns to 100 ms.

Table 1.1 shows the peripheral function to be used and its use.

Figure 1.1 shows the overview of operations.

Figure 1.2 shows the interval timer operation using WDT.

Specific method to calibrate the interval time is described in “1.1 Accuracy Calibration of Interval Time” and “1.2 Accuracy Calibration of Interval Time during Operation”.

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog timer</td>
<td>The base time of the interval timer is made by interval interruption of WDT.</td>
</tr>
<tr>
<td>INTP0 (External interrupt)</td>
<td>Changes the interval time of interval timer.</td>
</tr>
</tbody>
</table>
Figure 1.1  Overview of Operations

- **Interval time: 100ms**
  - LED repeats “lighting for 100 ms → Lights-out for 100ms”.
  - Press SW1 (INTP0)

- **Interval time: 200ms**
  - LED repeats “lighting for 200 ms → Lights-out for 200ms”.
  - Press SW1 (INTP0)

- **Interval time: 300ms**
  - LED repeats “lighting for 300 ms → Lights-out for 300ms”.
  - Press SW1 (INTP0)

- **Interval time: 400ms**
  - LED repeats “lighting for 400 ms → Lights-out for 400ms”.
  - Press SW1 (INTP0)

- **Interval time: 500ms**
  - LED repeats “lighting for 500 ms → Lights-out for 500ms”.
  - Press SW1 (INTP0)
An interval counter will be counted down, if the usual period count is performed and a counter is set to 0 for 100 ms.

Performs 100ms counter calibration processing when INTEDTI is generated in the state of 100ms counter is set to 0. Generation period of INTWDTI is measured by the software. Waits for generating of INTWDTI, counting up BC register used for the generating period measurement of INTWDTI.

Using the generation period (BC register value) of INTWDTI measured in the procedure<2>, the number of times of generating INTWDTI for approximately 100 ms is calculated, and it is set to the 100 ms counter.

The usual period count is performed. Whenever INTWDTI occurs, counts down 100ms counter.
1.1 Accuracy Calibration of Interval Time

(1) Period measurement of INTWDTI

Measures the generation period of INTWDTI by software. Figure 1.3 shows a period measurement program. This program clears WDT, and then counts BC register until INTWDTI is generated. Since the number of instruction execution clocks of CLOOP in this program is 7, if CPU clock is operated by 10MHz, execution of a CLOOP takes 0.7us. Since the count value of BC register is 5378 when INTWDTI’s cycle is the longest (3.76 ms (=2^6 / (15kHz±15%) × 0.75)), realization is fully possible by 16-bit BC register.

```
MOV WDTE, #0ACH ; clear watch dog timer
CLOOP:
    INCW BC        ; Count up (2 clocks)
    BF WDTIIF, $CLOOP ; Wait for WDTI interrupt (5 clocks)
```

Figure 1.3 INTWDTI Period Measurement by Software

(2) The calculation method of a 100ms counter.

Based on the result of measuring period of INTWDTI, calculates the number of times of INTWDTI generation which uses the closest time to 100 ms.

Generation period of INTWDTI is calculated by the following formula.

\[
\text{Generation period of INTWDTI} = 2^6 / f_{IL} \times 0.75
\]

\( f_{IL} \): Low-speed on-chip oscillator (LOCO) frequency

Since the accuracy of \( f_{IL} \) is 15kHz±15%, generation period of INTWDTI is from 2.783ms to 3.765ms. Therefore, the number of times of INTWDTI generation to use the time which is the closest to 100 ms will be 27 to 36 times.

Next, judgment conditions are calculated in order to calculate the number of times of INTWDTI generation from the count value of BC register which uses for 100 ms. In order to judge which shall become the number of times of INTWDTI generation between 27 and 28, BC counted value when the number of times of INTWDTI generating which is an intermediate value is 27.5 is calculated. Similarly, calculates BC count value (C) at the time that the number of times of INTWDTI generation is from 28.5 to 35.5 (on 1 to 1 basis). (Refer to Table 2.1.)
Table 1.2 The Number of Times of INTWDTI Generation to Use the Closest to 100 ms

<table>
<thead>
<tr>
<th>(A) The number of times of count</th>
<th>(B) Period (ms) Note</th>
<th>(C) BC count value =((B) / 0.7us)</th>
<th>(D) =((C) / 128)</th>
<th>(E) 66−(D)</th>
<th>The number of times that INTWDTI generation occurs for 100 ms.</th>
</tr>
</thead>
<tbody>
<tr>
<td>27.5</td>
<td>3.64</td>
<td>5194</td>
<td>40</td>
<td>26*</td>
<td>27</td>
</tr>
<tr>
<td>28.5</td>
<td>3.51</td>
<td>5012</td>
<td>39</td>
<td>27*</td>
<td>28</td>
</tr>
<tr>
<td>29.5</td>
<td>3.39</td>
<td>4842</td>
<td>37</td>
<td>29</td>
<td>29</td>
</tr>
<tr>
<td>30.5</td>
<td>3.28</td>
<td>4683</td>
<td>36</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>31.5</td>
<td>3.17</td>
<td>4535</td>
<td>35</td>
<td>31</td>
<td>31</td>
</tr>
<tr>
<td>32.5</td>
<td>3.08</td>
<td>4395</td>
<td>34</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>33.5</td>
<td>2.99</td>
<td>4264</td>
<td>33</td>
<td>33</td>
<td>33</td>
</tr>
<tr>
<td>34.5</td>
<td>2.90</td>
<td>4140</td>
<td>32</td>
<td>34</td>
<td>34</td>
</tr>
<tr>
<td>35.5</td>
<td>2.82</td>
<td>4024</td>
<td>31</td>
<td>35</td>
<td>35</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>36**</td>
</tr>
</tbody>
</table>

Note In this table, the value rounded off with the third place of the decimal is indicated.

* Target of calibration.

In order to compute simply this number of times of INTWDTI generation takes about 100 ms, asks for the approximate expression using the counted value (C) of BC register. If the counted value (C) of BC register is divided by 128 (A 1-bit shift to the left is carried out in fact, and the value of B register is taken), the result of an integer will be obtained mostly. In order to adjust this value of (D) to 27 to 36 which is the number of times of INTWDTI generation, the value of (D) is subtracted from 66. (E) If 1 is added to the discontinuous calibration of (E) (*), the continuous integral values from 27 to 36 will be acquired.

The program which performs this processing is Figure 1.4, and it is a program takes 7clocks.

```
SHLW BC, 1 ; 1bit shift left
MOV A, #66
SUB A, ; get loop count data
CMP A, #28 ; check less than 28
SKNC
INC A, ; adjust +1 if 27 or 26
```

Figure 1.4 The Program which Calculates the Number of Times of INTWDTI Generating for 100 ms

The 100 ms counter is realized by above-mentioned processing.

### 1.2 Accuracy Calibration of Interval Time during Operation

In order to maintain the accuracy of the interval time of the interval timer which uses the interruption function of a watchdog timer, it is necessary to perform measurement and calibration of interval time periodically. In this application note, when starting the count for 100 ms, measurement and calibration of INTWDTI generation period are performed.
1.3 Actual Measured Value of Interval Timer (Reference)

Table 1.3 Actual Measured Value of Interval Timer (TA = 25°C) realized in this application note. Actual measured values in Table 1.3 are results in ambient temperature (TA) = 25°C.

Since the relative error of 100ms which is the standard of each interval time is 2.3%, the relative error for 200ms to 500ms is 2.3% similarly.

Table 1.3 Actual Measured Value of Interval Timer (TA = 25°C)

<table>
<thead>
<tr>
<th>Target value (ms)</th>
<th>Actual measured value (ms)</th>
<th>Relative error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>97.7</td>
<td>2.3</td>
</tr>
<tr>
<td>200</td>
<td>195.4</td>
<td>2.3</td>
</tr>
<tr>
<td>300</td>
<td>293.1</td>
<td>2.3</td>
</tr>
<tr>
<td>400</td>
<td>390.7</td>
<td>2.3</td>
</tr>
<tr>
<td>500</td>
<td>488.4</td>
<td>2.3</td>
</tr>
</tbody>
</table>
2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller used</td>
<td>RL78/G10 (R5F10Y16)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>• High-speed on-chip oscillator (HOCO) clock: 10 MHz</td>
</tr>
<tr>
<td></td>
<td>• CPU/peripheral hardware clock: 10 MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5.0 V (Operation is possible over a voltage range of 2.9 to 5.5 V.)</td>
</tr>
<tr>
<td></td>
<td>SPOR Operating Voltage: Rising voltage: 2.90V Falling voltage: 2.84V</td>
</tr>
<tr>
<td>Integrated development</td>
<td>CubeSuite+ V2.02.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>environment (CubeSuite+)</td>
<td>RA78K0R V1.90 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Assembler (CubeSuite+)</td>
<td>e2studio V2.2.0.13 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development</td>
<td>KPIIT GNURL78-ELF Toolchain V14.0.1 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>environment (e2studio)</td>
<td>RL78/G10 target board (QB-R5F10Y16A-TB)</td>
</tr>
</tbody>
</table>

3. Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G10 Initialization (R01AN1454E) Application Note
4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

![Hardware Configuration Diagram]

Caution: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to \( V_{DD} \) or \( V_{SS} \) via a resistor).
2. \( V_{DD} \) must be held at not lower than the reset release voltage (\( V_{SPOR} \)) that is specified by SPOR.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their function.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P00</td>
<td>Output</td>
<td>Port for LED drive</td>
</tr>
<tr>
<td>P137/INTP0</td>
<td>Input</td>
<td>Switch input for interval time setup (SW1)</td>
</tr>
</tbody>
</table>
5. Description of the Software

5.1 Operation Outline

In this application note, waits for INTWDTI generating in the STOP mode after initial setting of an interval timer at a
main program.

At the time of the count start for 100 ms, accuracy calibration of the interval time is performed. The generation period
of INTWDTI is counted by software and a 100ms counter (variable TIMEBASE) is set up from the result. After that,
100ms counter is counted down to the every INTWDTI generating.

The switch (SW1) input for interval time setting is always received. If SW1 is pressed, a processing for countermeasure
against chattering is performed. If INTP0 interrupt occurs by keypress of SW1, INTP0 interruption is disabled, the
counter for a chattering measure (variable CHATCOUNT) will be set up, and INTP0 interruption will be disabled.
Whenever INTWDTI occurs, the counter for a chattering measure (variable CHATCOUNT) is counted down, and if
chattering removal time passes (variable CHATCOUNT = 0), the input level of P137-/INTP0 pin will be checked. If
P137-/INTP0 pin is a low level, it will judge with SW1 having been pushed, and INTP0 interruption is permitted again,
and the counter for the number of times of keypress of SW1 (variable KEYCOUNT) is counted up. The data
corresponding to the counter for the number of times of keypress of SW1 (variable KEYCOUNT) is set as an interval
counter (variable PERIOD) as next interval time.

100ms counter (variable TIMEBASE) counts down whenever INTWDTI occurs, and when it becomes the timing for
100 ms (variable TIMEBASE = 0), it will count down an interval counter (variable PERIOD). If the set-up interval time
passes (variable PERIOD = 0), the drive of LED will be reversed and the data corresponding to the counter for the
number of times of keypress of SW1 (variable KEYCOUNT) will be set as an interval counter (variable PERIOD) as
next interval time.

(1) Initializes peripheral functions to be used.

   <Setting conditions>
   a) Carries out the mask of the INTWDTI interruption and sets an interrupt-priorities level to a high priority.
   b) Sets the valid edge of INTP0 as the falling edge detection, and release the interrupt mask of INTP0.

(2) Initializes variables to be used.

   a) Sets the address of the processing for countermeasure against chattering (label: IINTWDTISUB) to the branch
destination address in an INTWDTI interrupt handler (variable: PROCEDURE).
   b) Clears the counter (variable KEYCOUNT) for the number of times of keypress of SW1.
   c) Clears the counter (variable CHATCOUNT) for countermeasure against chattering.

(3) Starts count of 100ms counter and measures the time to INTWDTI generating.

   a) Clears BC register which is used for measuring generation period of INTWDTI.
   b) Clears the counter of WDT.
   c) Waits for generating of INTWDTI, counting up BC register.
   d) If INTWDTI occurs, the number of times of INTWDTI generation which uses the closest time to 100 ms will
be calculated based on the generation period (BC register value) of INTWDTI, and it will set to a 100ms
counter (variable TIMEBASE).
(4) Sets the interval time.

Sets the value of interval storing table “TINTVL[KEYCOUNT]” to Interval setting variable “PERIOD”. After reset, KEYCOUNT is cleared before this processing, and TINTVL [KEYCOUNT] is set to 1. Therefore, the interval time after reset is set as 100ms (PERIOD=1).

(5) Switches off LED, releases interrupt mask of INTWDTI, and enables vector interrupt.

(6) Shifts to STOP mode and stands by interruption. The main program executes a STOP command by an infinite loop. All subsequent program processing is performed by the interrupt handler of INTP0, or the interrupt handler of INTWDTI.

(7) If INTP0 interrupt occurs, sets 9 to the counter for countermeasure against chattering (variable CHATCOUNT), disables INTP0 interruption, and escapes from processing.

(8) Generating of INTWDTI will perform chattering measure processing and 100ms count processing.

Generating of INTWDTI will run the program in the interrupt handler which is accepted by release of STOP mode. (From STOP mode release to start interruption processing, it will take tens us of the STOP release time. This is about 1 to 2% of INTWDTI generation period of 3.2ms. At the time of accuracy calibration of a 100ms counter, this STOP release time is rectified by the initial value of BC register.) The flow of concrete processing is shown below.

a) Clears WDT counter.

b) During the count operation for 100ms, chattering measure processing and 100ms count processing are performed.

The flow of chattering measure processing is shown below.

- When counted value for countermeasure against chattering (variable CHATCOUNT) is 0, moves to 100ms count processing. When counted value for countermeasure against chattering (variable CHATCOUNT) is other than 0, counts down the variable of CHATCOUNT.

- When Variable CHATCOUNT is set to zero and chattering judging waiting time passes, INTP0 interruption is permitted and the input level of P137/INTP0 pin is checked. When the variable of CHATCOUNT is other than 0, moves to 100ms count processing.

- If the input logic of P137/INTP0 pin is low level, judges that SW1 is pushed, and counts up the counter (variable KEYCOUNT) for the number of times of SW1 keypress. If the input logic of P137/INTP0 pin is high level, judges that SW1 is not pushed, and moves to the 100ms count processing.

- When the number of times of SW1 keypress (variable KEYCOUNT) exceeds the range of the interval table TINTVL, clears the number of times of SW1 keypress, and shifts to 100ms count processing.
The flow of 100ms count processing is shown below.

- Counts down the 100ms counter (variable TIMEBASE).
- When the value of 100ms counter (variable TIMEBASE) is 0, counts down the interval counter (variable PERIOD).
  When the value of 100ms counter (variable TIMEBASE) is other than 0, executes following processes.
- When the value of interval counter (variable PERIOD) is 0 (specified interval is completed), sets the value (variable TINTVL [KEYCOUNT]) of an interval table to an interval counter (variable PERIOD), and reverses the drive of LED. Next, sets the address of measurement processing (label: MEASURESUB) of the time to INTWDTI generating to the branch destination address in an INTWDTI interrupt handler (variable PROCEDURE).
  When the value of interval counter (variable PERIOD) is 0, executes following processes.

At the time of the count start for 100 ms, performs chattering measure processing and 100ms count processing after the generation period measurement of INTWDTI.

The flow of measuring generation period of INTWDTI is shown below.

- Sets the constant TMOFFSET + 1 to BC register as the initial value.
  In this application note, the constant TMOFFSET is set to 40. STOP mode release time takes 28.1us because it is 27us (TYP) + 11 clocks (if vector interrupt is performed) and RL78/G10 is operated by 10MHz in this application note. Since count-up of BC register takes 7 clocks (0.7us), the offset value is calculated as follows.

\[
TMOFFSET = (27\text{us} + 11 \times 0.1\text{us}) \div 0.7\text{us} = 40
\]

In order to reflect 6 clocks because of following 3 reasons, 1 is added to TMOFFSET. Before performing count-up processing of BC register, the contents of the BC register are evacuated to a stack (2 clocks). Sets the initial value to BC register (1 clock). And branches to BC register count-up processing (3 clocks).
  Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about STOP mode release time.

- Waits for generating of INTWDTI, counting up BC register.
- If INTWDTI occurs, calculates the number of times of INTWDTI generating for about 100ms based on BC register value, and sets it to the 100ms counter (variable TIMEBASE).
- Counts down the 100ms counter (variable TIMEBASE).
- Sets the address of chattering measure processing (label: IINTWDTISUB) to the branch destination address in an INTWDTI interrupt handler (variable PROCEDURE), and performs chattering measure processing and 100-ms count processing.
5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000C0H/010C0H</td>
<td>11110001B</td>
<td>Enables watchdog timer operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Starts count after reset release.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Interval interrupt time: $2^5 / f_{IL} \times 0.75$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Enables counter operation at the HALT/STOP mode.</td>
</tr>
<tr>
<td>000C1H/010C1H</td>
<td>11110111B</td>
<td>P125/RESET Pin: RESET input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(On-chip pull-up resistance is always valid.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SPOR voltage</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rising voltage: 2.90 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling voltage: 2.84 V</td>
</tr>
<tr>
<td>000C2H/010C2H</td>
<td>11111010B</td>
<td>HOCO : 10 MHz</td>
</tr>
<tr>
<td>000C3H/010C3H</td>
<td>10000101B</td>
<td>Enables the on-chip debugger.</td>
</tr>
</tbody>
</table>

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

<table>
<thead>
<tr>
<th>Constant</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMOFFSET</td>
<td>40</td>
<td>Offset value of BC register</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BC register counted value for STOP mode release time)</td>
</tr>
<tr>
<td>CHATNo</td>
<td>9</td>
<td>INTWDTI counted value for countermeasure against chattering.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In order to remove chattering, checks the input logic of a P137-/INTP pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>after waiting for 9 times of INTWDTI occurrence following INTP0 generation</td>
</tr>
</tbody>
</table>
5.4 List of Variables

Table 5.3 lists the variables that are used in this sample program.

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 bits arrays</td>
<td>TINTVL</td>
<td>Interval table</td>
<td>IINTWDTI, SETINTERVAL</td>
</tr>
<tr>
<td>1 bits</td>
<td>PROCEDURE</td>
<td>The branch destination address in an INTWDTI interrupt handler. It is set as (label: MEASURESUB) at the time of 100ms count starting, and as (label: IINTWDTISUB) under 100ms counting.</td>
<td>main, IINTWDTI,</td>
</tr>
<tr>
<td>8 bits</td>
<td>KEYCOUNT</td>
<td>Counter for the number of times of keypress of SW1</td>
<td>main, IINTWDTI, SETINTERVAL</td>
</tr>
<tr>
<td>8 bits</td>
<td>CHATCOUNT</td>
<td>Counter for countermeasure against chattering</td>
<td>main, IINTWDTI</td>
</tr>
<tr>
<td>8 bits</td>
<td>TIMEBASE</td>
<td>100ms counter</td>
<td>main, IINTWDTI</td>
</tr>
<tr>
<td>8 bits</td>
<td>PERIOD</td>
<td>Interval counter</td>
<td>IINTWDTI, SETINTERVAL</td>
</tr>
</tbody>
</table>
5.5 List of Functions (Subroutines)

Table 5.4 lists the functions (subroutines).

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET_START</td>
<td>Initialization of CPU</td>
</tr>
<tr>
<td>SINIPORT</td>
<td>Setup of I/O port</td>
</tr>
<tr>
<td>SINICLK</td>
<td>Setup of the clock generator</td>
</tr>
<tr>
<td>SINIINTP0</td>
<td>Initialization of INTP0</td>
</tr>
<tr>
<td>SINIWDT</td>
<td>Initialization of INTWDTI</td>
</tr>
<tr>
<td>SETINTERVAL</td>
<td>Setup of interval</td>
</tr>
<tr>
<td>GETINTERVAL</td>
<td>Measuring INTWDTI generation period (Clears the counter of BC register and WDT before measurement.)</td>
</tr>
<tr>
<td>CLOOP</td>
<td>Measuring INTWDTI generation period (Does not clears the counter of BC register and WDT before measurement.)</td>
</tr>
<tr>
<td>IINTP0</td>
<td>INTP0 Interrupt servicing</td>
</tr>
<tr>
<td>IINTWDTI</td>
<td>INTWDTI Interrupt servicing</td>
</tr>
</tbody>
</table>
5.6 Function Specifications
This section describes the specifications for the functions that are used in this sample program.

[Function Name] RESET_START

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Initialization of CPU in the case of reset/start</th>
</tr>
</thead>
<tbody>
<tr>
<td>Explanation</td>
<td>Calls main processing after setting up of the stack pointer and initialization of the hardware.</td>
</tr>
<tr>
<td>Arguments</td>
<td>• None</td>
</tr>
<tr>
<td>Return value</td>
<td>• None</td>
</tr>
<tr>
<td>Remarks</td>
<td>None</td>
</tr>
</tbody>
</table>

[Function Name] SINIPORT

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Initialization of P0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Explanation</td>
<td>Sets P01/AN10 to P04/ANI3 pins as the digital output.</td>
</tr>
<tr>
<td>Arguments</td>
<td>• None</td>
</tr>
<tr>
<td>Return value</td>
<td>• None</td>
</tr>
<tr>
<td>Remarks</td>
<td>None</td>
</tr>
</tbody>
</table>

[Function Name] SINICLK

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Initialization of HOCODIV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Explanation</td>
<td>Sets the frequency of high-speed on-chip oscillator clock to 10MHz.</td>
</tr>
<tr>
<td>Arguments</td>
<td>• None</td>
</tr>
<tr>
<td>Return value</td>
<td>• None</td>
</tr>
<tr>
<td>Remarks</td>
<td>None</td>
</tr>
</tbody>
</table>

[Function Name] SINIINTP0

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Initialization of INTP0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Explanation</td>
<td>Sets INTP0 as falling edge detection.</td>
</tr>
<tr>
<td>Arguments</td>
<td>• None</td>
</tr>
<tr>
<td>Return value</td>
<td>• None</td>
</tr>
<tr>
<td>Remarks</td>
<td>None</td>
</tr>
</tbody>
</table>

[Function Name] SINIWDT

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Initialization of INTWDTI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Explanation</td>
<td>Sets the 75% interval interrupt priorities of WDT to the level 0 (top priority).</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return value</td>
<td>None</td>
</tr>
<tr>
<td>Remarks</td>
<td>None</td>
</tr>
</tbody>
</table>
[Function Name] SETINTERVAL

Synopsis: Setup of interval

Explanation: Reads the interval according to the number of times of SW1 keypress from a table, and sets to the variable (PERIOD) for a count.

Arguments: None

Return value: None

Remarks: Refers to variable KEYCOUNT.

[Function Name] GETINTERVAL

Synopsis: Measuring INTWDTI generation period (Clears counters of BC register and WDT)

Explanation: Calculates the number of times of INTWDTI generation which uses the closest time to 100 ms by measuring an INTWDTI generating cycle, after clearing BC register and clearing the counter of WDT, and sets a calculation result to 100ms counter (variable TIMEBASE).

Arguments: None

Return value: None

Remarks: None

[Function Name] CLOOP

Synopsis: Measuring INTWDTI generation period

Explanation: The number of times of INTWDTI generation which uses the closest time to 100 ms is calculated by measuring an INTWDTI generation period, and sets a calculation result to a counter (variable TIMEBASE) for 100ms.

Arguments: None

Return value: None

Remarks: None

[Function Name] IINTP0

Synopsis: INTP0 interruption

Explanation: Receives the INTP0 interruption and sets a chattering prevention counter. Disables INTP0 interruption (mask).

Arguments: None

Return value: None

Remarks: None

[Function Name] IINTWDTI

Synopsis: WDT75% interval interruption

Explanation: Receives INTWDTI interruption and performs chattering measure processing at the time of SW1 keypress. Moreover, performs 100ms counter processing, and reverses LED when the set-up interval time passes.

Arguments: None

Return value: None

Remarks: None
5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

![Flowchart of Overall](image)

*The option bytes are referenced before RESET_START is called.

**Figure 5.1** Flowchart of Overall
5.7.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

- **RESET_START**
- Set ES register: \( ES \leftarrow 00H \) (for table reference)
- Set up stack pointer
- Set up redirection
  - Set up i/O ports \( \text{SINIPORT} \)
    - All the ports which can be set as an output are set as an output.
  - Set up clock generation \( \text{SINICLK} \)
    - Select HOCO (10 MHz) as an operation clock.
  - Set up INTPO \( \text{SINITP0} \)
    - Sets INTP0 as falling edge detection and interruption enabled (mask release).
  - Set up INTWDT \( \text{SINIWDT} \)
    - The interrupt-priorities level of INTWDT is set as a high priority.
- Call main routine \( \text{main} \)
- HALT

**Figure 5.2** CPU Initialization Function
5.7.2  I/O Port Setup

Figure 5.3 shows the flowchart for I/O port setup.

Setup of the port mode.

- Port Mode Control Register 0 (PMC0)
  Switching between analog input and digital I/O.
- Port Register 0 (P0)
  Setup of an output latch of each port
- Pull-up Resistor Option Register 0 (PU0)
  On-chip pull-up resistor selection.
- Port Mode Register 0 (PM0)
  Selection of the I/O mode of each port.

Symbol: PMC0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PMC04</td>
<td>PMC03</td>
<td>PMC02</td>
<td>PMC01</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit 4 to 1

<table>
<thead>
<tr>
<th>PMC0n</th>
<th>P0n pin digital I/O/analog input selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Digital I/O (alternate function other than analog input)</td>
</tr>
<tr>
<td>1</td>
<td>Analog input</td>
</tr>
</tbody>
</table>

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.
Symbol: P0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>P04</td>
<td>P03</td>
<td>P02</td>
<td>P01</td>
<td>P00</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>P00</th>
<th>P00 pin output data control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Output 0</td>
</tr>
<tr>
<td>1</td>
<td>Output 1</td>
</tr>
</tbody>
</table>

Symbol: PM0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PM04</td>
<td>PM03</td>
<td>PM02</td>
<td>PM01</td>
<td>PM00</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bit 4 to 0

<table>
<thead>
<tr>
<th>PM0n</th>
<th>P0n pin I/O mode selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Output mode (output buffer on)</td>
</tr>
<tr>
<td>1</td>
<td>Input mode (output buffer off)</td>
</tr>
</tbody>
</table>

Symbol: PU0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>PU04</td>
<td>PU03</td>
<td>PU02</td>
<td>PU01</td>
<td>PU00</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bit 4 to 0

<table>
<thead>
<tr>
<th>PU0n</th>
<th>P0n pin on-chip pull-up resistor selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>On-chip pull-up resistor not connected</td>
</tr>
<tr>
<td>1</td>
<td>On-chip pull-up resistor connected</td>
</tr>
</tbody>
</table>

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.
5.7.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for clock generation circuit setup.

Selection of high-speed on-chip oscillator frequency.

- High-Speed On-Chip Oscillator Frequency Selection Register (HOCODIV)
  Selects the frequency of high-speed on-chip oscillator.

Symbol: HOCODIV

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>HOCODIV2</td>
<td>HOCODIV1</td>
<td>HOCODIV0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Bit 2 to 0

<table>
<thead>
<tr>
<th>HOCODIV</th>
<th>High-speed on-chip oscillator clock frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 1 0</td>
<td></td>
</tr>
<tr>
<td>0 0 1</td>
<td>20MHz</td>
</tr>
<tr>
<td>0 1 0</td>
<td>10MHz</td>
</tr>
<tr>
<td>0 1 1</td>
<td>5MHz</td>
</tr>
<tr>
<td>1 0 0</td>
<td>2.5MHz</td>
</tr>
<tr>
<td>1 0 1</td>
<td>1.25MHz</td>
</tr>
<tr>
<td>Other than above</td>
<td>Setting prohibited</td>
</tr>
</tbody>
</table>
5.7.4 INTP0 Initialization

Figure 5.5 shows the flowchart for INTP0 Initialization.

```
SINIINTP0

Disable INTP0 interrupt
PMK0 bit ← 1

Disable rising edge detection

Enable falling edge detection
EGP0 register ← 00H
EGN0 register ← 01H

Clear INTP0 interrupt request flag
PIF0 bit ← 0

Enable INTP0 interrupt
PMK0 bit ← 0

RET
```

Figure 5.5 INTP0 Initialization
(1) Setup INTP0 pin edge detection.

- External interrupt rising/falling edge enable register (EGP0, EGN0)

  This register specifies the valid edge for INTP0.

  Symbol: EGP0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
</tr>
</tbody>
</table>

  Note: 16-pin products only.

  Symbol: EGN0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

  EGP0 | EGN0 | INTPn pin valid edge selection
  0 0  | 0 0  | Edge detection disabled
  0 1  | 0 1  | Falling edge
  1 0  | 1 0  | Rising edge
  1 1  | 1 1  | Both rising and falling edges

  Note: Refer to ‘RL78/G10 User’s Manual: Hardware’ for more information about the register setting
(2) Setup INTP0 edge detection interrupt.

- Interrupt request flag register (IF0L)
  Clears interrupt request flag.
- Interrupt mask flag register (MK0L)
  Sets up the interrupt mask flag.

Symbol: IF0L

<table>
<thead>
<tr>
<th>Bit</th>
<th>TMIF00</th>
<th>TMIF01H</th>
<th>SREIF0</th>
<th>SRIF0</th>
<th>STIF0</th>
<th>CSIIF00</th>
<th>IICIF00</th>
<th>PIF1</th>
<th>PIF0</th>
<th>WDTIIF</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td></td>
</tr>
</tbody>
</table>

Bit 1

<table>
<thead>
<tr>
<th>PIF0</th>
<th>Interrupt request flag</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt request signal is generated</td>
</tr>
<tr>
<td>1</td>
<td>Interrupt request is generated, interrupt request status</td>
</tr>
</tbody>
</table>

Symbol: MK0L

<table>
<thead>
<tr>
<th>Bit</th>
<th>TMMK00</th>
<th>TMMK01H</th>
<th>SREM0K</th>
<th>SRMK0</th>
<th>STMK0</th>
<th>CSIMK00</th>
<th>IICMK00</th>
<th>PMK1</th>
<th>PMK0</th>
<th>WDTIMK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0/1</td>
<td>x</td>
<td>x</td>
<td></td>
</tr>
</tbody>
</table>

Bit 1

<table>
<thead>
<tr>
<th>PMK0</th>
<th>Interrupt servicing control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Interrupt servicing enabled</td>
</tr>
<tr>
<td>1</td>
<td>Interrupt servicing disabled</td>
</tr>
</tbody>
</table>

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.
5.7.5 INTWDTI Initialization

Figure 5.6 shows the flowchart for INTWDTI Initialization.

![Flowchart for INTWDTI Initialization]

- **SINIWDT**
- Disable INTWDTI interrupt
- Set high priority to interruption
- Clear the INTWDTI interrupt request flag
- WDTIMK bit ← 1
- WDTIPR0 bit ← 0
- WDTIPR1 bit ← 0
- WDTIIF bit ← 0
- RET

Figure 5.6 INTWDTI Initialization
(1) Setup of INTWDTI interrupt

- Interrupt request flag register (IF0L)
  - Clears the interrupt request flag.
- Interrupt mask flag register (MK0L)
  - Sets up the interrupt mask.

Symbol: IF0L

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TMIF00</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>TMIF01H</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>SREIF0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>SRIF0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>STIF0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>CSIIF00</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>IICIF00</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>WDTIIF</th>
<th>Interrupt request flag</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt request signal is generated</td>
</tr>
<tr>
<td>1</td>
<td>Interrupt request is generated, interrupt request status</td>
</tr>
</tbody>
</table>

Symbol: MK0L

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TMMK00</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td>TMMK01H</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td>SREMK0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td>SRMK0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td>STMK0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td>CSIMK00</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td>IICMK00</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0/1</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>WDTIMK</th>
<th>Interrupt servicing control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Interrupt servicing enabled</td>
</tr>
<tr>
<td>1</td>
<td>Interrupt servicing disabled</td>
</tr>
</tbody>
</table>

Note: Refer to ‘RL78/G10 User’s Manual: Hardware’ for more information about the register setting method.
(2) Setup of an interruption priority

- Priority specification flag register (PR00L, PR10L)
  
  Clears the interrupt request flag.

Symbol: PR00L

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMPR000</td>
<td>TMPR001H</td>
<td>SREPR00</td>
<td>SRPR00</td>
<td>STPR00</td>
<td>CSIPR000</td>
<td>IICPR000</td>
<td>PPR01</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

Symbol: PR10L

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMPR100</td>
<td>TMPR101H</td>
<td>SREPR10</td>
<td>SRPR10</td>
<td>STPR10</td>
<td>CSIPR100</td>
<td>IICPR100</td>
<td>PPR11</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>xxPR1x</th>
<th>xxPR0x</th>
<th>Priority Level Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Specifying level 0 (high priority)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Specifying level 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Specifying level 2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Specifying level 3 (low priority)</td>
</tr>
</tbody>
</table>

Note: Refer to ‘RL78/G10 User's Manual: Hardware’ for more information about the register setting method.
5.7.6 **Main Processing**

Figure 5.7 shows the flow chart for main processing.

```
main

- Initialize the variable
- Counts the time to INTWDTI generation.

Setup of interval SETINTERVAL

- Switches off LED
- Releases INTWDTI interrupt mask
- Enable vector interrupt

STOP instruction

Variable: PROCEDURE ← An address of the measure against chattering (label: IINTWDTISUB)
Variable: KEYCOUNT ← 0: Clears counter of the number of times of SW1 keypress.
Variable: CHATCOUNT ← 0: Clears counter for the measure against chattering.
Variable: TIMEBASE ← The number of times of INTWDTI generating about for 100 ms.
Variable: PERIOD ← TINTVL[KEYCOUNT]

P0.0 bit ← 1
WDTIMK bit ← 0
IE bit ← 1

Waits for STOP mode interrupt (INTP0 / INTWDTI).
```

*Figure 5.7 Main Processing*
5.7.7 Interval Setup

Figure 5.8 shows the flow chart for the interval setup.

```
SETINTERVAL

Save BC registers
Saves BC registers on the stack.

Read of the number of times of SW1 keypress
B register ← Variable KEYCOUNT

Read of the interval time
A register ← Table TINTVL value (MOV A, ES:TINTVL[B])

Setup of the interval time
Variable PERIOD ← A register

Return of BC registers
Makes BC registers returned from a stack area.

RET
```

Figure 5.8 Interval Setup
5.7.8 INTWDTI Generation Period Measurement (BC register, WDT counter clear)

Figure 5.9 shows the flow chart for the INTWDTI generation period measurement (BC register, WDT counter clear).

![Flow Chart](image)

**Figure 5.9 Time Measurement to INTWDTI Generating (BC register, WDT clear)**
5.7.9 INTWDTI Generation Period Measurement

Figure 5.10 shows the flow chart for the INTWDTI generation period measurement.

![Flow chart of INTWDTI Generation Period Measurement](image)

Figure 5.10 Time Measurement to INTWDTI Generating

- CLOOP
- Counts up BC register: BC register ← BC register + 1
- INTWDTI is generated?
  - Yes: WDTIIF bit ← 0
  - No: Clears WDT interrupt request flag: WDTIIF bit ← 0
- Clears WDT counter: WDTE register ← ACH
- Calculates the count value: A register ← 66
  - A register ← A register ─ B register
- Count value is 27 or less?
  - No: Clears WDT interrupt request flag: WDTIIF bit ← 0
  - Yes: Calibrates the count value: A register ← A register + 1
- Sets the count value: Variable: TIMEBASE ← A register
- RET
5.7.10 INTP0 Interrupt Processing

Figure 5.11 shows the flowchart for the INTP0 interrupt processing.

INTP0

Disables INTP0 interrupts

PMK0 bit ← 1
(Measure against chattering)

Sets a counter for the measure against chattering

Variable CHATCOUNT ← Constant CHATNo

RETI

Figure 5.11 INTP0 Interrupt Processing
5.7.11 INTWDTI Interrupt Processing

Figure 5.12 shows the INTWDTI interrupt processing (1/3), Figure 5.13 shows the INTWDTI interrupt processing (2/3), and Figure 5.14 show the INTWDTI interrupt processing (3/3).

![INTWDTI Interrupt Processing Diagram]

Figure 5.12 INTWDTI Interrupt Processing (1/3)
Branches here, when the address of measure against chattering processing (label: INTWDTISUB) is set to AX register.

In the middle of the chattering count?

No

Yes

Counts down the counter for measure against chattering

The chattering count was

No

Yes

Enables INTP0 interrupt

Under keypress of SW1?

No

Yes

Counts up the number of times of SW1 keypress

The number of times of SW1 keypress exceeds the maximum?

No

Yes

Clears the number of times of SW1 keypress.

Counts down 100ms counter

A

B

Judges by whether Variable CHATCOUNT is 0.

Variable CHATCOUNT ← Variable CHATCOUNT \(\rightarrow\) 1

Judges by whether Variable CHATCOUNT is 0.

PIF0 bit \(\rightarrow\) 0: Clears the interrupt request flag.
PMK0 bit \(\rightarrow\) 0: Release the interrupt mask.

Judges by whether P13.7 bit is 0.

Variable KEYCOUNT ← KEYCOUNT + 1

Checks whether Variable KEYCOUNT exceeded the number of elements of Table TINTVL.

Variable KEYCOUNT ← 0

Variable TIMEBASE ← TIMEBASE \(\rightarrow\) 1

Yes

Counts down the counter for measure against chattering

Yes

Counts up the number of times of SW1 keypress

The number of times of SW1 keypress exceeds the maximum?

Yes

Clears the number of times of SW1 keypress.

Counts down 100ms counter

Figure 5.13 INTWDTI Interrupt Processing (2/3)
Figure 5.14 INTWDTI Interrupt Processing (3/3)
6. **Sample Code**
The sample code is available on the Renesas Electronics Website.

7. **Documents for Reference**
   RL78/G10 User's Manual: Hardware (R01UH0384E)
   RL78 Family User's Manual: Software (R01US0015E)
   (The latest versions of the documents are available on the Renesas Electronics Website.)

   Technical Updates/Technical Brochures
   (The latest versions of the documents are available on the Renesas Electronics Website.)

All trademarks and registered trademarks are the property of their respective owners.
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Description</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>2014.09.10</td>
<td>-</td>
<td></td>
<td>First Edition</td>
</tr>
<tr>
<td>1.10</td>
<td>2022.09.30</td>
<td>8</td>
<td>Delete IAR information from Table 2.1</td>
<td></td>
</tr>
</tbody>
</table>
General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sale, utilization, or disposal of any product incorporating Renesas Electronics products, if required.

5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.

7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.

8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics semiconductor products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1  October 2020)

Corporate Headquarters
TOYOSU FORESIA, 3-22-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2022 Renesas Electronics Corporation. All rights reserved.