RL78/G10

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A/D Converter (Software Trigger and Sequential Conversion Modes) CC-RL

Introduction

This application note describes the procedures for performing A/D conversion on analog voltages using the RL78/G10's A/D converter (supporting software trigger and sequential conversion modes).

The sample program discussed in this application note performs data conversion on the A/D conversion results and places the converted values in the RL78/G10's internal RAM.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specification

This application note provides examples of using the software trigger and sequential conversion modes of the A/D converter. The A/D converter is placed in select mode and the analog signal input from the P01/ANI0 pin is converted to digital values. Subsequently, the conversion result is subjected to data conversion (shifting the data to the right) and the result is stored in the RL78/G10's internal RAM.

Table 1.1 lists the Peripheral Function to be Used and its Use and Figure 1.1 shows the outline of the conversion operation of the A/D converter.

Table 1.1 Peripheral Function to be Used and its Use

Peripheral Function	Use
A/D converter	Converts the level of the analog signal input from the P01/ANI0 pin.

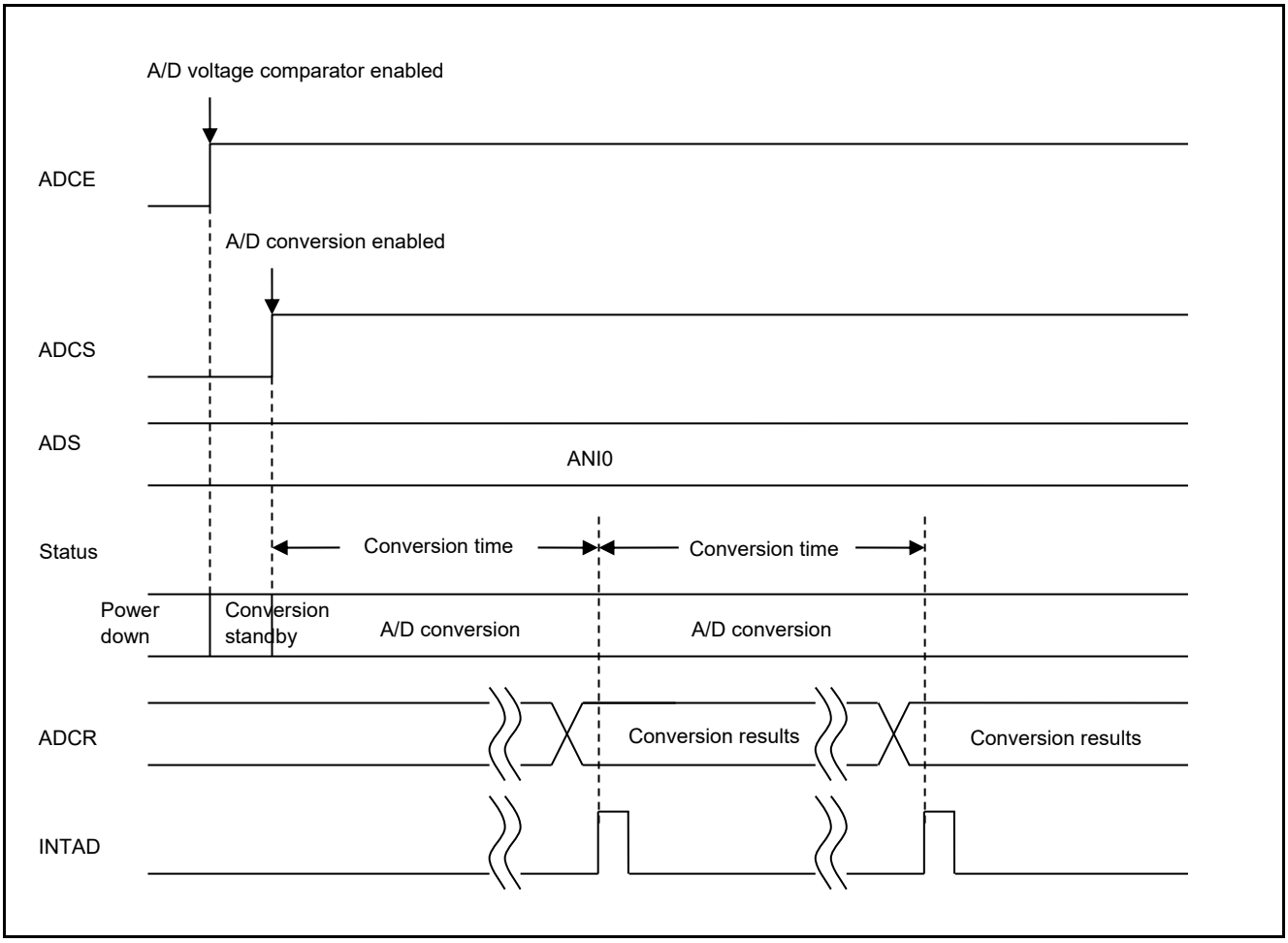

Figure 1.1 Outline of the A/D Converter Conversion Processing

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y16ASP)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 20 MHz • CPU/peripheral hardware clock: 20 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.7 V to 5.5 V.) SPOR detection voltage Falling edge 2.84 V Rising edge 2.90 V
Integrated development environment (CS+)	CS+ for CC V4.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.03.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.2.0.020 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.03.00 from Renesas Electronics Corp.

3. Related Application Note

The application note that is related to this application note is listed below for reference.

- RL78/G10 Initialization CC-RL (R01AN2668E) Application Note
- RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) CC-RL (R01AN2581E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

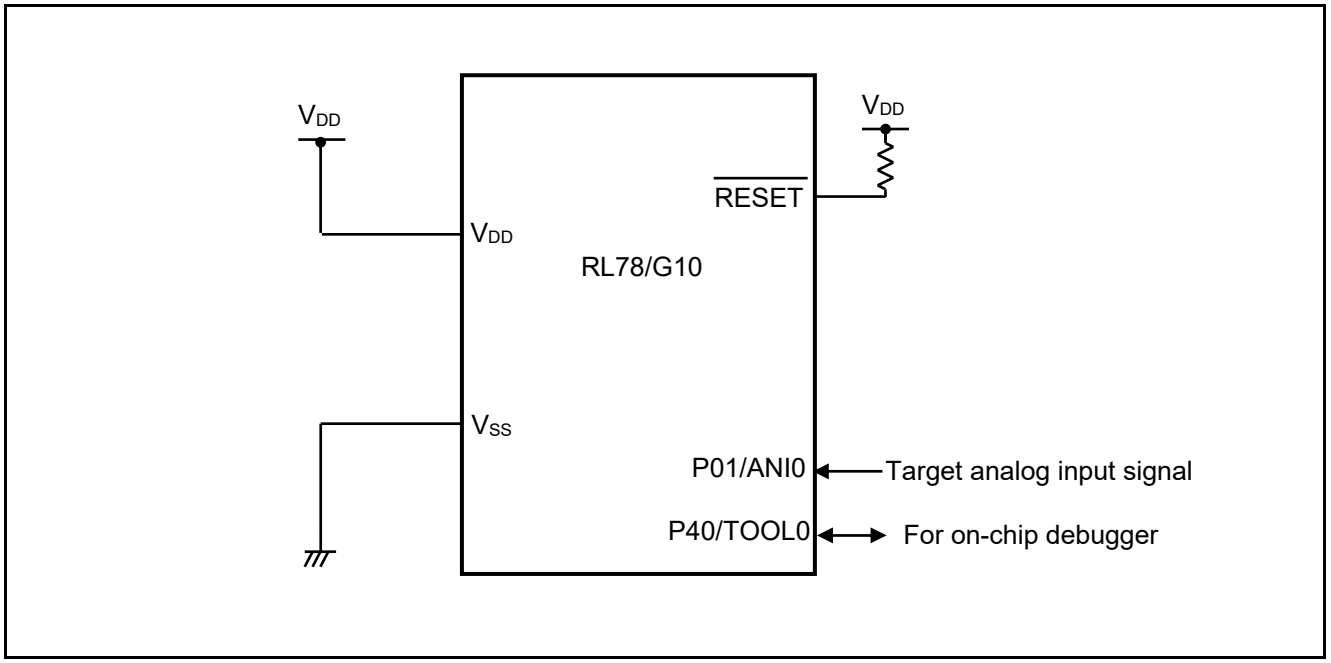

Figure 4.1 Hardware Configuration

Notes: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-dedicated ports separately to V_{DD} or V_{SS} via a resistor).

2 V_{DD} must be held at not lower than the reset release voltage (V_{SPOR}) that is specified as SPOR.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their function.

Table 4.1 Pin to be Used and its Function

Pin Name	I/O	Description
P01/ANI0	Input	A/D converter analog input port

5. Description of the Software

5.1 Operation Outline

This sample code performs A/D conversion on the analog voltage that is input to pin ANI0 using the software trigger and sequential conversion modes of the A/D converter. It awaits the end of A/D conversion in HALT mode. After A/D conversion is completed, the sample code shifts the result of A/D conversion 6 bits to the right and places the result in the internal RAM of the RL78/G10.

(1) Initialize the A/D converter.
<Setup conditions>

- Pin P20/ANI0 is used for the analog input.
- A/D conversion channel selection mode is set to select mode.
- A/D conversion operation mode is set to sequential conversion mode.
- A/D conversion is started using the software trigger.
- The A/D conversion end interrupt (INTAD) is used.

(2) The sample program sets the ADCS bit of the ADM0 register to 1 (A/D conversion start) to start A/D conversion and executes the HALT instruction to place the chip in the HALT mode and wait for an A/D conversion end interrupt.

(3) After completing the A/D conversion of the voltage input from pin ANI0, the A/D converter transfers the result of A/D conversion to the ADCR register and generates an A/D conversion end interrupt.

(4) On release from the HALT mode in response to the A/D conversion end interrupt, the sample program reads the result of A/D conversion from the ADCRL register, shifts the result 6 bits to the right, and stores the shifted data in the internal RAM of the RL78/G10.

(5) The chip returns to the HALT mode and waits for an A/D conversion end interrupt.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H	11101110B	Stops the watchdog timer operation. (Stops counting after the release of the reset state.)
000C1H	11110111B	SPOR detection voltage Falling edge 2.84 V Rising edge 2.90 V
000C2H	11111001B	HOCO: 20 MHz
000C3H	10000101B	Enables the on-chip debugging function.

5.3 List of Variables

Table 5.2 lists the global variable that is used by this sample program.

Table 5.2 Global Variable

Type	Variable Name	Contents	Function Used
unsigned short	g_result_buffer	Area for storing the A/D conversion results	main ()

5.4 List of Functions

Table 5.3 lists the functions that are used by this sample program.

Table 5.3 Functions

Function Name	Outline
R_ADC_Set_OperationOn	Enables the A/D voltage comparator.
R_ADC_Start	Starts A/D conversion.
R_ADC_Get_Result	Gets A/D conversion results.

5.5 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_ADC_Set_OperationOn

Synopsis	Enable A/D voltage comparator.
Header	r_cg_adc.h
Declaration	void R_ADC_Set_OperationOn (void)
Explanation	Enables the A/D voltage comparator for operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Start

Synopsis	Start A/D conversion.
Header	r_cg_adc.h
Declaration	void R_ADC_Start (void)
Explanation	Enables A/D conversion end interrupts and starts A/D conversion processing.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Get_Result

Synopsis	Get A/D conversion results.
Header	r_cg_adc.h
Declaration	void R_ADC_Get_Result (uint16_t *const buffer)
Explanation	Shifts the A/D conversion results 6 bits to the right and stores the results in the area designated by the argument.
Arguments	Address of the area for storing the A/D conversion results
Return value	None
Remarks	None

5.6 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

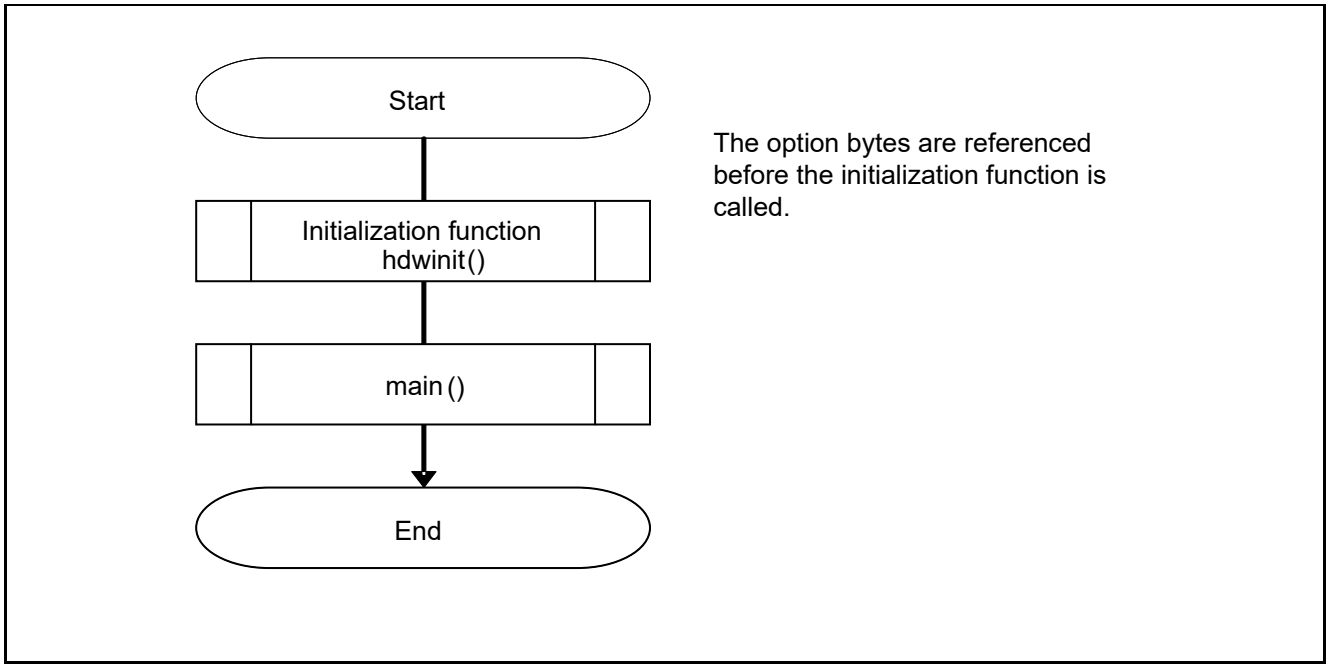

Figure 5.1 Overall Flow

Note: Startup routine is executed before and after the initialization function.

5.6.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

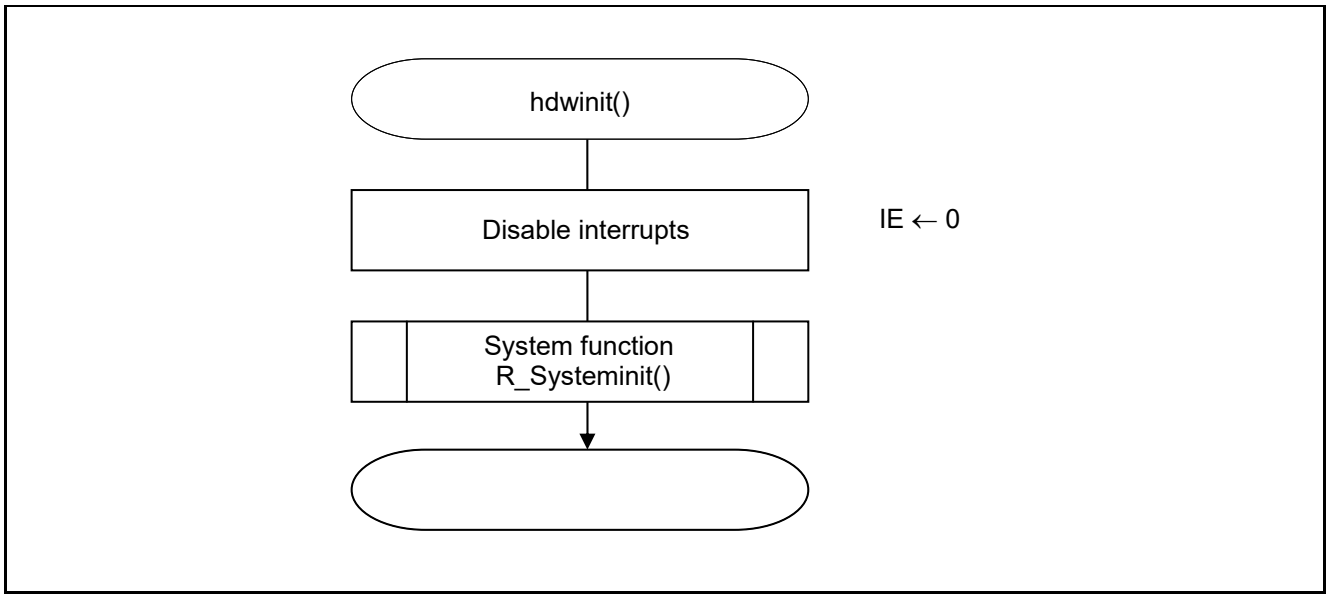

Figure 5.2 Initialization Function

5.6.2 System Function

Figure 5.3 shows the flowchart for the system function.

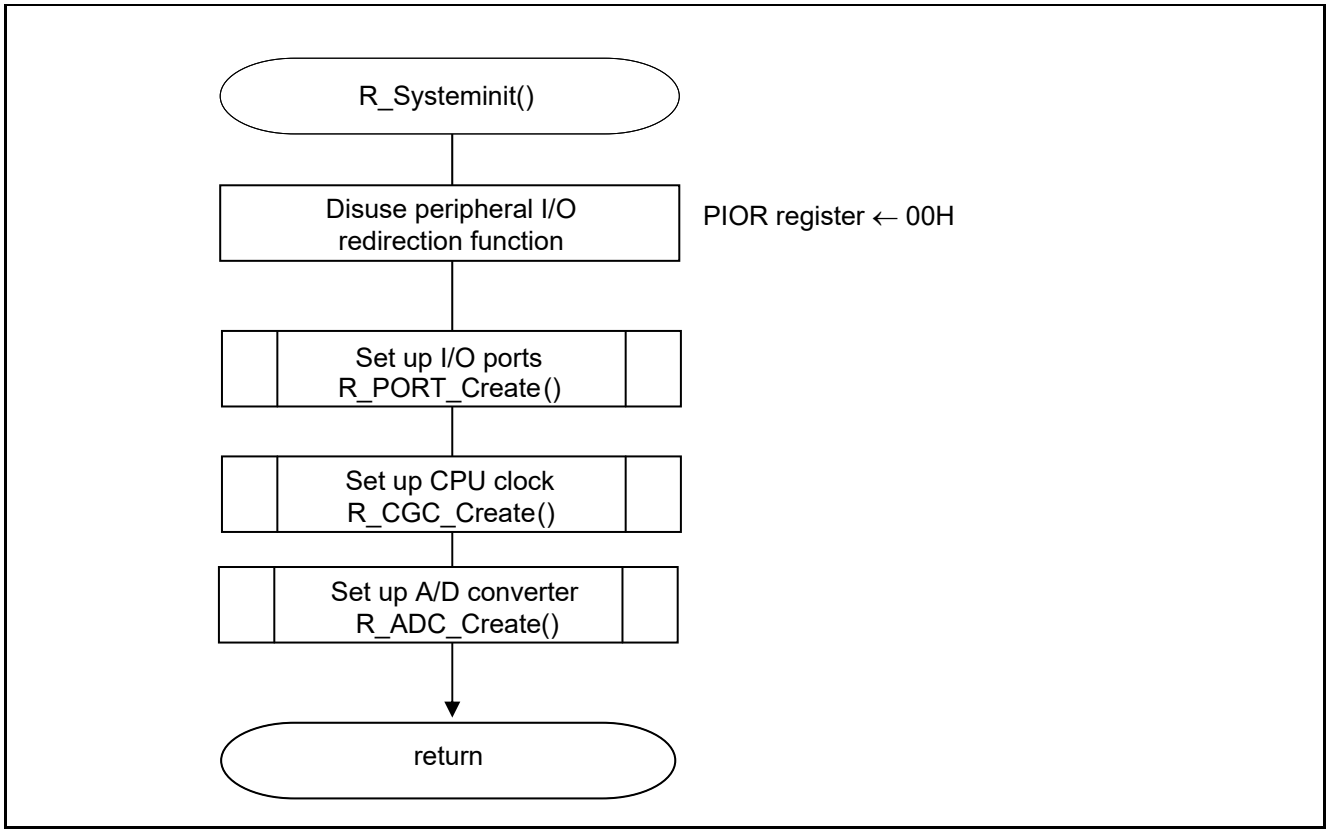

Figure 5.3 System Function

5.6.3 I/O Port Setup

Figure 5.4 shows the flowchart for I/O port setup.

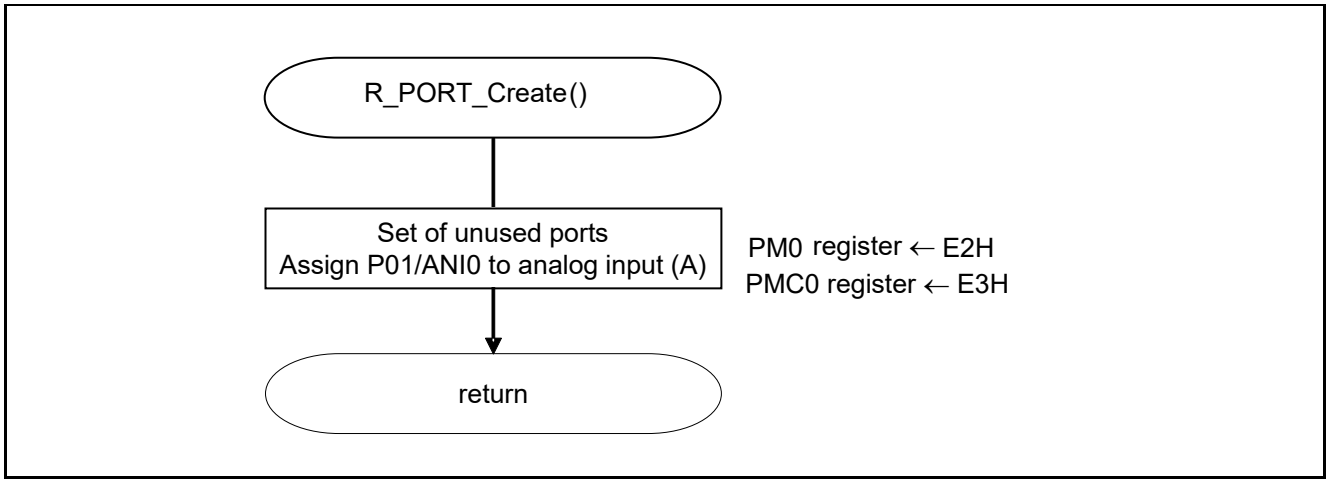

Figure 5.4 I/O Port Setup

Note: Refer to RL78/G10 User's Manual: Hardware (R01UH0384E) for the configuration of the unused ports.

Note: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via separate resistors.

Setting up the channel to be used for A/D conversion

- Port mode control register 0 (PMC0)
- Port mode register 0 (PM0)
  Selects the I/O mode of each port.

Symbol: PMC0

7	6	5	4	3	2	1	0
1	1	1	PMC04	PMC03	PMC02	PMC01	1
1	1	1	x	x	x	**1**	1

Bit 0

PMC01	P01 pin digital I/O/analog input selection
0	Digital I/O (analog function other than analog input)
1	**Analog input**

Symbol: PM0

7	6	5	4	3	2	1	0
1	1	1	PM04	PM03	PM02	PM01	PM00
1	1	1	x	x	x	**1**	x

Bit 0

PM01	P01 I/O Mode Select
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Note: For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

5.6.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

This setup is only for 16-pin products because 10-pin products do not have the resonator connection pins for the main system clock (X1 and X2) and the external clock input pin (EXCLK). Select only the high-speed on-chip oscillator frequency in 10-pin products.

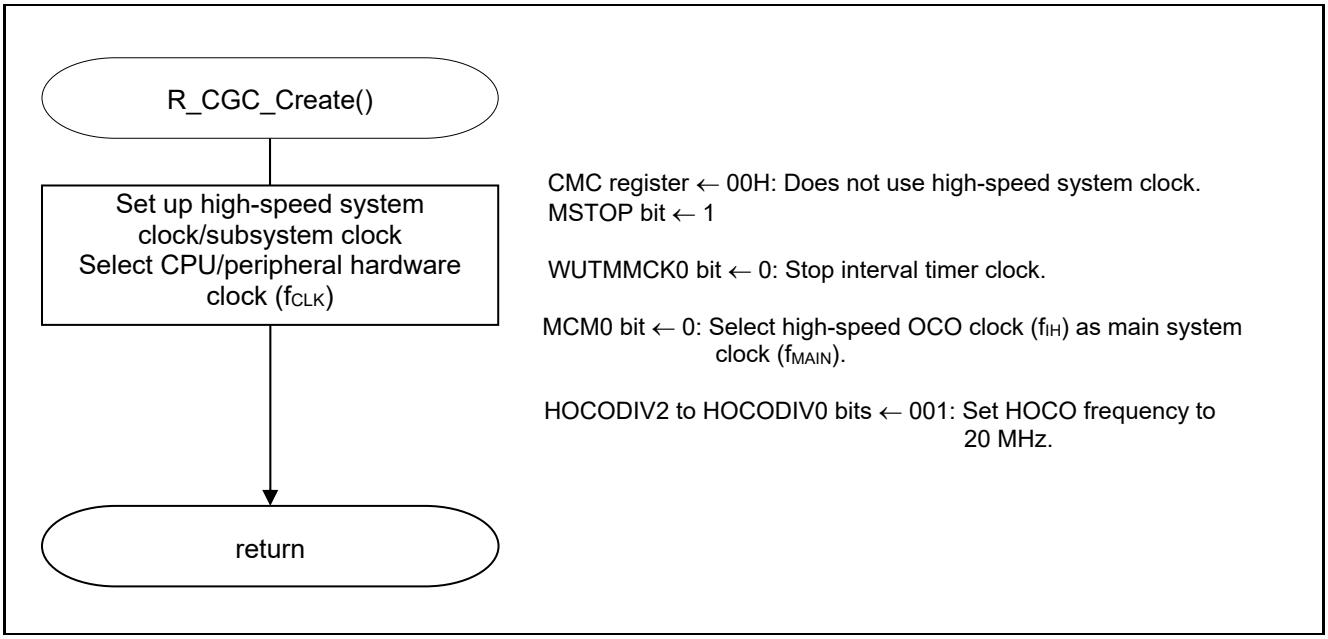

Figure 5.5 CPU Clock Setup

Note: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G10 User's Manual: Hardware (R01UH0384E).

5.6.5 Setting up the A/D Converter

Figure 5.6 shows the flowchart for setting up the A/D converter.

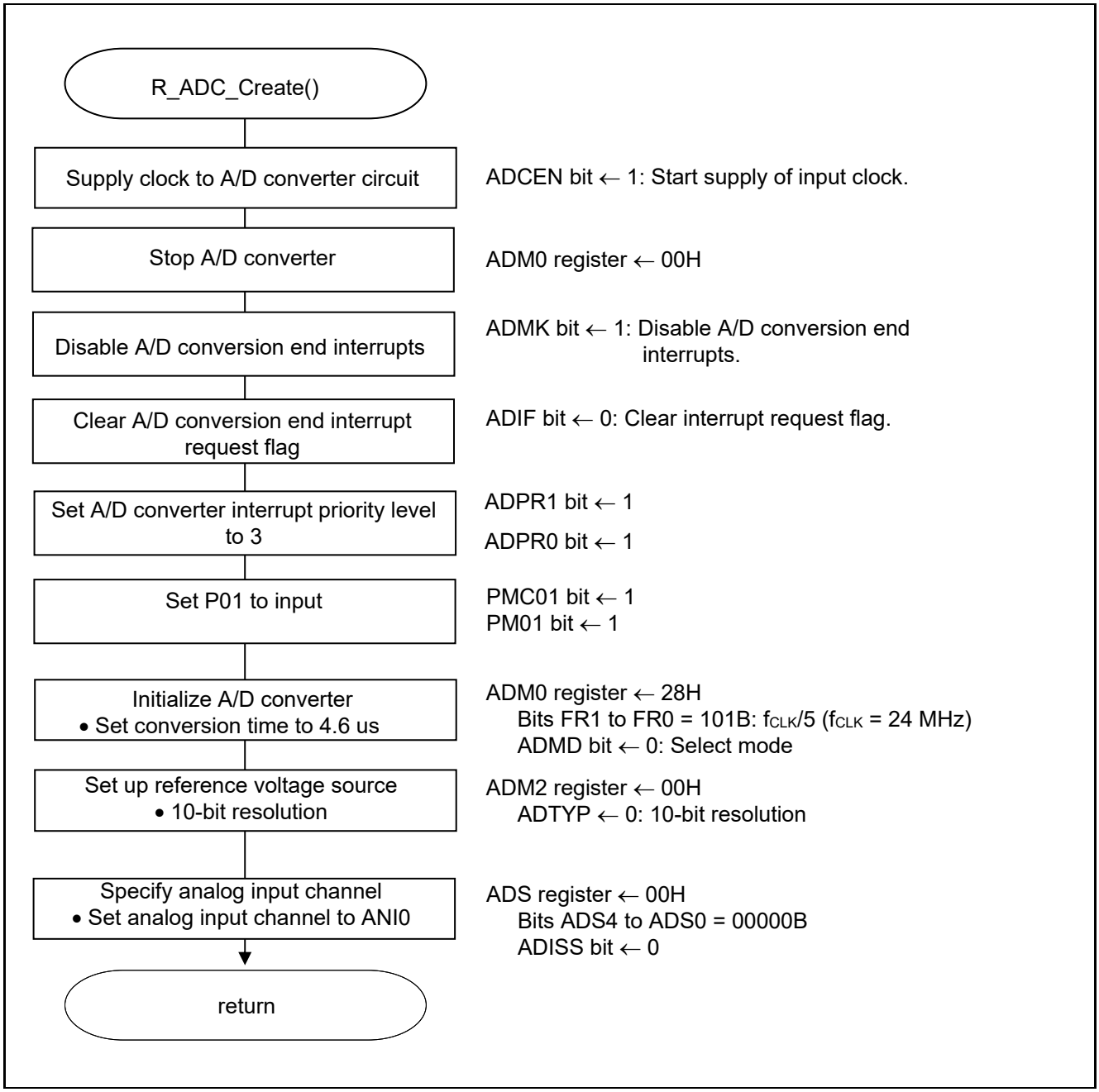

Figure 5.6 A/D Converter Setup Flowchart

Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN	IICA1EN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
x	x	**1**	x	0	x	0	x

Bit 5

ADCEN	A/D converter input clock control
0	Stops supply of input clock.
1	**Starts supply of input clock.**

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	0	0	FR1	FR0	0	LV0	ADCE
x	0	0	**0**	**1**	0	**0**	x

Bit 6

ADMD	A/D channel selection mode select
0	**Select mode**
1	Scan mode

Bits 4, 3, 1

ADM0			Conversion Clock	No. of conv. clock (Sampling clock)	Conversion Time	Conversion Time Selection				
FR1	FR0	LV0				f_{CLK} = 1.25 MHz	f_{CLK} = 2.5 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz
0	0	**0**	$f_{CLK}/8$	**23 f_{AD} (number of Sampling clock: 9 f_{AD})**	$184/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	18.4 µs	9.2 µs
0	**1**		**$f_{CLK}/4$**		**$92/f_{CLK}$**			18.4 µs	9.2 µs	**4.6 µs**
1	0		$f_{CLK}/2$		$46/f_{CLK}$		18.4 µs	9.2 µs	4.6 µs	Setting prohibited
1	1		f_{CLK}		$23/f_{CLK}$	18.4 µs	9.2 µs	4.6 µs	Setting prohibited	
0	0	1	$f_{CLK}/8$	17 f_{AD} (number of Sampling clock: 3 f_{AD})	$136/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	13.6 µs	6.8 µs
0	1		$f_{CLK}/4$		$68/f_{CLK}$			13.6 µs	6.8 µs	3.4 µs
1	0		$f_{CLK}/2$		$34/f_{CLK}$		13.6 µs	6.8 µs	3.4 µs	Setting prohibited
1	1		f_{CLK}		$17/f_{CLK}$	13.6 µs	6.8 µs	3.4 µs	Setting prohibited	

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the reference voltage

- A/D converter mode register 2 (ADM2)
  Sets up the reference voltage source.

Symbol: ADM2

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ADTYP
0	0	0	0	0	0	0	**0**

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up end of A/D conversion interrupts

- Interrupt request flag register (IF0H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK0H)
  Disables interrupts.

Symbol: IF0H

7	6	5	4	3	2	1	0
0	0	0	0	0	KRIF	ADIF	TMIF01
0	0	0	0	0	x	0	x

Bit 1

ADIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRMK	ADMK	TMMK01
1	1	1	1	1	x	**1**	x

Bit 1

ADMK	Interrupt processing control
0	Enables interrupt processing.
1	**Disables interrupt processing.**

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.6.6 Main Processing

Figure 5.7 shows the flowchart for the main processing routine.

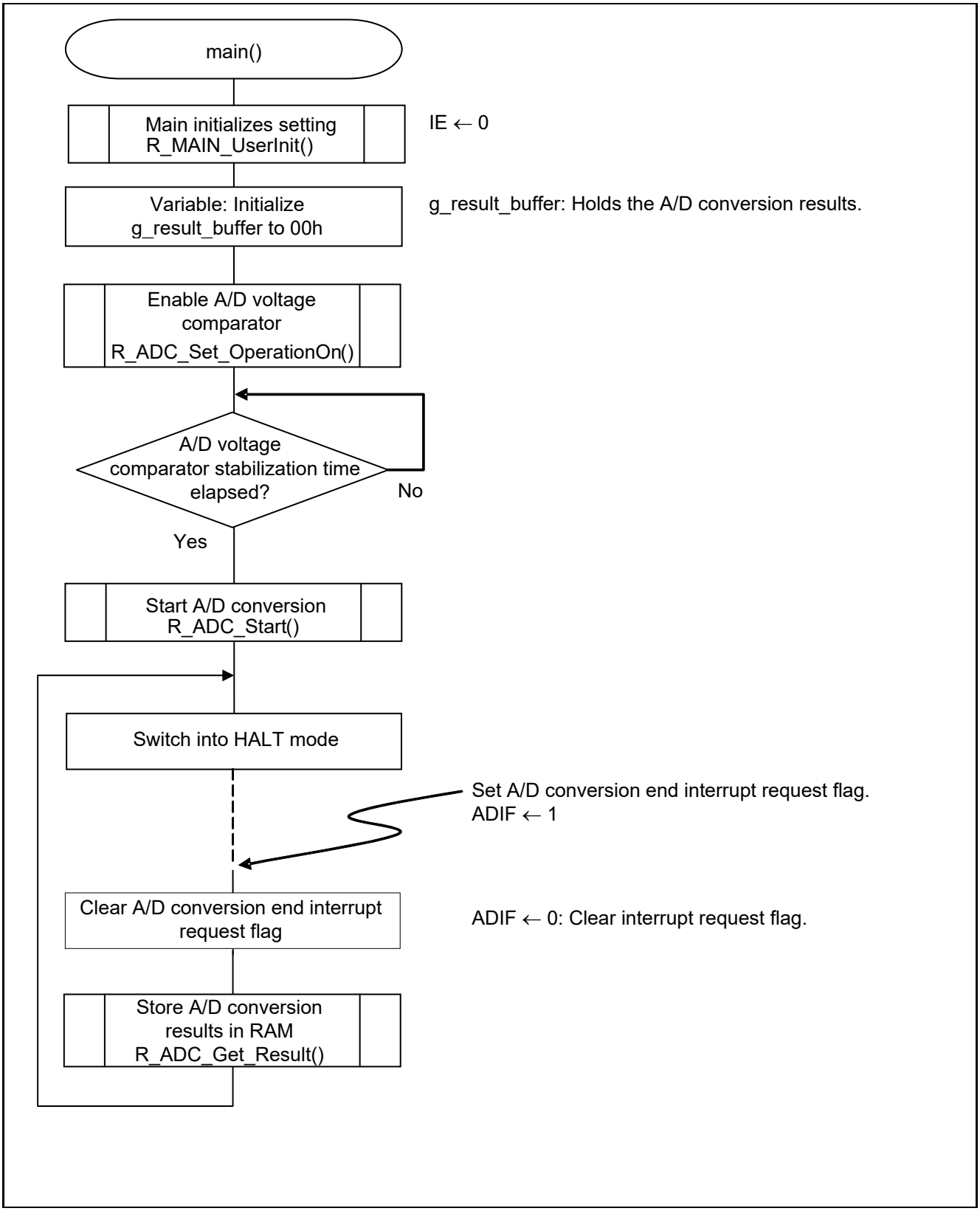

Figure 5.7 Main Processing

5.6.7 Main initializes settings

Figure 5.8 shows the flowchart for the main initializes settings.

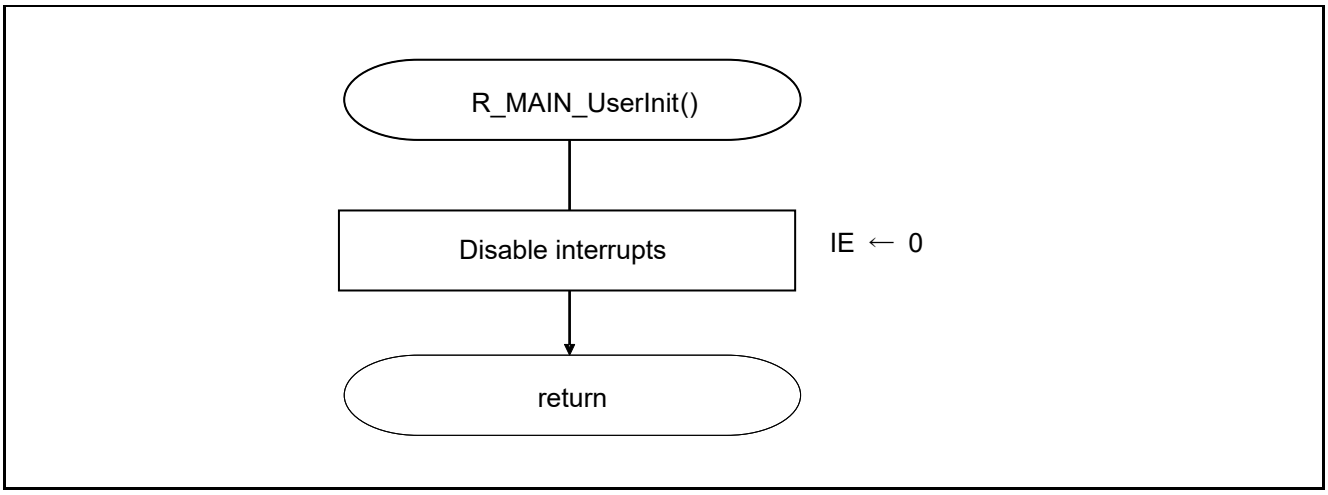

Figure 5.8 Main initializes settings

5.6.8 Enabling the A/D Voltage Comparator

Figure 5.9 shows the flowchart for enabling the A/D voltage comparator.

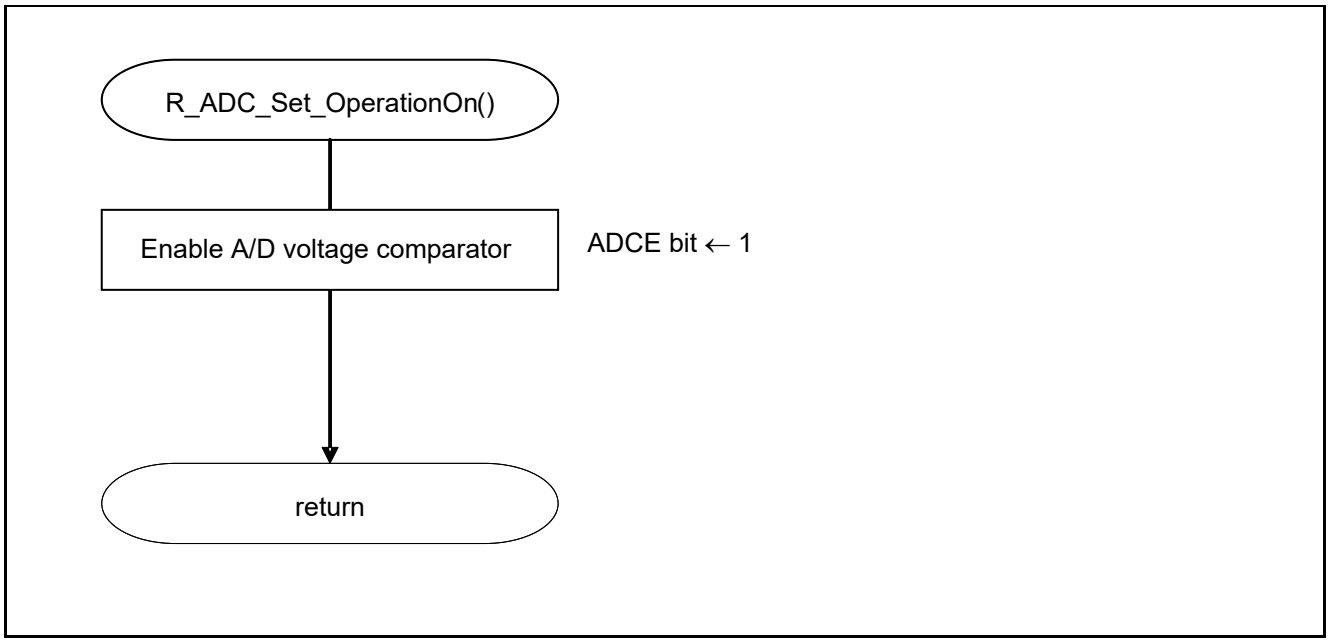

Figure 5.9 Enabling the A/D Voltage Comparator

Starting the A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  Controls the operation of the A/D voltage comparator.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	0	0	FR1	FR0	0	LV0	ADCE
x	0	0	x	x	0	x	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation.
1	**Enables A/D voltage comparator operation.**

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.6.9 Starting A/D Conversion

Figure 5.10 shows the flowchart for starting A/D conversion processing.

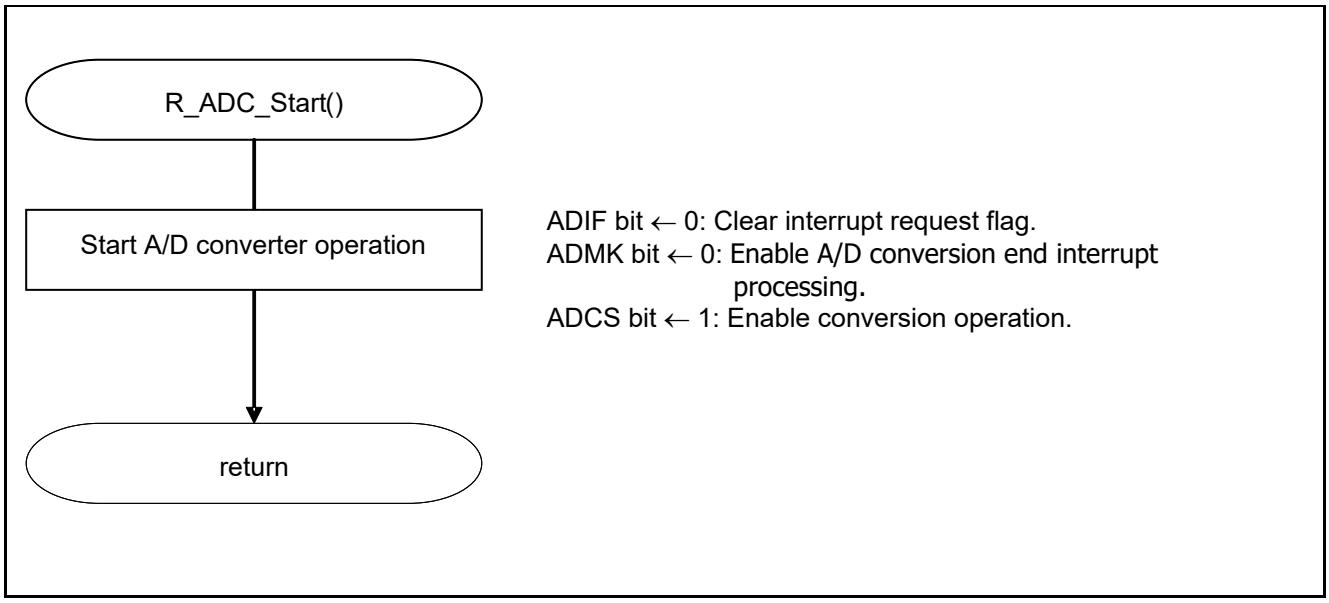

Figure 5.10 Starting A/D Conversion

Starting conversion operation

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	0	0	FR1	FR0	0	LV2	ADCE
1	0	0	x	x	0	x	1

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation.
1	**Enables conversion operation.**

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.6.10 Storing A/D Conversion Results in RAM

Figure 5.11 shows the flowchart for storing the A/D conversion results in RAM.

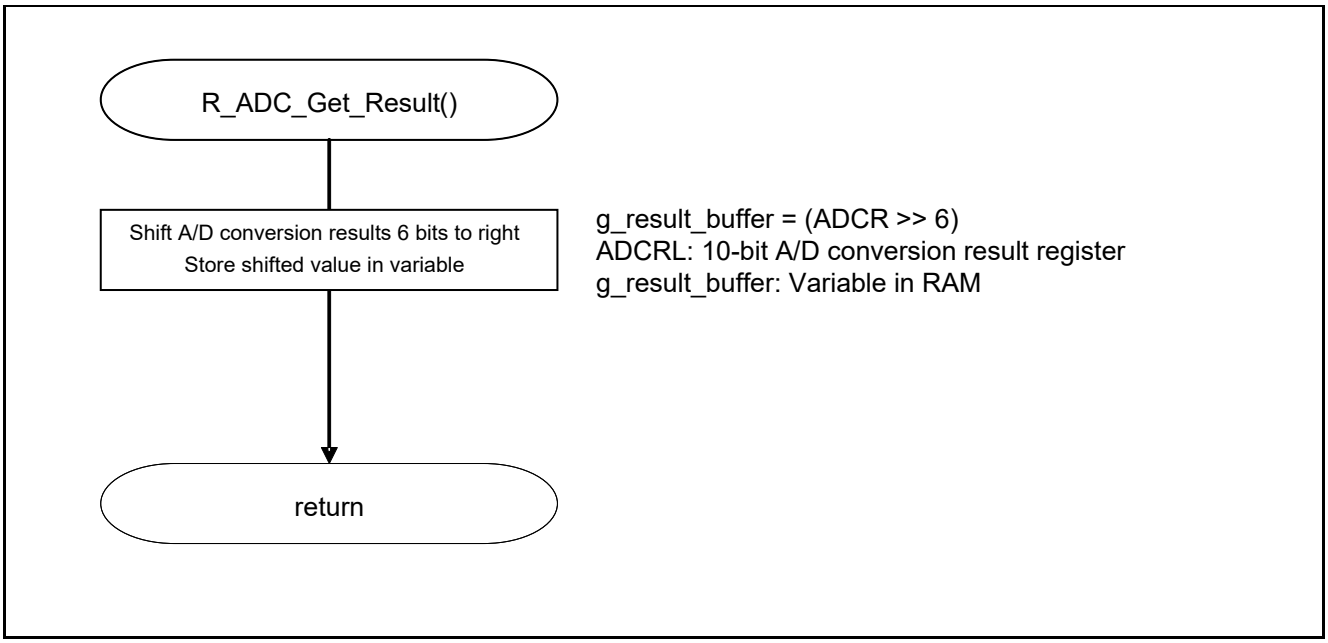

Figure 5.11 Storing the A/D Conversion Results in RAM

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

User's Manual:

RL78/G11 User's Manual: Hardware (R01UH0384E)
RL78 Family User's Manual: Software (R01US0015E)
The latest version can be downloaded from the Renesas Electronics website.

Technical Updates/Technical News

The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics Website

http://www.renesas.com/index.jsp

Inquiries

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Rev.	Date	Description	
		Page	Summary
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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