Introduction

This application note describes the procedures for performing A/D conversion on analog voltages using the RL78/G10's A/D converter (supporting software trigger and sequential conversion modes).

The sample program discussed in this application note performs data conversion on the A/D conversion results and places the converted values in the RL78/G10's internal RAM.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.
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1. Specification

This application note provides examples of using the software trigger and sequential conversion modes of the A/D converter. The A/D converter is placed in select mode and the analog signal input from the P01/ANI0 pin is converted to digital values. Subsequently, the conversion result is subjected to data conversion (shifting the data to the right) and the result is stored in the RL78/G10's internal RAM.

Table 1.1 lists the Peripheral Function to be Used and its Use and Figure 1.1 shows the outline of the conversion operation of the A/D converter.

### Table 1.1 Peripheral Function to be Used and its Use

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D converter</td>
<td>Converts the level of the analog signal input from the P01/ANI0 pin.</td>
</tr>
</tbody>
</table>

![Figure 1.1 Outline of the A/D Converter Conversion Processing](image-url)
2. Operation Check Conditions
The sample code contained in this application note has been checked under the conditions listed in the table below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller used</td>
<td>RL78/G10 (R5F10Y16ASP)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>• High-speed on-chip oscillator (HOCO) clock: 20 MHz</td>
</tr>
<tr>
<td></td>
<td>• CPU/peripheral hardware clock: 20 MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5.0 V (can run on a voltage range of 2.7 V to 5.5 V.)</td>
</tr>
<tr>
<td></td>
<td>SPOR detection voltage</td>
</tr>
<tr>
<td></td>
<td>Falling edge 2.84 V</td>
</tr>
<tr>
<td></td>
<td>Rising edge 2.90 V</td>
</tr>
<tr>
<td>Integrated development environment</td>
<td>CS+ for CC V4.01.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>(CS+)</td>
<td></td>
</tr>
<tr>
<td>C compiler (CS+)</td>
<td>CC-RL V1.03.00 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development environment</td>
<td>e² studio V5.2.0.020 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>(e² studio)</td>
<td></td>
</tr>
<tr>
<td>C compiler (e² studio)</td>
<td>CC-RL V1.03.00 from Renesas Electronics Corp.</td>
</tr>
</tbody>
</table>

3. Related Application Note
The application note that is related to this application note is listed below for reference.

- RL78/G10 Initialization CC-RL (R01AN2668E) Application Note
- RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) CC-RL (R01AN2581E) Application Note
4. Description of the Hardware

4.1 Hardware Configuration Example
Figure 4.1 shows an example of hardware configuration that is used for this application note.

![Figure 4.1 Hardware Configuration](image)

Notes:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-dedicated ports separately to VDD or VSS via a resistor).
2. VDD must be held at not lower than the reset release voltage (VSPOR) that is specified as SPOR.

4.2 List of Pins to be Used
Table 4.1 lists the pins to be used and their function.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P01/ANI0</td>
<td>Input</td>
<td>A/D converter analog input port</td>
</tr>
</tbody>
</table>
5. Description of the Software

5.1 Operation Outline

This sample code performs A/D conversion on the analog voltage that is input to pin ANI0 using the software trigger and sequential conversion modes of the A/D converter. It awaits the end of A/D conversion in HALT mode. After A/D conversion is completed, the sample code shifts the result of A/D conversion 6 bits to the right and places the result in the internal RAM of the RL78/G10.

(1) Initialize the A/D converter.

<Setup conditions>
- Pin P20/ANI0 is used for the analog input.
- A/D conversion channel selection mode is set to select mode.
- A/D conversion operation mode is set to sequential conversion mode.
- A/D conversion is started using the software trigger.
- The A/D conversion end interrupt (INTAD) is used.

(2) The sample program sets the ADCS bit of the ADM0 register to 1 (A/D conversion start) to start A/D conversion and executes the HALT instruction to place the chip in the HALT mode and wait for an A/D conversion end interrupt.

(3) After completing the A/D conversion of the voltage input from pin ANI0, the A/D converter transfers the result of A/D conversion to the ADCR register and generates an A/D conversion end interrupt.

(4) On release from the HALT mode in response to the A/D conversion end interrupt, the sample program reads the result of A/D conversion from the ADCRL register, shifts the result 6 bits to the right, and stores the shifted data in the internal RAM of the RL78/G10.

(5) The chip returns to the HALT mode and waits for an A/D conversion end interrupt.
5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1   Option Byte Settings

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000C0H</td>
<td>11101110B</td>
<td>Stops the watchdog timer operation. (Stops counting after the release of the reset state.)</td>
</tr>
<tr>
<td>000C1H</td>
<td>11110111B</td>
<td>SPOR detection voltage</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling edge 2.84 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rising edge 2.90 V</td>
</tr>
<tr>
<td>000C2H</td>
<td>11111001B</td>
<td>HOCO: 20 MHz</td>
</tr>
<tr>
<td>000C3H</td>
<td>10000101B</td>
<td>Enables the on-chip debugging function.</td>
</tr>
</tbody>
</table>

5.3 List of Variables

Table 5.2 lists the global variable that is used by this sample program.

Table 5.2   Global Variable

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned short</td>
<td>g_result_buffer</td>
<td>Area for storing the A/D conversion results</td>
<td>main ()</td>
</tr>
</tbody>
</table>
5.4 List of Functions

Table 5.3 lists the functions that are used by this sample program.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_ADC_Set_OperationOn</td>
<td>Enables the A/D voltage comparator.</td>
</tr>
<tr>
<td>R_ADC_Start</td>
<td>Starts A/D conversion.</td>
</tr>
<tr>
<td>R_ADC_Get_Result</td>
<td>Gets A/D conversion results.</td>
</tr>
</tbody>
</table>

5.5 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_ADC_Set_OperationOn

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Enable A/D voltage comparator.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>r_cg_adc.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_ADC_Set_OperationOn (void)</td>
</tr>
<tr>
<td>Explanation</td>
<td>Enables the A/D voltage comparator for operation.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return value</td>
<td>None</td>
</tr>
<tr>
<td>Remarks</td>
<td>None</td>
</tr>
</tbody>
</table>

[Function Name] R_ADC_Start

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Start A/D conversion.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>r_cg_adc.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_ADC_Start (void)</td>
</tr>
<tr>
<td>Explanation</td>
<td>Enables A/D conversion end interrupts and starts A/D conversion processing.</td>
</tr>
<tr>
<td>Arguments</td>
<td>None</td>
</tr>
<tr>
<td>Return value</td>
<td>None</td>
</tr>
<tr>
<td>Remarks</td>
<td>None</td>
</tr>
</tbody>
</table>

[Function Name] R_ADC_Get_Result

<table>
<thead>
<tr>
<th>Synopsis</th>
<th>Get A/D conversion results.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>r_cg_adc.h</td>
</tr>
<tr>
<td>Declaration</td>
<td>void R_ADC_Get_Result (uint16_t *const buffer)</td>
</tr>
<tr>
<td>Explanation</td>
<td>Shifts the A/D conversion results 6 bits to the right and stores the results in the area designated by the argument.</td>
</tr>
<tr>
<td>Arguments</td>
<td>Address of the area for storing the A/D conversion results</td>
</tr>
<tr>
<td>Return value</td>
<td>None</td>
</tr>
<tr>
<td>Remarks</td>
<td>None</td>
</tr>
</tbody>
</table>
5.6 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

![Flowchart of Overall Flow](image)

**Figure 5.1  Overall Flow**

Note: Startup routine is executed before and after the initialization function.

5.6.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

![Flowchart of Initialization Function](image)

**Figure 5.2  Initialization Function**
5.6.2 System Function

Figure 5.3 shows the flowchart for the system function.

![Flowchart of System Function](image)

- R_Systeminit()
- Disuse peripheral I/O redirection function
  - PIOR register ← 00H
- Set up I/O ports
  - R_PORT_Create()
- Set up CPU clock
  - R_CGC_Create()
- Set up A/D converter
  - R_ADC_Create()
- return

Figure 5.3 System Function
5.6.3 I/O Port Setup

Figure 5.4 shows the flowchart for I/O port setup.

Note: Refer to RL78/G10 User’s Manual: Hardware (R01UH0384E) for the configuration of the unused ports.

Note: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to $V_{DD}$ or $V_{SS}$ via separate resistors.
Setting up the channel to be used for A/D conversion

- Port mode control register 0 (PMC0)
- Port mode register 0 (PM0)

Selects the I/O mode of each port.

Symbol: PMC0

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PMC04</td>
<td>PMC03</td>
<td>PMC02</td>
<td>PMC01</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>PMC01</th>
<th>P01 pin digital I/O/analog input selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Digital I/O (analog function other than analog input)</td>
</tr>
<tr>
<td>1</td>
<td>Analog input</td>
</tr>
</tbody>
</table>

Symbol: PM0

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PM04</td>
<td>PM03</td>
<td>PM02</td>
<td>PM01</td>
<td>PM00</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>PM01</th>
<th>P01 I/O Mode Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Output mode (output buffer on)</td>
</tr>
<tr>
<td>1</td>
<td>Input mode (output buffer off)</td>
</tr>
</tbody>
</table>

Note: For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.
5.6.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

This setup is only for 16-pin products because 10-pin products do not have the resonator connection pins for the main system clock (X1 and X2) and the external clock input pin (EXCLK). Select only the high-speed on-chip oscillator frequency in 10-pin products.

![Flowchart of CPU Clock Setup](image)

- **R_CGC_Create()**
  - Set up high-speed system clock/subsystem clock
  - Select CPU/peripheral hardware clock (fCLK)

  - CMC register ← 00H: Does not use high-speed system clock.
  - MSTOP bit ← 1
  - WUTMMCK0 bit ← 0: Stop interval timer clock.
  - MCM0 bit ← 0: Select high-speed OCO clock (fIH) as main system clock (fMAIN).
  - HOCODIV2 to HOCODIV0 bits ← 001: Set HOCO frequency to 20 MHz.

**Figure 5.5 CPU Clock Setup**

Note: For details on the procedure for setting up the CPU clock (R_CGC_Create()), refer to the section entitled "Flowcharts" in RL78/G10 User’s Manual: Hardware (R01UH0384E).
5.6.5 Setting up the A/D Converter

Figure 5.6 shows the flowchart for setting up the A/D converter.

```
R_ADC_Create()
```

Supply clock to A/D converter circuit

```
ADCEN bit ← 1: Start supply of input clock.
```

Stop A/D converter

```
ADM0 register ← 00H
```

Disable A/D conversion end interrupts

```
ADMK bit ← 1: Disable A/D conversion end interrupts.
```

Clear A/D conversion end interrupt request flag

```
ADIF bit ← 0: Clear interrupt request flag.
```

Set A/D converter interrupt priority level to 3

```
ADPR1 bit ← 1
ADPR0 bit ← 1
```

Set P01 to input

```
PMC01 bit ← 1
PM01 bit ← 1
```

Initialize A/D converter

```
• Set conversion time to 4.6 us
```

Set up reference voltage source

```
• 10-bit resolution
```

Specify analog input channel

```
• Set analog input channel to ANI0
```

```
return
```

azen

```
R_ADC_Create()
```

```
MOD bit ← 1: Start A/D converter
```

```
ADM register ← 28H
```

```
Bits FR1 to FR0 = 101B: fCLK/5 (fCLK = 24 MHz)
```

```
ADMD bit ← 0: Select mode
```

```
ADM2 register ← 00H
```

```
ADTYP ← 0: 10-bit resolution
```

```
ADS register ← 00H
```

```
Bits ADS4 to ADS0 = 00000B
```

```
ADISS bit ← 0
```

Figure 5.6 A/D Converter Setup Flowchart
Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMKAEN</td>
<td>IICA1EN</td>
<td>ADCEN</td>
<td>IICA0EN</td>
<td>0</td>
<td>SAU0EN</td>
<td>0</td>
<td>TAU0EN</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>1</td>
<td>x</td>
<td>0</td>
<td>x</td>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 5

<table>
<thead>
<tr>
<th>ADCEN</th>
<th>A/D converter input clock control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Stops supply of input clock.</td>
</tr>
<tr>
<td>1</td>
<td>Starts supply of input clock.</td>
</tr>
</tbody>
</table>

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.
Setting up the A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)

  Controls the A/D conversion operation.
  Specifies the A/D conversion channel selection mode.

Symbol: ADM0

<table>
<thead>
<tr>
<th>Bit 6</th>
<th>A/D channel selection mode select</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Select mode</td>
</tr>
<tr>
<td>1</td>
<td>Scan mode</td>
</tr>
</tbody>
</table>

### Bits 4, 3, 1

<table>
<thead>
<tr>
<th>ADM0</th>
<th>Conversion Clock</th>
<th>No. of conv. clock (Sampling clock)</th>
<th>Conversion Time Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>f&lt;sub&gt;CLK&lt;/sub&gt; = 1.25 MHz</td>
</tr>
<tr>
<td>FR1</td>
<td>FR0</td>
<td>LV0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>23&lt;sub&gt;f&lt;sub&gt;AD&lt;/sub&gt;&lt;/sub&gt;</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
<td>92&lt;sub&gt;f&lt;sub&gt;CLK&lt;/sub&gt;&lt;/sub&gt;</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
<td>46&lt;sub&gt;f&lt;sub&gt;CLK&lt;/sub&gt;&lt;/sub&gt;</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td>23&lt;sub&gt;f&lt;sub&gt;CLK&lt;/sub&gt;&lt;/sub&gt;</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>17&lt;sub&gt;f&lt;sub&gt;AD&lt;/sub&gt;&lt;/sub&gt;</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
<td>68&lt;sub&gt;f&lt;sub&gt;CLK&lt;/sub&gt;&lt;/sub&gt;</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
<td>34&lt;sub&gt;f&lt;sub&gt;CLK&lt;/sub&gt;&lt;/sub&gt;</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td>17&lt;sub&gt;f&lt;sub&gt;CLK&lt;/sub&gt;&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.
Setting up the reference voltage

- **A/D converter mode register 2 (ADM2)**
  Sets up the reference voltage source.

Symbol: ADM2

<table>
<thead>
<tr>
<th>Bit</th>
<th>ADTYP Selection of the A/D conversion resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10-bit resolution</td>
</tr>
<tr>
<td>1</td>
<td>8-bit resolution</td>
</tr>
</tbody>
</table>

Bit 0

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.
Setting up end of A/D conversion interrupts

- Interrupt request flag register (IF0H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK0H)
  Disables interrupts.

Symbol: IF0H

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>KRIF</td>
<td>ADIF</td>
<td>TMIF01</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 1

<table>
<thead>
<tr>
<th>ADIF</th>
<th>Interrupt request flag</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt request signal is generated.</td>
</tr>
<tr>
<td>1</td>
<td>Interrupt request is generated, interrupt request status</td>
</tr>
</tbody>
</table>

Symbol: MK0H

<table>
<thead>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>KRMK</td>
<td>ADMK</td>
<td>TMMK01</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>x</td>
<td>1</td>
<td>x</td>
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Bit 1

<table>
<thead>
<tr>
<th>ADMK</th>
<th>Interrupt processing control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Enables interrupt processing.</td>
</tr>
<tr>
<td>1</td>
<td>Disables interrupt processing.</td>
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</table>

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.
5.6.6 Main Processing

Figure 5.7 shows the flowchart for the main processing routine.

```
main()

Main initializes setting
R_MAIN_UserInit()

IE ← 0

Variable: Initialize
g_result_buffer to 00h

Enable A/D voltage
comparator
R_ADC_Set_OperationOn()

A/D voltage
comparator stabilization time
elapsed?

No

Yes

Start A/D conversion
R_ADC_Start()

Switch into HALT mode

Set A/D conversion end interrupt request flag.
ADIF ← 1

Clear A/D conversion end interrupt
request flag

ADIF ← 0: Clear interrupt request flag.

Store A/D conversion
results in RAM
R_ADC_Get_Result()
```

Figure 5.7 Main Processing
5.6.7 Main initializes settings

Figure 5.8 shows the flowchart for the main initializes settings.

### Figure 5.8 Main initializes settings

```plaintext
R_MAIN_UserInit()

Disable interrupts

IE ← 0

return
```
5.6.8 Enabling the A/D Voltage Comparator

Figure 5.9 shows the flowchart for enabling the A/D voltage comparator.

```
R_ADC_Set_OperationOn()
```

Enable A/D voltage comparator

```
ADCE bit ← 1
```

return

![Figure 5.9 Enabling the A/D Voltage Comparator](image)

Starting the A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  - Controls the operation of the A/D voltage comparator.

Symbol: ADM0

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<tr>
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<td>ADCS</td>
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<td>0</td>
<td></td>
<td>FR1</td>
<td>FR0</td>
<td>0</td>
<td>LV0</td>
<td>ADCE</td>
</tr>
<tr>
<td>x</td>
<td></td>
<td>0</td>
<td></td>
<td>x</td>
<td></td>
<td>x</td>
<td>0</td>
<td>x</td>
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</tbody>
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Bit 0

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<tr>
<th>ADCE</th>
<th>A/D voltage comparator operation control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Stops A/D voltage comparator operation.</td>
</tr>
<tr>
<td>1</td>
<td>Enables A/D voltage comparator operation.</td>
</tr>
</tbody>
</table>

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.
5.6.9 Starting A/D Conversion

Figure 5.10 shows the flowchart for starting A/D conversion processing.

![Flowchart](image)

**Figure 5.10 Starting A/D Conversion**

Starting conversion operation

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.

Symbol: ADM0

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<thead>
<tr>
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<tbody>
<tr>
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<td>0</td>
<td>FR1</td>
<td>FR0</td>
<td>0</td>
<td>LV2</td>
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<td>x</td>
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Bit 7

<table>
<thead>
<tr>
<th>ADCS</th>
<th>A/D conversion operation control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Stops conversion operation.</td>
</tr>
<tr>
<td>1</td>
<td>Enables conversion operation.</td>
</tr>
</tbody>
</table>

Note: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.
5.6.10 Storing A/D Conversion Results in RAM

Figure 5.11 shows the flowchart for storing the A/D conversion results in RAM.

```
R_ADC_Get_Result()

Shift A/D conversion results 6 bits to right
Store shifted value in variable

g_result_buffer = (ADCR >> 6)
ADCRL: 10-bit A/D conversion result register
g_result_buffer: Variable in RAM

return
```

Figure 5.11 Storing the A/D Conversion Results in RAM
6. **Sample Code**

The sample code is available on the Renesas Electronics Website.

7. **Documents for Reference**

User’s Manual:
- RL78/G11 User's Manual: Hardware (R01UH0384E)
  The latest version can be downloaded from the Renesas Electronics website.

Technical Updates/Technical News
  The latest information can be downloaded from the Renesas Electronics website.

**Website and Support**

Renesas Electronics Website
  [http://www.renesas.com/index.jsp](http://www.renesas.com/index.jsp)

Inquiries
  [http://www.renesas.com/contact/](http://www.renesas.com/contact/)
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<td>May 12, 2017</td>
<td>—</td>
<td>First edition issued</td>
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   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
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   When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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