Introduction

This application note describes the procedures for performing A/D conversion on analog voltages using the RL78/G10's A/D converter.

The sample program discussed in this application note performs data conversion on the A/D conversion results (shifting the data right by six bits) and places the converted values in the internal RAM of the RL78/G10.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.
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1. Specification

This application note provides examples of using the software trigger and sequential conversion modes of the A/D converter. The analog signal input from the P01/ANI0 pin is converted to digital values. Subsequently, the conversion result is subjected to data conversion (shifting the data right by six bits) and the result is stored in the RL78/G10's internal RAM.

Table 1.1 lists the peripheral function to be used and its uses. Figure 1.1 shows the outline of the conversion operation of the A/D converter.

Table 1.1  Peripheral Function to be Used and its Use

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D converter</td>
<td>Converts the level of the analog signal input from the P01/ANI0 pin.</td>
</tr>
</tbody>
</table>

![Figure 1.1  Outline of the A/D Converter Conversion Processing](image-url)
2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller used</td>
<td>RL78/G10 (R5F10Y16ASP)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>• High-speed on-chip oscillator (HOCO) clock: 20 MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>• CPU/peripheral hardware clock: 20 MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5.0 V (can run at a voltage range of 2.9 V to 5.5 V.)</td>
</tr>
<tr>
<td>SPOR detection voltage</td>
<td>When reset occurs: $V_{DD} &lt; 2.82$ V</td>
</tr>
<tr>
<td></td>
<td>When reset is released: $V_{DD} \geq 2.88$ V</td>
</tr>
<tr>
<td>Integrated development environment (CubeSuite+)</td>
<td>CubeSuite + E1.03.00k01_RL78_G10 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Assembler (CubeSuite+)</td>
<td>RA78K0R V1.70 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development environment (e2studio)</td>
<td>e2studio V2.0.0.16 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Assembler (e2studio)</td>
<td>KPIT GNURL78-ELF Toolchain V13.02 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Board to be used</td>
<td>RL78/G10 target board (QB-R5F10Y16-TB)</td>
</tr>
</tbody>
</table>

3. Related Application Notes

The application notes that are related to this application note are listed below for reference.

RL78/G10 Initialization (R01AN1454E) Application Note
4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

![Figure 4.1 Hardware Configuration](image)

Cautions
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical characteristics conditions are met (connect the input-dedicated ports separately to V_DD or V_SS via a resistor).
2. V_DD must be held at not lower than the reset release voltage (V_SPOR) that is specified as SPOR.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their function.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P01/ANI0</td>
<td>Input</td>
<td>A/D converter analog input port</td>
</tr>
</tbody>
</table>

Table 4.1 Pins to be Used and their Function
5. Description of the Software

5.1 Operation Outline
This sample code performs A/D conversion on the analog voltage that is input to pin ANI0 using the A/D converter. It awaits the end of A/D conversion in HALT mode. After A/D conversion is completed, the sample code shifts the result of A/D conversion right by six bits and places the result in the internal RAM of the RL78/G10.

(1) Initialize the A/D converter.
<Setup conditions>
- Pin P01/ANI0 is used for the analog input.
- Ten-bit resolution is used for the A/D conversion resolution.

(2) The sample program sets the ADCS bit of the ADM0 register to 1 (A/D conversion start) to start A/D conversion, executes the HALT instruction, places the chip in the HALT mode, and waits for an A/D conversion end interrupt.

(3) After completing the A/D conversion of the voltage input from pin ANI0, the A/D converter transfers the result of A/D conversion to the ADCRH and ADCRL registers and generates an A/D conversion end interrupt.

(4) On release from the HALT mode in response to the A/D conversion end interrupt, the sample program reads the result of A/D conversion from the ADCRH and ADCRL registers, shifts the result right by six bits, and stores the shifted data in the internal RAM of the RL78/G10.

(5) The sample program sets the ADCS bit of the ADM0 register to 1 (A/D conversion start) to start A/D conversion, places the chip in the HALT mode again, and waits for an A/D conversion end interrupt.
5.2 List of Option Byte Settings
Table 5.1 summarizes the settings of the option bytes.

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000C0H</td>
<td>11101110B</td>
<td>Stops the watchdog timer operation. (Stops counting after the release of the reset state.)</td>
</tr>
</tbody>
</table>
| 000C1H  | 11110111B | SPOR detection voltage
  When reset occurs: VDD < 2.82 V
  When reset is released: VDD ≥ 2.88 V |
| 000C2H  | 1111001B  | HOCO: 20 MHz                                                                |
| 000C3H  | 10000101B | Enables the on-chip debugging function.                                     |

5.3 List of Variables
Table 5.2 lists the variable that is used by this sample program.

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-bit variable</td>
<td>RADCBUF</td>
<td>Area for storing the A/D conversion results</td>
<td>main</td>
</tr>
</tbody>
</table>
5.4 List of Functions (Subroutines)

Table 5.3 lists the functions (subroutines) that are used by this sample program.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINIADC</td>
<td>Initializes A/D converter</td>
</tr>
<tr>
<td>SSTARTAD</td>
<td>Starts A/D conversion</td>
</tr>
</tbody>
</table>

5.5 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] RESET_START

Synopsis: Initializes the CPU at reset start.
Explanation: Calls the main function after setting the stack pointer and initializing the hardware.
Arguments: None
Return value: None
Remarks: None

[Function Name] SINIADC

Synopsis: Initializes the A/D converter.
Explanation: Sets the conversion time, resolution (10-bit conversion), and analog input channels of the A/D converter.
Arguments: None
Return value: None
Remarks: None

[Function Name] SSTARTAD

Synopsis: Starts A/D conversion.
Explanation: Enables A/D conversion end interrupts and starts A/D conversion processing.
Arguments: None
Return value: None
Remarks: None
5.6 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

![Flowchart](image)

Figure 5.1 Overall Flow

The option bytes are referenced before the CPU initialization function is called.
5.6.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

![Flowchart for CPU Initialization Function]

- **RESET_START**
- Set up ES register
  - \( \text{ES} \leftarrow 00 \text{H} \) (for table reference)
- Set up stack pointer
- Set up redirection
- Set up clock generation circuit \( \text{SINICLK} \)
- Set up I/O ports \( \text{SINIPORT} \)
  - \( \text{PIOR} \leftarrow 00000000\text{B} \)
  - \( \text{PM0} \leftarrow 11100010\text{B} \) (10-pin products)
    - \( 10000010\text{B} \) (16-pin products)
  - \( \text{PMCO} \leftarrow 11100011\text{B} \) (10-pin products)
    - \( 11000010\text{B} \) (16-pin products)
  - Select HOCO (20 MHz) as an operation clock.
- Set up A/D converter \( \text{SINIADC} \)
  - \( \text{ADM0} \leftarrow 00000000\text{B} \)
    - Mask A/D conversion end interrupts.
- Call main routine \( \text{main} \)
- **HALT**
5.6.2 I/O Port Setup Function

Figure 5.3 shows the flowchart for the I/O port setup function.

![Flowchart for I/O Port Setup Function](image)

**Note**  
Refer to the section entitled "Flowcharts" in RL78/G10 Initialization Application Note (R01AN1454E) for the configuration of the unused ports.

**Caution**  
Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to $V_{DD}$ or $V_{SS}$ via separate resistors.
5.6.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for clock generation circuit setup. Because 10-pin products do not have the resonator connection pins for the main system clock (X1 and X2) and the external clock input pin (EXCLK), only the high-speed on-chip oscillator frequency should be set in 10-pin products.

![Flowchart for clock generation circuit setup](image)

- **SINICLK**
- **Set up high-speed system clock Note**: CMC register ← 00000000B: Do not use high-speed system clock. MSTOP bit ← 1
- **Set up operation speed mode control register Note**: WUTMMCK0 bit ← 0: Stop interval timer clock.
- **Select CPU/peripheral hardware clock (fCLK) Note**: MCM0 bit ← 0: Select HOCO clock (fHOCO) as main system clock (fMAIN).
- **Select frequency of high-speed on-chip oscillator**: HOCODIV2 to HOCODIV0 bits ← 001: Set HOCO frequency to 20 MHz.

**Figure 5.4 Clock Generation Circuit Setup**

Note 16-pin products only.

Caution For details on the procedure for setting up the clock generation circuit (SINICLK), refer to the section entitled "Flowcharts" in RL78/G10 Initialization Application Note (R01AN1454E).
5.6.4 A/D Converter Setup

Figure 5.5 shows the flowchart for setting up the A/D converter.

1. Supply clock to A/D converter
   - ADCEN bit ← 1: Start supply of input clock.

2. Initialize A/D converter
   - Set conversion time to about 4.6 µs
   - ADM0 register ← 08H
   - Bits FR1 and FR0 = 01B: \( f_{CLK}/4 \) (\( f_{CLK} = 20 \text{ MHz} \))

3. Set resolution
   - 10-bit resolution
   - ADM2 register ← 00H
   - ADTYPE ← 0: 10-bit resolution

4. Specify analog input channel
   - Set analog input channel to ANI0
   - ADS register ← 00H

5. Clear A/D conversion end interrupt request flag
   - ADIF bit ← 0: Clear interrupt request flag.

6. Disable A/D conversion end interrupts
   - ADMK bit ← 1: Disable A/D conversion end interrupts.

Figure 5.5 A/D Converter Setup
Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMKAEN</td>
<td>Note</td>
<td>0</td>
<td>ADCEN</td>
<td>Note</td>
<td>0</td>
<td>SAU0EN</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: 16-pin products only.

Caution: For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.
Setting up the A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D conversion channel selection mode.

Symbol: ADM0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCS</td>
<td>0</td>
<td>0</td>
<td>FR1</td>
<td>FR0</td>
<td>0</td>
<td>LV0</td>
<td>Note 1</td>
</tr>
<tr>
<td>x</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Bits 4, 3, and 1

(1) $2.4 \, \text{V} \leq V_{DD} \leq 5.5 \, \text{V}$

<table>
<thead>
<tr>
<th>ADM0</th>
<th>Conversion Clock</th>
<th>Number of Conversion Clock</th>
<th>Conversion Time</th>
<th>Conversion Time Selection [µs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR1</td>
<td>FR0</td>
<td>LV0</td>
<td>fCLK/8</td>
<td>19 fAD (Number of sampling clock: 7 fAD)</td>
</tr>
<tr>
<td>0 0 0</td>
<td>fCLK/4</td>
<td>$92/fCLK$</td>
<td>18.4</td>
<td>9.2</td>
</tr>
<tr>
<td>1 0</td>
<td>fCLK/2</td>
<td>$46/fCLK$</td>
<td>18.4</td>
<td>9.2</td>
</tr>
<tr>
<td>1 1</td>
<td>fCLK</td>
<td>$23/fCLK$</td>
<td>18.4</td>
<td>9.2</td>
</tr>
</tbody>
</table>

(2) $2.7 \, \text{V} \leq V_{DD} \leq 5.5 \, \text{V}$

<table>
<thead>
<tr>
<th>ADM0</th>
<th>Conversion Clock</th>
<th>Number of Conversion Clock</th>
<th>Conversion Time</th>
<th>Conversion Time Selection [µs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR1</td>
<td>FR0</td>
<td>LV0</td>
<td>fCLK/8</td>
<td>19 fAD (Number of sampling clock: 7 fAD)</td>
</tr>
<tr>
<td>0 0 0</td>
<td>fCLK/4</td>
<td>$92/fCLK$</td>
<td>18.4</td>
<td>9.2</td>
</tr>
<tr>
<td>1 0</td>
<td>fCLK/2</td>
<td>$46/fCLK$</td>
<td>18.4</td>
<td>9.2</td>
</tr>
<tr>
<td>1 1</td>
<td>fCLK</td>
<td>$23/fCLK$</td>
<td>18.4</td>
<td>9.2</td>
</tr>
</tbody>
</table>

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.
Setting up the resolution

- A/D converter mode register 2 (ADM2)
  Sets the resolution.

Symbol: ADM2

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ADTYP</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>ADTYP</th>
<th>Resolution of A/D conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10-bit resolution</td>
</tr>
<tr>
<td>1</td>
<td>8-bit resolution</td>
</tr>
</tbody>
</table>

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.
Specifying the input channel
- Analog input channel specification register (ADS)
  Specifies the input channel for the analog voltage to be subjected to A/D conversion.

Symbol: ADS

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ADS2</td>
<td>ADS1</td>
<td>ADS0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

10-pin products

<table>
<thead>
<tr>
<th>ADS1</th>
<th>ADS0</th>
<th>Analog input channel</th>
<th>Input source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>ANI0</td>
<td>P01/ANI0 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>ANI1</td>
<td>P02/ANI1 pin</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>ANI2</td>
<td>P03/ANI2 pin</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>ANI3</td>
<td>P04/ANI3 pin</td>
</tr>
</tbody>
</table>

16-pin products

<table>
<thead>
<tr>
<th>ADS2</th>
<th>ADS1</th>
<th>ADS0</th>
<th>Analog input channel</th>
<th>Input source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ANI0</td>
<td>P01/ANI0 pin</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>ANI1</td>
<td>P02/ANI1 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>ANI2</td>
<td>P03/ANI2 pin</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>ANI3</td>
<td>P04/ANI3 pin</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ANI4</td>
<td>P05/ANI4 pin</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>ANI5</td>
<td>P10/ANI5 pin</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ANI6</td>
<td>P11/ANI6 pin</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>ANI7</td>
<td>P00/ANI7 pin</td>
</tr>
</tbody>
</table>

Note  16-pin products only.
Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.
Setting up A/D conversion end interrupts

- Interrupt request flag register (IF0H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK0H)
  Disables interrupts.

Symbol: IF0H

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>KRIF</td>
</tr>
<tr>
<td>6</td>
<td>ADIF</td>
</tr>
<tr>
<td>5</td>
<td>TMIF01</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt request signal is generated</td>
</tr>
<tr>
<td>1</td>
<td>Interrupt request is generated, interrupt request status</td>
</tr>
</tbody>
</table>

Symbol: MK0H

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>KRMK</td>
</tr>
<tr>
<td>6</td>
<td>ADMK</td>
</tr>
<tr>
<td>5</td>
<td>TMMK01</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Bit 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Interrupt servicing enabled</td>
</tr>
<tr>
<td>1</td>
<td>Interrupt servicing disabled</td>
</tr>
</tbody>
</table>

Caution  For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.
5.6.5 Main Processing

Figure 5.6 shows the flowchart for the main processing.

Figure 5.6 Main Processing

- Disable interrupts
  - Do not use vector interrupts.

- Start A/D conversion
  - SSTARTAD
  - Start A/D conversion.

- Switch into HALT mode
  - Upon end of conversion, set A/D conversion end interrupt request flag (ADIF ← 1) and cancel the HALT mode.

- Clear A/D conversion end interrupt request flag
  - ADIF ← 0: Clear interrupt request flag.

- Read conversion results
  - Read conversion results.
  - ADCRH register → A register
  - ADCRL register → X register

- Shift the conversion results right by 6 bits
  - AX register >> 6

- Store the results
  - RADCBUF ← AX register

- Start A/D converter operation
  - ADCS bit ← 1
5.6.6 A/D Conversion Start Processing

Figure 5.7 shows the flowchart for the A/D conversion start processing.

![Flowchart for A/D Conversion Start Processing](image)

- **SSTARTAD**
  - Enable A/D voltage comparator
  - A/D voltage comparator stabilization time elapsed?
    - Yes
      - Start A/D converter operation
      - Clear A/D conversion end interrupt request flag
      - Enable A/D conversion end interrupt request
      - RET
    - No
      - ADCE bit ← 1
      - Wait for 1 µs.
      - ADCS bit ← 1
      - ADIF ← 0: Clear interrupt request flag.
      - ADMK ← 0: Clear interrupt mask.

*Figure 5.7 A/D Conversion Start Processing*
Starting conversion operation

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.

Symbol: ADM0

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
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<tr>
<td>ADCS</td>
<td>0</td>
<td>0</td>
<td>FR1</td>
<td>FR0</td>
<td>0</td>
<td>LV0</td>
<td>ADCE</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>x</td>
<td>x</td>
<td>1</td>
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**Bit 7**

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<tr>
<th>ADCS</th>
<th>A/D conversion operation control</th>
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<tr>
<td>0</td>
<td>Stops conversion operation</td>
</tr>
<tr>
<td>1</td>
<td>Enables conversion operation</td>
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</tbody>
</table>

**Bit 0**

<table>
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<tr>
<th>ADCE</th>
<th>A/D voltage comparator operation control</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>Stops A/D voltage comparator operation</td>
</tr>
<tr>
<td>1</td>
<td>Enables A/D voltage comparator operation</td>
</tr>
</tbody>
</table>

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.
6. **Sample Code**

The sample code is available on the Renesas Electronics Website.

7. **Documents for Reference**

RL78/G10 User's Manual: Hardware (R01UH0384E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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