RL78/F23, RL78/F24

Porting Guide from RL78/F13, F14 to RL78/F23, F24 Products

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Introduction

RL78/F23, F24 products are successors of RL78/F13, F14 products and support security, CAN-FD, 12-bit A/D converter and other enhanced peripheral functions.

RL78/F23, F24 products have the same functions of general-timers and serial interfaces as RL78/F13, F14 products. Pin assignments and software of RL78/F23, F24 products are compatible to current products.

This application note provides comparisons between RL78/F13, F14 products and RL78/F23, F24 products, and can be used as a general guide during the migration from RL78/F13, F14 products to RL78/F23, F24 products.

Target Devices

Source Devices	Destination Devices
RL78/F14 (100/80/64/48/32/30-pin)	**RL78/F24 (100/80/64/48/32-pin)**
RL78/F13 (CAN & LIN) (80/64/48/32/30-pin)	**RL78/F24 (100/80/64/48/32-pin)**
RL78/F13 (LIN) (80/64/48/32/30/20-pin)	**RL78/F23 (80/64/48/32-pin)**

Contents

1. Overview

This document describes differences between RL78/F23, F24 products and RL78/F13, F14 products, and provides notes when replacing RL78/F13, F14 products with RL78/F23, F24 products.

A thorough evaluation needs to be performed when replacing RL78/F13, F14 products with RL78/F23, F24 products. For details of each product, refer to the hardware user's manuals.

1.1 Product Lineup

Tables below show the lineup of RL78/F24 and RL78/F23 products together with corresponding RL78/F14 and RL78/F13 products.

Table 1-1. RL78/F24 Products Lineup, Compared with RL78/F14

Source Devices: RL78/F14 Products						Destination Devices: RL78/F24 Products					
Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature (Ta)	Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature (Ta)
100QFP	256/192/128	8	20/16/10	32	-40 to 105	100QFP	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
	96/64	4	8/6	32	-40 to 105						-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
80QFP	256/192/128	8	20/16/10	32	-40 to 105	80QFP	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
	96/64	4	8/6	32	-40 to 105						-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
64QFP	256/192/128	8	20/16/10	32	-40 to 105	64QFP	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
	96/64	4	8/6	32	-40 to 105						-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
48QFP 48QFN	256/192/128	8	20/16/10	32	-40 to 105	48QFP	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
	96/64/48	4	8/6/4	32	-40 to 105						-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
32QFN	64/48	4	6/4	32	-40 to 105	32QFN	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
30SSOP	64/48	4	6/4	32	-40 to 105	32QFN or 48QFP	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150

Table 1-2. RL78/F24 Products Lineup, Compared with RL78/F13 (CAN & LIN)

Source Devices: RL78/F13 (CAN & LIN) Products						Destination Devices: RL78/F24 Products					
Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature (Ta)	Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature (Ta)
80QFP	128/96/64	4	8/6/4	32	-40 to 105	80QFP	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
64QFP	128/96/64/ 48/32	4	8/6/4/ 3/2	32	-40 to 105	64QFP	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
48QFP 48QFN	128/96/64/ 48/32	4	8/6/4/ 3/2	32	-40 to 105	48QFP	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
32QFN	128/96/64/ 48/32	4	8/6/4/ 3/2	32	-40 to 105	32QFN	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
30SSOP	128/96/64/ 48/32	4	8/6/4/ 3/2	32	-40 to 105	32QFN or 48QFP	256	16	24	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150

Table 1-3. RL78/F23 Products Lineup, Compared with RL78/F13 (LIN)

Source Devices: RL78/F13 (LIN) Products						Destination Devices: RL78/F23 Products					
Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature (Ta)	Pin Count	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Freq. (MHz)	Temperature (Ta)
80QFP	128/96/64	4	8/6/4	32	-40 to 105	80QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
64QFP	128/96/64/ 48/32	4	8/6/4/ 3/2	32	-40 to 105	64QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
48QFP 48QFN	128/96/64/ 48/32/16	4	8/6/4/ 3/2/1	32	-40 to 105	48QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
32QFN	64/48/32/16	4	4/3/2/1	32	-40 to 105	32QFN	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
30SSOP	64/48/32/16	4	4/3/2/1	32	-40 to 105	32QFN or 48QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150
20SSOP	64/48/32/16	4	4/3/2/1	32	-40 to 105	32QFN or 48QFP	128	8	12	40	-40 to 105
				24	-40 to 125						-40 to 125
				24	-40 to 150						-40 to 150

1.2 Product Feature Comparison

Tables below show the feature comparisons between RL78/F23, F24 products and RL78/F13, F14 products. Each function of RL78/F14 product and RL78/F13 (LIN) product shown in the table below is an example of the maximum memory product.

Table 1-4. Main Features of RL78/F24, Compared with RL78/F14

Features [Note 1]		RL78/F24					RL78/F14					Reference pages [Note 2]
		100 QFP	80 QFP	64 QFP	48 QFP	32 QFN	100 QFP	80 QFP	64 QFP	48 QFP	32 QFN	
CPU		RL78 CPU Core					RL78 CPU Core					-
Memory	Code Flash	256KB					48/64/96/128/192/256KB					P.12
	Data Flash	16KB					4/8KB					
	RAM	24KB					4/6/8/10/16/20KB					
Supply Voltage		2.7V to 5.5V					2.7V to 5.5V					-
Operation Frequency		(max) 40MHz					(max) 32MHz, 24MHz@K,Y-grade					P.19
System Clock	f_X	2MHz to 20MHz					1MHz to 20MHz					
	f_{IH}	40MHz					32MHz, 24MHz@K, Y-grade					
	f_{IL}	15kHz					15kHz					
	f_{SUB} [Note 4]	32.768kHz				-	32.768kHz				-	
	f_{PLL}	40MHz					32MHz, 24MHz@K, Y-grade					
Clock for Peripherals	f_{WDT}	15kHz					15kHz					
	f_{PLL}	80MHz					64MHz, 48MHz@K, Y-grade					
	f_{IH}	80MHz					64MHz, 48MHz@K, Y-grade					
POR		Yes					Yes					-
LVD		Yes					Yes					-
Window Watchdog Timer		Yes					Yes					-
Illegal Instruction Execution Detection Function		Yes					Yes					P.26
Flash Memory CRC Operation Function		Yes					Yes					
RAM ECC Detection Function		Yes					Yes					
CAN-FD RAM ECC Detection Function		Yes					-					
Code Flash Memory ECC Function		Yes					-					
Invalid Memory Access Detection Function		Yes					Yes					
Frequency Detection Function		Yes					Yes					
Clock Monitor Function		Yes					Yes					
Stack Pointer Monitor Function		Yes					Yes					
I/O Port Output Level Detection Function		Yes					Yes					
A/D Test Function		Yes					Yes					
I/O Port		86ch	68ch	52ch	38ch	25ch	86ch	68ch	52ch	38ch	25ch	P.18
	Output Only	1ch	1ch	1ch	1ch	-	1ch	1ch	1ch	1ch	-	
	Input Only	5ch	5ch	5ch	5ch	3ch	5ch	5ch	5ch	5ch	3ch	
Power Supply Pin	Internal Circuit	V_{DD}, V_{SS}, REGC					V_{DD}, V_{SS}, REGC					
	I/O Port	EV_{DD}, EV_{SS} [Note 3]					EV_{DD}, EV_{SS} [Note 3]					
	Analog	V_{DD}, V_{SS}, AV_{REFP}, AV_{REFM}					V_{DD}, V_{SS}, AV_{REFP}, AV_{REFM}					
Interrupt	External	16ch	16ch	15ch	14ch	10ch	16ch	16ch	15ch	14ch	9ch	P.29
	Internal	51ch	51ch	51ch	51ch	51ch	48ch	48ch	48ch	48ch	41ch	
Key Return Detection		8	8	8	8	6	8	8	8	8	6	-
DTC		44	44	44	44	43	44	44	44	44	37	-
Timer	TAU	16-bit×16ch					16-bit×16ch					P.21
	Timer RD	16-bit×2ch (w/ PWMOPA and Dithering/Gate)					16-bit×2ch					
	Timer RJ	16-bit×1ch					16-bit×1ch					
	RTC	1ch					1ch					
Serial I/F	SAU CSI/simplified I^2C/UART	4ch/4ch/2ch				3ch/3ch/2ch	4ch/4ch/2ch				3ch/3ch/2ch	P.23
	SPI	Yes					Yes					
	Multimaster I^2C	1ch					1ch					
	LIN/UART module	RLIN3: 2ch					RLIN3: 2ch				1ch	
	CAN interface	CAN-FD: 1ch					CAN: 1ch					
A/D Converter	Resolution	12-bit					10-bits					P.24
	Number of ch	31ch	25ch	24ch	19ch	10ch	31ch	25ch	20ch	18ch	10ch	
8-bit D/A Converter		1ch					1ch					-
Comparator		1ch					1ch					P.25
Secure Module		Yes					-					-
ELC		Yes					Yes					P.27

Notes 1. The table does not list all the features of RL78/F24.
2. Refers to the detail page of each function.
3. 100-pin products: EV_{DD0}/EV_{DD1} and EV_{SS0}/EV_{SS1}, 80-/64-pin products: EV_{DD0} and EV_{SS0}, Others: (Common with V_{DD} and V_{SS})
4. Do not use the XT1 and XT2 pin functions in products support Ta = -40 to 150°C.

Table 1-5. Main Features of RL78/F23, Compared with RL78/F13

Features Note 1		RL78/F23				RL78/F13 (LIN)				Reference pages Note 2
		80 QFP	64 QFP	48 QFP	32 QFN	80 QFP	64 QFP	48 QFP	32 QFN	
CPU		RL78 CPU Core				RL78 CPU Core				-
Memory	Code Flash	128KB				128/96/64/48/32/16KB				P.12
	Data Flash	8KB				4KB				
	RAM	12KB				8/6/4/3/2/1KB				
Supply Voltage		2.7V to 5.5V				2.7V to 5.5V				-
Operation Frequency		(max) 40MHz				(max) 32MHz, 24MHz@K,Y-grade				P.19
System Clock	f_X	2MHz to 20MHz				1MHz to 20MHz				
	f_{IH}	40MHz				32MHz, 24MHz@K, Y-grade				
	f_{IL}	15kHz				15kHz				
	f_{SUB} Note 4	32.768kHz			-	32.768kHz			-	
	f_{PLL}	40MHz				32MHz, 24MHz@K, Y-grade				
Clock for Peripherals	f_{WDT}	15kHz				15kHz				
	f_{PLL}	80MHz				64MHz, 48MHz@K, Y-grade				
	f_{IH}	80MHz				64MHz, 48MHz@K, Y-grade				
POR		Yes				Yes				-
LVD		Yes				Yes				-
Window Watchdog Timer		Yes				Yes				-
Illegal Instruction Execution Detection Function		Yes				Yes				P.26
Flash Memory CRC Operation Function		Yes				Yes				
RAM ECC Detection Function		Yes				Yes				
CAN-FD RAM ECC Detection Function		-				-				
Code Flash Memory ECC Function		Yes				-				
Invalid Memory Access Detection Function		Yes				Yes				
Frequency Detection Function		Yes				Yes				
Clock Monitor Function		Yes				Yes				
Stack Pointer Monitor Function		Yes				Yes				
I/O Port Output Level Detection Function		Yes				Yes				
A/D Test Function		Yes				Yes				
I/O Port		68ch	52ch	38ch	25ch	68ch	52ch	38ch	25ch	P.18
	Output Only	1ch	1ch	1ch	-	1ch	1ch	1ch	-	
	Input Only	5ch	5ch	5ch	3ch	5ch	5ch	5ch	3ch	
Power Supply Pin	Internal Circuit	V_{DD}, V_{SS}, REGC				V_{DD}, V_{SS}, REGC				
	I/O Port	EV_{DD}, EV_{SS} Note 3				EV_{DD}, EV_{SS} Note 3				
	Analog	V_{DD}, V_{SS}, AV_{REFP}, AV_{REFM}				V_{DD}, V_{SS}, AV_{REFP}, AV_{REFM}				
Interrupt	External	15ch	14ch	12ch	8ch	14ch	14ch	13ch	9ch	P.29
	Internal	36ch	36ch	36ch	36ch	40ch	40ch	40ch	40ch	
DTC		36	36	36	35	36	36	36	29	-
Timer	TAU	16-bit×12ch				16-bit×12ch				P.21
	Timer RD	16-bit×2ch (w/ PWMOPA and Dithering/Gate)				16-bit×2ch				
	Timer RJ	16-bit×1ch				16-bit×1ch				
	RTC	1ch				1ch				
Serial I/F	SAU CSI/simplified I^2C/UART	4ch/4ch/2ch			3ch/ 3ch/ 2ch	4ch/4ch/2ch			3ch/ 3ch/ 2ch	P.23
	SPI	Yes				Yes				
	Multimaster I^2C	1ch				1ch				
	LIN/UART module	RLIN3: 1ch				RLIN3: 1ch				
	CAN interface	-				-				
A/D Converter	Resolution	12-bit				10-bit				P.24
	Number of ch	25ch	24ch	19ch	10ch	22ch	20ch	18ch	10ch	
8-bit D/A Converter		-				-				-
Comparator		-				-				-
Secure Module		Yes				-				-
ELC		-				-				-

Notes 1. The table does not list all the features of RL78/F23.
2. Refers to the detail page of each function.
3. 80-/64-pin products: EV_{DD0} and EV_{SS0}, Others: (Common with V_{DD} and V_{SS})
4. Do not use the XT1 and XT2 pin functions in products support Ta = -40 to 150°C.

2. Pin Assignment

2.1 Pin Assignment Comparison

Tables below show the pin functional comparisons and differences between RL78/F24 product and RL78/F14 product, and RL78/F23 product and RL78/F13 product. Each function of RL78/F14 product and RL78/F13 (LIN) product shown in the tables below is an example of the maximum memory product.

Table 2-1. Port Functions of RL78/F24, Compared with RL78/F14 (1/2)

Pin No					RL78/F24	RL78/F14
100QFP	80QFP	64QFP	48QFP	32QFN		
100	1	1	1	1	P120/ANI25/TI07/TO07/TRDIOD0/SO01/(SCK10)/(LTXD1)/INTP4	P120/ANI25/TI07/TO07/TRDIOD0/SO01/(SCK10)/INTP4
1	-	-	-	-	P153/(SCK11)	P153/(SCK11)
2	-	-	-	-	P152/(SI11)	P152/(SI11)
3	-	-	-	-	P151/(SO11)	P151/(SO11)
4	-	-	-	-	P150/(SSI11)	P150/(SSI11)
5	2	-	-	-	P47/INTP13	P47/INTP13
6	3	-	-	-	P46/(TI12)/(TO12)	P46/(TI12)/(TO12)
7	4	-	-	-	P45/(TI10)/(TO10)	P45/(TI10)/(TO10)
8	5	-	-	-	P44/(TI07)/(TO07)	P44/(TI07)/(TO07)
9	6	2	-	-	P43/(LRXD0)	P43/(LRXD0)
10	7	3	-	-	P42/(LTXD0)	P42/(LTXD0)
11	8	4	2	2	P41/TI10/TO10/TRJIO0/TRD0RES/(SI10)/(RXD1)/VCOUT0/SNZOUT2	P41/TI10/TO10/TRJIO0/VCOUT0/SNZOUT2
12	9	5	3	3	P40/TOOL0	P40/TOOL0
13	10	6	4	4	RESET	RESET
14	11	7	5	-	P124/XT2/EXCLKS	P124/XT2/EXCLKS
15	12	8	6	-	P123/XT1	P123/XT1
16	13	9	7	5	P137/INTP0	P137/INTP0
17	14	10	8	6	P122/X2/EXCLK	P122/X2/EXCLK
18	15	11	9	7	P121/X1	P121/X1
19	16	12	10	8	REGC	REGC
20	17	13	11	9	VSS	VSS
21	18	14	-	-	EVSS0	EVSS0
22	19	15	12	10	V_{DD}	V_{DD}
23	20	16	-	-	EV_{DD0}	EV_{DD0}
24	21	17	13	11	P60/(TO01)/(SCK00)/(SCL00)	P60/(SCK00)/(SCL00)
25	22	18	14	12	P61/(TO02)/(SI00)/(SDA00)/(RXD0)	P61/(SI00)/(SDA00)/(RXD0)
26	23	19	15	13	P62/(TO03)/(SO00)/(TXD0)/SCLA0	P62/(SO00)/(TXD0)/SCLA0
27	24	20	16	14	P63/(TO07)/(SSI00)/SDAA0	P63/(SSI00)/SDAA0
28	25	-	-	-	P64/(TI14)/(TO14)/(SNZOUT3)	P64/(TI14)/(TO14)/(SNZOUT3)
29	26	-	-	-	P65/(TI16)/(TO16)/(SNZOUT2)	P65/(TI16)/(TO16)/(SNZOUT2)
30	27	-	-	-	P66/(TI00)/(TO00)	P66/(TI00)/(TO00)
31	28	-	-	-	P67/(TI02)/(TO02)	P67/(TI02)/(TO02)
32	-	-	-	-	P154/(SNZOUT7)	P154/(SNZOUT7)
33	-	-	-	-	P155/(SNZOUT6)	P155/(SNZOUT6)
34	29	21	17	-	P00/(TI05)/(TO05)/INTP9	P00/(TI05)/(TO05)/INTP9
35	-	-	-	-	P156/(SNZOUT5)	P156/(SNZOUT5)
36	-	-	-	-	P157/(SNZOUT4)	P157/(SNZOUT4)
37	30	22	18	-	P140/TRD1RES/PCLBUZ0	P140/PCLBUZ0
38	31	23	19	-	P130/RESOUT	P130/RESOUT
39	32	24	-	-	P77/(SSI10)/INTP12	P77/(SSI10)/INTP12
40	33	25	-	-	P76/(SCK10)/INTP12	P76/(SCK10)/INTP12
41	34	26	-	-	P75/(SI10)/(RXD1)	P75/(SI10)/(RXD1)
42	35	27	-	-	P74/ANI30/(SO10)/(TXD1)	P74/ANI30/(SO10)/(TXD1)
43	-	-	-	-	EVSS1	EVSS1
44	36	28	20	-	P73/ANI29/SSI11/(CRXD0)/SNZOUT7	P73/ANI29/SSI11/(CRXD0)/SNZOUT7
45	37	29	21	-	P72/ANI28/SO11/(CTXD0)/SNZOUT6	P72/ANI28/SO11/(CTXD0)/SNZOUT6
46	38	30	22	-	P71/ANI27/TI17/TO17/SCK11/SCL11/INTP6/SNZOUT5	P71/ANI27/TI17/TO17/SCK11/SCL11/INTP6/SNZOUT5
47	39	31	23	-	P70/ANI26/TI15/TO15/SI11/SDA11/INTP8/SNZOUT4	P70/ANI26/TI15/TO15/SI11/SDA11/INTP8/SNZOUT4
48	-	-	-	-	P03/(RTC1HZ)	P03/(RTC1HZ)
49	40	32	24	-	P32/TI16/TO16/(SO11)/INTP7	P32/TI16/TO16/INTP7

Table 2-1. Port Functions of RL78/F24, Compared with RL78/F14 (2/2)

Pin No					RL78/F24	RL78/F14
100QFP	80QFP	64QFP	48QFP	32QFN		
50	41	33	25	15	P30/TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT2	P30/TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT2
51	42	34	26	16	P17/TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3	P17/TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3
52	43	35	27	17	P16/TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD	P16/TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
53	-	-	-	-	EV_{DD1}	EV_{DD1}
54	44	36	28	18	P15/TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/ RTC1HZ/TOOLTXD	P15/TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/ RTC1HZ/TOOLTXD
55	45	37	29	-	P31/TI14/TO14/(INTP2)/STOPST	P31/TI14/TO14/(INTP2)/STOPST
56	46	38	-	-	P50/(SSI01)/(INTP3)	P50/(SSI01)/(INTP3)
57	47	39	-	-	P51/(SO01)/INTP11	P51/(SO01)/INTP11
58	48	40	-	-	P52/(SCK01)/(STOPST)	P52/(SCK01)/(STOPST)
59	49	41	-	-	P53/(SI01)/INTP10	P53/(SI01)/INTP10
60	50	42	30	19	P14/TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0	P14/TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0
61	51	43	31	20	P13/TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0	P13/TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
62	52	44	32	21	P12/TI11/TO11/(TRDIOD0)/SO10/TXD1/INTP5/SNZOUT3	P12/TI11/TO11/(TRDIOD0)/SO10/TXD1/INTP5/SNZOUT3
63	53	45	33	22	P11/TI13/TO13/TRJO0/SI10/SDA10/RXD1/CRXD0/LRXD1	P11/TI13/TO13/TRJO0/SI10/SDA10/RXD1/CRXD0/LRXD1
64	54	46	34	23	P10/TI13/TO13/TRJO0/SCK10/SCL10/CXTD0/LTXD1	P10/TI13/TO13/TRJO0/SCK10/SCL10/CXTD0/LTXD1
65	55	-	-	-	P54/(TI11)/(TO11)/SSI10	P54/(TI11)/(TO11)/SSI10
66	56	-	-	-	P55/(TI13)/(TO13)	P55/(TI13)/(TO13)
67	57	-	-	-	P56/(TI15)/(TO15)/(SNZOUT1)	P56/(TI15)/(TO15)/(SNZOUT1)
68	58	-	-	-	P57/(TI17)/(TO17)/(SNZOUT0)	P57/(TI17)/(TO17)/(SNZOUT0)
69	-	-	-	-	P107/(LRXD1)	P107/(LRXD1)
70	-	-	-	-	P106/(LTXD1)	P106/(LTXD1)
71	-	-	-	-	P105/ANI23	P105/ANI23
72	-	-	-	-	P104/ANI22	P104/ANI22
73	59	47	35	24	P33/AV_{REFP}/ANI6	P33/AV_{REFP}/ANI0
74	60	48	36	25	P34/AV_{REFM}/ANI7	P34/AV_{REFM}/ANI1
75	61	49	37	26	P80/ANI0/ANO0	P80/ANI2/ANO0
76	62	50	38	27	P81/ANI1	P81/ANI3/IVCMP00
77	63	51	39	28	P82/ANI2/IVCMP00	P82/ANI4/IVCMP01
78	64	52	40	29	P83/ANI3/IVCMP01	P83/ANI5/IVCMP02
79	65	53	41	30	P84/ANI4/IVCMP02	P84/ANI6/IVCMP03
80	66	54	42	31	P85/ANI5/IVREF0/IVCMP03	P85/ANI7/IVREF0
81	67	55	43	-	P86/ANI8	P86/ANI8
82	68	56	44	-	P87/ANI9	P87/ANI9
83	69	57	45	-	P90/ANI10	P90/ANI10
84	70	58	46	-	P91/ANI11	P91/ANI11
85	71	59	47	-	P92/ANI12	P92/ANI12
86	72	60	-	-	P93/ANI13	P93/ANI13
87	73	61	-	-	P94/ANI14	P94/ANI14
88	74	62	-	-	P95/ANI15	P95/ANI15
89	75	63	-	-	P96/ANI16	P96/ANI16
90	76	-	-	-	P97/ANI17	P97/ANI17
91	-	-	-	-	P100/ANI18	P100/ANI18
92	-	-	-	-	P101/ANI19	P101/ANI19
93	-	-	-	-	P102/ANI20	P102/ANI20
94	-	-	-	-	P103/ANI21	P103/ANI21
95	77	-	-	-	P02/(TI06)/(TO06)	P02/(TI06)/(TO06)
96	-	-	-	-	P127/(TI03)/(TO03)	P127/(TI03)/(TO03)
97	78	-	-	-	P126/(TI01)/(TO01)	P126/(TI01)/(TO01)
98	79	-	-	-	P01/(TI04)/(TO04)	P01/(TI04)/(TO04)
99	80	64	48	32	P125/ANI24/TI03/TO03/TRDIOB0/SSI01/(LRXD1)/INTP1/ SNZOUT1	P125/ANI24/TI03/TO03/TRDIOB0/SSI01/INTP1/SNZOUT1

Remark: KRx (Key Return) function depends on the product. For details, see “Table 2-3. Pin Assignment for KRx Function”.

Table 2-2. Port Functions of RL78/F23, Compared with RL78/F13 (LIN) (1/2)

Pin No					RL78/F23	RL78/F13 (LIN)
100QFP	80QFP	64QFP	48QFP	32QFN		
-	1	1	1	1	P120/ANI25/TI07/TO07/TRDIOD0/SO01/(SCK10)/INTP4	P120/ANI25/TI07/TO07/TRDIOD0/SO01/(SCK10)/INTP4
-	2	-	-	-	P47/INTP13	P47/INTP13
-	3	-	-	-	P46/(TI12)/(TO12)	P46/(TI12)/(TO12)
-	4	-	-	-	P45/(TI10)/(TO10)	P45/(TI10)/(TO10)
-	5	-	-	-	P44/(TI07)/(TO07)	P44/(TI07)/(TO07)
-	6	2	-	-	P43/(LRXD0)	P43/(LRXD0)
-	7	3	-	-	P42/(LTXD0)	P42/(LTXD0)
-	8	4	2	2	P41/TI10/TO10/TRJIO0/TRD0RES/(SI10)/(RXD1)/SNZOUT2	P41/TI10/TO10/TRJIO0/SNZOUT2
-	9	5	3	3	P40/TOOL0	P40/TOOL0
-	10	6	4	4	RESET	RESET
-	11	7	5	-	P124/XT2/EXCLKS	P124/XT2/EXCLKS
-	12	8	6	-	P123/XT1	P123/XT1
-	13	9	7	5	P137/INTP0	P137/INTP0
-	14	10	8	6	P122/X2/EXCLK	P122/X2/EXCLK
-	15	11	9	7	P121/X1	P121/X1
-	16	12	10	8	REGC	REGC
-	17	13	11	9	V_{SS}	V_{SS}
-	18	14	-	-	EV_{SS0}	EV_{SS0}
-	19	15	12	10	V_{DD}	V_{DD}
-	20	16	-	-	EV_{DD0}	EV_{DD0}
-	21	17	13	11	P60/(TO01)/(SCK00)/(SCL00)	P60/(SCK00)/(SCL00)
-	22	18	14	12	P61/(TO02)/(SI00)/(SDA00)/(RXD0)	P61/(SI00)/(SDA00)/(RXD0)
-	23	19	15	13	P62/(TO03)/(SO00)/(TXD0)/SCLA0	P62/(SO00)/(TXD0)/SCLA0
-	24	20	16	14	P63/(TO07)/(SSI00)/SDAA0	P63/(SSI00)/SDAA0
-	25	-	-	-	P64/(SNZOUT3)	P64/(SNZOUT3)
-	26	-	-	-	P65/(SNZOUT2)	P65/(SNZOUT2)
-	27	-	-	-	P66/(TI00)/(TO00)	P66/(TI00)/(TO00)
-	28	-	-	-	P67/(TI02)/(TO02)	P67/(TI02)/(TO02)
-	29	21	17	-	P00/(TI05)/(TO05)/INTP9	P00/(TI05)/(TO05)/INTP9
-	30	22	18	-	P140/TRD1RES/PCLBUZ0	P140/PCLBUZ0
-	31	23	19	-	P130/RESOUT	P130/RESOUT
-	32	24	-	-	P77/(SSI10)/INTP12	P77/(SSI10)/INTP12
-	33	25	-	-	P76/(SCK10)/INTP12	P76/(SCK10)/INTP12
-	34	26	-	-	P75/(SI10)/(RXD1)	P75/(SI10)/(RXD1)
-	35	27	-	-	P74/ANI30/(SO10)/(TXD1)	P74/ANI30/(SO10)/(TXD1)
-	36	28	20	-	P73/ANI29/SSI11/SNZOUT7	P73/ANI29/SSI11/SNZOUT7
-	37	29	21	-	P72/ANI28/SO11/SNZOUT6	P72/ANI28/SO11/SNZOUT6
-	38	30	22	-	P71/ANI27/SCK11/SCL11/INTP6/SNZOUT5	P71/ANI27/SCK11/SCL11/INTP6/SNZOUT5
-	39	31	23	-	P70/ANI26/SI11/SDA11/INTP8/SNZOUT4	P70/ANI26/SI11/SDA11/INTP8/SNZOUT4
-	40	32	24	-	P32/(SO11)/INTP7	P32/INTP7
-	41	33	25	15	P30/TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT2	P30/TI01/TO01/TRDIOD1/SSI00/INTP2/SNZOUT2
-	42	34	26	16	P17/TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3	P17/TI00/TO00/TRDIOB1/SCK00/SCL00/INTP3
-	43	35	27	17	P16/TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD	P16/TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
-	44	36	28	18	P15/TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/RTC1HZ/TOOLTXD	P15/TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/RTC1HZ/TOOLTXD
-	45	37	29	-	P31/(INTP2)/STOPST	P31/(INTP2)/STOPST
-	46	38	-	-	P50/(SSI01)/(INTP3)	P50/(SSI01)/(INTP3)
-	47	39	-	-	P51/(SO01)/INTP11	P51/(SO01)/INTP11
-	48	40	-	-	P52/(SCK01)/(STOPST)	P52/(SCK01)/(STOPST)
-	49	41	-	-	P53/(SI01)/INTP10	P53/(SI01)/INTP10
-	50	42	30	19	P14/TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0	P14/TI06/TO06/TRDIOC0/SCK01/SCL01/LRXD0
-	51	43	31	20	P13/TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0	P13/TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
-	52	44	32	21	P12/TI11/TO11/(TRDIOD0)/SO10/TXD1/INTP5/SNZOUT3	P12/TI11/TO11/(TRDIOD0)/SO10/TXD1/INTP5/SNZOUT3
-	53	45	33	22	P11/TI13/TO13/TRJO0/SI10/SDA10/RXD1	P11/TI13/TO13/TRJO0/SI10/SDA10/RXD1
-	54	46	34	23	P10/TI13/TO13/TRJO0/SCK10/SCL10	P10/TI13/TO13/TRJO0/SCK10/SCL10
-	55	-	-	-	P54/(TI11)/(TO11)/SSI10	P54/(TI11)/(TO11)/SSI10

Table 2-2. Port Functions of RL78/F23, Compared with RL78/F13 (LIN) (2/2)

Pin No					RL78/F23	RL78/F13 (LIN)
100QFP	80QFP	64QFP	48QFP	32QFN		
-	56	-	-	-	P55/(TI13)/(TO13)	P55/(TI13)/(TO13)
-	57	-	-	-	P56/(SNZOUT1)	P56/(SNZOUT1)
-	58	-	-	-	P57/(SNZOUT0)	P57/(SNZOUT0)
-	59	47	35	24	P33/AV_{REFP}/ANI6	P33/AV_{REFP}/ANI0
-	60	48	36	25	P34/AV_{REFM}/ANI7	P34/AV_{REFM}/ANI1
-	61	49	37	26	P80/ANI0	P80/ANI2
-	62	50	38	27	P81/ANI1	P81/ANI3
-	63	51	39	28	P82/ANI2	P82/ANI4
-	64	52	40	29	P83/ANI3	P83/ANI5
-	65	53	41	30	P84/ANI4	P84/ANI6
-	66	54	42	31	P85/ANI5	P85/ANI7
-	67	55	43	-	P86/ANI8	P86/ANI8
-	68	56	44	-	P87/ANI9	P87/ANI9
-	69	57	45	-	P90/ANI10	P90/ANI10
-	70	58	46	-	P91/ANI11	P91/ANI11
-	71	59	47	-	P92/ANI12	P92/ANI12
-	72	60	-	-	P93/ANI13	P93/ANI13
-	73	61	-	-	P94/ANI14	P94/ANI14
-	74	62	-	-	P95/ANI15	P95/ANI15
-	75	63	-	-	P96/ANI16	P96/ANI16
-	76	-	-	-	P97/ANI17	P97/ANI17
-	77	-	-	-	P02/(TI06)/(TO06)	P02/(TI06)/(TO06)
-	78	-	-	-	P126/(TI01)/(TO01)	P126/(TI01)/(TO01)
-	79	-	-	-	P01/(TI04)/(TO04)	P01/(TI04)/(TO04)
-	80	64	48	32	P125/ANI24/TI03/TO03/TRDIOB0/SSI01/INTP1/SNZOUT1	P125/ANI24/TI03/TO03/TRDIOB0/SSI01/INTP1/SNZOUT1

Remark: KRx (Key Return) function depends on the product. For details, see “Table 2-3. Pin Assignment for KRx Function”.

Table 2-3. Pin Assignment for KRx Function

Pin Function (Key return)	KRx Assigned Pin (No difference between RL78/F23, F24 products and RL78/F13, F14 products)									
	100QFP		80QFP		64QFP		48QFP		32QFN	
	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1
KR7	P77	-	P77	-	P77	P96	-	P92	-	-
KR6	P76	-	P76	-	P76	P95	-	P91	-	-
KR5	P75	-	P75	-	P75	P94	-	P90	-	P85
KR4	P74	-	P74	-	P74	P93	-	P87	-	P84
KR3	P73	-	P73	-	P73	P92	P73	P86	-	P83
KR2	P72	-	P72	-	P72	P91	P72	P85	-	P82
KR1	P71	-	P71	-	P71	P90	P71	P84	-	P81
KR0	P70	-	P70	-	P70	P87	P70	P83	-	P80

The table below shows extended functions on RL78/F23, F24 products.

Table 2-4. RL78/F23, F24 Pin Function Added from RL78/F13, F14 Products

Added Pin Function	Added Purpose	Setting to Use
P32/**(SO11)**	**Expanded pin allocation**	PIOR43 = 0, PIOR92 = 1
P41/**TRD0RES**	**Expanded the Timer RDe function**	- (TRD0 for Timer RDe counter reset signal input)
P41/**(SI10)/(RXD1)**	**Expanded pin allocation**	PIOR42 = 0, PIOR91 = 1
P60/**(TO01)**	**Expanded pin allocation**	PIOR11 = 1, PIOR90 = 1
P61/**(TO02)**	**Expanded pin allocation**	PIOR12 = 1, PIOR90 = 1
P62/**(TO03)**	**Expanded pin allocation**	PIOR13 = 1, PIOR90 = 1
P63/**(TO07)**	**Expanded pin allocation**	PIOR17 = 1, PIOR90 = 1
P120/**(LTXD0)**	**Expanded pin allocation**	PIOR45 = 1, PIOR93 = 1
P125/**(LRXD0)**	**Expanded pin allocation**	PIOR45 = 1, PIOR93 = 1
P140/**TRD1RES**	**Expanded the Timer RDe function**	- (TRD1 for Timer RDe counter reset signal input)

Remarks: PIOR11, PIOR12, PIOR13, PIOR17: Bit of the PIOR1 register
PIOR42, PIOR43, PIOR45: Bit of the PIOR4 register
PIOR90, PIOR91, PIOR92, PIOR93: Bit of the PIOR9 register (This register has been added to the RL78/F23, F24 products.)

The table below shows functions changed on RL78/F23, F24 products.

Table 2-5. RL78/F23, F24 Pin Function Changed from RL78/F13, F14 Products

Pin Function	Source Device (RL78/F13, F14)	RL78/F23, F24	Purpose of Change
ANI0	P33	P80	ANI0 has dedicated-channel S&H circuit, and P33 is assigned AV_{REFP} (analog reference voltage (+) input).
ANI1	P34	P81	ANI1 has dedicated-channel S&H circuit, and P34 is assigned AV_{REFM} (analog reference voltage (-) input).
ANI2 to ANI7	P80 to P85	P82 to P85, P33, and P34	Changed ANI0 and ANI1 pin assignment
IVCMP00	P81	P82	P81 assigned ANI1 function. (ANI1 has dedicated-channel S&H circuit.)
IVCMP01 to IVCMP03	P82 to P84	P83 to P85	Changed IVCMP0x pin assignment

For details, refer to chapters on functions A/D converter and comparator in this document.

3. Memory Map

3.1 Memory Size by Products

RL78/F24 memory sizes are Code Flash: 256 KB, Data Flash: 16 KB, and RAM: 24 KB. Also, RL78/F23 memory sizes are Code Flash: 128 KB, Data Flash: 8 KB, and RAM: 12 KB. The memory size of Data Flash and RAM are expanded from RL78/F13, F14 products.

Key Points for Porting:

- **Difference in memory size**

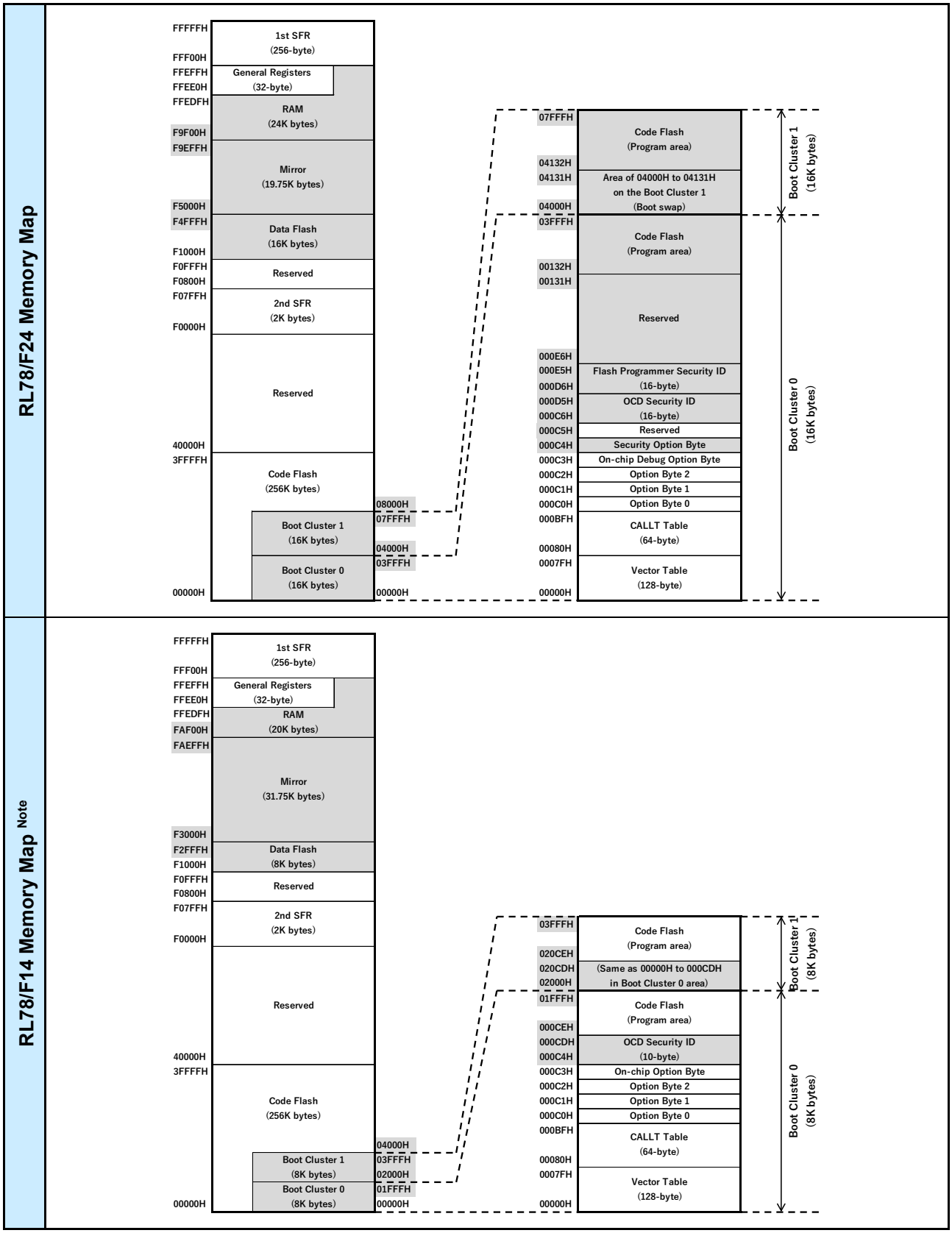
  The memory sizes have been expanded from RL78/F14 product to RL78/F24 product, and from RL78/F13 product to RL78/F23 product.

- **Difference in package**

  RL78/F23, F24 products do not have a 20-SSOP, 30-SSOP, or a 48-QFN package. Consider 32-QFN or 48-QFP products when migrating from those products.

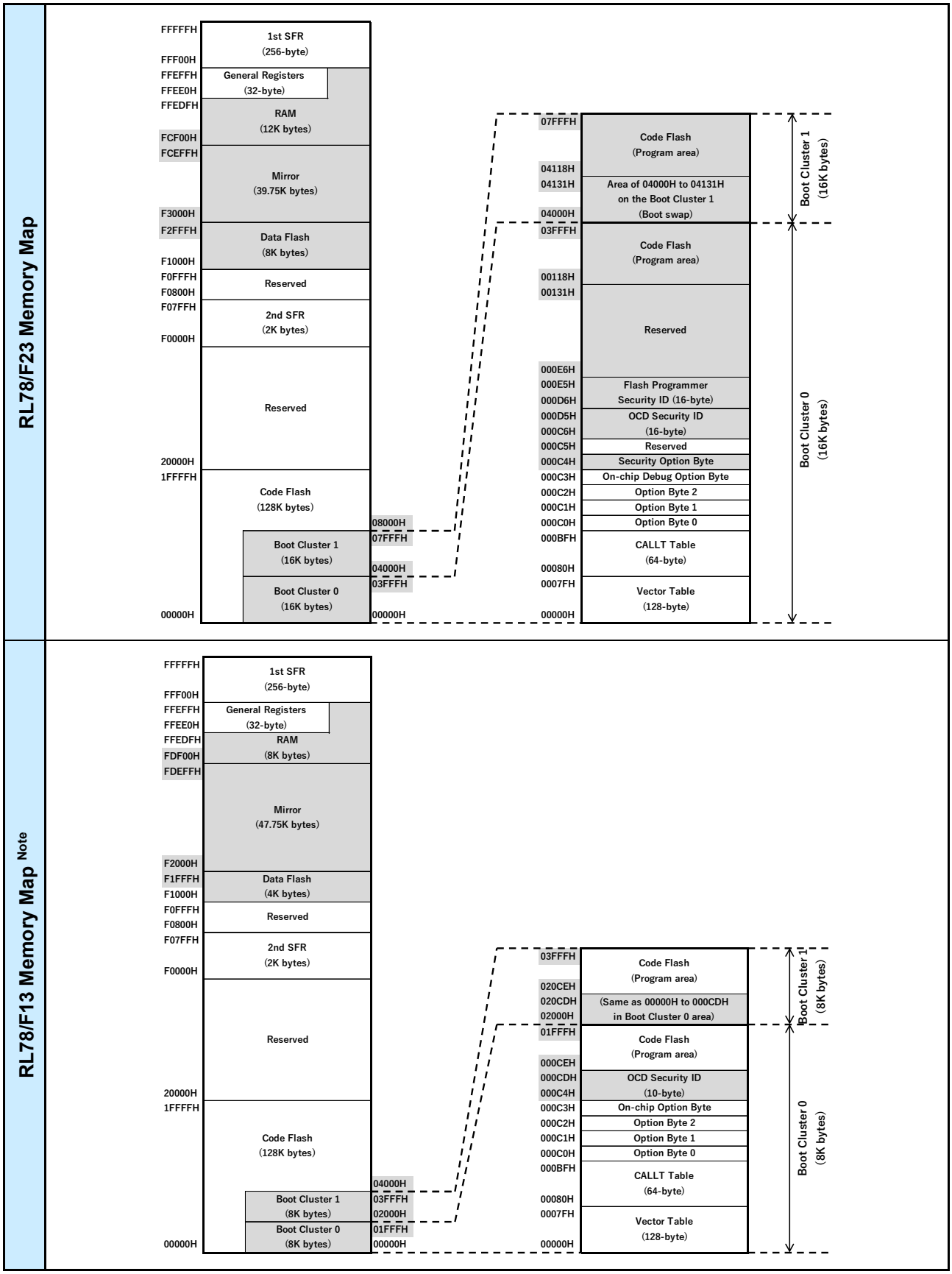
3.2 Memory Map

Figures below show the comparison of memory maps for products of RL78/F24 and RL78/F14 and products of RL78/F23 and RL78/F13.



Note. Illustrate products with maximum memory size.

Figure 3-1. Memory Map of RL78/F24, Compared with RL78/F14



Note. Illustrate products with maximum memory size.

Figure 3-2. Memory Map of RL78/F23, Compared with RL78/F13

The differences in memory map between RL78/F23, F24 products and RL78/F13, F14 products are shown below.
- Added Security Option Byte (000C4H)
- Expanded On-chip Debug Security ID area (000C6H – 000D5H) from 80-bit to 128-bit
- Added Flash Programmer Security ID area (000D6H – 000E5H)
- Expanded Boot Cluster 0/1 memory sizes from 8 KB to 16 KB

The table below shows the difference between option bytes for RL78/F23, F24 products and RL78/F13, F14 products.

Table 3-1. Option Bytes Area of RL78/F23, F24, Compared with RL78/F13, F14

Item	RL78/F23, F24	RL78/F13, F14
User Option Byte 0	WDT control	WDT control
User Option Byte 1	LVD, CLM control	LVD, CLM control
User Option Byte 2	HOCO frequency setting, RESOUTB control	HOCO frequency setting, RESOUTB control
On-chip Debug Option Byte	OCD, Hot plug-in, **Flash programmer** control	OCD, Hot plug-in control
Security Option Byte	**Security ID (On-chip debug security ID, and flash programmer security ID) read protection**	No features

Key Points for Porting:

- **Difference in memory map**

  Security option byte, on-chip debug security ID area, and flash programmer security ID area have been expanded with the addition of security features on RL78/F23, F24 products. Set the data according to this specification for security option byte (000C4H) added in RL78/F23, F24 products.

The differences in mirror area for the code flash between RL78/F23, F24 products and RL78/F13, F14 products are shown below.
The RL78/F23 and RL78/F24 products mirror the code flash area of 00000H to 0FFFFH or 10000H to 1FFFFH, to F0000H to FFFFFH (the code flash area to be mirrored is set by the processor mode control register (PMC)), same as RL78/F13 and RL78/F14 products.
The code flash area is not mirrored to the SFR, extended SFR, RAM, data flash memory, and use prohibited areas, so the size of the mirror area varies by product. The figure below shows a comparison of the mirror area for each product.

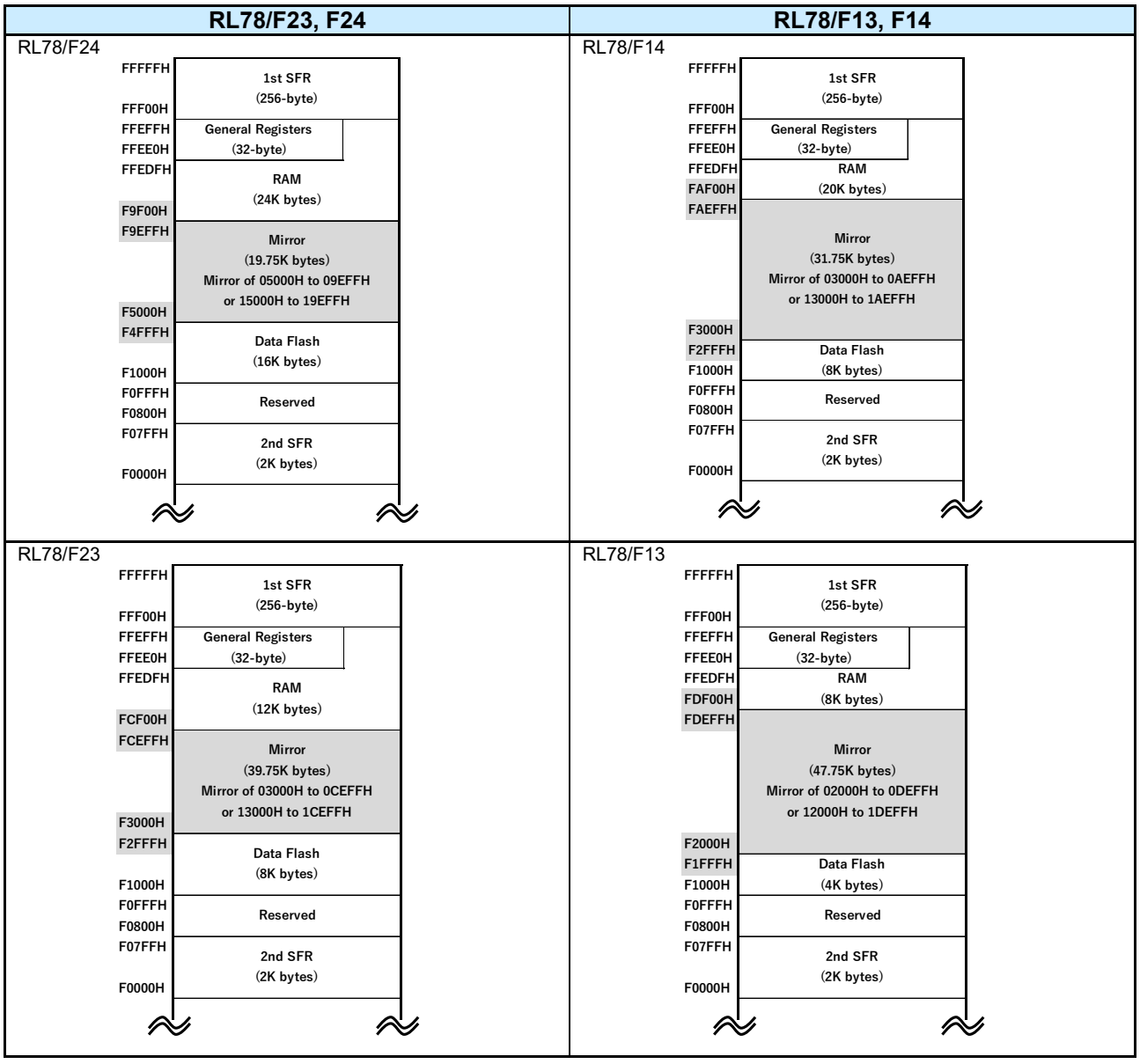


Figure 3-3. Mirror Area of RL78/F23, F24, Compared with RL78/F13, F14

Key Points for Porting:

- **Code flash mirror area**

  The mirror area (mirror the code flash area of 00000H to 0FFFFH or 10000H to 1FFFFH, to F0000H to FFFFFH) varies by product. When using the mirror area, place the data table used in the mirror area in the code flash area of the corresponding area. See Figure 3-3.
  RAM and code flash memory are increased from RL78/F13, F14 products. With this increase, the area available in Mirror area is decreasing. If Mirror area is insufficient, access the code flash memory area directly. Alternatively, copy the data from the code flash memory to the RAM area and access the RAM area.

In RL78/F23, F24 products, the start address of the RAM used can be set to a user-specified value. Set RAMSAR register to the RAM start address (bits 15 to 8; reset value = EFH; valid RAM area = FEF00H to FFEFFH). By using this setting and invalid memory access detection function, writing to an unused RAM area can be guarded.

- MCU reset occurs when writing to an invalid RAM area by using invalid memory access detection function.
- Memory guards writing to the area of 128-/256-/512-byte selected by RAM guard function.

The table below shows an example of the valid area of RAM by RAMSAR register, and the effective area of RAM guard function.

Table 3-2. RAMSAR Register Setting Example

RAMSAR register [Note]	IAWCTL.GRAM[1:0] bits	Valid RAM Area	RAM Guard Space
9FH	01B (128 bytes)	F9F00H – FFEFFH (24KB)	F9F00H – F9F7FH
	10B (256 bytes)		F9F00H – F9FFFH
	11B (512 bytes)		F9F00H – FA0FFH
AFH	01B (128 bytes)	FAF00H – FFEFFH (20KB)	FAF00H – FAF7FH
	10B (256 bytes)		FAF00H – FAFFFH
	11B (512 bytes)		FAF00H – FB0FFH
CFH	01B (128 bytes)	FCF00H – FFEFFH (12KB)	FCF00H – FCF7FH
	10B (256 bytes)		FCF00H – FCFFFH
	11B (512 bytes)		FCF00H – FD0FFH
DFH	01B (128 bytes)	FDF00H – FFEFFH (8KB)	FDF00H – FDF7FH
	10B (256 bytes)		FDF00H – FDFFFH
	11B (512 bytes)		FDF00H – FE0FFH
EFH	01B (128 bytes)	FEF00H – FFEFFH (4KB)	FEF00H – FEF7FH
	10B (256 bytes)		FEF00H – FEFFFH
	11B (512 bytes)		FEF00H – FF0FFH

Note. Be sure to set it within the memory range of the product to be used.

Key Points for Porting:

- **Difference in RAMSAR register**

  RL78/F23, F24 products specify the RAM start address by RAMSAR register setting. The reset value of this register is EFH (valid RAM area: FEF00H to FFEFFH, 4 KB). Be sure to set the required value in the start-up program.

- **Difference in invalid memory access detection function**

  In RL78/F23, F24 products, the unused area of RAM is expanded to the detection area of invalid memory access detection function.

4. Port Function

The number of I/O ports in RL78/F23, F24 products and RL78/F13, F14 products is the same. However, some port related registers that control the function have been changed.

4.1 Port Function Comparison

The table below shows the differences between RL78/F23, F24 products and RL78/F13, F14 products port function.

Table 4-1. I/O Port Register Differences of RL78/F23, F24, Compared with RL78/F13, F14

Register	Register Description	RL78/F23, F24
PMx	Port mode register (Input or output mode setting)	Same as RL78/F13, F14
Px	Port register (Input or output level)	Same as RL78/F13, F14
PUx	Pull-up resistor option register (Internal pull-up setting)	Same as RL78/F13, F14
PIMx	Port input mode register (C-MOS or TTL level)	Same as RL78/F13, F14
POMx	Port output mode register (C-MOS or N-ch open drain)	Added POM32 bit from RL78/F13, F14
PMCx	Port mode control register (Digital I/O or analog I/O)	Added PMC3, 8, 9, 10 registers from RL78/F13, F14
ADPC	A/D port configuration register (Digital I/O or analog I/O)	Deleted from RL78/F13, F14 (correspond with PMCx)
PITHLx	Port input threshold control register (Schmitt 1, 3, or TTL level)	Added PITHL41, PITHL120 bits from RL78/F13, F14
PIORx	Peripheral I/O redirection register	Added PIOR9 register from RL78/F13, F14
PSRSEL	Port output slew rate register (Normal or slow)	Same as RL78/F13, F14
PSNZCNTx	SNOOZE status output control register (Output pun setting)	Same as RL78/F13, F14
PMS	Port mode select register (Read from output pin level)	Same as RL78/F13, F14

Key Points for Porting:

- **Analog port selection**

  Select analog input/output port with PMCx register for each pin. If the system is concerned about a short circuit between analog input adjacent pins, an open pin which output low level can be assigned between analog input pin (A) and analog input pin (B).

- **Added PIOR9 register**

In RL78/F23, F24 products, output pin is extended so that PWM output and serial I/F can be used independently. For details, see Table 2-1 and Table 2-2.

5. Clock Generator

The table below shows the differences between RL78/F23, F24 products and RL78/F13, F14 products clock generator circuit.

Table 5-1. Clock Generator of RL78/F23, F24, Compared with RL78/F13, F14

Clock Generator	RL78/F23, F24	RL78/F13, F14
X1 clock	2MHz to 20MHz	1MHz to 20MHz
XT1 clock	Same as RL78/F13, F14	32.768kHz
PLL circuit	Max. output frequency: 80MHz	Max. output frequency: 64MHz
High-speed OCO	2MHz to 80MHz	1MHz to 64MHz
Low-speed OCO	Same as RL78/F13, F14	15kHz
Low-speed OCO for WDT	Same as RL78/F13, F14	15kHz

5.1 PLL Clock Circuit

PLL clock circuit of RL78/F23, F24 products is expanded PLL clock frequency to 80 MHz. RL78/F23, F24 products can use up to 80 MHz PLL clock frequency or high-speed on-chip oscillator clock frequency when using RS-CANFD lite module or Timer RDe module.

The table below shows the PLL clock circuit specifications in RL78/F23, F24 products.

Table 5-2. PLL Clock Settings of RL78/F23, F24

X1 Clock	X1 Clock Divider (FMAINDIV)	PLL Multiplier (PLLMULA, PLLMUL)	PLL Divider (PLLDIV0, FPLLDIV)	PLL Frequency
4MHz	00B (×1/1)	11B (×20)	01B (×1/1)	80MHz
	00B (×1/1)	11B (×20)	00B (×1/2)	40MHz
8MHz	00B (×1/1)	10B (×10)	01B (×1/1)	80MHz
	00B (×1/1)	01B (×16)	00B (×1/2)	64MHz
	00B (×1/1)	00B (×12)	00B (×1/2)	48MHz
	00B (×1/1)	10B (×10)	00B (×1/2)	40MHz
	00B (×1/1)	01B (×16)	10B (×1/4)	32MHz
	00B (×1/1)	00B (×12)	10B (×1/4)	24MHz
16MHz	10B (×1/2)	10B (×10)	01B (×1/1)	80MHz
	10B (×1/2)	01B (×16)	00B (×1/2)	64MHz
	10B (×1/2)	00B (×12)	00B (×1/2)	48MHz
	10B (×1/2)	10B (×10)	00B (×1/2)	40MHz
	10B (×1/2)	01B (×16)	10B (×1/4)	32MHz
	10B (×1/2)	00B (×12)	10B (×1/4)	24MHz
20MHz	11B (×1/4)	01B (×16)	01B (×1/1)	80MHz
	11B (×1/4)	01B (×16)	00B (×1/2)	40MHz

Caution: Bit values other than above are prohibited.

Remarks: FMAINDIV, FPLLDIV: Bits of the CKSEL register
PLLMULA, PLLMUL, PLLDIV0: Bits of the PLLCTL register

Key Points for Porting:

- **Using PLL clock circuit**

When using PLL clock circuit, be sure to select settings shown in the table.

5.2 High-speed On-chip Oscillator Frequency Selection

High-speed on-chip oscillator frequency is selected by user option byte (000C2H) and HOCODIV register. In RL78/F23, F24 products, the frequency of HOCO frequency is also expanded to 80 MHz as the maximum operating frequency is expanded. The table below shows the differences between RL78/F23, F24 products and RL78/F13, F14 products HOCO specifications.

Table 5-3. High-Speed OCO of RL78/F23, F24, Compared with RL78/F13, F14

HOCO DIV2	HOCO DIV1	HOCO DIV0	RL78/F23, F24				RL78/F13, F14			
			High-speed on-chip oscillator frequency (f_{IH})				High-speed on-chip oscillator frequency (f_{IH})			
			32 MHz base	40 MHz base	64 MHz base	80 MHz base	24 MHz base	32 MHz base	48 MHz base	64 MHz base
			FRQSEL4 = 0		FRQSEL4 = 1		FRQSEL4 = 0		FRQSEL4 = 1	
			FRQSEL3 = 0	FRQSEL3 = 1	FRQSEL3 = 0	FRQSEL3 = 1	FRQSEL3 = 0	FRQSEL3 = 1	FRQSEL3 = 0	FRQSEL3 = 1
0	0	0	32 MHz	40 MHz	64 MHz	80 MHz	24 MHz	32 MHz	48 MHz	64 MHz
0	0	1	16 MHz	20 MHz	32 MHz	40 MHz	12 MHz	16 MHz	24 MHz	32 MHz
0	1	0	8 MHz	10 MHz	16 MHz	20 MHz	6 MHz	8 MHz	12 MHz	16 MHz
0	1	1	4 MHz	5 MHz	8 MHz	10 MHz	3 MHz	4 MHz	6 MHz	8 MHz
1	0	0	2 MHz	prohibited	4 MHz	5 MHz	prohibited	2 MHz	prohibited	4 MHz
1	0	1	prohibited	prohibited	prohibited	prohibited	prohibited	1 MHz	prohibited	2 MHz
Settings other than the above are prohibited.										

Remarks: HOCODIV[2:0]: Bits of the HOCODIV register
FRQSEL4, 3: Bits of the User Option Byte (000C2H/040C2H)

Key Points for Porting:

- **HOCO frequency setting**

  High-speed on-chip oscillator frequency is selected by FRQSEL[4:0] bits of the user option byte (000C2H/040C2H) and HOCODIV register. Set user option byte (000C2H/040C2H) according to the frequency used by the system.

- **PLL clock setting when FRQSEL3 bit is 0**

  If the FRQSEL3 bit in the user option byte 2 is se to 0 (HOCO frequency = 64/ 32/ 16/ 8/ 4/ 2 MHz), and moreover the CPU/peripheral hardware clock (f_{CLK}) is selected as the PLL clock, the f_{CLK} must not be set to 40 MHz.

6. Timer Functions

Timer functions of RL78/F23, F24 products are extended for the maximum operating frequency. In addition, the Timer RDe extends the PWM output control function in addition to the conventional functions. Tables below show the differences between RL78/F23, F24 products and RL78/F13, F14 products timer functions.

Table 6-1. Timer Functions of RL78/F24, Compared with RL78/F14

Timer Function	RL78/F24	RL78/F14
Timer Array Unit (TAU)	16-bit × 16ch Operating frequency: 40MHz	16-bit × 16ch Operating frequency: 32MHz
Timer RD	16-bit × 2ch (Timer RDe) Operating frequency: 80MHz with PWMOPA, Dithering/Gate control	16-bit × 2ch Operating frequency: 64MHz
Timer RJ	16-bit × 1ch Operating frequency: 40MHz	16-bit × 1ch Operating frequency: 32MHz
Real-time Clock	1ch	1ch

Table 6-2. Timer Functions of RL78/F23, Compared with RL78/F13

Timer Function	RL78/F23	RL78/F13
Timer Array Unit (TAU)	16-bit × 12ch Operating frequency: 40MHz	16-bit × 12ch Operating frequency: 32MHz
Timer RD	16-bit × 2ch (Timer RDe) Operating frequency: 80MHz with PWMOPA, Dithering/Gate control	16-bit × 2ch Operating frequency: 64MHz
Timer RJ	16-bit × 1ch Operating frequency: 40MHz	16-bit × 1ch Operating frequency: 32MHz
Real-time Clock	1ch	1ch

Table 6-3. Timer RDe Functions of RL78/F23, F24

Timer RDe Features		RL78/F23, F24 Timer RDe
Input capture function		Same as RL78/F13, F14
Output compare function		Same as RL78/F13, F14
PWM function	Reset synchronous PWM mode	Same as RL78/F13, F14
	Complementary PWM mode	Same as RL78/F13, F14
	PWM3 mode	Same as RL78/F13, F14
	Extended PWM mode	**Dithering function, Gate function, Reset start function**
	Extended complementary PWM mode	**Asymmetric PWM pulse control, Interrupt and A/D trigger signal decimation function**
PWM output forced cutoff function		**PWMOPA**
A/D trigger		The following A/D trigger signals have been added from RL78/F13, F14. • **INTTRD0_IFA, INTTRD1_IFA, INTTRD1_IFB, INTTDR1_UDF, INTTRD_ADTRG**

Key Points for Porting:

- **Difference in the number of timer channels**

  The number of timer channels is the same for RL78/F23 and RL78/F13, and RL78/F24 product and RL78/F14 product. Set the count register and clock source of each timer as the maximum operating frequency of RL78/F23, F24 products are expanded.

- **Timer RDe extended functionality**

  Timer RDe of RL78/F23, F24 products extends the function from Timer RD of RL78/F13, F14 products. Extended complementary PWM mode (synchronous/asynchronous three-phase PWM output), extended PWM mode (with dithering/gate, and counter reset input function), and PWM forced cutoff circuit (PWMOPA) have been added while maintaining the conventional specifications. Moreover, the resolution of a timer is improved by expanding the maximum operating frequency.

7. Serial Interfaces

RL78/F24 implements RS-CANFD lite module corresponding to CAN-FD communication. Tables below show the differences between RL78/F23, F24 products and RL78/F13, F14 products serial I/F.

Table 7-1. Serial I/F of RL78/F24, Compared with RL78/F14

Serial I/F	RL78/F24	RL78/F14
Serial Array Unit (SAU)	CSI/Simplified-I²C/UART: 4ch/4ch/2ch	CSI/Simplified-I²C/UART: 4ch/4ch/2ch
Multimaster I²C (IICA)	1ch	1ch
LIN/UART module (RLIN3)	2ch	2ch
CAN interface	RS-CANFD lite: 1ch	RS-CAN lite: 1ch

Table 7-2. Serial I/F of RL78/F23, Compared with RL78/F13

Serial I/F	RL78/F23	RL78/F13
Serial Array Unit (SAU)	CSI/Simplified-I²C/UART: 4ch/4ch/2ch	CSI/Simplified-I²C/UART: 4ch/4ch/2ch
Multimaster I²C (IICA)	1ch	1ch
LIN/UART module (RLIN3)	1ch	1ch
CAN interface	-	-

Table 7-3. CAN Interface Differences of RL78/F24 Compared with RL78/F14

Item	RL78/F24	RL78/F14
Module name	RS-CANFD lite	RS-CAN lite
Protocol	ISO11898-1(2015) compliant Using CAN-FD frames is selectable by switching interface modes.	ISO11898-1 compliant
Communication speed	・Classical CAN only mode Maximum 1 Mbps ・CAN-FD mode and CAN-FD only mode Data bit rate: max.5 Mbps	・Classical CAN only mode Maximum 1 Mbps
Buffer	20 buffers in total ・Individual buffers: 4 buffers (4 buffers for one channel ・Shared buffers: 16 buffers ・CAN RAM ECC included	20 buffers in total ・Individual buffers: 4 buffers (4 buffers for one channel) ・Shared buffers: 16 buffers
Interrupt source	8 sources ・Global (3 sources) Added: CAN global RXMB receive interrupt ・Channel (3 sources/channel) ・Wakeup detection ・CAN RAM ECC detection	6 sources ・Global (2 sources) ・Channel (3 sources/channel) ・Wakeup detection
CAN clock source	Selects the clock obtained by frequency-f_{CLK} or the X1 clock (f_X).	Selects the clock obtained by frequency-f_{CLK} or the X1 clock (f_X).
Test function	Test function for user evaluation ・Basic test mode ・Listen-only mode ・Self-test mode 0 (external loopback) ・Self-test mode 1 (internal loopback) ・Restricted operation mode	Test function for user evaluation ・Listen-only mode ・Self-test mode 0 (external loopback) ・Self-test mode 1 (internal loopback)

Key Points for Porting:

- **Difference in the number of Serial I/F channels**

  The number of serial I/F channels is the same for RL78/F23 and RL78/F13, and RL78/F24 product and RL78/F14 product. Set the communication baud rate clock of each serial I/F module as the maximum operating frequency of RL78/F23, F24 products are expanded.

- **CAN-FD module**

  When using RS-CANFD lite function, be sure to set the clock to the "$f_{MP}/2 = f_{CLK} \geq f_{CAN}$" condition (Setting example: f_{MP} = 80MHz, f_{CLK} = 40MHz, f_{CAN} = 40MHz). In RS-CANFD lite module, the register is window type because it corresponds to 64 payloads. Select a window to access the corresponding register.

8. Analog Functions

RL78/F23, F24 products implement A/D converter, D/A converter, and comparator as analog functions. D/A converter has no difference between RL78/F24 and RL78/F14. This section describes the differences between RL78/F23, F24 products and RL78/F13, F14 products for A/D converter and comparator. Note that D/A converter and comparator are implemented only for RL78/F24 and RL78/F14.

8.1 A/D Converter

The table below shows differences between RL78/F23, F24 products and RL78/F13, F14 products A/D converter.

Table 8-1. A/D Converter of RL78/F23, F24, Compared with RL78/F13, F14

A/D Converter Features	RL78/F23, F24	RL78/F13, F14
Resolution	12 bits	10 bits
Analog input channels	31ch/25ch/24ch/19ch/10ch High-speed channels: ANI0 to ANI15 Normal-speed channels: ANI16 to ANI30	31ch/25ch/20ch/18ch/10ch
Expansion input channels	• Internal reference voltage (V_{BGR})	• Internal reference voltage (V_{BGR}) • Internal temperature sensor
Operating modes	• Single scan mode • Continuous scan mode • Group scan mode (group A and B)	• One-shot conversion mode • Sequential conversion mode
A/D trigger	• Software trigger • Hardware trigger	• Software trigger • Hardware trigger (no-wait or wait mode)
Interrupt	• INTAD (A/D conversion end) • INTADGB (group B A/D conversion end)	• INTAD (A/D conversion end)
Others	Channel-dedicated S&H circuit (ANI1, ANI2)	-
	Sampling state cycle setting for each channel	-
	Self-diagnosis mode (ANin=Vref, Vref/2, 0)	Self-diagnosis mode (ANin=Vref, 0)
	Addition/Average operation mode	-
	Disconnection detection assist function	Self-diagnosis mode

Key Points for Porting:

- **Difference in the number of analog input channels**

  The number of analog input channels is the same or extended for RL78/F23 and RL78/F13, and RL78/F24 and RL78/F14, respectively. In addition, ANI1 and ANI2 implement channel dedicated sample & hold circuit and can be sampled at the same time by hardware trigger input. Use ANI0 to ANI15 analog input channels when fast A/D conversion time and high accuracy are required.

- **A/D data register**

  RL78/F23, F24 products A/D data registers (stores A/D conversion result) are implemented for each channel. In addition, the A/D data register can be right-aligned (store in bits 0 to 11) or left-aligned (store in bits 4 to 15) when storing the A / D conversion result.

- **A/D-related register**

  In RL78/F23, F24 A/D module, the register is window type. Select a window to access the corresponding register. A/D data register from ANI0 to ANI7 can be accessed as mirror register without setting the window. Software processing can be reduced by preferentially using the ANI0 to ANI7 inputs.

8.2 Comparator (RL78/F24 Only)

The table below shows the differences between RL78/F24 and RL78/F14 comparator.

Table 8-2. Comparator Function Differences of RL78/F24, Compared with RL78/F14

Function		RL78/F24	RL78/F14
Port Control Register		PMC8	ADPC
Comparator Input Port	IVCMP00	P82 / ANI2 / IVCMP00	P81 / ANI3 / IVCMP00
	IVCMP01	P83 / ANI3 / IVCMP01	P82 / ANI4 / IVCMP01
	IVCMP02	P84 / ANI4 / IVCMP02	P83 / ANI5 / IVCMP02
	IVCMP03	P85 / ANI5 / IVCMP03 / IVREF0	P84 / ANI6 / IVCMP03
	IVREF0		P85 / ANI7 / IVREF0

Key Points for Porting:

- **Difference in the comparator input pins**

  RL78/F24 does not implement the comparator input on P81 pin. Also, when P85/IVREF0 input is used, the input of IVCMP03 cannot be used at the same time. Be caution of pin assignments when using comparator function.

9. Safety Functions

The table below shows the differences between RL78/F23, F24 products and RL78/F13, F14 products safety functions.

Table 9-1. Safety Function Differences of RL78/F23, F24, Compared with RL78/F13, F14

Safety Features	RL78/F23, F24	RL78/F13, F14
Window watchdog timer	Same as RL78/F13, F14	with WWDT
Illegal instruction execution detection function	Same as RL78/F13, F14	with illegal instruction detection
Flash memory CRC operation function	Same as RL78/F13, F14	with Flash memory CRC
General-purpose CRC function	Same as RL78/F13, F14	with general-purpose CRC
RAM ECC (1-bit correction/ 2-bit detection)	Same as RL78/F13, F14	with RAM ECC
Invalid memory access detection function	Same as RL78/F13, F14, added RAM start address setting register	with invalid memory access detection
Frequency detection function	Same as RL78/F13, F14	with frequency detection
Clock monitor function	Added self-diagnosis mode from RL78/F13, F14	with clock monitor function
Stack pointer monitor function	Same as RL78/F13, F14	with stack pointer monitor
I/O port output level detection function	Same as RL78/F13, F14	with output port monitoring function
A/D test function	Disconnection assist (pre-charge/discharge → Target pin A/D conversion) Self-diagnosis (VREF, VREF/2, 0V)	Disconnection assist (VREFL A/D conversion → Target pin A/D conversion) Self-diagnosis (VREFH, VREFL)
SFR, RAM guard function	Same as RL78/F13, F14, added RAM start address setting register	with memory guard function
Code Flash memory ECC function	Yes (1-bit correction, bit error detection, accumulation error detection)	No
CAN RAM ECC (1-bit correction / 2-bit detection)	Yes (only RL78/F24 product)	No

9.1 Memory Guard Function

The table below shows the differences between RL78/F23, F24 products and RL78/F13, F14 products memory guard function.

Table 9-2. SFR Guard Function of RL78/F23, F24, Compared with RL78/F13, F14

SFR Guard Function	RL78/F23, F24	RL78/F13, F14
	Guarded SFRs	Guarded SFRs
Port function SFR guard controlled by IAWCTL.GPORT bit	PMxx, PUxx, PIMxx, POMxx, PMCxx, PITHLxx, PIORx Note	PMxx, PUxx, PIMxx, POMxx, PMCxx, PITHLxx, PIORx Note
		ADPC
Interrupt function SFR guard controlled by IAWCTL.GINT bit	IFxx, MKxx, PRxx, EGPx, EGNx	IFxx, MKxx, PRxx, EGPx, EGNx
Clock control function SFR guard controlled by IAWCTL.GCSC bit	CMC, CSC, OSTS, CKC, PERx, OSMC, LVIM, LVIS, CANCKSEL, LINCKSEL, CKSEL, PLLCTL, MDIV, RTCCL, POCRES, STPSTC	CMC, CSC, OSTS, CKC, PERx, OSMC, LVIM, LVIS, CANCKSEL, LINCKSEL, CKSEL, PLLCTL, MDIV, RTCCL, POCRES, STPSTC
	CLMTES, ADCKS	

Note. Pxx (Port register) is not guarded.

Key Points for Porting:

- **Difference in SFR guard function**

  As shown in the table above, some registers have been added and some have been deleted.

10. Other Features

10.1 ELC (RL78/F24 Only)

Tables below show the differences between RL78/F24 and RL78/F14 ELC function.

Table 10-1. ELC Functions of RL78/F24, Compared with RL78/F14

Event	Event Source Trigger	Trigger Control Register	RL78/F24	RL78/F14
INTP0	INTP0 (Pin edge detection)	ELSELR00	○	○
INTP1	INTP1 (Pin edge detection)	ELSELR01	○	○
INTP2	INTP2 (Pin edge detection)	ELSELR02	○	○
INTP3	INTP3 (Pin edge detection)	ELSELR03	○	○
INTP4	INTP4 (Pin edge detection)	ELSELR04	○	○
INTP5	INTP5 (Pin edge detection)	ELSELR05	○	○
INTKR	INTKR (Key return function interrupt)	ELSELR06	○	○
INTRTC	INTRTC (RTC function interrupt)	ELSELR07	○	○
INTTRD0	INTTRD0_IFA (Timer RD0 interrupt)	ELSELR08	○	○
INTTRD0	INTTRD0_IFB (Timer RD0 interrupt)	ELSELR09	○	○
INTTRD1	INTTRD1_IFA (Timer RD1 interrupt)	ELSELR10	○	○
INTTRD1	INTTRD1_IFB (Timer RD1 interrupt)	ELSELR11	○	○
INTTRD1	INTTRD1_UDF (Timer RD1 interrupt)	ELSELR12	○	○
INTTRJ0	INTTRJ0 (Timer RJ0 interrupt)	ELSELR13	○	○
INTTM00	INTTM00 (TAU0 ch0 interrupt)	ELSELR14	○	○
INTTM01	INTTM01 (TAU0 ch1 interrupt)	ELSELR15	○	○
INTTM02	INTTM02 (TAU0 ch2 interrupt)	ELSELR16	○	○
INTTM03	INTTM03 (TAU0 ch3 interrupt)	ELSELR17	○	○
INTTM04	INTTM04 (TAU0 ch4 interrupt)	ELSELR18	○	○
INTCMP0	INTCMP0 (Comparator detection)	ELSELR19	○	○
INTTM05	INTTM05 (TAU0 ch5 interrupt)	ELSELR20	○	○
INTTM06	INTTM06 (TAU0 ch6 interrupt)	ELSELR21	○	○
INTTM07	INTTM07 (TAU0 ch7 interrupt)	ELSELR22	○	○
INTTM10	INTTM10 (TAU1 ch0 interrupt)	ELSELR23	○	○
INTTM11	INTTM11 (TAU1 ch1 interrupt)	ELSELR24	○	○
INTTM12	INTTM12 (TAU1 ch2 interrupt)	ELSELR25	○	○

Table 10-2. ELC Functions of RL78/F24, Compared with RL78/F14 (Link Destination)

Link Destination Function	Operation	ELSELRn[3:0]	RL78/F24	RL78/F14
A/D Converter	A/D conversion starts	0001B	○	○
TAU0 channel.0	Delay counter. Input pulse interval measurement.	0010B	○	○
TAU0 channel.1	Delay counter. Input pulse interval measurement.	0011B	○	○
Timer RJ	Count source for Timer RJ	0100B	○	○
Timer RD 0	TRDIOD0 input capture. Pulse output cutoff	0101B	○	○
Timer RD 1	TRDIOD1 input capture. Pulse output cutoff	0110B	○	○
D/A Converter	DA0 real-time output	0111B	○	○
TAU0 channel.2	Delay counter. Input pulse interval measurement.	1000B	○	○
TAU0 channel.3	Delay counter. Input pulse interval measurement.	1001B	○	○
PWMOPA	Pulse output cutoff	1010B	○	-

Key Points for Porting:

- **Difference in ELC function**

  PWMOPA (Timer RDe PWM pulse forced cutoff function) has been added to link destination function.

10.2 AAU (Application Accelerator Unit)

The table below describes the AAU function added in RL78/F23, F24 products.

Table 10-3. AAU Functions of RL78/F23, F24

No.	AAU Algorithm Mode	Data Type	Execution Time Note 1	RL78/ F23, F24	RL78/ F13, F14
1	Sine operation	Input, Output: 16-bit (integer)	1 clock	○	-
2	Cosine operation	Input, Output: 16-bit (integer)	1 clock	○	-
3	Clarke and Park transformation (for FOC controls) Note 2	Input, Output: 16-bit (integer)	7 clocks	○	-
4	Inverse Park (I-Park) transformation (for FOC controls)	Input, Output: 16-bit (integer)	6 clocks	○	-
5	Inverse Clarke (I-Clarke) transformation (for FOC controls) Note 2	Input, Output: 16-bit (integer)	5 clocks	○	-
6	PI control for motor (for FOC controls)	Input, Output: 16-bit (integer)	15 clocks	○	-
7	Clarke & Park transformation and PI control for motor (for FOC controls) Note 2	Input, Output: 16-bit (integer)	22 clocks	○	-
8	I-Park & I-Clarke transformation (for FOC controls) Note 2	Input, Output: 16-bit (integer)	11 clocks	○	-
9	PI control for DC/DC control	Input, Output: 16-bit (integer)	6 clocks / ch	○	-
10	Multiply: 32-bit × 32-bit = 64-bit	Input: 32-bit (integer), Output: 64-bit (integer)	5 clocks	○	-

Notes 1. If STM=1 (Software trigger), the execution time is added by 1 cycle.
2. The AAU supports both algorithms, power invariant transformation and amplitude invariant transformation.

Key Points for Porting:

- **AAU function**

  AAU is a new function added in RL78/F23, F24 products. By using this function, software processing such as 32-bit multiplication can execute faster than RL78/F13, F14 products.

11. Interrupt

RL78/F23, F24 products add some interrupt sources compared to RL78/F13, F14 product. Tables below show the differences between RL78/F23, F24 products and RL78/F13, F14 products interrupt source.

Table 11-1. Interrupt Functions of RL78/F24, Compared with RL78/F14 (1/2)

Vector Address	Interrupt Factor	RL78/F24					RL78/F14				
		100 QFP	80 QFP	64 QFP	48 QFP	32 QFN	100 QFP	80 QFP	64 QFP	48 QFP	32 QFN
0000H	RESET/POR/LVD/WDT/TRAP/IAW/CLM	○	○	○	○	○	○	○	○	○	○
0002H	Reserved	-	-	-	-	-	-	-	-	-	-
0004H	INTWDTI (Watchdog timer interval)	○	○	○	○	○	○	○	○	○	○
0006H	INTLVI (Voltage detection)	○	○	○	○	○	○	○	○	○	○
0008H	INTP0 (Pin edge detection)	○	○	○	○	○	○	○	○	○	○
000AH	INTP1 (Pin edge detection)	○	○	○	○	○	○	○	○	○	○
000CH	INTP2 (Pin edge detection)	○	○	○	○	○	○	○	○	○	○
000EH	INTP3 (Pin edge detection)	○	○	○	○	○	○	○	○	○	○
0010H	INTP4 (Pin edge detection)	○	○	○	○	○	○	○	○	○	○
	INTSPM (Stack pointer overflow / underflow)	○	○	○	○	○	○	○	○	○	○
0012H	INTP5 (Pin edge detection)	○	○	○	○	○	○	○	○	○	○
	INTCMP0 (Comparator detection)	○	○	○	○	○	○	○	○	○	○
0014H	INTP13 (Pin edge detection)	○	○	-	-	-	○	○	-	-	-
	INTCLM (PLL clock stop detection)	○	○	○	○	○	○	○	○	○	○
0016H	INTST0/INTCSI00/INTIIC00 (SAU0 ch0 interrupt)	○	○	○	○	○	○	○	○	○	○
0018H	INTSR0/INTCSI01/INTIIC01 (SAU0 ch1 interrupt)	○	○	○	○	○	○	○	○	○	○
001AH	INTTRD0 (Timer RD0 interrupt)	○	○	○	○	○	○	○	○	○	○
001CH	INTTRD1 (Timer RD1 interrupt)	○	○	○	○	○	○	○	○	○	○
001EH	INTTRJ0 (Timer RJ0 interrupt)	○	○	○	○	○	○	○	○	○	○
0020H	INTRAM (RAM ECC detection)	○	○	○	○	○	○	○	○	○	○
0022H	INTLIN0TRM (LIN0 transmission)	○	○	○	○	○	○	○	○	○	○
0024H	INTLIN0RVC (LIN0 reception)	○	○	○	○	○	○	○	○	○	○
0026H	INTLIN0STA/INTLIN0 (LIN0 interrupt)	○	○	○	○	○	○	○	○	○	○
0028H	INTIICA0 (Multimaster I2C interrupt)	○	○	○	○	○	○	○	○	○	○
002AH	INTP8 (Pin edge detection)	○	○	○	○	-	○	○	○	○	-
	INTRTC (RTC interrupt)	○	○	○	○	○	○	○	○	○	○
002CH	INTTM00 (TAU0 ch0 interrupt)	○	○	○	○	○	○	○	○	○	○
002EH	INTTM01 (TAU0 ch1 interrupt)	○	○	○	○	○	○	○	○	○	○
0030H	INTTM02 (TAU0 ch2 interrupt)	○	○	○	○	○	○	○	○	○	○
0032H	INTTM03 (TAU0 ch3 interrupt)	○	○	○	○	○	○	○	○	○	○
0034H	INTAD (A/D interrupt)	○	○	○	○	○	○	○	○	○	○
0036H	INTP6 (Pin edge detection)	○	○	○	○	-	○	○	○	○	-
	INTTM11H (TAU1 ch1 8-bit timer interrupt)	○	○	○	○	○	○	○	○	○	○
0038H	INTP7 (Pin edge detection)	○	○	○	○	-	○	○	○	○	-
	INTTM13H (TAU1 ch3 8-bit timer interrupt)	○	○	○	○	○	○	○	○	○	○
003AH	INTP9 (Pin edge detection)	○	○	○	○	-	○	○	○	○	-
	INTTM01H (TAU0 ch1 8-bit timer interrupt)	○	○	○	○	○	○	○	○	○	○
003CH	INTP10 (Pin edge detection)	○	○	○	-	-	○	○	○	-	-
	INTTM03H (TAU0 ch3 8-bit timer interrupt)	○	○	○	○	○	○	○	○	○	○
003EH	INTST1/INTCSI10/INTIIC10 (SAU1 ch0 interrupt)	○	○	○	○	○	○	○	○	○	○

Table 11-1. Interrupt Functions of RL78/F24, Compared with RL78/F14 (2/2)

Vector Address	Interrupt Factor	RL78/F24					RL78/F14				
		100 QFP	80 QFP	64 QFP	48 QFP	32 QFN	100 QFP	80 QFP	64 QFP	48 QFP	32 QFN
0040H	INTSR1 (SAU1 UART reception interrupt)	○	○	○	○	○	○	○	○	○	○
	INTCSI11/INTIIC11 (SAU1 ch1 interrupt)	○	○	○	○	-	○	○	○	○	-
0042H	INTTM04 (TAU0 ch4 interrupt)	○	○	○	○	○	○	○	○	○	○
0044H	INTTM05 (TAU0 ch5 interrupt)	○	○	○	○	○	○	○	○	○	○
0046H	INTTM06 (TAU0 ch6 interrupt)	○	○	○	○	○	○	○	○	○	○
0048H	INTTM07 (TAU0 ch7 interrupt)	○	○	○	○	○	○	○	○	○	○
004AH	INTP11 (Pin edge detection)	○	○	○	-	-	○	○	○	-	-
	INTLIN0WUP (LIN0 wakeup interrupt)	○	○	○	○	○	○	○	○	○	○
004CH	INTKR (Key return function interrupt)	○	○	○	○	○	○	○	○	○	○
	INTRCAN0RVC (CAN0 channel receive interrupt)	○	○	○	○	○	-	-	-	-	-
004EH	INTRCAN0ERR (CAN0 channel error interrupt)	○	○	○	○	○	○	○	○	○	○
0050H	INTRCAN0WUP (CAN0 wakeup interrupt)	○	○	○	○	○	○	○	○	○	○
0052H	INTRCAN0CFR (CAN0 transmit/ receive FIFO receive interrupt)	○	○	○	○	○	○	○	○	○	○
0054H	INTRCAN0TRM (CAN0 channel transmit interrupt)	○	○	○	○	○	○	○	○	○	○
0056H	INTRCANGRFR (CAN0 global receive FIFO interrupt)	○	○	○	○	○	○	○	○	○	○
0058H	INTRCANGERR (CAN0 global error interrupt)	○	○	○	○	○	○	○	○	○	○
005AH	INTTM10 (TAU1 ch0 interrupt)	○	○	○	○	○	○	○	○	○	○
005CH	INTTM11 (TAU1 ch1 interrupt)	○	○	○	○	○	○	○	○	○	○
005EH	INTTM12 (TAU1 ch2 interrupt)	○	○	○	○	○	○	○	○	○	○
0060H	INTTM13 (TAU1 ch3 interrupt)	○	○	○	○	○	○	○	○	○	○
0062H	Reserved	-	-	-	-	-	-	-	-	-	-
0064H	INTP12 (Pin edge detection)	○	○	○	-	-	○	○	○	-	-
	INTLIN1WUP (LIN1 wakeup interrupt)	○	○	○	○	○	○	○	○	○	○
0066H	INTLIN1TRM (LIN1 transmission interrupt)	○	○	○	○	○	○	○	○	○	○
0068H	INTLIN1RVC (LIN1 reception interrupt)	○	○	○	○	○	○	○	○	○	○
006AH	INTLIN1STA/INTLIN1 (LIN1 interrupt)	○	○	○	○	○	○	○	○	○	○
006CH	INTTM14 (TAU1 ch4 interrupt)	○	○	○	○	○	○	○	○	○	○
006EH	INTTM15 (TAU1 ch5 interrupt)	○	○	○	○	○	○	○	○	○	○
0070H	INTTM16 (TAU1 ch6 interrupt)	○	○	○	○	○	○	○	○	○	○
0072H	INTTM17 (TAU1 ch7 interrupt)	○	○	○	○	○	○	○	○	○	○
0074H	Reserved	-	-	-	-	-	-	-	-	-	-
0076H	Reserved	-	-	-	-	-	-	-	-	-	-
0078H	INTADGB (A/D (group-B) interrupt)	○	○	○	○	○	-	-	-	-	-
007AH	INTCRAM (RAM for RS-CANFD lite ECC 1-bit / 2-bit error detection)	○	○	○	○	○	-	-	-	-	-
007CH	INTROM (Code Flash bit error detection)	○	○	○	○	○	-	-	-	-	-
007EH	BRK (BRK instruction interrupt)	○	○	○	○	○	○	○	○	○	○

Table 11-2. Interrupt Functions of RL78/F23, Compared with RL78/F13 (1/2)

Vector Address	Interrupt Factor	RL78/F23				RL78/F13			
		80 QFP	64 QFP	48 QFP	32 QFN	80 QFP	64 QFP	48 QFP	32 QFN
0000H	RESET/POR/LVD/WDT/TRAP/IAW/CLM	○	○	○	○	○	○	○	○
0002H	Reserved	-	-	-	-	-	-	-	-
0004H	INTWDTI (Watchdog timer interval)	○	○	○	○	○	○	○	○
0006H	INTLVI (Voltage detection)	○	○	○	○	○	○	○	○
0008H	INTP0 (Pin edge detection)	○	○	○	○	○	○	○	○
000AH	INTP1 (Pin edge detection)	○	○	○	○	○	○	○	○
000CH	INTP2 (Pin edge detection)	○	○	○	○	○	○	○	○
000EH	INTP3 (Pin edge detection)	○	○	○	○	○	○	○	○
0010H	INTP4 (Pin edge detection)	○	○	○	○	○	○	○	○
	INTSPM (Stack pointer overflow / underflow)	○	○	○	○	○	○	○	○
0012H	INTP5 (Pin edge detection)	○	○	○	○	○	○	○	○
	INTCMP0 (Comparator detection)	-	-	-	-	-	-	-	-
0014H	INTP13 (Pin edge detection)	○	-	-	-	○	-	-	-
	INTCLM (PLL clock stop detection)	○	○	○	○	○	○	○	○
0016H	INTST0/INTCSI00/INTIIC00 (SAU0 ch0 interrupt)	○	○	○	○	○	○	○	○
0018H	INTSR0/INTCSI01/INTIIC01 (SAU0 ch1 interrupt)	○	○	○	○	○	○	○	○
001AH	INTTRD0 (Timer RD0 interrupt)	○	○	○	○	○	○	○	○
001CH	INTTRD1 (Timer RD1 interrupt)	○	○	○	○	○	○	○	○
001EH	INTTRJ0 (Timer RJ0 interrupt)	○	○	○	○	○	○	○	○
0020H	INTRAM (RAM ECC detection)	○	○	○	○	○	○	○	○
0022H	INTLIN0TRM (LIN0 transmission)	○	○	○	○	○	○	○	○
0024H	INTLIN0RVC (LIN0 reception)	○	○	○	○	○	○	○	○
0026H	INTLIN0STA/INTLIN0 (LIN0 interrupt)	○	○	○	○	○	○	○	○
0028H	INTIICA0 (Multimaster I2C interrupt)	○	○	○	○	○	○	○	○
002AH	INTP8 (Pin edge detection)	○	○	○	-	○	○	○	-
	INTRTC (RTC interrupt)	○	○	○	○	○	○	○	○
002CH	INTTM00 (TAU0 ch0 interrupt)	○	○	○	○	○	○	○	○
002EH	INTTM01 (TAU0 ch1 interrupt)	○	○	○	○	○	○	○	○
0030H	INTTM02 (TAU0 ch2 interrupt)	○	○	○	○	○	○	○	○
0032H	INTTM03 (TAU0 ch3 interrupt)	○	○	○	○	○	○	○	○
0034H	INTAD (A/D interrupt)	○	○	○	○	○	○	○	○
0036H	INTP6 (Pin edge detection)	○	○	○	-	○	○	○	-
	INTTM11H (TAU1 ch1 8-bit timer interrupt)	○	○	○	○	○	○	○	○
0038H	INTP7 (Pin edge detection)	○	○	○	-	○	○	○	-
	INTTM13H (TAU1 ch3 8-bit timer interrupt)	○	○	○	○	○	○	○	○
003AH	INTP9 (Pin edge detection)	○	○	○	-	○	○	○	-
	INTTM01H (TAU0 ch1 8-bit timer interrupt)	○	○	○	○	○	○	○	○
003CH	INTP10 (Pin edge detection)	○	○	-	-	○	○	-	-
	INTTM03H (TAU0 ch3 8-bit timer interrupt)	○	○	○	○	○	○	○	○
003EH	INTST1/INTCSI10/INTIIC10 (SAU1 ch0 interrupt)	○	○	○	○	○	○	○	○

Table 11-2. Interrupt Functions of RL78/F23, Compared with RL78/F13 (2/2)

Vector Address	Interrupt Factor	RL78/F23				RL78/F13			
		80 QFP	64 QFP	48 QFP	32 QFN	80 QFP	64 QFP	48 QFP	32 QFN
0040H	INTSR1 (SAU1 UART reception interrupt)	○	○	○	○	○	○	○	○
	INTCSI11/INTIIC11 (SAU1 ch1 interrupt)	○	○	○	-	○	○	○	-
0042H	INTTM04 (TAU0 ch4 interrupt)	○	○	○	○	○	○	○	○
0044H	INTTM05 (TAU0 ch5 interrupt)	○	○	○	○	○	○	○	○
0046H	INTTM06 (TAU0 ch6 interrupt)	○	○	○	○	○	○	○	○
0048H	INTTM07 (TAU0 ch7 interrupt)	○	○	○	○	○	○	○	○
004AH	INTP11 (Pin edge detection)	○	○	-	-	○	○	-	-
	INTLIN0WUP (LIN0 wakeup interrupt)	○	○	○	○	○	○	○	○
004CH	INTKR (Key return function interrupt)	○	○	○	○	○	○	○	○
	INTRCAN0RVC (CAN0 channel receive interrupt)	-	-	-	-	-	-	-	-
004EH	INTRCAN0ERR (CAN0 channel error interrupt)	-	-	-	-	-	-	-	-
0050H	INTRCAN0WUP (CAN0 wakeup interrupt)	-	-	-	-	-	-	-	-
0052H	INTRCAN0CFR (CAN0 transmit/ receive FIFO receive interrupt)	-	-	-	-	-	-	-	-
0054H	INTRCAN0TRM (CAN0 channel transmit interrupt)	-	-	-	-	-	-	-	-
0056H	INTRCANGRFR (CAN0 global receive FIFO interrupt)	-	-	-	-	-	-	-	-
0058H	INTRCANGERR (CAN0 global error interrupt)	-	-	-	-	-	-	-	-
005AH	INTTM10 (TAU1 ch0 interrupt)	○	○	○	○	○	○	○	○
005CH	INTTM11 (TAU1 ch1 interrupt)	○	○	○	○	○	○	○	○
005EH	INTTM12 (TAU1 ch2 interrupt)	○	○	○	○	○	○	○	○
0060H	INTTM13 (TAU1 ch3 interrupt)	○	○	○	○	○	○	○	○
0062H	Reserved	-	-	-	-	-	-	-	-
0064H	INTP12 (Pin edge detection)	○	○	-	-	○	○	-	-
	INTLIN1WUP (LIN1 wakeup interrupt)	-	-	-	-	-	-	-	-
0066H	INTLIN1TRM (LIN1 transmission interrupt)	-	-	-	-	-	-	-	-
0068H	INTLIN1RVC (LIN1 reception interrupt)	-	-	-	-	-	-	-	-
006AH	INTLIN1STA/INTLIN1 (LIN1 interrupt)	-	-	-	-	-	-	-	-
006CH	INTTM14 (TAU1 ch4 interrupt)	-	-	-	-	-	-	-	-
006EH	INTTM15 (TAU1 ch5 interrupt)	-	-	-	-	-	-	-	-
0070H	INTTM16 (TAU1 ch6 interrupt)	-	-	-	-	-	-	-	-
0072H	INTTM17 (TAU1 ch7 interrupt)	-	-	-	-	-	-	-	-
0074H	Reserved	-	-	-	-	-	-	-	-
0076H	Reserved	-	-	-	-	-	-	-	-
0078H	INTADGB (A/D (group-B) interrupt)	○	○	○	○	-	-	-	-
007AH	INTCRAM (RAM for RS-CANFD lite ECC 1-bit / 2-bit error detection)	-	-	-	-	-	-	-	-
007CH	INTROM (Code Flash bit error detection)	○	○	○	○	-	-	-	-
007EH	BRK (BRK instruction interrupt)	○	○	○	○	○	○	○	○

Key Points for Porting:

- **Difference in interrupt functions**

  RL78/F23, F24 products add some sources from RL78/F13, F14 products. With the addition of these functions, the related registers (IFxx, MKxx, and PRxx) have also been expanded. When using the additional interrupt, set the interrupt vector and the register related to that interrupt.

12. Standby Control

The table below shows the differences between RL78/F23, F24 products and RL78/F13, F14 products standby control.

Table 12-1. Stand-by Functions of RL78/F23, F24, Compared with RL78/F13, F14

Item		RL78/F23, F24	RL78/F13, F14
HALT mode		Yes	Yes
STOP mode		Yes	Yes
SNOOZE mode			
	LIN/UART module (RLIN3)	Yes	Yes
	A/D converter	No Use interrupt to handle with software (refer to the figure below)	Yes
	DTC	Yes	Yes

RL78/F23, F24 products do not support A/D converter in the SNOOZE mode. However, the same measures are possible as shown in the figure below.

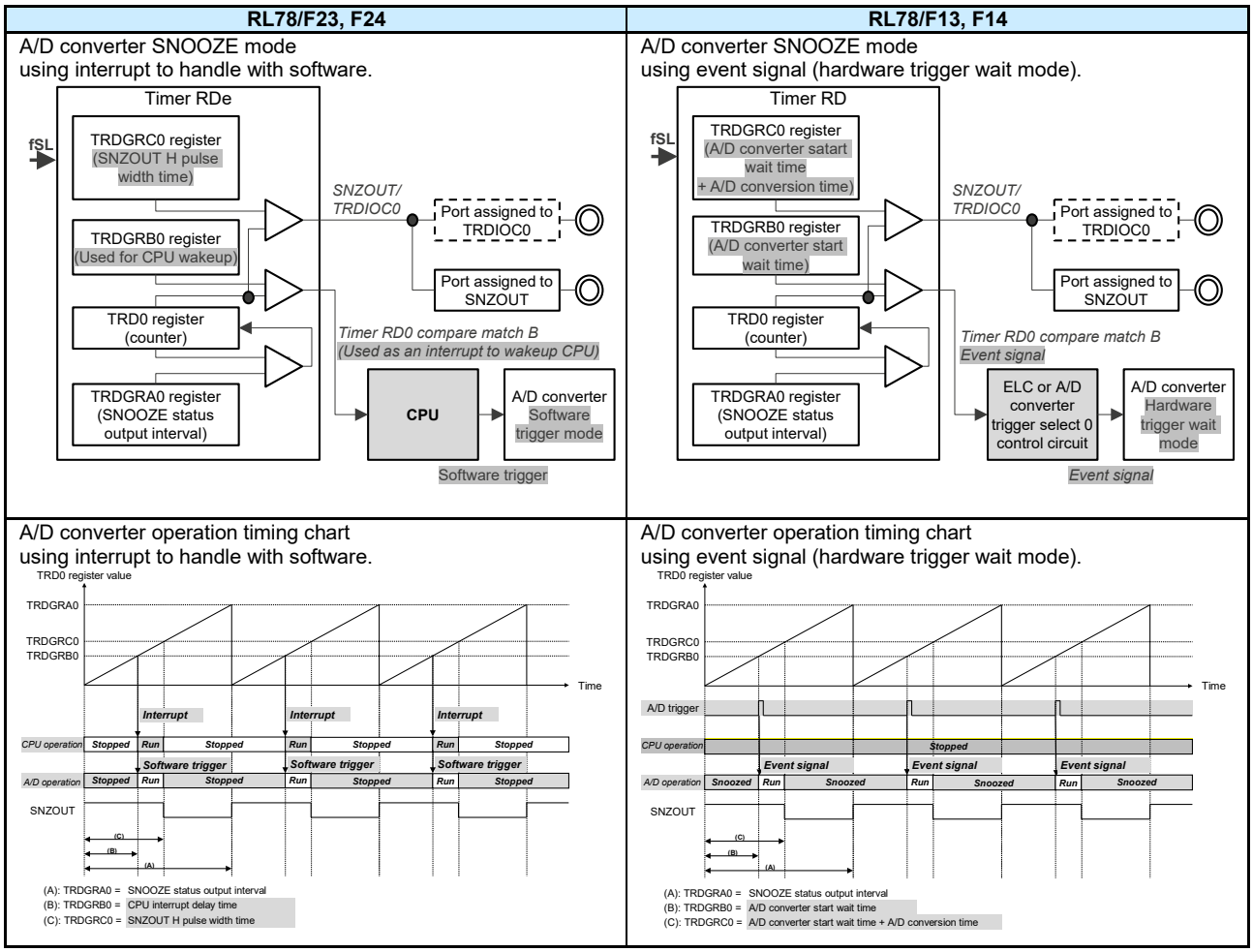


Figure 12-1. A/D Converter SNOOZE Mode of RL78/F23, F24, Compared with RL78/F13, F14

Key Points for Porting:

- **A/D conversion in SNOOZE mode**

  RL78/F23, F24 products do not support A/D conversion in the SNOOZE mode. Refer to the figure shown above when performing the same process as A/D conversion in SNOOZE mode on RL78/F23, F24 products.

13. Flash Memory

RL78/F13, F14 product used FSL (Flash Self Library) and FDL, EEL (Data Flash Library) to rewrite Flash Memory (Code/ Data Flash), but RL78/F23, F24 products use user software. The flash memory control software (RFD: Renesas Flash Drivers) will be provided in the same way as conventional products.

Key Points for Porting:

- **Flash memory rewriting**

  The flash memory control software (RFD: Renesas Flash Drivers) is provided as source code.

14. Development Environment

The table below shows the differences between RL78/F23, F24 products and RL78/F13, F14 products software development environment.

Table 14-1. Software Development Environment of RL78/F23, F24, Compared with RL78/F13, F14

Item	RL78/F23, F24	RL78/F13, F14
Integrated Development Environment / Compiler	CS+, e^2 studio / CC-RL	CS+, e^2 studio / CC-RL, CA78K0R
	Embedded Workbench / IAR Compiler	Embedded Workbench / IAR Compiler
Emulator	E2, E2 Lite	IECUBE E1, E2, E2 Lite

15. Electrical Specifications

Comparisons of the electrical characteristics of RL78/F23, F24 and RL78/F13, F14 are shown below. For details, refer to the user's manual of the target product.

15.1 Supply Current Characteristics

Shown below is comparison of supply current consumptions in each operation mode between RL78/F24 and RL78/F14, and RL78/F23 and RL78/F13.

Table 15-1. Supply Current Characteristics of RL78/F24, Compared with RL78/F14

Mode	RL78/F24		RL78/F14	
	Conditions	Supply Current Specifications	Conditions	Supply Current Specifications
Operation Mode	f_{CLK} = 40 MHz, f_{PLL} = 80 MHz, f_{MX} = 20 MHz	Grade-3: (TYP.) 10.6 mA, (MAX.) 20.0 mA Grade-4: (TYP.) 10.6 mA, (MAX.) 20.0 mA Grade-5: (TYP.) 10.6 mA, (MAX.) 21.0 mA	f_{CLK} = 32 MHz, f_{PLL} = 64 MHz, f_{MX} = 8 MHz	L-grade: (TYP.) 6.4 mA, (MAX.) 14.0 mA
			f_{CLK} = 24 MHz, f_{PLL} = 48 MHz, f_{MX} = 8 MHz	K-grade: (TYP.) 5.0 mA, (MAX.) 12.0 mA Y-grade: (TYP.) 5.0 mA, (MAX.) 12.5 mA
HALT Mode	f_{CLK} = 40 MHz, f_{PLL} = 80 MHz, f_{MX} = 20 MHz	Grade-3: (TYP.) 3.2 mA, (MAX.) 12.0 mA Grade-4: (TYP.) 3.2 mA, (MAX.) 12.0 mA Grade-5: (TYP.) 3.2 mA, (MAX.) 13.0 mA	f_{CLK} = 32 MHz, f_{PLL} = 64 MHz, f_{MX} = 8 MHz	L-grade: (TYP.) 1.1 mA, (MAX.) 10.0 mA
			f_{CLK} = 24 MHz, f_{PLL} = 48 MHz, f_{MX} = 8 MHz	K-grade: (TYP.) 0.9 mA, (MAX.) 8.0 mA Y-grade: (TYP.) 0.9 mA, (MAX.) 8.5 mA
STOP Mode	-	Grade-3: (TYP.) 0.6 µA, (MAX.) 115.0 µA Grade-4: (TYP.) 0.6 µA, (MAX.) 270.0 µA Grade-5: (TYP.) 0.6 µA, (MAX.) 700.0 µA	-	L-grade: Group D: (TYP.) 0.5 µA, (MAX.) 30.0 µA Group E: (TYP.) 0.5 µA, (MAX.) 50.0 µA K-grade: Group D: (TYP.) 0.5 µA, (MAX.) 60.0 µA Group E: (TYP.) 0.5 µA, (MAX.) 100.0 µA Y-grade: Group D: (TYP.) 0.5 µA, (MAX.) 150.0 µA Group E: (TYP.) 0.5 µA, (MAX.) 200.0 µA

Remarks: Group D products: RL78/F14 products with 30, 32, 48, 64, or 80 pins and products with 96 KB or less code flash memory.
Group E products: RL78/F14 products with 100 pins and products with 128 KB or more code flash memory.

Table 15-2. Supply Current Characteristics of RL78/F23, Compared with RL78/F13

Mode	RL78/F23		RL78/F13	
	Conditions	Supply Current Specifications	Conditions	Supply Current Specifications
Operation Mode	f_{CLK} = 40 MHz, f_{PLL} = 80 MHz, f_{MX} = 20 MHz	Grade-3: (TYP.) 9.2 mA, (MAX.) 17.0 mA Grade-4: (TYP.) 9.2 mA, (MAX.) 17.0 mA Grade-5: (TYP.) 9.2 mA, (MAX.) 18.0 mA	f_{CLK} = 32 MHz, f_{PLL} = 64 MHz, f_{MX} = 8 MHz	L-grade: (TYP.) 6.4 mA, (MAX.) 14.0 mA
			f_{CLK} = 24 MHz, f_{PLL} = 48 MHz, f_{MX} = 8 MHz	K-grade: (TYP.) 5.0 mA, (MAX.) 12.0 mA Y-grade: (TYP.) 5.0 mA, (MAX.) 12.5 mA
HALT Mode	f_{CLK} = 40 MHz, f_{PLL} = 80 MHz, f_{MX} = 20 MHz	Grade-3: (TYP.) 3.1 mA, (MAX.) 11.0 mA Grade-4: (TYP.) 3.1 mA, (MAX.) 11.0 mA Grade-5: (TYP.) 3.1 mA, (MAX.) 12.0 mA	f_{CLK} = 32 MHz, f_{PLL} = 64 MHz, f_{MX} = 8 MHz	L-grade: (TYP.) 1.1 mA, (MAX.) 10.0 mA
			f_{CLK} = 24 MHz, f_{PLL} = 48 MHz, f_{MX} = 8 MHz	K-grade: (TYP.) 0.9 mA, (MAX.) 8.0 mA Y-grade: (TYP.) 0.9 mA, (MAX.) 8.5 mA
STOP Mode	-	Grade-3: (TYP.) 0.5 µA, (MAX.) 51.0 µA Grade-4: (TYP.) 0.5 µA, (MAX.) 110.0 µA Grade-5: (TYP.) 0.5 µA, (MAX.) 300.0 µA	-	L-grade: (TYP.) 0.5 µA, (MAX.) 30.0 µA K-grade: (TYP.) 0.5 µA, (MAX.) 60.0 µA Y-grade: (TYP.) 0.5 µA, (MAX.) 150.0 µA

Table 15-3. Operation Current Characteristics of RL78/F23, F24, Compared with RL78/F13, F14

Mode	RL78/F23, F24		RL78/F13, F14	
	Conditions	Supply Current Specifications	Conditions	Supply Current Specifications
Watchdog timer	f_{WDT} = 15 kHz	Grade-3, Grade-4, Grade-5: (TYP.) 0.3 µA	f_{WDT} = 15 kHz	L-grade, K-grade, Y-grade: (TYP.) 0.22 µA
A/D converter	During conversion	Grade-3, Grade-4, Grade-5: (TYP.) 1.3 mA, (MAX.) 1.7 mA	During conversion	L-grade, K-grade, Y-grade: (TYP.) 1.3 mA, (MAX.) 1.7 mA
	Added current $AV_{REF} = V_{DD}$	Grade-3, Grade-4, Grade-5: (TYP.) 75.0 µA	Added current $AV_{REF} = V_{DD}$	L-grade, K-grade, Y-grade: (TYP.) 75.0 µA
	Added current $AV_{REF} = AV_{REFP}$, AV_{REFP} = 5.0V	Grade-3, Grade-4, Grade-5: (TYP.) 65.0 µA	-	-
	Added current Sample-and-hold circuit operation	Grade-3, Grade-4, Grade-5: (TYP.) 0.8 mA, (MAX.) 1.2 mA	-	-
LVD operation	-	Grade-3, Grade-4, Grade-5: (TYP.) 0.08 µA	-	L-grade, K-grade, Y-grade: (TYP.) 0.08 µA
D/A converter	-	Grade-3, Grade-4, Grade-5: (TYP.) 0.8 mA, (MAX.) 1.5 mA	-	L-grade, K-grade, Y-grade: (TYP.) 0.8 mA, (MAX.) 1.5 mA
Comparator	-	Grade-3, Grade-4, Grade-5: (TYP.) 50.0 µA	-	L-grade, K-grade, Y-grade: (TYP.) 50.0 µA
BGO operation	-	Grade-3, Grade-4, Grade-5: (TYP.) 2.5 mA, (MAX.) 12.2 mA	-	L-grade, K-grade, Y-grade: (TYP.) 2.5 mA, (MAX.) 12.2 mA

Key Points for Porting:

- **Supply current characteristics**

  Please design the power supply of the target system according to the power supply current specifications of the product to be used.

15.2 Pin Current Characteristics

Shown below is comparison of pin current characteristics in each parameter of RL78/F23, F24 and RL78/F13, F14.

Table 15-4. Pin Current Characteristics of RL78/F23, F24, Compared with RL78/F13, F14

Mode	RL78/F23, F24		RL78/F13, F14	
	Conditions	Pin Current Specifications	Conditions	Pin Current Specifications
Pin output current: High (IOH1)	4.0V ≤ EV_{DD} ≤ 5.5V	Grade-3: (MAX.) -5.0 mA / pin (MAX.) -50.0 mA / total of pins Grade-4: (MAX.) -5.0 mA / pin (MAX.) -42.0 mA / total of pins Grade-5: (MAX.) -5.0 mA / pin (MAX.) -32.0 mA / total of pins	4.0V ≤ EV_{DD} ≤ 5.5V	L-grade: (MAX.) -5.0 mA / pin (MAX.) -50.0 mA / total of pins K-grade: (MAX.) -5.0 mA / pin (MAX.) -42.0 mA / total of pins Y-grade: (MAX.) -5.0 mA / pin (MAX.) -32.0 mA / total of pins
	2.7V ≤ EV_{DD} < 4.0V	Grade-3, Grade-4, Grade-5: (MAX.) -3.0 mA / pin (MAX.) -29.0 mA / total of pins	2.7V ≤ EV_{DD} < 4.0V	L-grade, K-grade, Y-grade: (MAX.) -3.0 mA / pin (MAX.) -29.0 mA / total of pins
Pin output current: Low (IOL1)	4.0V ≤ EV_{DD} ≤ 5.5V	Grade-3, Grade-4: (MAX.) 8.5 mA / pin (MAX.) 65.0 mA / total of pins Grade-5: (MAX.) 8.5 mA / pin (MAX.) 55.0 mA / total of pins	4.0V ≤ EV_{DD} ≤ 5.5V	L-grade, K-grade: (MAX.) 8.5 mA / pin (MAX.) 65.0 mA / total of pins Y-grade: (MAX.) 8.5 mA / pin (MAX.) 55.0 mA / total of pins
	2.7V ≤ EV_{DD} < 4.0V	Grade-3, Grade-4: (MAX.) 4.0 mA / pin (MAX.) 50.0 mA / total of pins Grade-5: (MAX.) 4.0 mA / pin (MAX.) 45.0 mA / total of pins	2.7V ≤ EV_{DD} < 4.0V	L-grade, K-grade: (MAX.) 4.0 mA / pin (MAX.) 50.0 mA / total of pins Y-grade: (MAX.) 4.0 mA / pin (MAX.) 45.0 mA / total of pins
Pin output current: High (IOH2)	2.7V ≤ V_{DD} ≤ 5.5V	Grade-3, Grade-4, Grade-5: (MAX.) -0.1 mA / pin (MAX.) -2.0 mA / total of pins	2.7V ≤ V_{DD} ≤ 5.5V	L-grade, K-grade, Y-grade: (MAX.) -0.1 mA / pin (MAX.) -2.0 mA / total of pins
Pin output current: Low (IOL2)	2.7V ≤ V_{DD} ≤ 5.5V	Grade-3, Grade-4, Grade-5: (MAX.) 0.4 mA / pin (MAX.) 5.0 mA / total of pins	2.7V ≤ V_{DD} ≤ 5.5V	L-grade, K-grade, Y-grade: (MAX.) 0.4 mA / pin (MAX.) 5.0 mA / total of pins

Key Points for Porting:

- **Pin current characteristics**

  Pin specifications vary depending on the pin block of the product. Please refer the user's manual for details.

16. Appendix

16.1 SFR Comparison between RL78/F23, F24 Products and RL78/F13, F14 Products

This section shows SFR (Special Function Registers) comparison between RL78/F23, F24 products and RL78/F13, F14 products. For details on each register and bit, refer to the User's Manual: Hardware.

References to item in the Table 16-2 and Table 16-3, refer to chapters in the RL78/F23, F24 User's Manual: Hardware. Also, refer to "RL78/F23, F24 List of Special Function Registers (R01AN6253)" for a list by product.

This table does not show differences in operating clocks or electrical characteristics. See the User's Manual: Hardware for details on these.

Table 16-1. SFRs Newly Added in RL78/F23, F24 Products

Newly Added Features	Added SFR
RAM start addresses setting function	RAMSAR (F0076H) Changed bit specifications for GRAM[1:0] of the IAWCTL register.
Port function Analog I/O selection Expanded peripheral function pin assignment	 PMC3 (F0063H), PMC8, PMC9 (bits 0 to 5), PMC10 (F0068H, F0069H, F006AH) PIOR9 (F001FH), Added bits PITHL4.1, PITHL12.0, and POM3.2.
Clock generator HOCO (supports 40/80 MHz) PLL (supports 40/80 MHz)	 HOCODIV (bits 0 to 2) (F00A8H) CKSEL (bits 5 to 7) (F02C4H), PLLCTL (bits 1, 3, 5 to 7) (F02C5H)
Flash memory control	FLPMC, …, FLWH (F00C0H to F00CFH), FLSEC, …, FLWE (FFFB0H to FFFC6H)
Timer RDe Added modes (Extended PWM mode, Extended complementary PWM mode) Added function (PWMOPA, TRDMBK)	 TRDCMPD0, …, TRDDGCR1 (FFF60H to FFF6FH), TRDCMPB0, …, TRDEMR1 (F0280H to F029BH) OPCTL0, …, OPSR (F0248H to F024CH), TRDMBKCTL, TRDMBKCMP (F024EH, F024FH), Added bits EPWM and CPSS of the TRDFCR register. Added the UDS bit of the TRDSR1 register. Added the PWMOPEN bit of the PER1 register.
12-bit A/D Converter	ADDR0M, …, ADDR7M (F06A0H to F06AFH), ADC window registers (F06B0H to F06BFH), ADWINR (FFF30H), ADCKS (F00E0H), Added bit specification for GCSC bit of the IAWCTL register.
CAN interface (RS-CANFD lite)	C0NCFGL, …, C0FDCRCH (F0300H to F0413H), CAN0 window registers (F0420H to F067FH)
LIN/UART module (RLIN3) Added function (Break/Sync field detection, Dominant level detection in response space)	 LBSS0/1, LRSS0/1 (F06ECH, F06EEH)
Application Accelerator Unit (AAU)	AAU window registers (F02B0H to F02BFH), AAUWINR (FFF32H), Added the AAUEN bit of the PER2 register
Event Link Controller (ELC) Added PWMOPA (PWM output cutoff) as a link destination function	ELSELR00 to ELSELR25 (F0780H to F0799H)
Functional Safety • Code flash memory ECC function • CAN RAM ECC function • Clock monitor (test function)	 • CFERRCTLR, …, ERRADRH (F00B8H to F00BDH) • CFDECCTL, …, CFDECEAD (F07C0H to F07D1H) • CLMTES (F02CCH)
Interrupt function Added interruption (Code flash ECC function, CAN RAM ECC function, 12-bit ADC function, RS-CANFD lite function)	IF3H, MK3H, PR03H, PR13H (FFFD3H, FFFD6H, FFFDBH, FFFDFH) Added bits of INTRCANGRVC to registers IF2L, MK2L, PR02L, and PR12L. Changed the bit names of INTRCAN0ERR, INTRCAN0WUP, INTRCAN0CFR, INTRCAN0TRM, INTRCANGRFR, and INTRCANGERR (registers IF2L, IF2H, MK2L, MK2H, PR02L, PR02H, PR12L, and PR12H). Added bit specification for GINT bit of the IAWCTL register.
Security function	**Note.** A contract is required for the details of security function.

Table 16-2. List of SFR Differences Between RL78/F23, F24 and RL78/F13, F14

Address	RL78/F23, F24 SFR	Difference from RL78/F13, F14 product	References
FFF00H – FFF0FH	Port related registers (P0 to P15)	No difference	4.3
FFF10H – FFF13H	SAU0 related registers (SDR00, SDR01)	No difference	15.2
FFF18H – FFF1BH	TAU0 related registers (TDR00, TDR01)	No difference	6.2
FFF1EH, FFF1FH	–	(Deleted the ADCR register.)	–
FFF20H – FFF2FH	Port related registers (PM0 to PM15)	No difference	4.3
FFF30H	ADC related register (**ADWINR**)	**New**, (Deleted the ADM0 register.)	12.2
FFF31H	–	(Deleted the ADS register.)	–
FFF32H	AAU related register (**AAUWINR**)	**New**, (Deleted the ADM1 register.)	27.2
FFF34H, FFF36H	DAC related registers (DACS0, DAM)	No difference	13.3
FFF37H	Key return related register (KRM)	No difference	22.3
FFF38H – FFF3BH	External interrupt pin related registers (EGP0, EGN0, EGP1, EGN1)	No difference	21.3
FFF48H – FFF4BH	SAU1 related registers (SDR10, SDR11)	No difference	15.2
FFF50H – FFF52H	IICA0 related registers (IICA0, IICS0, IICF0)	No difference	16.2 16.3
FFF54H, FFF55H	RTC related register (SUBCUDW)	No difference	9.3
FFF58H – FFF5FH	Timer RDe related registers (TRDGRC0, TRDGRD0, TRDGRC1, TRDGRD1)	No difference (Timer RD registers). Each register has additional specifications for extended PWM mode and extended complementary PWM mode.	8.2
FFF60H – FFF6FH	Timer RDe related registers (**TRDCMPD0, …, TRDDGCR1**)	**New**, (Moved TAU0 related registers (TDR02 to TDR07).)	8.2
FFF70H – FFF73H	–	(Moved TAU1 related registers (TDR10, TDR11).)	–
FFF74H – FFF7FH	TAU0 related registers (TDR02 to TDR07)	(Moved TAU1 related registers (TDR12 to TDR17).)	6.2
FFF80H – FFF8FH	TAU1 related registers (TDR10 to TDR17)	(No register in these addresses.)	6.2
FFF92H – FFF9EH	RTC related registers (SEC, …, RTCC1)	No difference	9.3
FFFA0H – FFFA4H	OSC related registers (CMC, …, CKC)	No difference	5.3
FFFA5H	Clock/Buzzer output related register (CKS0)	No difference	10.3
FFFA8H	RESET related register (RESF)	No difference	24.1
FFFA9H, FFFAAH	LVD related registers (LVIM, LVIS)	No difference	26.3
FFFABH	WWDT related register (WDTE)	No difference	11.3
FFFACH	General purpose CRC related register (CRCIN)	No difference	28.3.2
FFFB0H – FFFC6H	Flash memory related registers (**FLSEC, …, FLWE**)	**New**	28.3.5 32.7.2
FFFD0H – FFFEFH	Interrupt related registers (IF2L, …, PR11H)	Added registers **IF3H, MK3H, PR03H, and PR13H**. Added bits related to **INTRCANGRVC** (IF2L, MK2L, PR02L, and PR12L). Changed bit names related to INTRCAN0ERR, INTRCAN0WUP, INTRCAN0CFR, INTRCAN0TRM, INTRCANGRFR, and INTRCANGERR of RS-CANFD lite.	21.3
FFFF0H – FFFF3H	MAC instruction related registers (MACRL, MACRH)	No difference	35.1.5
FFFFEH	Processor related register (PMC)	No difference	3.5

Table 16-3. List of 2nd SFR Differences Between RL78/F23, F24 and RL78/F13, F14 (1/2)

Address	RL78/F23, F24 SFR	Difference from RL78/F13, F14 product	References
F0010H – F0013H	–	(Deleted ADC related registers (ADM2, ADUL, ADLL, ADTES).)	–
F0016H – F001EH	Port related registers (PIOR0 to PIOR8)	No difference	4.3
F001FH	Port related register (**PIOR9**)	**New**	4.3
F0021H – F002FH	Port related registers (PITHL1, …, PITHL15)	Added **PITHL4.1** and **PITHL12.0** bits.	4.3
F0030H – F003FH	Port related registers (PU0, …, PU15)	(Deleted the PU9 register.)	4.3
F0041H – F004CH	Port related registers (PIM1, …, PIM12)	No difference	4.3
F0051H – F005CH	Port related registers (POM1, …, POM12)	Added the **POM3.2** bit.	4.3
F0063H – F006CH	Port related registers (PMC3, …, PMC12)	Added registers **PMC3, PMC8** and **PMC10**. Added bits **PMC9.0 to PMC9.5**.	4.3
F0070H – F0072H	Noise filter registers (NFEN0, NFEN1, NFEN2)	No difference	15.3 6.3
F0073H – F0075H	Input signals select registers (ISC, TIS0, TIS1)	No difference	15.3 17.2 6.3
F0076H	RAM address selects register (**RAMSAR**)	**New**	3.5
F0077H	Port related register (PMS)	No difference	4.3
F0078H	Safety functions related register (IAWCTL)	Changed bit specifications for **GRAM[1:0], GPORT, GINT,** and **GCSC** bits.	3.5 28.3.8
F0079H	Interrupt related register (INTFLG0)	No difference	21.3
F007AH	Input signals select register (TIS2)	No difference	6.3 9.3
F007BH	RLIN3 related register (LCHSEL)	No difference	17.2
F007CH	Interrupt related register (INTMSK)	No difference	21.3
F0090H	Data flash memory related register (DFLCTL)	No difference	32.7.2
F00A0H	HOCO related register (HIOTRM)	No difference	5.3
F00A8H	HOCO related register (HOCODIV)	Changed bit specifications for **HOCODIV[2:0]** bits.	5.3
F00B8H – F00BDH	Code flash ECC related registers (**CFERRCTLR, …, ERRADRH**)	**New**	28.3.5
F00C0H – F00CFH	Flash memory related registers (**FLPMC, …, FLWH**)	**New**	28.3.5 32.7.2
F00D8H – F00DDH	Stack pointer monitor related registers (SPMCTRL, SPOFR, SPUFR)	No difference	28.3.6
F00E0H	ADC related register (**ADCKS**)	**New**	12.2
F00F0H, F00F3H	Clock related register (PER0, OSMC)	No difference	5.3
F00FEH	BCD related register (BCDADJ)	No difference	34.2
F0100H – F0123H	SAU0 related registers (SSR00, …, SSE0)	No difference	15.3
F0140H – F0163H	SAU1 related registers (SSR10, …, SSE1)	No difference	15.3
F0180H – F01BFH	TAU0 related registers (TCR00, …, TOM0)	No difference	6.2 6.3
F01C0H – F01FFH	TAU1 related registers (TCR10, …, TOM1)	No difference	6.2 6.3
F0200H – F0207H	RAM ECC related registers (ERADR, …, ECCDWRVR)	No difference	28.3.3
F0220H	Port related register (PSRSEL)	No difference	4.3
F0222H – F0225H	SNOOZE status registers (PSNZCNT0 to PSNZCNT3)	No difference	4.3
F0227H	DAC related register (DAM2)	No difference	13.3

Table 16-3. List of 2nd SFR Differences Between RL78/F23, F24 and RL78/F13, F14 (2/2)

Address	RL78/F23, F24 SFR	Difference from RL78/F13, F14 product	References
F0228H – F022DH	PWM delay control registers (PWMDLY0, PWMDLY1, PWMDLY2)	No difference	6.3 8.2
F0230H – F0234H	IICA0 related registers (IICCTL00, …, SVA0)	No difference	16.2 16.3
F0240H – F0243H	Timer RJ0 related registers (TRJCR0, …, TRJISR0)	No difference	7.3
F0248H – F024CH	PWMOPA related registers (**OPCTL0, …, OPSR**)	**New**	8.6.2
F024EH, F024FH	TRDMBK related registers (**TRDMBKCTL, TRDMBKCMP**)	**New**	8.7.2
F0250H – F027BH	Timer RDe related registers (TRDELC, …, TRDGRB1)	(Timer RD related registers moved from address (F0260H to F028BH).) Added bits **EPWM** and **CPSS** of the TRDFCR register. Added the **UDS** bit of the TRDSR1 register. Each register has additional specifications for extended PWM mode and extended complementary PWM mode.	8.2
F0280H – F029BH	Timer RDe related registers (**TRDCMPB0, …, TRDEMR1**)	**New**	8.2
F02A0H – F02A2H	Comparator related registers (CMPCTL, CMPSEL, CMPMON)	No difference (Different pin assignments)	14.2
F02B0H – F02BFH	**AAU related registers**	**New**	27.2
F02C0H	Clock related register (PER1)	Added the **PWMOPEN** bit.	5.3
F02C1H	Clock related register (PER2)	Added the **AAUEN** bit.	5.3
F02C2H, F02C3H	Clock related register (CANCKSEL, LINCKSEL)	No difference	5.3
F02C4H	Clock related register (CKSEL)	Added bits **FPLLDIV** and **FMAINDIV[1:0]**.	5.3
F02C5H	Clock related register (PLLCTL)	Changed bit specifications for **LCKSEL[1:0], PLLDIV1**, and **PLLMUL** bits. Added the **PLLMULA** bit.	5.3
F02C6H, F02C7H	Clock related registers (PLLSTS, MDIV)	No difference	5.3
F02C8H	RTC related register (RTCCL)	No difference	9.3
F02C9H	RESET related register (POCRES)	No difference	24.1
F02CAH	STOP status related register (STPSTC)	No difference	23.2
F02CCH	Clock monitor related register (**CLMTES**)	**New**	28.3.7
F02D0H – F02EDH	DTC related registers (HDTCCR0, …, DTCEN5)	No difference	19.2
F02F0H – F02F3H	Flash memory CRC related registers (CRC0CTL, PGCRCL)	No difference	28.3.1
F02F9H – F02FBH	General purpose CRC related registers (CRCMD, CRCD)	No difference	28.3.2
F0300H – F067FH	**RS-CANFD lite related registers**	**New**, (Changed from RS-CAN lite SFRs (address: F0300H to F0681H).)	18.3
F06A0H – F06BFH	**12-bit ADC related registers**	**New**	12.2
F06C1H – F06E9H	RLIN3 related registers (LWBR0/1, …, LUWTDR0/1)	No difference	17.2
F06ECH, F06EEH	RLIN3 related register (**LBSS0/1, LRSS0/1**)	**New**	17.2.2
F06F0H, F06F1H	Timer RJ0 related register (TRJ0)	No difference	7.3
F0780H – F0799H	ELC related registers (ELSELR00 to ELSELR25)	Added bit specifications of **ELSELRn[3:0]** bits.	20.2
F07C0H – F07D1H	CAN RAM ECC related registers (**CFDECCTL, …, CFDECEAD**)	**New**	28.3.4

17. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F23, F24 User's Manual: Hardware Rev. 1.00
- RL78/ F13, F14 User’s Manual: Hardware Rev. 2.10
- RL78 Family User's Manual: Software Rev. 2.30

Revision History

Rev.	Date	Description	
		Page	Summary
0.50	2022.02.15	-	Provisional edition issued.
1.00	2022.09.30		First edition issued.
		P.16	Revised key points of porting for the mirror area.
		P.23	Revised key points of porting for the CAN-FD.
		P.27	Revised tables (10-1 and 10-2) for the ELC.
		P.35-37	Added new tables (15-1 to 15-4) for the electrical specifications.
1.10	2023. 7.30	P.38-41	Added the description of “SFR comparison between RL78/F23, F24 products and RL78/F13, F14 products” as an appendix.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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