RL78/F23, F24

Setting of port related register when using alternate function

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Introduction

The purpose of this application note is to describe the port settings on using peripheral functions of RL78/F23 and F24.

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1. Port Peripheral Function Settings for RL78/F23 and F24

This section describes the setting procedure of Port Related Registers about using port as the digital I/O port, the analog input port, and the peripheral function port.

1.1 Port Related Register

Table 1.1 shows the port related register for using port setting.

Table 1.1 Port Related Register

Register Name	Function
Port mode registers (PMm)	Set input or output mode for the port
Port registers (Pm)	Set the output latch value of a port
Pull-up registers (PUm)	Set the on-chip pull-up resistors are to be used or not
Port input mode registers (PIMm)	Select the input type (normal or TTL)
Port output mode registers (POMm)	Select the output type (normal or N-ch open drain)
Port mode control registers (PMCm)	Select the port mode type (analog input or digital I/O)
Peripheral I/O redirection registers (PIORp)	Set to enable or disable the peripheral I/O redirect function
Port input threshold control registers (PITHLm)	Select the threshold value of the input buffer (Schmitt1 or Schmitt3)
Port output slew rate select register (PSRSEL)	Select the slew rate of the output buffer (normal or special)
SNOOZE status output control registers (PSNZCNTx)	Select the output signal indicating of the SNOOZE mode

1.2 Port Function Setting

Table 1.2 shows the settings of port related registers (port mode registers or output latches) when port pins of the RL78/F23 and F24 products are used as an alternate function pin.

Table 1.2 Port Related Register Settings When Using Each Peripheral Function (1/7)

Port	Pin Function	I/O	Bit in the Port Related Registers								RL78/F24					RL78/F23			
			Pmn	PMmn	PUmn	PIMmn	POMmn	PMCmn	PITHLmn	PIORpq	100	80	64	48	32	80	64	48	32
P00	P00	I	×	1	0 or 1	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	0	–	–	–	–										
	(TI05)	I	×	1	0 or 1	–	–	–	–	PIOR05=1	✓	✓	✓	✓	–	✓	✓	✓	–
	(TO05)	O	0	0	0	–	–	–	–	PIOR15=1	✓	✓	✓	✓	–	✓	✓	✓	–
	INTP9	I	×	1	0 or 1	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P01	P01	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI04)	I	×	1	0 or 1	–	–	–	–	PIOR04=1	✓	✓	–	–	–	✓	–	–	–
	(TO04)	O	0	0	0	–	–	–	–	PIOR14=1	✓	✓	–	–	–	✓	–	–	–
P02	P02	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI06)	I	×	1	0 or 1	–	–	–	–	PIOR06=1	✓	✓	–	–	–	✓	–	–	–
	(TO06)	O	0	0	0	–	–	–	–	PIOR16=1	✓	✓	–	–	–	✓	–	–	–
P03	P03	I	×	1	0 or 1	–	–	–	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	–		✓	–	–	–	–	–	–	–	–
	(RTC1HZ)	O	0	0	0	–	–	–	–	PIOR80=1	✓	–	–	–	–	–	–	–	–
P10	P10	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	0	–	×										
	TI13	I	×	1	0 or 1	0	×	–	0 or 1	PIOR23=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO13	O	0	0	0	×	0	–	×	PIOR33=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRJO0	O	0	0	0	×	0	–	×	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SCK10	I	×	1	0 or 1	0 or 1	×	–	0	PIOR42=0 PIOR91=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	1	0	0	×	0 or 1	–	×										
	SCL10	O	1	0	0	×	0 or 1	–	×	PIOR42=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	LTXD1	O	1	0	0	×	0	–	×	PIOR45=0	✓	✓	✓	✓	✓	–	–	–	–
	CTXD0	O	1	0	0	×	0	–	×	PIOR46=0	✓	✓	✓	✓	✓	–	–	–	–
P11	P11	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	0	–	×										
	TI12	I	×	1	0 or 1	0	×	–	0 or 1	PIOR22=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO12	O	0	0	0	×	0	–	×	PIOR32=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(TRDIOB0)	I	×	1	0 or 1	0	×	–	0 or 1	PIOR71=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	×	0	–	×										
	SI10	I	×	1	0 or 1	0 or 1	×	–	0	PIOR42=0 PIOR91=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SDA10	I/O	1	0	0	0 or 1	1	–	0	PIOR42=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	RXD1	I	×	1	0 or 1	0 or 1	×	–	0	PIOR42=0 PIOR91=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	LRXD1	I	×	1	0 or 1	0	×	–	0	PIOR45=0	✓	✓	✓	✓	✓	–	–	–	–
	CRXD0	I	×	1	0	0	×	–	0	PIOR46=0	✓	✓	✓	✓	✓	–	–	–	–
P12	P12	I	×	1	0 or 1	–	0	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	–	0	–	–										
	TI11	I	×	1	0 or 1	–	×	–	–	PIOR21=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO11	O	0	0	0	–	0	–	–	PIOR31=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(TRDIOD0)	I	×	1	0 or 1	–	×	–	–	PIOR73=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	–	0	–	–										
	INTP5	I	×	1	0 or 1	–	×	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SO10	O	1	0	0	–	0 or 1	–	–	PIOR42=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TXD1	O	1	0	0	–	0 or 1	–	–	PIOR42=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SNZOUT3	O	0	0	0	–	0	–	–	PIOR63=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
P13	P13	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	0	–	×										
	TI04	I	×	1	0 or 1	0	×	–	0 or 1	PIOR04=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO04	O	0	0	0	×	0	–	×	PIOR14=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRDIOA0	I	×	1	0 or 1	0	×	–	0 or 1	PIOR70=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	×	0	–	×										
	TRDCLK0	I	×	1	0 or 1	0	×	–	0 or 1	PIOR70=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SI01	I	×	1	0 or 1	0 or 1	×	–	0	PIOR41=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SDA01	I/O	1	0	0	0 or 1	1	–	0	PIOR41=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	LTXD0	O	1	1	0	×	0	–	×	PIOR44=0	✓	✓	✓	✓	✓	✓	✓	✓	✓

Table 1.2 Port Related Register Settings When Using Each Peripheral Function (2/7)

Port	Pin Function	I/O	Bit in the Port Related Registers								RL78/F24					RL78/F23			
			Pmn	PMmn	PUmn	PIMmn	POMmn	PMCmn	PITHLmn	PIORpq	100	80	64	48	32	80	64	48	32
P14	P14	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	0	–	×										
	TI06	I	×	1	0 or 1	0	×	–	0 or 1	PIOR06=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO06	O	0	0	0	×	0	–	×	PIOR16=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRDIOC0	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	×	0	–	×										
	SCK01	I	×	1	0 or 1	0 or 1	×	–	0	PIOR41=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	1	0	0	×	0 or 1	–	×										
	SCL01	O	1	0	0	×	0 or 1	–	×	PIOR41=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	LRXD0	I	×	1	0	0	×	–	0	PIOR44=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
P15	P15	I	×	1	0 or 1	–	×	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	–	0	–	–										
	TI05	I	×	1	0 or 1	–	×	–	–	PIOR05=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO05	O	0	0	0	–	0	–	–	PIOR15=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRDIOA1	I	×	1	0 or 1	–	×	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	–	0	–	–										
	(TRDIOA0)	I	×	1	0 or 1	–	×	–	–	PIOR70=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	–	0	–	–										
	(TRDCLK0)	I	×	1	0 or 1	–	×	–	–	PIOR70=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SO00	O	1	0	0	–	0 or 1	–	–	PIOR40=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TXD0	O	1	0	0	–	0 or 1	–	–	PIOR40=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	RTC1HZ	O	0	0	0	–	0	–	–	PIOR80=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TOOLTXD	–	–	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P16	P16	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	0	–	×										
	TI02	I	×	1	0 or 1	0	×	–	0 or 1	PIOR02=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO02	O	0	0	0	×	0	–	×	PIOR12=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRDIOC1	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	×	0	–	×										
	SI00	I	×	1	0 or 1	0 or 1	×	–	0	PIOR40=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SDA00	I/O	1	0	0	0 or 1	1	–	0	PIOR40=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	RXD0	I	×	1	0 or 1	0 or 1	×	–	0	PIOR40=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TOOLRXD	–	–	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P17	P17	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	0	–	×										
	TI00	I	×	1	0 or 1	0	×	–	0 or 1	PIOR00=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO00	O	0	0	0	×	0	–	×	PIOR10=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRDIOB1	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	×	0	–	×										
	SCK00	I	×	1	0 or 1	0 or 1	×	–	0	PIOR40=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	1	1	0	×	0 or 1	–	×										
	SCL00	O	1	0	0	×	0 or 1	–	×	PIOR40=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	INTP3	I	×	1	0 or 1	0	×	–	0 or 1	PIOR53=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
P30	P30	I	×	1	0 or 1	0	–	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	–	–	×										
	TI01	I	×	1	0 or 1	0	–	–	0 or 1	PIOR01=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO01	O	0	0	0	×	–	–	×	PIOR11=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRDIOD1	I	×	1	0 or 1	0	–	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	×	–	–	×										
	SSI00	I	×	1	0 or 1	0 or 1	–	–	0	PIOR40=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	INTP2	I	×	1	0 or 1	0	–	–	0 or 1	PIOR52=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SNZOUT0	O	0	0	0	×	–	–	×	PIOR60=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
P31	P31	I	×	1	0 or 1	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	0	–	–	–	–										
	TI14	I	×	1	0 or 1	–	–	–	–	PIOR24=0	✓	✓	✓	✓	–	–	–	–	–
	TO14	O	0	0	0	–	–	–	–	PIOR34=0	✓	✓	✓	✓	–	–	–	–	–
	STOPST	O	0	0	0	–	–	–	–	(Note)	✓	✓	✓	✓	–	✓	✓	✓	–
	(INTP2)	I	×	1	0 or 1	–	–	–	–	PIOR52=1	✓	✓	✓	✓	–	✓	✓	✓	–
P32	P32	I	×	1	0 or 1	–	×	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	0	–	0	–	–										
	TI16	I	×	1	0 or 1	–	×	–	–	PIOR26=0	✓	✓	✓	✓	–	–	–	–	–
	TO16	O	0	0	0	–	0	–	–	PIOR36=0	✓	✓	✓	✓	–	–	–	–	–
	(SO11)	O	1	0	0	–	0 or 1	–	–	PIOR43=0 PIOR92=1	✓	✓	✓	✓	–	✓	✓	✓	–
	INTP7	I	×	1	0 or 1	–	×	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P33	P33	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	–	–	–	0	–										
	AV_{REFP}	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ANI6	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P34	P34	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	–	–	–	0	–										
	AV_{REFM}	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ANI7	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note. The STOPST function is selected when the STPSEL bit in the STPSTC register is clear to 0.

Table 1.2 Port Related Register Settings When Using Each Peripheral Function (3/7)

Port	Pin Function	I/O	Bit in the Port Related Registers								RL78/F24					RL78/F23			
			Pmn	PMmn	PUmn	PIMmn	POMmn	PMCmn	PITHLmn	PIORpq	100	80	64	48	32	80	64	48	32
P40	P40	I	×	1	0 or 1	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	–	–	–	–										
	TOOL0	–	–	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P41	P41	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	–	–	–	×										
	TI10	I	×	1	0 or 1	–	–	–	0 or 1	PIOR20=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO10	O	0	0	0	–	–	–	×	PIOR30=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRJIO0	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	–	–	–	×										
	TRD0RES	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(SI10)	I	×	1	0 or 1	–	–	–	0	PIOR42=0 PIOR91=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(RXD1)	I	×	1	0 or 1	–	–	–	0 or 1	PIOR42=0 PIOR91=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	VCOUT0	O	×	0	0	–	–	–	×	–	✓	✓	✓	✓	✓	–	–	–	–
	SNZOUT2	O	0	0	0	–	–	–	×	PIOR62=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
P42	P42	I	×	1	0 or 1	–	–	–	–	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	–	–										
	(LTXD0)	O	1	0	0	–	–	–	–	PIOR44=1	✓	✓	✓	–	–	✓	✓	–	–
P43	P43	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	–	×										
	(LRXD0)	I	×	1	0	–	–	–	0	PIOR44=1	✓	✓	✓	–	–	✓	✓	–	–
P44	P44	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI07)	I	×	1	0 or 1	–	–	–	–	PIOR07=1	✓	✓	–	–	–	✓	–	–	–
	(TO07)	O	0	0	0	–	–	–	–	PIOR17=1 PIOR90=0	✓	✓	–	–	–	✓	–	–	–
P45	P45	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI10)	I	×	1	0 or 1	–	–	–	–	PIOR20=1	✓	✓	–	–	–	✓	–	–	–
	(TO10)	O	0	0	0	–	–	–	–	PIOR30=1	✓	✓	–	–	–	✓	–	–	–
P46	P46	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI12)	I	×	1	0 or 1	–	–	–	–	PIOR22=1	✓	✓	–	–	–	✓	–	–	–
	(TO12)	O	0	0	0	–	–	–	–	PIOR32=1	✓	✓	–	–	–	✓	–	–	–
P47	P47	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	INTP13	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
P50	P50	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	–	×										
	SSI01	I	×	1	0 or 1	–	–	–	0	PIOR41=1	✓	✓	✓	–	–	✓	✓	–	–
	(INTP3)	I	×	1	0 or 1	–	–	–	0 or 1	PIOR53=1	✓	✓	✓	–	–	✓	✓	–	–
P51	P51	I	×	1	0 or 1	–	–	–	–	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	–	–										
	(SO01)	I	1	0	0	–	–	–	–	PIOR41=1	✓	✓	✓	–	–	✓	✓	–	–
	INTP11	I	×	1	0 or 1	–	–	–	–	–	✓	✓	✓	–	–	✓	✓	–	–
P52	P52	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	–	×										
	SCK01	I	×	1	0 or 1	–	–	–	0	PIOR41=1	✓	✓	✓	–	–	✓	✓	–	–
		O	1	0	0	–	–	–	×										
	(STOPST)	O	0	0	0	–	–	–	×	(Note)	✓	✓	✓	–	–	✓	✓	–	–
P53	P53	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	–	×										
	(SI01)	I	×	1	0 or 1	–	–	–	0	PIOR41=1	✓	✓	✓	–	–	✓	✓	–	–
	INTP10	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	–	–	✓	✓	–	–
P54	P54	I	×	1	0 or 1	0	–	–	0 or 1	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	×	–	–	×										
	(TI11)	I	×	1	0 or 1	0	–	–	0 or 1	PIOR21=1	✓	✓	–	–	–	✓	–	–	–
	(TO11)	O	0	0	0	×	–	–	×	PIOR31=1	✓	✓	–	–	–	✓	–	–	–
	SSI10	I	×	1	0 or 1	0 or 1	–	–	0	PIOR42=0	✓	✓	–	–	–	✓	–	–	–
P55	P55	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI13)	I	×	1	0 or 1	–	–	–	–	PIOR23=1	✓	✓	–	–	–	✓	–	–	–
	(TO13)	O	0	0	0	–	–	–	–	PIOR33=1	✓	✓	–	–	–	✓	–	–	–
P56	P56	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI15)	I	×	1	0 or 1	–	–	–	–	PIOR25=1	✓	✓	–	–	–	–	–	–	–
	(TO15)	O	0	0	0	–	–	–	–	PIOR35=1	✓	✓	–	–	–	–	–	–	–
	(SNZOUT1)	O	0	0	0	–	–	–	–	PIOR61=1	✓	✓	–	–	–	✓	–	–	–
P57	P57	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI17)	I	×	1	0 or 1	–	–	–	–	PIOR27=1	✓	✓	–	–	–	–	–	–	–
	(TO17)	O	0	0	0	–	–	–	–	PIOR37=1	✓	✓	–	–	–	–	–	–	–
	(SNZOUT0)	O	0	0	0	–	–	–	–	PIOR60=1	✓	✓	–	–	–	✓	–	–	–

Note. The STOPST function is selected when the STPSEL bit in the STPSTC register is set to 1.

Table 1.2 Port Related Register Settings When Using Each Peripheral Function (4/7)

Port	Pin Function	I/O	Bit in the Port Related Registers								RL78/F24					RL78/F23			
			Pmn	PMmn	PUmn	PIMmn	POMmn	PMCmn	PITHLmn	PIORpq	100	80	64	48	32	80	64	48	32
P60	P60	I	×	1	0 or 1	–	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	–	0	–	×										
	(TO01)	O	0	0	0	–	0	–	×	PIOR11=1 PIOR90=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(SCK00)	I	×	1	0 or 1	–	×	–	0	PIOR40=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	1	0	0	–	0 or 1	–	×										
	(SCL00)	O	1	0	0	–	0 or 1	–	×	PIOR40=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
P61	P61	I	×	1	0 or 1	–	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	–	0	–	×										
	(TO02)	O	0	0	0	–	0	–	×	PIOR12=1 PIOR90=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(SI00)	I	×	1	0 or 1	–	×	–	0	PIOR40=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(SDA00)	I/O	1	0	0	–	1	–	0	PIOR40=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(RXD0)	I	×	1	0 or 1	–	×	–	0 or 1	PIOR40=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
P62	P62	I	×	1	0 or 1	0	×	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	0	–	×										
	(TO03)	O	0	0	0	×	0	–	×	PIOR13=1 PIOR90=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(SO00)	O	1	0	0	×	0 or 1	–	×	PIOR40=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(TXD0)	O	1	0	0	×	0 or 1	–	×	PIOR40=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SCLA0	I/O	1	0	0	0 or 1	1	–	0	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P63	P63	I	×	1	0 or 1	0	x	–	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	0	–	×										
	(TO07)	O	0	0	0	×	0	–	×	PIOR17=1 PIOR90=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(SSI00)	I	×	1	0 or 1	0 or 1	×	–	0	PIOR40=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SDAA0	I/O	1	0	0	0 or 1	1	–	0	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P64	P64	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI14)	I	×	1	0 or 1	–	–	–	–	PIOR24=1	✓	✓	–	–	–	–	–	–	–
	(TO14)	O	0	0	0	–	–	–	–	PIOR34=1	✓	✓	–	–	–	–	–	–	–
	(SNZOUT3)	O	0	0	0	–	–	–	–	PIOR63=1	✓	✓	–	–	–	✓	–	–	–
P65	P65	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI16)	I	×	1	0 or 1	–	–	–	–	PIOR26=1	✓	✓	–	–	–	–	–	–	–
	(TO16)	O	0	0	0	–	–	–	–	PIOR36=1	✓	✓	–	–	–	–	–	–	–
	(SNZOUT2)	O	0	0	0	–	–	–	–	PIOR62=1	✓	✓	–	–	–	✓	–	–	–
P66	P66	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI00)	I	×	1	0 or 1	–	–	–	–	PIOR00=1	✓	✓	–	–	–	✓	–	–	–
	(TO00)	O	0	0	0	–	–	–	–	PIOR10=1	✓	✓	–	–	–	✓	–	–	–
P67	P67	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI02)	I	×	1	0 or 1	–	–	–	–	PIOR02=1	✓	✓	–	–	–	✓	–	–	–
	(TO02)	O	0	0	0	–	–	–	–	PIOR12=1 PIOR90=0	✓	✓	–	–	–	✓	–	–	–
P70	P70	I	×	1	0 or 1	0	×	0 or 1	0 or 1	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	0	×	0	0	×										
	ANI26	I	×	1	0	×	×	1	×	–	✓	✓	✓	✓	–	✓	✓	✓	–
	TI15	I	×	1	0 or 1	0	×	0	0 or 1	PIOR25=0	✓	✓	✓	✓	–	–	–	–	–
	TO15	O	0	0	0	×	0	0	×	PIOR35=0	✓	✓	✓	✓	–	–	–	–	–
	INTP8	I	×	1	0 or 1	0	×	0	0 or 1	–	✓	✓	✓	✓	–	✓	✓	✓	–
	SI11	I	×	1	0 or 1	0 or 1	×	0	0	PIOR43=0	✓	✓	✓	✓	–	✓	✓	✓	–
	SDA11	I/O	1	0	0	0 or 1	1	0	0	PIOR43=0	✓	✓	✓	✓	–	✓	✓	✓	–
	SNZOUT4	O	0	0	0	×	0	0	×	PIOR64=0	✓	✓	✓	✓	–	✓	✓	✓	–
P71	P71	I	×	1	0 or 1	0	×	0	0 or 1	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	0	×	0	0	×										
	ANI27	I	×	1	0	×	×	1	×	–	✓	✓	✓	✓	–	✓	✓	✓	–
	TI17	I	×	1	0 or 1	0	×	0	0 or 1	PIOR27=0	✓	✓	✓	✓	–	✓	✓	✓	–
	TO17	O	0	0	0	×	0	0	×	PIOR37=0	✓	✓	✓	✓	–	✓	✓	✓	–
	INTP6	I	×	1	0 or 1	0	×	0	0 or 1	–	✓	✓	✓	✓	–	✓	✓	✓	–
	SCK11	I	×	1	0 or 1	0 or 1	×	0	0	PIOR43=0	✓	✓	✓	✓	–	✓	✓	✓	–
		O	1	0	0	×	0 or 1	0	×										
	SCL11	O	1	0	0	×	0 or 1	0	×	PIOR43=0	✓	✓	✓	✓	–	✓	✓	✓	–
	SNZOUT5	O	0	0	0	×	0	0	×	PIOR65=0	✓	✓	✓	✓	–	✓	✓	✓	–
P72	P72	I	×	1	0 or 1	–	0	0	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	0	–	0	0	–										
	ANI28	I	×	1	0	–	×	1	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
	(CTXD0)	O	1	0	0	–	0	0	–	PIOR46=1	✓	✓	✓	✓	–	–	–	–	–
	SO11	O	1	0	0	–	0 or 1	0	–	PIOR43=0 PIOR92=0	✓	✓	✓	✓	–	✓	✓	✓	–
	SNZOUT6	O	0	0	0	–	0	0	–	PIOR66=0	✓	✓	✓	✓	–	✓	✓	✓	–

Table 1.2 Port Related Register Settings When Using Each Peripheral Function (5/7)

Port	Pin Function	I/O	Bit in the Port Related Registers								RL78/F24					RL78/F23			
			Pmn	PMmn	PUmn	PIMmn	POMmn	PMCmn	PITHLmn	PIORpq	100	80	64	48	32	80	64	48	32
P73	P73	I	×	1	0 or 1	0	–	0	0 or 1	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	0	×	–	0	×										
	ANI29	I	×	1	0	×	–	1	×	–	✓	✓	✓	✓	–	✓	✓	✓	–
	(CRXD0)	I	×	1	0	0	–	0	0	PIOR46=1	✓	✓	✓	✓	–	–	–	–	–
	SSI11	I	×	1	0 or 1	0 or 1	–	0	0	PIOR43=0	✓	✓	✓	✓	–	✓	✓	✓	–
	SNZOUT7	O	0	0	0	×	–	0	×	PIOR67=0	✓	✓	✓	✓	–	✓	✓	✓	–
P74	P74	I	×	1	0 or 1	–	–	0	–	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	0	–										
	ANI30	I	×	1	0	–	–	1	–	–	✓	✓	✓	–	–	✓	✓	–	–
	(SO10)	O	1	0	0	–	–	0	–	PIOR42=1	✓	✓	✓	–	–	✓	✓	–	–
	(TXD1)	O	1	0	0	–	–	0	–	PIOR42=1	✓	✓	✓	–	–	✓	✓	–	–
P75	P75	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	–	×										
	(SI10)	I	×	1	0 or 1	–	–	–	0	PIOR42=1	✓	✓	✓	–	–	✓	✓	–	–
	(RXD1)	I	×	1	0 or 1	–	–	–	0	PIOR42=1	✓	✓	✓	–	–	✓	✓	–	–
P76	P76	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	–	×										
	SCK10	I	×	1	0 or 1	–	–	–	0	PIOR42=1	✓	✓	✓	–	–	✓	✓	–	–
		O	1	0	0	–	–	–	×										
P77	P77	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	0	–	–	–	×										
	(SSI10)	I	×	1	0 or 1	–	–	–	0	PIOR42=1	✓	✓	✓	–	–	✓	✓	–	–
	INTP12	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	✓	✓	–	–	✓	✓	–	–
P80	P80	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	–	–	–	0	–										
	ANI0	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ANO0	O	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	–	–	–	–
P81	P81	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	–	–	–	0	–										
	ANI1	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P82	P82	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	–	–	–	0	–										
	ANI2	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IVCMP00	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	–	–	–	–
P83	P83	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	–	–	–	0	–										
	ANI3	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IVCMP01	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	–	–	–	–
P84	P84	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	–	–	–	0	–										
	ANI4	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IVCMP02	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	–	–	–	–
P85	P85	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	–	–	–	0	–										
	ANI5	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IVCMP03	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	–	–	–	–
	IVREF0	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	✓	–	–	–	–
P86	P86	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	–	–	–	0	–										
	ANI8	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P87	P87	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	–	–	–	0	–										
	ANI9	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P90	P90	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	–	–	–	0	–										
	ANI10	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P91	P91	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	–	–	–	0	–										
	ANI11	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P92	P92	I	×	1	–	–	–	0	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	–	–	–	0	–										
	ANI12	I	×	1	–	–	–	1	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P93	P93	I	×	1	–	–	–	0	–	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	–	–	–	0	–										
	ANI13	I	×	1	–	–	–	1	–	–	✓	✓	✓	–	–	✓	✓	–	–
P94	P94	I	×	1	–	–	–	0	–	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	–	–	–	0	–										
	ANI14	I	×	1	–	–	–	1	–	–	✓	✓	✓	–	–	✓	✓	–	–
P95	P95	I	×	1	–	–	–	0	–	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	–	–	–	0	–										
	ANI15	I	×	1	–	–	–	1	–	–	✓	✓	✓	–	–	✓	✓	–	–
P96	P96	I	×	1	–	–	–	0	–	–	✓	✓	✓	–	–	✓	✓	–	–
		O	×	0	–	–	–	0	–										
	ANI16	I	×	1	–	–	–	1	–	–	✓	✓	✓	–	–	✓	✓	–	–
P97	P97	I	×	1	–	–	–	0	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	–	–	–	0	–										
	ANI17	I	×	1	–	–	–	1	–	–	✓	✓	–	–	–	✓	–	–	–

Table 1.2 Port Related Register Settings When Using Each Peripheral Function (6/7)

Port	Pin Function	I/O	Bit in the Port Related Registers								RL78/F24					RL78/F23			
			Pmn	PMmn	PUmn	PIMmn	POMmn	PMCmn	PITHLmn	PIORpq	100	80	64	48	32	80	64	48	32
P100	P100	I	×	1	–	–	–	0	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	–	–	–	0	–										
	ANI18	I	×	1	–	–	–	1	–	–	✓	–	–	–	–	–	–	–	–
P101	P101	I	×	1	–	–	–	0	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	–	–	–	0	–										
	ANI19	I	×	1	–	–	–	1	–	–	✓	–	–	–	–	–	–	–	–
P102	P102	I	×	1	–	–	–	0	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	–	–	–	0	–										
	ANI20	I	×	1	–	–	–	1	–	–	✓	–	–	–	–	–	–	–	–
P103	P103	I	×	1	–	–	–	0	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	–	–	–	0	–										
	ANI21	I	×	1	–	–	–	1	–	–	✓	–	–	–	–	–	–	–	–
P104	P104	I	×	1	–	–	–	0	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	–	–	–	0	–										
	ANI22	I	×	1	–	–	–	1	–	–	✓	–	–	–	–	–	–	–	–
P105	P105	I	×	1	–	–	–	0	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	–	–	–	0	–										
	ANI23	I	×	1	–	–	–	1	–	–	✓	–	–	–	–	–	–	–	–
P106	P106	I	×	1	0 or 1	–	–	–	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	–										
	(LTXD1)	O	1	0	0	–	–	–	–	PIOR45=1 PIOR93=0	✓	–	–	–	–	–	–	–	–
P107	P107	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	×										
	(LRXD1)	I	×	1	0 or 1	–	–	–	0	PIOR45=1 PIOR93=0	✓	–	–	–	–	–	–	–	–
P120	P120	I	×	1	0 or 1	–	×	0	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	–	0	0	×										
	ANI25	I	×	1	0	–	×	1	×	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TI07	I	×	1	0 or 1	–	×	0	0 or 1	PIOR07=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO07	O	0	0	0	–	0	0	×	PIOR17=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRDIOD0	I	×	1	0 or 1	–	×	0	0 or 1	PIOR73=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	–	0	0	×										
	SO01	O	1	0	0	–	0 or 1	0	×	PIOR41=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(SCK10)	I	×	1	0 or 1	–	×	0	0	PIOR42=0 PIOR91=1	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	1	0	0	–	0 or 1	0	×										
	(LTXD1)	O	1	0	0	–	0	0	×	PIOR45=1 PIOR93=1	✓	✓	✓	✓	✓	–	–	–	–
	INTP4	I	×	1	0 or 1	–	×	0	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P121	P121	I	×	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	X1	–	×	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P122	P122	I	×	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	X2	–	×	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	EXCLK	I	×	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
P123	P123	I	×	–	–	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
	XT1	–	×	–	–	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P124	P124	I	×	–	–	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
	XT2	–	×	–	–	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
	EXCLKS	I	×	–	–	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P125	P125	I	×	1	0 or 1	0	–	0	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	×	0	0	×	–	0	×										
	ANI24	I	×	1	0	×	–	1	×	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TI03	I	×	1	0 or 1	0	–	0	0 or 1	PIOR03=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TO03	O	0	0	0	×	–	0	×	PIOR13=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	TRDIOB0	I	×	1	0 or 1	0	–	0	0 or 1	PIOR71=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
		O	0	0	0	×	–	0	×										
	SSI01	I	×	1	0 or 1	0 or 1	–	0	0	PIOR41=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
	(LRXD1)	I	×	1	0 or 1	0	–	0	0	PIOR45=1 PIOR93=1	✓	✓	✓	✓	✓	–	–	–	–
	INTP1	I	×	1	0 or 1	0	–	0	0 or 1	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	SNZOUT1	O	0	0	0	×	–	0	×	PIOR61=0	✓	✓	✓	✓	✓	✓	✓	✓	✓
P126	P126	I	×	1	0 or 1	–	–	–	–	–	✓	✓	–	–	–	✓	–	–	–
		O	×	0	0	–	–	–	–										
	(TI01)	I	×	1	0 or 1	–	–	–	–	PIOR01=1	✓	✓	–	–	–	✓	–	–	–
	(TO01)	O	0	0	0	–	–	–	–	PIOR11=1 PIOR90=0	✓	✓	–	–	–	✓	–	–	–
P127	P127	I	×	1	0 or 1	–	–	–	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	–										
	(TI03)	I	×	1	0 or 1	–	–	–	–	PIOR03=1	✓	–	–	–	–	–	–	–	–
	(TO03)	O	0	0	0	–	–	–	–	PIOR13=1 PIOR90=0	✓	–	–	–	–	–	–	–	–
P130	P130	O	×	–	–	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
	RESOUT	O	0	–	–	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P137	P137	I	×	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓
	INTP0	I	×	–	–	–	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓

Table 1.2 Port Related Register Settings When Using Each Peripheral Function (7/7)

Port	Pin Function	I/O	Bit in the Port Related Registers								RL78/F24					RL78/F23			
			Pmn	PMmn	PUmn	PIMmn	POMmn	PMCmn	PITHLmn	PIORpq	100	80	64	48	32	80	64	48	32
P140	P140	I	×	1	0 or 1	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
		O	×	0	0	–	–	–	–										
	TRD1RES	I	×	1	0 or 1	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
	PCLBUZ0	O	0	0	0	–	–	–	–	–	✓	✓	✓	✓	–	✓	✓	✓	–
P150	P150	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	×										
	(SSI11)	I	×	1	0 or 1	–	–	–	0	PIOR43=1	✓	–	–	–	–	–	–	–	–
P151	P151	I	×	1	0 or 1	–	–	–	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	–										
	(SO11)	O	1	0	0	–	–	–	–	–	✓	–	–	–	–	–	–	–	–
P152	P152	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	×										
	(SI11)	I	×	1	0 or 1	–	–	–	0	PIOR43=1	✓	–	–	–	–	–	–	–	–
P153	P153	I	×	1	0 or 1	–	–	–	0 or 1	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	×										
	(SCK11)	I	×	1	0 or 1	–	–	–	0	PIOR43=1	✓	–	–	–	–	–	–	–	–
		O	1	0	0	–	–	–	×										
P154	P154	I	×	1	0 or 1	–	–	–	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	–										
	(SNZOUT7)	O	0	0	0	–	–	–	–	PIOR67=1	✓	–	–	–	–	–	–	–	–
P155	P155	I	×	1	0 or 1	–	–	–	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	–										
	(SNZOUT6)	O	0	0	0	–	–	–	–	PIOR66=1	✓	–	–	–	–	–	–	–	–
P156	P156	I	×	1	0 or 1	–	–	–	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	–										
	(SNZOUT5)	O	0	0	0	–	–	–	–	PIOR65=1	✓	–	–	–	–	–	–	–	–
P157	P157	I	×	1	0 or 1	–	–	–	–	–	✓	–	–	–	–	–	–	–	–
		O	×	0	0	–	–	–	–										
	(SNZOUT4)	O	0	0	0	–	–	–	–	PIOR64=1	✓	–	–	–	–	–	–	–	–

Remarks

× : Don't care
– : No function
PIORpq : Bit q of Peripheral I/O redirection register p
POMmn : Bit n of Port output mode register m
PMCmn : Bit n of Port mode control register m
PMmn : Bit n of Port mode register m
Pmn : Bit n of Port register m
PUmn : Bit n of Pull-up resistor option register m
PIMmn : Bit n of Port input mode register m
PITHLmn : Bit n of Port input threshold control register m

Table 1.3 KR (Key Return) Pin Assignment

Function	KR Pin Assignment									
	100-pin		80-pin		64-pin		48-pin		32-pin	
	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1	PIOR50=0	PIOR50=1
KR0	P70	–	P70	–	P70	P87	P70	P83	–	P80
KR1	P71	–	P71	–	P71	P90	P71	P84	–	P81
KR2	P72	–	P72	–	P72	P91	P72	P85	–	P82
KR3	P73	–	P73	–	P73	P92	P73	P86	–	P83
KR4	P74	–	P74	–	P74	P93	–	P87	–	P84
KR5	P75	–	P75	–	P75	P94	–	P90	–	P85
KR6	P76	–	P76	–	P76	P95	–	P91	–	–
KR7	P77	–	P77	–	P77	P96	–	P92	–	–

Remarks – : No function

Table 1.4 Port Related Register Setting When KR Pin Selection

Function	I/O	Pmn	PMmn	PUmn	PIMmn	POMmn	PMCmn	PITHLmn	PIORpq
KR0	I	×	1	0 or 1	0	×	0	0 or 1	PIOR50=×
KR1	I	×	1	0 or 1	0	×	0	0 or 1	PIOR50=×
KR2	I	×	1	0 or 1	0	×	0	0 or 1	PIOR50=×
KR3	I	×	1	0 or 1	0	×	0	0 or 1	PIOR50=×
KR4	I	×	1	0 or 1	0	×	0	0 or 1	PIOR50=×
KR5	I	×	1	0 or 1	0	×	0	0 or 1	PIOR50=×
KR6	I	×	1	0 or 1	0	×	0	0 or 1	PIOR50=×
KR7	I	×	1	0 or 1	0	×	0	0 or 1	PIOR50=×

Remarks × : Don't care

1.3 Setting of Output Port When Use a Peripheral Function

When use a peripheral function output, it is necessary to set the port latch (Pmn) of the output terminal.

Table 1.5 Port Latch Setting in Peripheral Function

Output Pins	Function	Port Latch Value	PMmn Value
TOmn	Timer array unit output	Pmn=0	PMmn=0
TRJIO0, TRJO0	Timer RJ output	Pmn=0	PMmn=0
TRDIOji	Timer RDe output	Pmn=0	PMmn=0
RTC1HZ	Real-time clock output	Pmn=0	PMmn=0
PCLBUZ0	Clock / Buzzer output	Pmn=0	PMmn=0
TxDq, SOp, SCKp, SCLr	Serial array unit output	Pmn=1	PMmn=0
CTXD0	CAN / CAN-FD output	Pmn=1	PMmn=0
LTXDn	RLIN3 output	Pmn=1	PMmn=0
RESOUT	Reset output	Pmn=0	–
STOPST	Standby function (stop status output)	Pmn=0	PMmn=0
SNZOUTn	Standby function (SNOOZE status output)	Pmn=0	PMmn=0
SDAr	Serial array unit input / output	Pmn=1	PMmn=0
SCLA0, SDAA0	IICA0 input / output	Pmn=0	PMmn=0
VCOUT0	Comparator output	Pmn=0	PMmn=0

Remarks

–	: No function
TOmn	: Timer array unit output pin (m: 0, 1, n = 0 to 7)
TRDIOji	: Timer RDe output pin (j: A, B, C, D, i = 0, 1)
TXD_q	: Serial array unit UART data transmission pin (q: 0, 1)
SOp	: Serial array unit CSI data transmission pin (p: 00, 01, 10, 11)
SCKp	: Serial array unit CSI clock output pin (p: 00, 01, 10, 11)
SCLr	: Serial array unit simplified-I2C clock output pin (r: 00, 01, 10, 11)
LTXDn	: LIN / UART module (RLIN3) data transmission pin (n: 0, 1)
SNZOUTn	: SNOOZE status output pin (n: 0 to 7)
SDAr	: Serial array unit simplified-I2C data input / output pin (r: 00, 01, 10, 11)
Pmn	: Bit n of Port register m (m: 0 to 15, n: 0 to 7)
PMmn	: Bit n of Port mode register m (m: 0 to 15, n: 0 to 7)

1.4 Steps of Setting for Port Related Register

This section describes the steps of setting “1.2 Port Function Setting” by each function.

1.4.1 Digital I/O Port (Pmn)

1.4.1.1 Digital Output Port

The setting procedure for using a pin as digital output is shown below.

In using a port as digital output, the pin output from peripheral function need stop. The register settings for stop the output of peripheral function are shown Table 1.6.

(1) Disables the function assigned to the target pin. Note
(2) PMCmn = 0; (Select digital I/O pin)
(3) POMmn = 0; (Set the port output mode (C-MOS))
(4) PSRSEL.PSRxx = X; (Set the port output slew rate (Normal or Slow))
(5) Pmn = X; (Set the port output latch)
(6) PMmn = 0; (Set the port direction (output mode))

Note: To disable the assigned function, take one of the followings.
- Set the PIORpq to assign it to another pin.
- Stop the assigned function. (See Table 1.6.)

Table 1.6 Settings to Stop Peripheral Function Digital Output

Output Pin	Related Function	Digital Output Stop Setting
TOmn	Timer array unit output	TOm.TOmn = 0, TOEm.TOEmn = 0
TRJIO0	Timer RJ output	TRJMR0.TMOD[2:0] = other “001B”
TRJO0	Timer RJ output	TRJIOC0.TOENA = 0
TRDIOAi, TRDIOBi, TRDIOCi, TRDIODi	Timer RDe output	TRDOER1.bit[7:0] = 1
TXDq, SDAr, Sop	Serial array unit output	SOm.SOmn = 1, SOEm.SOEmn = 0, SEm.SEmn = 0
SCKp, SCLr	Serial array unit output	SOm.CKOmn = 1, SOEm.SOEmn = 0, SEm.SEmn = 0
SCLA0, SDAA0	IICA0 output	PER0.IICA0EN = 0
CTXD0	CAN / CAN-FD output	PER2.CAN0EN = 0
LTXD0, LTXD1	LIN output	PER2.LINnEN = 0
RESOUT	Reset status output	RESOUTB in the User option byte 2 (000C2H) = 0
PCLBUZ0	Clock output / Buzzer output	CKS0.PCLOE0 = 0
RTC1HZ	Real-time clock output with error correction	RTCC0.RCLOE1 = 0
STOPST	STOP status output	STPSTC.STPOEN = 0
SNZOUTn	SNOOZE status output	PSNZCNTx.OUTENn = 0
VCOUT0	Comparator output	CMPCTL.COE = 0

1.4.1.2 Digital Input Port (Pmn)

The setting procedure for using a pin as digital input is shown below.

(1) PMCmn = 0; (Select digital I/O pin)
(2) PMmn = 1; (Set the port direction (input mode))
(3) PUmn = X; (Set the internal pull-up resistor (enable or disable))
(4) PIMmn = 0; (Set the port input mode (C-MOS))
(5) PITHLmn = X; (Set the input threshold (Schmitt 1 or Schmitt 3))

1.4.2 Analog Function

1.4.2.1 Analog Input / Output Port (ANIx, IVCMPx, IVREF0, ANO0)

The setting procedure for using a pin as analog input / output is shown below.

(1) PMCmn = 1; (Select analog I/O pin)
(2) PMmn = 1; (Set the port direction (input mode))
(3) Set the analog function.

1.4.2.2 Comparator Digital Output Port (VCOUT0)

The setting procedure for using the P41 pin as the VCOUT0 is shown below.

(1) Disables other functions assigned to the target pin. Note
(2) P41 = 0; (Set the port output latch (value = 0))
(3) PM41 = 0; (Set the port direction (output mode))
(4) Set the comparator function.

Note: Refer to Table 1.6.

1.4.3 Timer Function

1.4.3.1 Timer Output Port

(a) TOmn (Timer array unit output)

The setting procedure for using the P30 pin as the TO01 is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) PIOR1.PIOR11 = 0; (Assign the timer output pin)
(3) POM30 = 0; (Set the port output mode (C-MOS))
(4) P30 = 0; (Set the port output latch (value = 0))
(5) PM30 = 0; (Set the port direction (output mode))
(6) Set the timer function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(b) TRJIO0, TRJO0 (Timer RJ output)

The setting procedure for using the P41 pin as the TRJO0 is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) P41 = 0; (Set the port output latch (value = 0))
(3) PM41 = 0; (Set the port direction (output mode))
(4) Set the timer function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(c) TRDIOji (Timer RDe output)

The setting procedure for using the P125 pin as the TRDIOB0 is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) PMC125 = 0; (Select digital I/O pin)
(3) PIOR7.PIOR71 = 0; (Assign the timer output pin)
(4) P125 = 0; (Set the port output latch (value = 0))
(5) PM125 = 0; (Set the port direction (output mode))
(6) Set the timer function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(d) RTC1HZ (Real-time clock output)

The setting procedure for using the P15 pin as the RTC1HZ is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) PIOR8.PIOR80 = 0; (Assign the timer output pin)
(3) POM15 = 0; (Set the port output mode (C-MOS))
(4) P15 = 0; (Set the port output latch (value = 0))
(5) PM15 = 0; (Set the port direction (output mode))
(6) Set the timer function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(e) PCLBUZ0 (Clock / Buzzer output)

The setting procedure for using the P140 pin as the PCLBUZ0 is shown below.

(1) Disables other functions assigned to the target pin. Note
(2) P140 = 0; (Set the port output latch (value = 0))
(3) PM140 = 0; (Set the port direction (output mode))
(4) Set the timer function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

1.4.3.2 Timer Input Port

(a) TImn (Timer array unit input)

The setting procedure for using the P17 pin as the TI00 is shown below.

(1) PIOR0.PIOR00 = 0; (Assign the timer input pin)
(2) PM17 = 1; (Set the port direction (input mode))
(3) PU17 = X; (Set the internal pull-up resistor (enable or disable))
(4) PIM17 = 0; (Set the port input mode (C-MOS))
(5) PITHL17 = X; (Set the input threshold (Schmitt 1 or Schmitt 3))
(6) Set the timer function.

Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(b) TRJIO0 (Timer RJ input)

The setting procedure for using the P41 pin as the TRJIO0 is shown below.

(1) PM41 = 1; (Set the port direction (input mode))
(2) PU41 = X; (Set the internal pull-up resistor (enable or disable))
(3) PITHL41 = X; (Set the input threshold (Schmitt 1 or Schmitt 3))
(4) Set the timer function.

Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(c) TRDCLK0, TRDIOji, TRDxRES (Timer RDe input)

The setting procedure for using the P13 pin as the TRDIOA0 is shown below.

(1) PIOR7.PIOR70 = 0; (Assign the timer input pin)
(2) PM13 = 1; (Set the port direction (input mode))
(3) PU13 = X; (Set the internal pull-up resistor (enable or disable))
(4) PIM13 = 0; (Set the port input mode (C-MOS))
(5) PITHL13 = X; (Set the input threshold (Schmitt 1 or Schmitt 3))
(6) Set the timer function.

Remark: Port related registers are different of each pin. Refer to the Table 1.2.

1.4.4 Serial Interface

1.4.4.1 Serial Interface Output Port

(a) TXDq, SCKp, SOp, SCLr (Serial array unit output)

The setting procedure for using the P62 pin as the TXD0 is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) PIOR4.PIOR40 = 1; (Assign the serial output pin)
(3) POM62 = X; (Set the port output mode (C-MOS or N-ch open drain))
(4) P62 = 1; (Set the port output latch (value = 1))
(5) PM62 = 0; (Set the port direction (output mode))
(6) Set the serial function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(b) CTXD0 (RS-CANFD lite output)

The setting procedure for using the P10 pin as the CTXD0 is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) PIOR4.PIOR46 = 0; (Assign the serial output pin)
(3) POM10 = 0; (Set the port output mode (C-MOS))
(4) P10 = 1; (Set the port output latch (value = 1))
(5) PM10 = 0; (Set the port direction (output mode))
(6) Set the serial function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(c) LTXDn (RLIN3 output)

The setting procedure for using the P120 pin as the LTXD1 is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) PIOR4.PIOR45 = 1, PIOR9.PIOR93 = 1; (Assign the RLIN3 output pin)
(3) PMC120 = 0; (Select digital I/O pin)
(4) POM120 = 0; (Set the port output mode (C-MOS))
(5) P120 = 1; (Set the port output latch (value = 1))
(6) PM120 = 0; (Set the port direction (output mode))
(7) Set the serial function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

1.4.4.2 Serial Interface Input Port

(a) RXDq, SCKp, SIp, SSIp (Serial array unit input)

The setting procedure for using the P16 pin as the RXD0 is shown below.

(1) PIOR4.PIOR40 = 0; (Assign the Serial array unit input pin)
(2) PM16 = 1; (Set the port direction (input mode))
(3) PU16 = X; (Set the internal pull-up resistor (enable or disable))
(4) PITHL16 = 0; (Set the input threshold (Schmitt 1))
(5) PIM16 = X; (Set the port input mode (Normal or TTL input buffer))
(6) Set the serial function.

Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(b) CRXD0 (RS-CANFD lite Input)

The setting procedure for using the P11 pin as the CRXD0 is shown below.

(1) PIOR4.PIOR46 = 0; (Assign the RS-CANFD lite input pin)
(2) PM11 = 1; (Set the port direction (input mode))
(3) PU11 = 0; (Set the internal pull-up resistor (disabled))
(4) PITHL11 = 0; (Set the input threshold (Schmitt 1))
(5) PIM11 = 0; (Set the port input mode (C-MOS))
(6) Set the serial function.

Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(c) LRXDn (RLIN3 Input)

The setting procedure for using the P14 pin as the LRXD0 is shown below.

(1) PIOR4.PIOR44 = 0; (Assign the RLIN3 input pin)
(2) PM14 = 1; (Set the port direction (input mode))
(3) PU14 = 0; (Set the internal pull-up resistor (disabled))
(4) PITHL14 = 0; (Set the input threshold (Schmitt 1))
(5) PIM14 = 0; (Set the port input mode (C-MOS))
(6) Set the serial function.

Remark: Port related registers are different of each pin. Refer to the Table 1.2.

1.4.4.3 Serial Interface I/O Port

(a) SDAr (Serial array unit input / output)

The setting procedure for using the P16 pin as the SDA00 is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) PIOR4.PIOR40 = 0; (Assign the serial I/O pin)
(3) POM16 = 1; (Set the port output mode (N-ch open drain))
(4) PU16 = 0; (Set the internal pull-up resistor (disabled))
(5) PITHL16 = 0; (Set the input threshold (Schmitt 1))
(6) PIM16 = X; (Set the port input mode (Schmitt 1 or TTL))
(7) P16 = 1; (Set the port output latch (value = 1))
(8) PM16 = 0; (Set the port direction (output mode))
(9) Set the serial function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

(b) SCLA0, SDAA0 (IICA0 input / output)

The setting procedure for using the P63 pin as the SDAA0 is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) POM63 = 1; (Set the port output mode (N-ch open drain))
(3) PU63 = 0; (Set the internal pull-up resistor (disabled))
(4) PITHL63 = 0; (Set the input threshold (Schmitt 1))
(5) PIM63 = X; (Set the port input mode (Schmitt 1 or TTL))
(6) P63 = 1; (Set the port output latch (value = 1))
(7) PM63 = 0; (Set the port direction (output mode))
(8) Set the serial function.

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

1.4.5 External Interrupt (INTPx, KRx)

The setting procedure for using the P30 pin as the INTP2 is shown below.

(1) PIOR5.PIOR52 = 0; (Assign the INTP2 input pin)
(2) PM30 = 1; (Set the port direction (input mode))
(3) PU30 = X; (Set the internal pull-up resistor (enable or disable))
(4) PIM30 = 0; (Set the port input mode (C-MOS))
(5) PITHL30 = X; (Set the input threshold (Schmitt 1 or Schmitt 3))
(6) Set the external interrupt function.

Remark: Port related registers are different of each pin. Refer to the Table 1.2.

1.4.6 Other Output Port (RESOUT, STOPST, SNZOUTx)

The setting procedure for using the P31 pin as the STOPST is shown below.

(1) Disable other functions assigned to the target pin. Note
(2) STPSTC.STPSEL = 0; (Assign the STOPST pin (P31))
(3) STPSTC.STPLV = X; (Set the STOPST output level)
(4) P31 = 0; (Set the port output latch (value = 0))
(5) PM31 = 0; (Set the port direction (output mode))
(6) STPSTC.STPOEN = 1; (Enable the STOPST output)

Note: Refer to Table 1.6.
Remark: Port related registers are different of each pin. Refer to the Table 1.2.

2. References

References documents for this application note are shown below. Be sure to obtain the latest version of each document from the website of Renesas Electronics Corporation when designing.

- RL78/ F23, F24 User's Manual: Hardware Rev. 1.00

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022.09.30	–	First edition issued.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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