RL78/F23, F24

Option Byte Setting

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Introduction

This application note describes the setting of option byte (user option byte (000C0H to 000C2H), on-chip debug option byte (000C3H), and security option byte (000C4H)) and issues to be considered when setting them for the RL78/F23, RL78/F24 microcontrollers (MCUs).

For details, be sure to refer to User's Manual: Hardware.

Target Device

- RL78/F23, RL78/F24

Contents

1. Option Byte for RL78/F23, F24

The option byte of RL78/F23, F24 are located in the code flash memory 000C0H to 000C4H. Option byte contains of user option byte (000C0H to 000C2H), on-chip debug option byte (000C3H), and security option byte (000C4H), device automatically refers to these value in advance at reset released and controls the corresponding function.

When using boot swap function, set boot cluster 0 (000C0H to 000C4H) and boot cluster 1 (040C0H to 040C4H) to the same value in order to switch boot cluster 0 (00000H to 03FFFH) and boot cluster 1 (04000H to 07FFFH).

Figure 1-1 shows the option byte placement area for RL78/F23, F24 products.

This document provides some notes when using the RL78/F23 and F24 option byte function.

Address		
04132H to 07FFFH	User Program Area	Boot Cluster 1 Area 04000H to 07FFFH (16 KB)
040E6H to 04131H	Reserved	
040D6H to 040E5H	Flash Serial Programming Security ID (16 bytes) [Note]	
040C6H to 040D5H	On-chip Debug Security ID (16 bytes) [Note]	
040C5H	Reserved	
040C4H	Security Option Byte [Note]	
040C3H	On-chip Debug Option Byte [Note]	
040C2H	User Option Byte (000C2H) [Note]	
040C1H	User Option Byte (000C1H) [Note]	
040C0H	User Option Byte (000C0H) [Note]	
04080H to 040BFH	CALLT Table (64 bytes)	
04000H to 0407FH	Vector Table (128 bytes)	
00132H to 03FFFH	User Program Area of Boot Cluster 0	Boot Cluster 0 Area 00000H to 03FFFH (16 KB)
000E6H to 00131H	Reserved	
000D6H to 000E5H	Flash Serial Programming Security ID (16 bytes)	
000C6H to 000D5H	On-chip Debug Security ID (16 bytes)	
000C5H	Reserved	
000C4H	Security Option Byte	
000C3H	On-chip Debug Option Byte	
000C2H	User Option Byte (000C2H)	
000C1H	User Option Byte (000C1H)	
000C0H	User Option Byte (000C0H)	
00080H to 000BFH	CALLT Table (64 bytes)	
00000H to 0007FH	Vector Table (128 bytes)	

Note Set the same values as boot cluster 0 in the area shown in the “Note” for boot cluster 1 when the boot swap function is used. If boot swap function is not used, this area can be used as user program area.

Figure 1-1 Usage area of RL78/F23, F24 Option Byte function

1.1 User Option Byte (000C0H)

User option byte (000C0H) controls the operation of watch-dog timer. Bits of user option byte (000C0H) are shown in Figure 1-2, and the notes on setting are shown in Table 1-1.

b7	b6	b5	b4	b3	b2	b1	b0
WDTINT	WINDOW [1:0]		WDTON	WDCS [2:0]			WDSTBYON

Bit	Bit Name	Bit Description
7	WDTINT	0: Interval interrupt of watchdog timer is not used 1: Interval interrupt of watchdog timer is used
6-5	WINDOW [1:0]	01B: Watchdog timer window open period: 50% 10B: Watchdog timer window open period: 75% Note 2 11B: Watchdog timer window open period: 100% 00B: Setting prohibited
4	WDTON	0: Watchdog counter operation disabled (counting stopped after reset) 1: Watchdog counter operation enabled (counting started after reset)
3-1	WDCS [2:0]	Watchdog timer over-flow time select bits (Count source: f_{WDT} Note 1) 000B: $2^6/f_{WDT}$, 001B: $2^7/f_{WDT}$, 010B: $2^8/f_{WDT}$, 011B: $2^9/f_{WDT}$, 100B: $2^{11}/f_{WDT}$, 101B: $2^{13}/f_{WDT}$, 110B: $2^{14}/f_{WDT}$, 111B: $2^{16}/f_{WDT}$
0	WDSTBYON	0: Counter operation stopped in HALT / STOP / SNOOZE mode 1: Counter operation enabled in HALT / STOP / SNOOZE mode

Notes 1. Oscillator characteristics of f_{WDT} (WDT dedicated low-speed on-chip oscillator clock frequency) is (TYP.) 15 kHz. To clear the watchdog timer counter, perform within the range of the oscillator characteristic of f_{WDT}.

2. When the window open period is set to 75%, clearing the counter of the watchdog timer (writing ACH to WDTE) must proceed outside the corresponding period from among those listed below, over which clearing of the counter is prohibited (for example, confirming that the interval timer interrupt request flag (WDTIIF) of the watchdog timer is set).

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time (f_{WDT} = 17.25 kHz (MAX.))	Period over which clearing the counter is prohibited when the window open period is set to 75%
0	0	0	$2^6/f_{WDT}$ (3.71 ms)	1.85 ms to 2.51 ms
0	0	1	$2^7/f_{WDT}$ (7.42 ms)	3.71 ms to 5.02 ms
0	1	0	$2^8/f_{WDT}$ (14.84 ms)	7.42 ms to 10.04 ms
0	1	1	$2^9/f_{WDT}$ (29.68 ms)	14.84 ms to 20.08 ms
1	0	0	$2^{11}/f_{WDT}$ (118.72 ms)	59.36 ms to 80.32 ms
1	0	1	$2^{13}/f_{WDT}$ (474.89 ms)	237.44 ms to 321.26 ms
1	1	0	$2^{14}/f_{WDT}$ (949.79 ms)	474.89 ms to 642.51 ms
1	1	1	$2^{16}/f_{WDT}$ (3799.18 ms)	1899.59 ms to 2570.04 ms

Figure 1-2 User Option Byte (000C0H)

Table 1-1. Notes of User Option Byte (000C0H) Setting

Bit Name	Note of Setting
WDSTBYON	• The window open period is 100% when WDSTBYON = 0, regardless the value of the WINDOW1 and WINDOW0 bits.
WDCS [2:0]	• Clear the counter within the window open period. (set by WINDOW [1:0] bits)
WDTON	• The invalid memory access detection function is always enabled when this bit is 1, regardless of the setting of the IAWEN bit of IAWCTL register. When not using the watchdog timer, clear this bit to 0.
WINDOW [1:0]	• Be sure to set any of 01B, 10B, and 11B. • When using the window open period 75% setting, there is a WDT counter clear prohibition period. For details, see “1.1.1 Processing Example when the WDT Window Open Period is set to 75 %”. • If “WDSTBYON = 0” is set, the window open period will be 100% regardless of the setting of these bits.
WDTINT	• Set this bit to 1 when use interval interrupt of watchdog timer and judging the interrupt request by the WDTIF flag of IF0L register.

Caution Set the same value as 000C0H to 040C0H when the boot swap operation is used.

1.1.1 Processing Example when the WDT Window Open Period is set to 75 %

When the window open period is set to 75 %, clear the watchdog timer counter (writing ACH to WDTE register) at a timing other than the WDT counter clear prohibition period.

Figure 1-3 shows how the procedure for clear the WDT counter using the WDT interval timer interrupt request flag (WDTIIF).

WDCS [2:0]	Watchdog timer overflow time	WDT counter clear prohibition period when window open period is 75 %
000B	$2^6/f_{WDT}$	1.85 ms to 2.51 ms
001B	$2^7/f_{WDT}$	3.71 ms to 5.02 ms
010B	$2^8/f_{WDT}$	7.42 ms to 10.04 ms
011B	$2^9/f_{WDT}$	14.84 ms to 20.08 ms
100B	$2^{11}/f_{WDT}$	59.36 ms to 80.32 ms
101B	$2^{13}/f_{WDT}$	237.44 ms to 321.26 ms
110B	$2^{14}/f_{WDT}$	474.89 ms to 642.51 ms
111B	$2^{16}/f_{WDT}$	1899.59 ms to 2570.04 ms

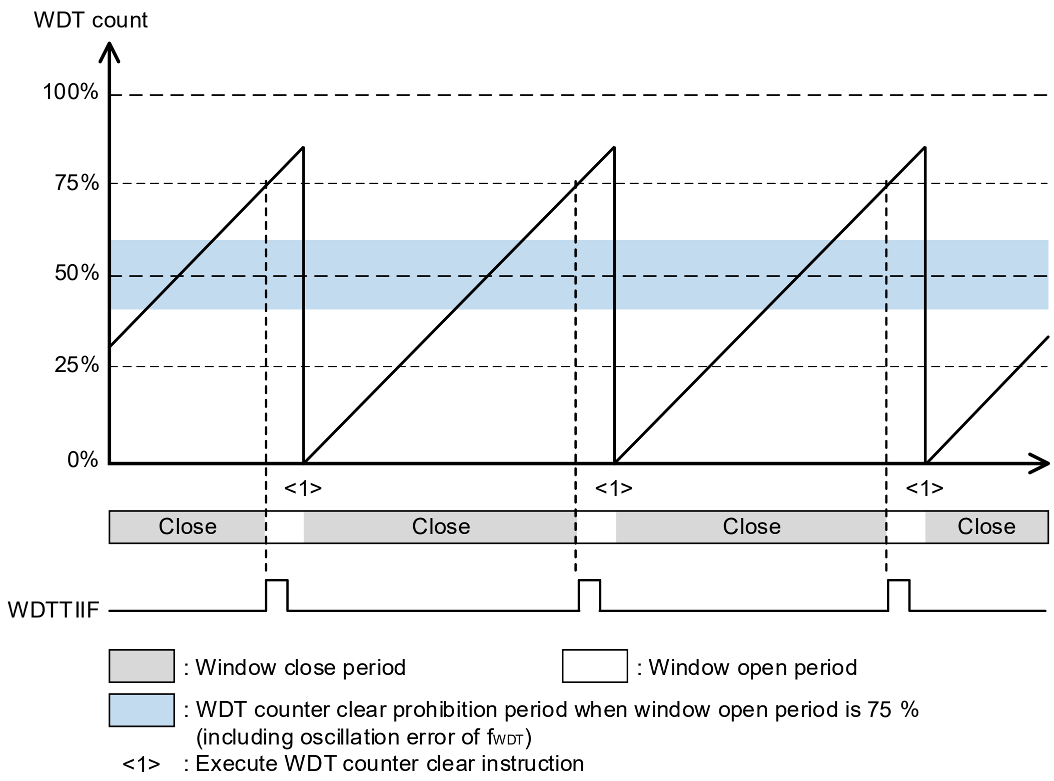

Figure 1-3 Example of Clearing the WDT Counter Using the WDT Interval Timer Interrupt Flag

1.2 User Option Byte (000C1H)

In the user option byte (000C1H), set the operation mode of the voltage detector and the operation of the clock monitor function. Bits of user option byte (000C1H) are shown in Figure 1-4, and the notes on setting are shown in Table 1-5.

b7	b6	b5	b4	b3	b2	b1	b0
VPOC [2:0]			CLKMB	LVIS [1:0]		LVIMDS [1:0]	

Bit	Bit Name	Bit Description
7-5	VPOC [2:0]	It depends on the operation mode of the used LVD (set by LVIMDS [1:0]). Refer to Table 1-2 and Table 1-3.
4	CLKMB	0: Clock monitor operation is enabled 1: Clock monitor operation is stopped
3-2	LVIS [1:0]	It depends on the operation mode of the used LVD (set by LVIMDS [1:0]). Refer to Table 1-2 and Table 1-3.
1-0	LVIMDS [1:0]	Set the operation mode of voltage detector 01B: Interrupt mode 10B: Interrupt & reset mode 11B: Reset mode 00B: Setting prohibited

Figure 1-4 User Option Byte (000C1H)

Table 1-2. Setting of Bits VPOC [2:0] and LVIS [1:0] when Interrupt Mode Note 1 and Reset Mode

VPOC[2:0]	LVIS[1:0]	Function
000B	01B	Select the V_{LVD4} Grade-3 product: Rise: 3.02 V [2.95 V - 3.09 V], Fall: 2.96 V [2.89 V - 3.02 V] Grade-4 product: Rise: 3.02 V [2.95 V - 3.17 V], Fall: 2.96 V [2.89 V - 3.09 V] Grade-5 product: Rise: 3.02 V [2.95 V - 3.44 V], Fall: 2.96 V [2.89 V - 3.31 V]
001B	00B	Select the V_{LVD2} Grade-3 product: Rise: 4.42 V [4.30 V - 4.51 V], Fall: 4.32 V [4.21 V - 4.41 V] Grade-4 product: Rise: 4.42 V [4.30 V - 4.61 V], Fall: 4.32 V [4.21 V - 4.51 V] Grade-5 product: Rise: 4.42 V [4.30 V - 4.92 V], Fall: 4.32 V [4.21 V - 4.76 V]
010B	00B	Select the V_{LVD1} Grade-3 product: Rise: 4.62 V [4.50 V - 4.72 V], Fall: 4.52 V [4.40 V - 4.62 V] Grade-4 product: Rise: 4.62 V [4.50 V - 4.82 V], Fall: 4.52 V [4.40 V - 4.71 V] Grade-5 product: Rise: 4.62 V [4.50 V - 5.12 V], Fall: 4.52 V [4.40 V - 4.98 V]
011B	00B	Select the V_{LVD0} Grade-3 product: Rise: 4.74 V [4.62 V - 4.84 V], Fall: 4.64 V [4.52 V - 4.74 V] Grade-4 product: Rise: 4.74 V [4.62 V - 4.94 V], Fall: 4.64 V [4.52 V - 4.84 V] Grade-5 product: Rise: 4.74 V [4.62 V - 5.25 V], Fall: 4.64 V [4.52 V - 5.11 V]
	01B	Select the V_{LVD3} Grade-3 product: Rise: 3.22 V [3.13 V - 3.29 V], Fall: 3.15 V [3.07 V - 3.22 V] Grade-4 product: Rise: 3.22 V [3.13 V - 3.39 V], Fall: 3.15 V [3.07 V - 3.31 V] Grade-5 product: Rise: 3.22 V [3.13 V - 3.66 V], Fall: 3.15 V [3.07 V - 3.52 V]
	11B	Select the V_{LVD5} Note 2 Grade-3 product: Rise: 2.81 V [2.74 V - 2.87 V], Fall: 2.75 V [2.68 V - 2.81 V] Grade-4 product: Rise: 2.81 V [2.74 V - 2.95 V], Fall: 2.75 V [2.68 V - 2.88 V] Grade-5 product: Rise: 2.81 V [2.74 V - 3.22 V], Fall: 2.75 V [2.68 V - 3.06 V]
Other than above		Setting prohibited

Notes 1. If interrupt mode is used (LVIMDS [1:0] = 01B), the reset voltage (at falling voltage) is V_{PDR} (TYP. 1.55 V). In this case the V_{PDR} will be out of the specified operation voltage for this product. After the occurrence of an interrupt (INTLVI), disable other interrupt factors as long as the power supply voltage is within the valid operation range (*) and shift to STOP mode, or generate an internal reset by user software (execution of illegal instruction, reset of watchdog timer function). When supply voltage exceeds selected V_{LVD}, STOP mode or reset state is released.

(*) Use operating conditions (V_{DD} (supply voltage): 2.7 V to 5.5 V, f_{CLK} (CPU / Peripheral hardware clock frequency): 15 kHz to 40 MHz).

2. In this condition, reset mode can be set, but interrupt mode is prohibited.

Table 1-3 Setting of Bits VPOC [2:0] and LVIS [1:0] when Interrupt & Reset Mode

VPOC [2:0]	LVIS [1:0]	Function
001B	00B	Select the V_{LVD2} Grade-3 product: Reset: 2.75 V [2.68 V - 2.81 V], Reset release: 4.42 V [4.30 V - 4.51 V] Interrupt (V_{LVDH}: 4.42 V [4.30 V - 4.51 V], V_{LVDL}: 4.32 V [4.21 V - 4.41 V]) Grade-4 product: Reset: 2.75 V [2.68 V - 2.88 V], Reset release: 4.42 V [4.30 V - 4.61 V] Interrupt (V_{LVDH}: 4.42 V [4.30 V - 4.61 V], V_{LVDL}: 4.32 V [4.21 V - 4.51 V]) Grade-5 product: Reset: 2.75 V [2.68 V - 3.06 V], Reset release: 4.42 V [4.30 V - 4.92 V] Interrupt (V_{LVDH}: 4.42 V [4.30 V - 4.92 V], V_{LVDL}: 4.32 V [4.21 V - 4.76 V])
010B	00B	Select the V_{LVD1} Grade-3 product: Reset: 2.75 V [2.68 V - 2.81 V], Reset release: 4.62 V [4.50 V - 4.72 V] Interrupt (V_{LVDH}: 4.62 V [4.50 V - 4.72 V], V_{LVDL}: 4.52 V [4.40 V - 4.62 V]) Grade-4 product: Reset: 2.75 V [2.68 V - 2.88 V], Reset release: 4.62 V [4.50 V - 4.82 V] Interrupt (V_{LVDH}: 4.62 V [4.50 V - 4.82 V], V_{LVDL}: 4.52 V [4.40 V - 4.71 V]) Grade-5 product: Reset: 2.75 V [2.68 V - 3.06 V], Reset release: 4.62 V [4.50 V - 5.12 V] Interrupt (V_{LVDH}: 4.62 V [4.50 V - 5.12 V], V_{LVDL}: 4.52 V [4.40 V - 4.98 V])
011B	00B	Select the V_{LVD0} Grade-3 product: Reset: 2.75 V [2.68 V - 2.81 V], Reset release: 4.74 V [4.62 V - 4.84 V] Interrupt (V_{LVDH}: 4.74 V [4.62 V - 4.84 V], V_{LVDL}: 4.64 V [4.52 V - 4.74 V]) Grade-4 product: Reset: 2.75 V [2.68 V - 2.88 V], Reset release: 4.74 V [4.62 V - 4.94 V] Interrupt (V_{LVDH}: 4.74 V [4.62 V - 4.94 V], V_{LVDL}: 4.64 V [4.52 V - 4.84 V]) Grade-5 product: Reset: 2.75 V [2.68 V - 3.06 V], Reset release: 4.74 V [4.62 V - 5.25 V] Interrupt (V_{LVDH}: 4.74 V [4.62 V - 5.25 V], V_{LVDL}: 4.64 V [4.52 V - 5.11 V])
	01B	Select the V_{LVD3} Grade-3 product: Reset: 2.75 V [2.68 V - 2.81 V], Reset release: 3.22 V [3.13 V - 3.29 V] Interrupt (V_{LVDH}: 3.22 V [3.13 V - 3.29 V], V_{LVDL}: 3.15 V [3.07 V - 3.22 V]) Grade-4 product: Reset: 2.75 V [2.68 V - 2.88 V], Reset release: 3.22 V [3.13 V - 3.39 V] Interrupt (V_{LVDH}: 3.22 V [3.13 V - 3.39 V], V_{LVDL}: 3.15 V [3.07 V - 3.31 V]) Grade-5 product: Reset: 2.75 V [2.68 V - 3.06 V], Reset release: 3.22 V [3.13 V - 3.66 V] Interrupt (V_{LVDH}: 3.22 V [3.13 V - 3.66 V], V_{LVDL}: 3.15 V [3.07 V - 3.52 V])
Other than above		Setting prohibited

Table 1-4 Setting of Bits VPOC [2:0] and LVIS [1:0] when LVD Off

VPOC [2:0]	LVIS [1:0]	LVIMDS [1:0]	Function
111B	00B	11B	LVD off

Table 1-5 Notes of User Option Byte (000C1H) Setting

Bit Name	Note of Setting
LVIMDS [1:0]	• Do not set 00B to these bits. • If do not use the LVD circuit, set 11B. • If use 01B (Interrupt mode), do not select V_{LVD5}.
LVIS [1:0]	• If do not use the LVD circuit, set 00B. • Use the Interrupt mode or Reset mode: Refer to Table 1-2. • Use the Interrupt & Reset mode: Refer to Table 1-3.
CLKMB	• To use the clock monitor function, set this bit to 0.
VPOC [2:0]	• If do not use the LVD circuit, set 111B. • The LVD circuit is used, not set values other than 000B, 001B, 010B, 011B.

Cautions 1. The setting when not using the LVD circuit is refer to Table 1-4. And have a reset circuit on user's system.

2. Set the same value as 000C1H to 040C1H when the boot swap operation is used.

1.3 User Option Byte (000C2H)

User option byte (000C2H) sets the frequency of high-speed on-chip oscillator, and P130/RESOUT pin operation mode. Bits of user option byte (000C2H) are shown in Figure 1-5, and the notes on setting are shown in Table 1-6.

b7	b6	b5	b4	b3	b2	b1	b0
1	1	RESOUTB	FRQSEL [4:0]				

Bit	Bit Name	Bit Description
7-6	–	Be sure to set these bits to 11B. Setting of other values is prohibited.
5	RESOUTB	0: Selects P130 as the RESOUT pin 1: Selects P130 as a general port pin (output only)
4-0	FRQSEL [4:0]	Set the frequency of high-speed on-chip oscillator. (Following table)

FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	High-speed On-chip Oscillator Frequency
1	1	0	0	0	80 MHz
1	0	0	0	0	64 MHz
0	1	0	0	0	40 MHz
0	0	0	0	0	32 MHz
0	1	0	0	1	20 MHz
0	0	0	0	1	16 MHz
0	0	0	1	0	8 MHz
0	0	0	1	1	4 MHz
0	0	1	0	0	2 MHz
Other than those above:					Setting prohibited

Figure 1-5 User Option Byte (000C2H)

Table 1-6 Notes of User Option Byte (000C2H) Setting

Bit Name	Note of Setting
FRQSEL [4:0]	• Be sure to set one of 00000B, 00001B, 00010B, 00011B, 00100B, 01000B, 01001B, 10000B, or 11000B.
RESOUTB	• P130/RESOUT pin is not available for 32-pin product. When using 32-pin product, it is recommended that this bit be set to the initial value (“1”). • P130 pin outputs low-level during reset regardless of the setting of this bit. • When this bit is set to 0, P130/RESOUT pin automatically outputs high-level after reset release. Regardless of port latch (P130 bit), high-level is output until it is reset.
b6	• Be sure to write this bit to 1.
b7	• Be sure to write this bit to 1.

Caution Set the same value as 000C2H to 040C2H when the boot swap operation is used.

1.4 On-chip Debug Option Byte (000C3H)

On-chip debug option byte (000C3H) sets the operation when debugger is connected. Bits of on-chip debug option byte (000C3H) are shown in Figure 1-6, and the notes on setting are shown in Table 1-8.

b7	b6	b5	b4	b3	b2	b1	b0
OCDENSET	0	FLPEN	0	0	1	HPIEN	OCDERSD

Bit	Bit Name	Bit Description
7	OCDENSET	Control in on-chip debug operation with OCDERSD bit. Refer to Table 1-7.
6	–	Be sure to write “0” for this bit. If write “1”, the operation is not guaranteed.
5	FLPEN	Controls flash serial programming and on-chip debug operations. Refer to Table 1-7 for details. 0: Operation disabled 1: Operation enabled
4-2	–	Be sure to write "001B" for these bits. Do not set other value.
1	HPIEN	Control hot plug-in operation. Refer to Table 1-7.
0	OCDERSD	Control on-chip debug operation with OCDENSET. Refer to Table 1-7.

Figure 1-6 On-chip Debug Option Byte (000C3H)

Table 1-7 Function of On-chip Debug Option Byte

OCDENSET	FLPEN	HPIEN	OCDERSD	Function
0	1	0	0	Disable on-chip debug and hot plug-in operation. Enable flash serial programming operation.
1	1	0	0	Enable on-chip debug and flash serial programming operation. Disable hot plug-in operation. Erases data of flash memory [Note 2] in case of failures in authenticating on-chip debug security ID [Note 1].
1	1	0	1	Enable on-chip debug and flash serial programming operation. Disable hot plug-in operation. Does not erase data of flash memory in case of failures in authenticating on-chip debug security ID [Note 1].
1	1	1	1	Enable on-chip debug, hot plug-in and flash serial programming operation. Does not erase data of flash memory in case of failures in authenticating on-chip debug security ID [Note 1].
0	0	0	0	Disable on-chip debug, hot plug-in, flash serial programming operation.
1	0	0	0	
1	0	0	1	
1	0	1	1	Disable on-chip debug and flash serial programming operation. Enable hot plug-in operation.
Other than above				Setting prohibited.

Notes 1. The security ID is the 16-byte ID located at 000C6H to 000D5H.

2. Both code flash memory and data flash memory are targeted.

Caution If FLPEN = 0, on-chip debug and flash serial programming are disabled.

Table 1-8 Notes of On-chip Debug Option Byte (000C3H) Setting

Bit Name	Note of Setting
OCDERSD	• Do not set 1 to OCDERSD bit when OCDENSET bit is 0.
HPIEN [Note]	• When the HPIEN bit is set to 1, the f_{IL} (low-speed on-chip oscillator) operates and cannot be stopped by the user program. The f_{IL} can be stopped by register setting only in standby mode. For details, refer to User's Manual: Hardware.
b4 to b2 [Note]	• Be sure to set these bits to 001B.
FLPEN	• When the FLPEN bit is set to 0, flash serial programming function and on-chip debug function are disabled. Note that flash memory can only be rewritten by self-programming.
b6	• Be sure to set “0”.
OCDENSET	• Do not set 0 to OCDENSET bit when OCDERSD bit is 1.

Note When on-chip debug function is used, HPIEN and bit 3 to 2 changes bits value to other. Be sure to write 01B when writing to these bits.

Caution Set the same value as 000C3H to 040C3H when the boot swap operation is used. When using on-chip debugging and hot plug-in functions, some internal RAM area cannot be used depending on the product. Refer to User's Manual: Hardware.

1.5 Security Option Byte (000C4H)

Security option byte (000C4H) can mask the reading of the ID area (on-chip debug security ID and flash serial programming security ID). Bit of security option byte (000C4H) are shown in Figure 1-7, and the notes on setting are shown in Table 1-9.

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	1	IDRDEN	1	0

Bit	Bit Name	Bit Description
7-3	–	Be sure to set these bits to 11111B. Setting of other values is strictly prohibited.
2	IDRDEN	On-chip debug security ID (000C6H to 000D5H) and flash serial programming security ID (000D6H to 000E5H) control the read operation. 0: Read operation disabled (When reading, readable "0") 1: Read operation enabled
1-0	–	Be sure to write “10B”. Setting of other values is strictly prohibited.

Figure 1-7 Security Option Byte (000C4H)

Table 1-9 Notes of Security Option Byte (000C4H) Setting

Bit Name	Note of Setting
b1, b0	• Be sure to set these bits to 10B.
IDRDEN	• When IDRDEN is set to “0”, on-chip debug security ID and Flash serial programming security ID are readable “0”. • Even if IDRDEN is set to “0”, reading to the area of 040C6H to 040D5H, and 040D6H to 040E5H is not prohibited. • Even if IDRDEN is set to “0”, the high-speed CRC function can read the value and calculates the CRC. • When IDRDEN is set to “0”, be sure to enable the prohibition of rewriting boot cluster 0 (00000H to 3FFFFH).
b7 to b3	• Be sure to set these bits to 11111B.

Cautions 1. The setting of prohibition of rewriting boot cluster 0 refer to the flash memory section in RL78/F23, F24 User’s manual (Hardware).

2. Set the same value as 000C4H to 040C4H when the boot swap operation is used.

2. Setting Range of Option Byte for RL78/F23, F24

The setting range of Option Bytes are shown in the Table 2-1.

Table 2-1 Setting Range of Option Byte

Option Bytes		RL78/F23, F24 V_{DD} = 2.7 V to 5.5 V, f_{CLK} = 15 kHz to 40 MHz, T_A = - 40 °C to 105 °C (Grade-3), T_A = - 40 °C to 125 °C (Grade-4), T_A = - 40 °C to 150 °C (Grade-5)
000C0H/ 040C0H	WDSTBYON	0 or 1
	WDCS [2:0]	000B to 111B
	WDTON	0 or 1
	WINDOW [1:0]	01B, 10B, or 11B (00B setting prohibited)
	WDTINT	0 or 1
000C1H/ 040C1H	LVIMDS [1:0]	01B, 10B, or 11B (00B setting prohibited)
	LVIS [1:0]	· LVIMDS=01B, VPOC=000B: 01B · LVIMDS=01B, VPOC=001B: 00B · LVIMDS=01B, VPOC=010B: 00B · LVIMDS=01B, VPOC=011B: 00B, 01B, or 11B · LVIMDS=10B, VPOC=001B: 00B · LVIMDS=10B, VPOC=010B: 00B · LVIMDS=10B, VPOC=011B: 00B or 01B · LVIMDS=11B, VPOC=000B: 01B · LVIMDS=11B, VPOC=001B: 00B · LVIMDS=11B, VPOC=010B: 00B · LVIMDS=11B, VPOC=011B: 00B, 01B, or 11B · LVIMDS=11B, VPOC=111B: 00B (Other than the above: Setting prohibited)
	CLKMB	0 or 1
	VPOC [2:0]	· LVIMDS=01B: 000B, 001B, 010B, or 011B · LVIMDS=10B: 001B, 010B, or 011B · LVIMDS=11B: 000B, 001B, 010B, 011B, or 111B (LVD off) (Other than the above: Setting prohibited)
000C2H/ 040C2H	FRQSEL [4:0]	00000B, 00001B, 00010B, 00011B, 00100B, 01000B, 01001B, 10000B, or 11000B (Other than the above: Setting prohibited)
	RESOUTB	0 or 1
	bit7, bit6	11B (Setting prohibited except 11B)
000C3H/ 040C3H	OCDERSD	[OCDENSET, HPIEN, OCDERSD] = 000B, 100B, 101B, or 111B (Other than the above: Setting prohibited)
	HPIEN	
	OCDENSET	
	FLPEN	0 or 1
	bit4 to bit2	001B (Setting prohibited except 001B)
	bit6	0 (1 setting prohibited)
000C4H/ 040C4H	IDRDEN	0 or 1
	bit1, bit0	10B (Setting prohibited except 10B)
	bit7 to bit3	11111B (Setting prohibited except 11111B)

Caution When using boot swap operation, set the same value in areas 040C0H to 040C4H as in areas 000C0H to 000C4H.

3. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F23, F24 User's Manual: Hardware Rev. 1.00
- RL78 family User's Manual: Software Rev. 2.30

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022. 9.30	–	First edition issued.
1.10	2023.12.31	P.5	Added “1.1.1 Processing Example when the WDT Window Open Period is set to 75 %”.
		P.11	Revised “Table 1-7 Function of On-chip Debug Option Byte”.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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