

# **RL78**

R01AN3996EJ0100 Rev.1.00 2017.11.17

## Troubleshooting of the LCD controller/driver

### Introduction

In this application note, troubleshooting of the LCD controller/driver installed in the RL78/L1x is explained.

### **Target Device**

RL78/L1x

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.



### RL78

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### 1. Troubleshooting the LCD Controller/Driver

### 1.1 Nothing at All Displayed on the LCD Panel

When the LCD panel displays nothing at all, check (1) through (3) below.

### (1) LCD port function register (PFSEG)

The PFSEG register sets whether pins are to be used as ports (other than segment output) or for segment output. In the initial settings, check that the PFSEG bits corresponding to the segment pins to be used are set to "segment output" (PFSEGxx = 1). When pins are used for segment output, the PUmn bits of the PUm register, the POMmn bits of the POMm register, and the PIMmn bits of the PIMm register must all be set to "0".

			LCD Por	t Functior	n Register	S		
Symbol	7	6	5	4	3	2	1	0
PFSEGx	PFSEGxx	PFSEGxx	PFSEGxx	PFSEGxx	PFSEGxx	PFSEGxx	PFSEGxx	PFSEGxx

PFSEGxx	Specification of port (other than segment output)/segment output
	for Pmn pins
0	Used as port (other than segment output)
1	Used as segment output

### (2) External circuit

In the LCD controller/driver installed in the RL78, the LCD drive voltage generator can be switched between external resistance division, internal voltage boosting, and capacitor split methods. The external circuit must be modified according to the method used and the bias method for LCD display. The external circuit must be confirmed to be compatible with the method set in LCD mode register 0 (LCDM0). An example of the external circuit is described in the "Supplying LCD Drive Voltages VL1, VL2, VL3, and VL4" section of the user's manual.

LCD mode register 0	(LCDM0)	(Excerpt)
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Symbol	7	6	5	4	3	2	1	0
LCDM0	MDSET1	MDSET0	LWAVE	LDTY2	LDTY1	LDTY0	LBAS1	LBAS0

MDSET1	MDSET0	LCD drive voltage generator selection
0	0	External resistance division method
0	1	Internal voltage boosting method
1	0	Capacitor split method
1	1	Setting prohibited

LBAS1	LBAS0	LCD display bias mode selection
0	0	1/2 bias method
0	1	1/3 bias method
1	0	1/4 bias method
1	1	Setting prohibited









Figure 1-2 Examples of LCD Drive Power Connections (Internal Voltage Boosting Method, 1/3 bias method)





Figure 1-3 Examples of LCD Drive Power Connections (Capacitor Split Method, 1/3 bias method)

### (3) LCD panel

The number of time divisions for LCD display, the bias method, and the frame frequency differ depending on the LCD panel specifications. The LCD controller/driver should be set according to the specifications of the LCD panel to be used. Regarding compatibility of the LCD panel and the LCD controller/driver, refer to the datasheets for each.

### 1.2 No Display in Specific Places of the LCD Panel

When there is no display in specific places of the LCD panel, check (1) and (2) below.

(1) Check that the LCD port function register (PFSEG) is set correctly.

Refer to the preceding section "1.1, Nothing at All Displayed on the LCD Panel".

### (2) COM/SEM pin connections

If the PFSEG register settings are correct, there may be a problem with the COM/SEM pin connections. Check the state of the physical connections on the board. In particular, check the connection of the COM/SEM pin that controls the specific place at which there is no display.



### 1.3 LCD Panel Display Is Faint

When the LCD panel display is faint, check ① through ③ below.

(1) Check the LCD driving voltages

The LCD driving voltages VL1 to VL4 should be checked to ensure they are being supplied normally. Measure the voltage at each pin, and confirm that they are within the voltage ranges stipulated in the "LCD Characteristics" in the "Electrical Specifications" section of the user's manual.

When a voltage drop is observed in the waveforms of the driving voltages VL1 to VL4, it is possible that the capacitance values of the capacitors connected to the external circuit for driving voltage supply are not appropriate. After evaluations, change the capacitance values.

External capacitance division method: Capacitors connected between the VL1 to VL4 pins and GND for reference voltage stabilization<sup>(note 1)</sup>

Internal voltage boosting method, capacitor split method: Capacitors connected for drive voltage generator operation (0.47  $\mu$ F ±30%).

Note 1: The capacitance value given in the user's manual for capacitors connected to an external circuit  $(0.22 \ \mu F)$  is a reference value. The appropriate value depends on the LCD panel used, the number of segment pins, the number of common pins, the frame frequency, and other parameters of the usage environment. The value should be adjusted and determined after thorough evaluations according to the system characteristics.

### (2) COM/SEM pin connections

It is possible that there may be a problem with COM/SEM pin connections. Check the state of physical connections on the board. For example, with the PFSEG register, change one pin set to "used as segment output" at a time to an output port (low-level output or high-level output), and check whether there is any improvement in the LCD panel display.

To change to an output port, set a bit in the port mode register (PMxx) to "output mode (output buffer on)" (PMxx = 0), and in the PFSEG register, change the bit to "used as port (other than segment output)".



### (3) Frame frequency

Check whether the frame frequency setting is compatible with the LCD panel specifications.

Further, there are constraints on the combinations of display modes (display waveforms, number of time slices, bias method), driving voltage generation method, and frame frequencies that can be used with the LCD controller/driver installed in the RL78. Refer to "Combinations of Display Waveform, Time Slices, Bias Method, and Frame Frequency" in the user's manual for the RL78 product to be used.

Combinations of Display Waveform, Time Slices, Bias Method, and Frame Frequency(RL78/L13)

Displ	Set Value						Driving Voltage Generation Method				
Display Waveform	Number of Time Slices	Bias Mode	LWAVE	LDTY2	LDTY1	LDTY0	LBAS1	LBAS0	External Resistance Division	Internal Voltage Boosting	Capacitor Split
Waveform A	8	1/4	0	1	0	1	1	0	⊖ (24 to 128 Hz)	○ (24 to 64 Hz)	×
Waveform A	4	1/3	0	0	1	1	0	1	⊖ (24 to 128 Hz)	○ (24 to 128 Hz)	○ (24 to 128 Hz)
Waveform A	3	1/3	0	0	1	0	0	1	⊖ (32 to 128 Hz)	⊖ (32 to 128 Hz)	⊖ (32 to 128 Hz)
Waveform A	3	1/2	0	0	1	0	0	0	⊖ (32 to 128 Hz)	×	×
Waveform A	2	1/2	0	0	0	1	0	0	⊖ (24 to 128 Hz)	×	×
Waveform A	Sta	atic	0	0	0	0	0	0	⊖ (24 to 128 Hz)	×	×
Waveform B	8	1/4	1	1	0	1	1	0	⊖ (24 to 128 Hz)	⊖ (24 to 64 Hz)	×
Waveform B	4	1/3	1	0	1	1	0	1	⊖ (24 to 128 Hz)	⊖ (24 to 128 Hz)	⊖ (24 to 128 Hz)

Remark O: Supported

×: Not supported



### (4) Contrast adjustment (case of internal voltage boosting method)

When the internal voltage boosting method is selected, with the LCD boost level control register (VLCD), the contrast can be adjusted in 16 levels. For details, refer to the user's manual for the RL78 product to be used.

Symbol	7	6	5	4	3	2	1	0
VLCD	0	0	0	VLCD4	VLCD3	VLCD2	VLCD1	VLCD0
-								
ſ	VLCD4	VLCD3	VLCD2	VLCD1	VLCD0	Reference	VL4	Voltage
						voltage select	tion 1/3 bias	1/4 bias
						(contrast	method	method
l						adjustment)		
ſ	0	0	1	0	0	1.00 V	2.00.1/	4.00.1/
						(default)	3.00 v	4.00 V
Ĩ	0	0	1	0	1	1.05 V	3.15 V	4.20 V
	0	0	1	1	0	1.10 V	3.30 V	4.40 V
	0	0	1	1	1	1.15 V	3.45 V	4.60 V
Ĩ	0	1	0	0	0	1.20 V	3.60 V	4.80 V
Ī	0	1	0	0	1	1.25 V	3.75 V	5.00 V
Ī	0	1	0	1	0	1.30 V	3.90 V	5.20 V
Ī	0	1	0	1	1	1.35 V	4.05.1/	Setting
							4.05 v	prohibited
Ī	0	1	1	0	0	1.40 V	4.00.1/	Setting
							4.20 V	prohibited
Ĩ	0	1	1	0	1	1.45 V	4.05.1/	Setting
							4.35 V	prohibited
Ĩ	0	1	1	1	0	1.50 V	4.50.1/	Setting
							4.50 v	prohibited
Ĩ	0	1	1	1	1	1.55 V	4.65.1/	Setting
							4.65 V	prohibited
Ĩ	1	0	0	0	0	1.60 V	4 90 1/	Setting
							4.80 v	prohibited
	1	0	0	0	1	1.65 V	4.05.1/	Setting
							4.95 v	prohibited
Ĩ	1	0	0	1	0	1.70 V	E 40 V	Setting
							5.10 v	prohibited
Ĩ	1	0	0	1	1	1.75 V		Setting
							5.25 V	prohibited
F		0	ther than abo	Setting prohib	oited			



### 2. Frequently Asked Questions

### Question 1

In the internal voltage boosting method, is there any problem with setting "display on" without waiting for the reference voltage setup time and the voltage boosting wait time,?

#### Answer 1

Yes, there would be problems. "display on" is set before the LCD driving voltage reaches the voltage setting, and so the LCD panel display would become unstable. Always be sure to wait for the stipulated time.

#### Question 2

When using the internal voltage boosting method, on setting the LCD boost level control register (VLCD), would it be alright if the VL4 voltage were higher than the power supply voltage of the RL78 product?

#### Answer 2

No, this would not cause a problem because the LCD driving voltage is generated within the RL78 product, and does not depend on the power supply voltage.

#### Question 3

Can the LCD driving voltage be supplied externally?

#### Answer 3

No, the LCD driving voltage for the LCD controller/driver installed in the RL78 cannot be supplied from an external device.

The LCD driving voltage is supplied from an LCD drive voltage generator within the RL78 product.



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## **Revision History**

			Description
Rev.	Date	Page	Summary
1.00	2017.11.17		First edition issued

### General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

— The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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(Rev.3.0-1 November 2016)



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